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EASE64162/164

Program Development Support System for the MSM64162 /MSM64164

User's Manual

Rev. 2.00

JAN. 1995

OKI

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PREFACE

This manual explains the operation of the EASE64162/164 in-circuit emulator for the MSM64162, MSM64162D, and MSM64164 micro-controllers built on Oki Electric's nX-4/20 CMOS 4-bit core.

For customers who use the EASE64162/164 as an emulator for the MSM64162D, please substitute all references in this manual to the MSM64162 with MSM64162D.

The following are related manuals.

- MSM64162 User's Manual
  - MSM64162 hardware description

- MSM64162D User's Manual
  - MSM64162D hardware description

- MSM64164 User's Manual
  - MSM64164 hardware description

- nX-4/20, 4/30 Core Instruction Manual
  - OLMS 64K series instruction set description

- ASM64K Cross Assembler User's Manual
  - ASM64K assembler operation description
  - ASM64K assembly language description

- MASK162 User's Manual
  - MASK162 (MSM64162 mask option generator) operation description

- MASK164 User's Manual
  - MASK164 (MSM64164 mask option generator) operation description

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TABLE OF CONTENTS

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Appendix

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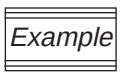
Explanation of Symbols

Indicates a supplemental explanation of particular importance that relates to the topic of the current text.

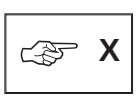


Indicates a specific example of the topic of the current text.

Indicates a section number or page number to reference for related information on the topic of the current text.

(☞ x)

Indicates the number of a footnote with a supplemental explanation of particular words in the current text.



Indicates a footnote with a supplemental explanation of words marked with the above-described symbol. The numbers following each symbol correspond to each other.

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Chapter 1

Before Starting

This chapter describes procedures to follow after receiving delivery of an EASE64162/164 program development support system. It is recommended that this chapter be read before supplying power to the emulator.

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Thank you for buying Oki Electric's EASE64162/164 program development support system. When your system was shipped we made every effort to ensure that it would not be damaged or mispacked, but we recommend that you confirm once more that this did not occur following the explanations in this chapter.

The RS232C cable, floppy disks, or other items may differ depending on the model of host computer that you will use. Use with a different model could cause damage to the hardware, so please take particular care to avoid this. If the system shipped to you was damaged, if any components were missing, or if your host computer model is different, then please contact the dealer from whom you purchased the system or Oki Electric's sales department.

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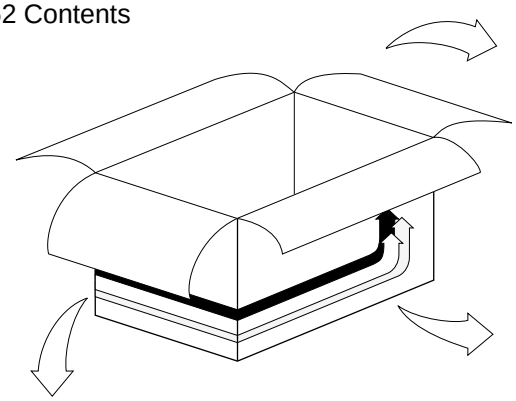
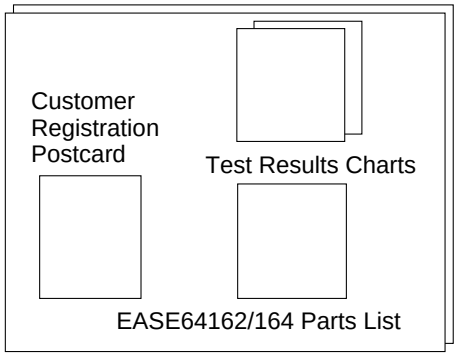
1.1. Confirm Shipping Contents

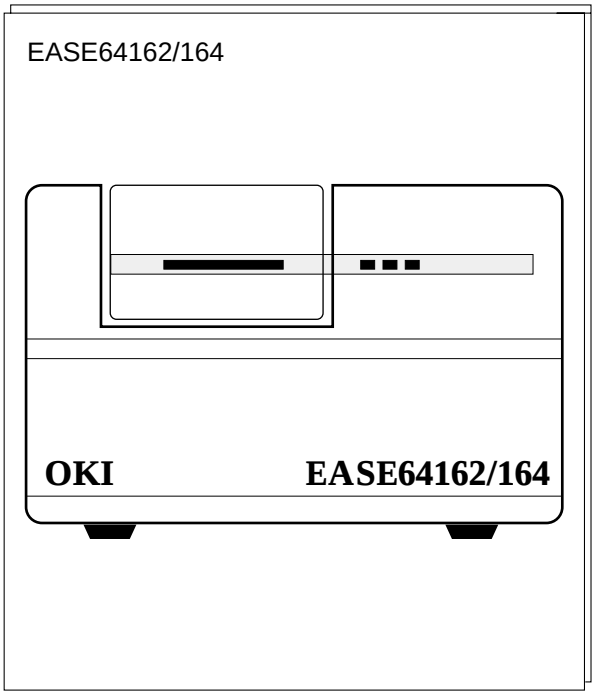
EASE64162 Contents



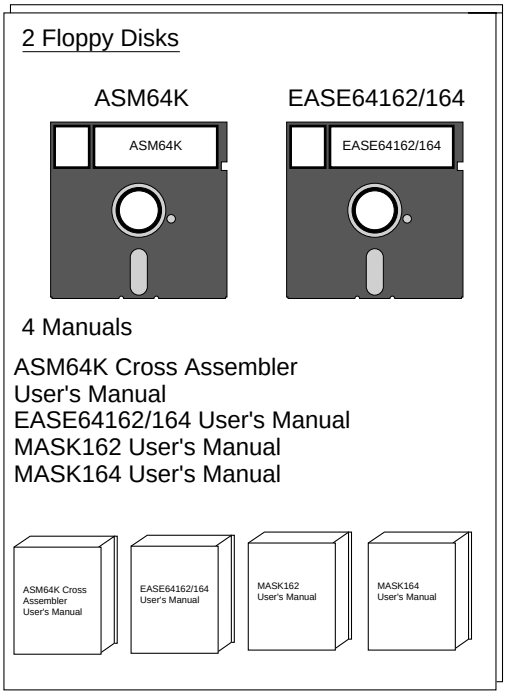
Documentation



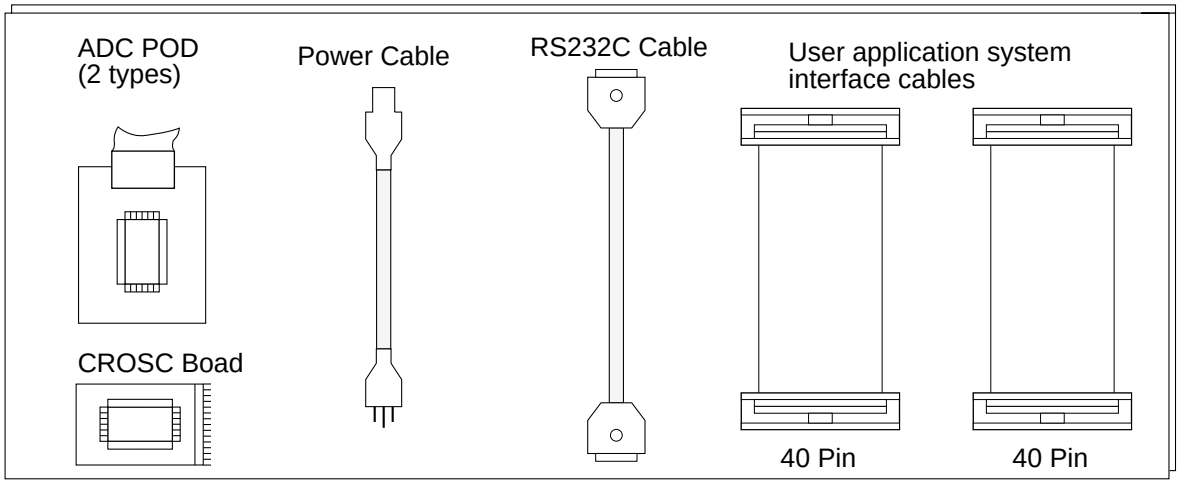
Hardware



Software



Accessories



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Your purchase of the EASE64162/164 will be followed by delivery of the necessary hardware, software, and manuals in the shipping box illustrated in the upper left of page 1-3. After taking delivery, open the box and confirm that it contains all the contents illustrated on page 1-3.

Each component is described below. Note that those marked with ☞ will differ depending on the model of host computer.

Documents

Customer Registration Postcard

Oki Electric uses this to record you in our customer list in order to inform you of product maintenance and version upgrades. Please fill out the requested items and send the postcard in as soon as possible. If you do not send in the registration postcard, it will it more difficult to provide you with maintenance and version upgrade service.

EASE64162/164 Components

This is a list of the items shipped.

Test Results Charts

This chart shows that the EASE64162/164 passed all tests before shipping.

Hardware

EASE64162/164

This is the EASE64162/164 emulation kit. It contains hardware for host computer communications, EPROM programming, and emulation of MSM64162/MSM64164 operation.

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Software

☞ 1	**Floppy Disk: ASM64K**	This disk contains the ASM64K executable files. It can be supplied in the formats described below. Floppy disk contents are explained in Section 1.2.
☞ 1	**Floppy Disk: EASE64162/164**	This disk contains the executable files for EASE64X, MASK162 and MASK164. It can be supplied in the formats described below. Floppy disk contents are explained in Section 1.2.
	ASM64K Cross-Assembler User's Manual	This is the user's manual for the ASM64K cross-assembler.
	EASE64162/164 User's Manual	This is the user's manual (this manual) for the EASE64162/164.
	MASK162 User's Manual	This is the MASK162 user's manual for the MSM64162 Mask Option Generator.
	MASK164 User's Manual	This is the MASK164 user's manual for the MSM64164 Mask Option Generator.

☞ **1** Available floppy disk formats

MS-DOS format
- (1) 3.5-inch 2HD (1.21 Mbytes)
- (2) 5.25-inch 2HD (1.21 Mbytes)

PC-DOS format (for IBM PC/AT personal computers)
- (1) 3.5-inch 2HD (1.44 Mbytes)
- (2) 5.25-inch 2HD (1.232 Mbytes)

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Accessories

☞ 2	**M64162/164 ADC POD (1.5V)**	This is the MSM64162 and MSM64164's 1.5V ADC POD, used as the interface with EASE64162/164. The CR oscillator for MSM64162 and MSM64164 A/D conversion is removed from the ADC POD, so the capacitor and resistor for oscillation must be added.
☞ 2	**M64162/164 ADC POD (3.0V)**	This is the MSM64162 and MSM64164's 3.0V ADC POD, used as the interface with EASE64162/164.
☞ 3	**M64162/164 CROSC Board (1.5V)**	This is the MSM64162 and MSM64164's 1.5V CROSC board. The CR oscillator for the MSM64162 and MSM64164 high-speed clock is removed from the CROSC board, so the resistor for oscillation must be added.
	Power Supply Cable	This cable connects to the power supply connector.
☞ 4	**RS232C Cable**	This cable connects the EASE64162/164 with a host computer. There are two types: one for NEC-PC9801 and Oki if800 series computers, and one for IBM-PC/AT computers.
☞ 5	**User Application System Interface Cables**	These cables connect the EASE6464162/164 to the user's application system. Two cables are supplied: two 40-pin flat cables.

☞ 2 The oscillation characteristics of the CR oscillator for AD conversion differ for the 1.5V and 3.0V versions of MSM64162 and MSM64164. Select the ADC POD that matches your version. A label on the board identifies the ADC POD as 1.5V or 3.0V.

☞ 3 The oscillation characteristics of the CR oscillator for the high-speed clock differ for the 1.5V and 3.0V versions of MSM64162 and MSM64164. Select the CROSC board that matches your version. A label on the board identifies theCROSC board as 1.5V or 3.0V. The 3.0V CROSC board is mounted in the EASE64162/164 when it is shipped.

☞ 4 Unless specified before the EASE64162/164 is shipped, a cable for the NEC-PC9801 series will be shipped. If you will use an Oki if800 series computer, then you can also use this cable. If you will use an IBM-PC, then please tell the responsible salesperson before your system is shipped so that a special-purpose cable will be included. If you forget to specify the personal computer that you will be using, then please contact the responsible salesperson to exchange cables.

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To identify which type of cable was shipped to you, please refer to the features listed below.

(1) NEC-PC9801 series	Cable has a 25-pin male connector and 25-pin male connector.
(2) IBM-PC/AT	Cable has a 25-pin male connector and 9-pin female connector.

If you will be using a host computer other than an NEC-PC9801 series, Oki if800 series, or IBM PC/AT, then the connectors and their cable connections may have to be changed. Refer to Appendix 4 and 5 to change the connectors or cable connections to match the host computer you will use.

The user application system interface cables are used for the following applications.

40-pin flat cable

The cable connects the user application system with the EASE64162/164's USER connector. The voltage level of the USER connector's interface power supply is set by the CIPS command to an internal voltage (5V) or an external voltage (3V~5V).

CIPS command

40-pin flat cable

The cable connects the user application system with the EASE64162/164 LCD connector or LED connector.

The LCD and LED connectors correspond to pins L0~L33 of the MSM64162/MSM64164. LCD drive signals (0V~4.5V) are output from the LCD connector. LED drive signals (0V~5V) are output from the LED connector.

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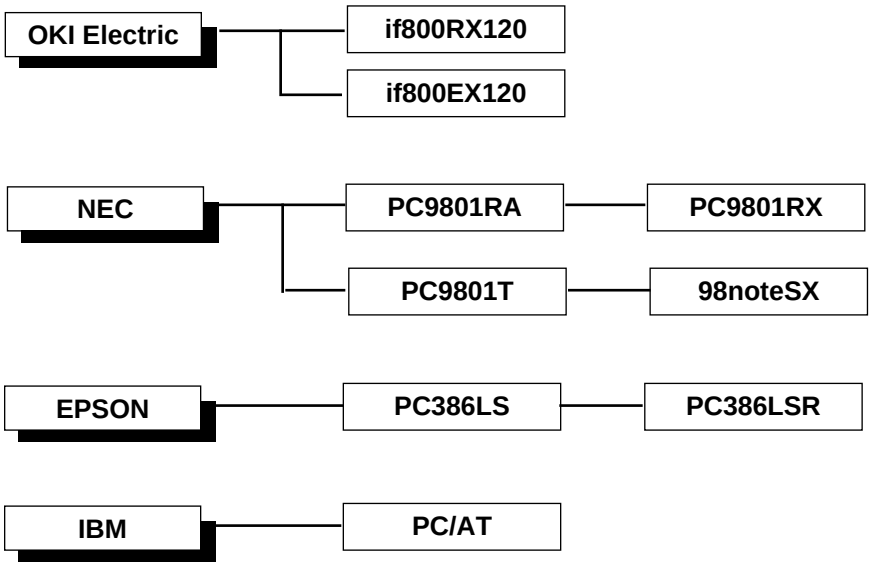
1.2. Confirm Floppy Disk Contents

1.2.1. Host Computer

EASE64X, the debugger for EASE64162/164, has been confirmed to operate with the following computer models.



All of the above models must have at least 640 Kbytes of memory.

Oki Electric has not confirmed direct operation with computers other than those listed above.

Before purchasing the EASE64162/164, your sales dealer or the Oki Electric sales department should verify the computer model that you will use. However, if after buying the system you want to consider a model other than those listed above, then please consult with Oki Electric's application engineering section.

1.2.2. Operating System

The operating system of computers other than IBM-PCs should be Japanese MS-DOS version 3.1 or later. For IBM-PCs, it should be PC-DOS version 3.1 or higher.

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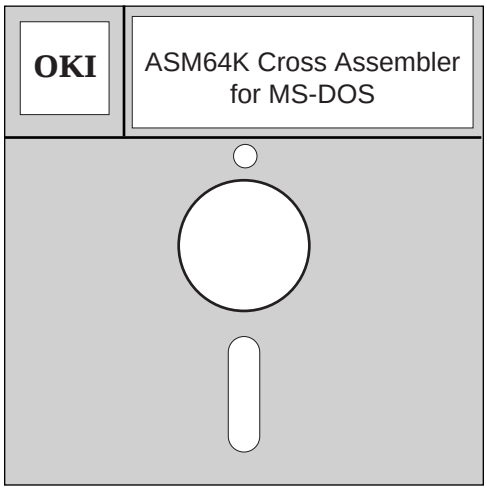
1.2.3. Floppy Disk Contents

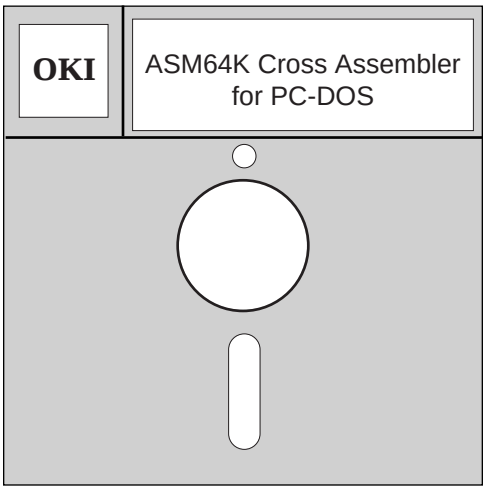
If the conditions described in Sections 1.2.1 and 1.2.2 are satisfied, then there will be no problem with your host computer model. Next, check the contents of the floppy disks.

(1) ASM64K floppy disk contents

As shown below, the label pasted on the floppy disk will differ for the PC9801/if800 series and the IBM-PC/AT.

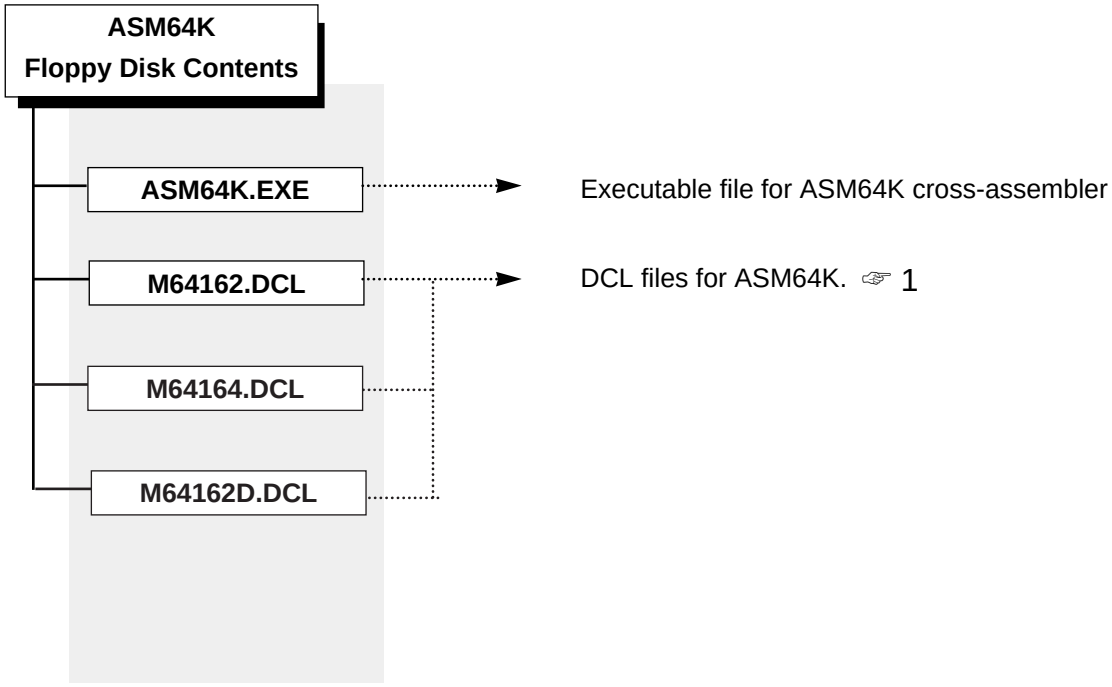


For PC9801/if800 Series



For IBM-PC/AT

If you use the floppy disk for the wrong type of computer, then it will not be able to read the floppy disk contents, so check whether or not the correct disk is inserted. Each file included on the floppy disk and a brief explanation is given below.



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☞ 1

The DCL file for ASM64K includes the following definitions for MSM64162, MSM64162D and MSM64164.

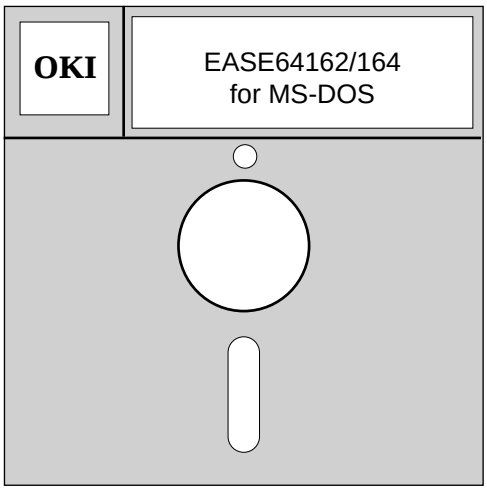
a. SFR (Special Function Register) address and access attributes
b. Code memory (program memory) address range
c. Data memory address range

The following DCL files are provided for the MSM64162, MSM64162D, and MSM64164. (The floppy disk contains DCL files for all the devices supported by ASM64K.)

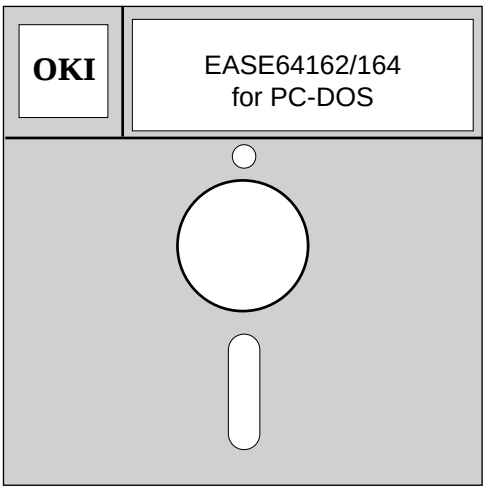
For MSM64162:	M64162.DCL
For MSM64162D:	M64162D.DCL
For MSM64164:	M64164.DCL

(2) EASE64162/164 Floppy Disk Contents

As shown below, the label pasted on the floppy disk will differ for the PC9801/if800 series and the IBM-PC/AT.



For PC9801/if800 Series



For IBM-PC/AT

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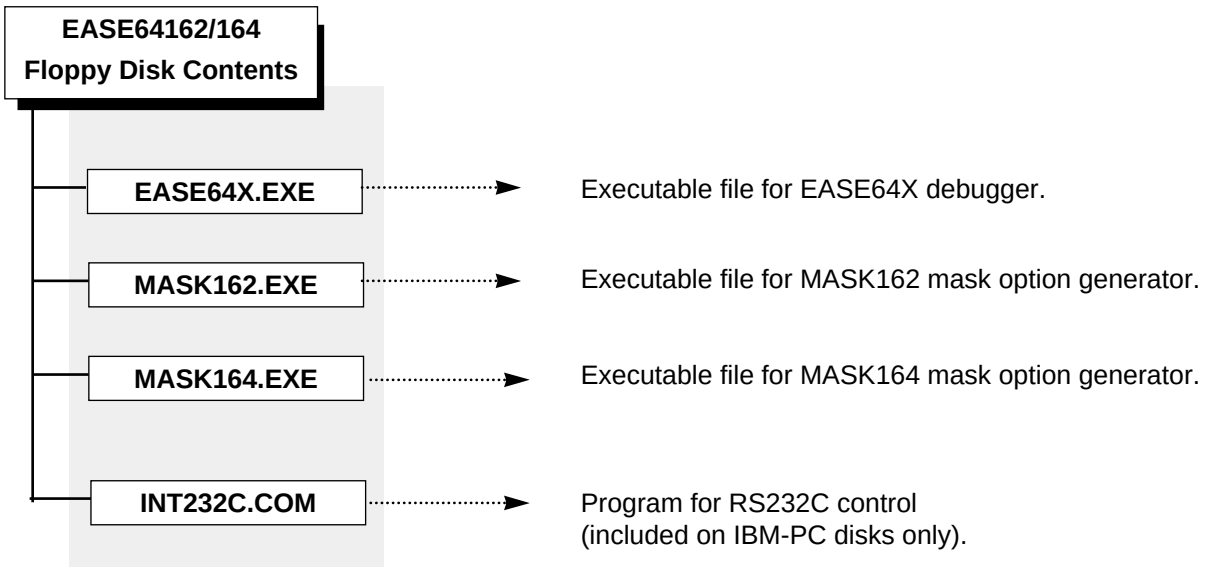
If you use the floppy disk for the wrong type of computer, then it will not be able to read the floppy disk contents, so check whether or not the correct disk is inserted. Each file included on the floppy disk and a brief explanation is given below.



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Chapter 2

Overview

This chapter provides an overview of EASE64162/164 system configuration, describes the program development procedure with the EASE64162/164 system.

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2.1. EASE64162/164 Emulator Configuration

2.1.1. EASE64162/164 Emulation Kit

The EASE64162/164 is a general-purpose control system for in-circuit emulators for Oki Electric's MSM64162 and MSM64164 CMOS 4-bit microcontrollers.

The internal configuration of the EASE64162/164 is as follows.

	• System controller	MC68000
☞1	• Code memory	8192 x 8 bits
☞2	• Data memory	256 x 4 bits
☞1	• Trace memory	8192 steps x 64 bits
☞1	• Attribute memory	8192 x 8 bits
	• Instruction executed bit memory	8192 x 1 bit
	• EPROM programmer	For 2764/128/256/512
	• RS232C ports	1 channel
☞3	• Evaluation board	For MSM64162 and MSM64164
	• System power supplies	1

☞ 1 The maximum address of code memory, attribute memory, and instruction executed memory is 0FDFH, but in MSM64162 mode addresses to 7DFH are valid, and in MSM64164 mode addresses to 0FDFH are valid. The maximum address can be extended up to 1FFFH with the EXPAND command.

☞ 2 Data memory size is 128x4 bits (data memory addresses 780H~7FFH) in MSM64162 mode, and 256x4 bits (data memory addresses 700H~7FFH) in MSM64614 mode.

☞ 3 The evaluation board emulates the functions of the MSM64162 and MSM64164. It is internal to the EASE64162/164.

The evaluation board consists of an MSM64E900 evaluation chip with an nX-4/20 core that matches the MSM64162 and MSM64164 CPU core, hardware that matches the I/O portion of the MSM64162 and MSM64164 (excluding the CR oscillator for A/D conversion), and hardware that matches the MSM64162 and MSM64164's LCD drivers.

The I/O hardware is constructed from ordinary discrete components, so the electrical characteristics of the ports will differ from those of the MSM64162 and MSM64164.

The emulator uses special hardware to allocate the mask option registers of the LCD drivers, so display timing will differ from the MSM64162 and MSM64164.

The CR oscillator for the MSM64162 and MSM64164 A/D converter is added to the optional M64162/164 ADC POD. An MSM64164 is mounted in the M64162/614 ADC POD, so CR oscillation will be with the same electrical characteristics as the MSM64164. The CR oscillation clock is input to the EASE64162/164 and performs A/D conversions.

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2.1.2. ASM64K Cross-Assembler

ASM64K is a cross-assembler developed for the OLMS-64K series. It is stored on a floppy disk that comes with the purchase of an EASE64162/164 development support system.

Source files constructed from OLMS-64K series instruction mnemonics and directives are converted to Intel HEX formal object files with ASM64K. Object files (machine language files) generated this way are read and executed by EASE64X, explained in the next section.

ASM64K can be used with host computers that satisfy the following conditions.

- The operating system is MS-DOS or PC-DOS version 3.1 or higher.
- There is a free area of at least 128K bytes in main memory.

For details about ASM64K, refer to the ASM64K Cross-Assembler User's Manual.

2.1.3. EASE64X Debugger

The EASE64X debugger is software that supports debugging.

EASE64X is stored on a floppy disk that comes with the purchase of an EASE64162/164 development support system.

EASE64X can be used with host computers that satisfy the following conditions.

- The operating system is MS-DOS or PC-DOS version 3.1 or higher.
- There is a free area of at least 100K bytes in main memory.
- A channel for an RS232C interface.

2.1.4. MASK162/MASK164 Mask Option Generators

The MASK162 and MASK164 mask option generators allow an operator to input the MSM64162 and MSM64164 mask option settings shown below, and convert the input data to mask option files in Intel HEX format.

- LCD driver duty value
- Assignment of segment pins (L0~L33) to ports, commons, and segments
- Assignment of segment pins to display registers
- Operating power supply voltage
- Presence of capacitor for Crystal oscillator

The mask option files generated by MASK64162 and MASK64164 are used to create the mask needed to manufacture the MSM64162 or MSM64164.

The EASE64X debugger reads the mask option files so the EASE64162/164 can determine the above settings (except for operating power supply voltage and presence of capacitor for Crystal oscillator).

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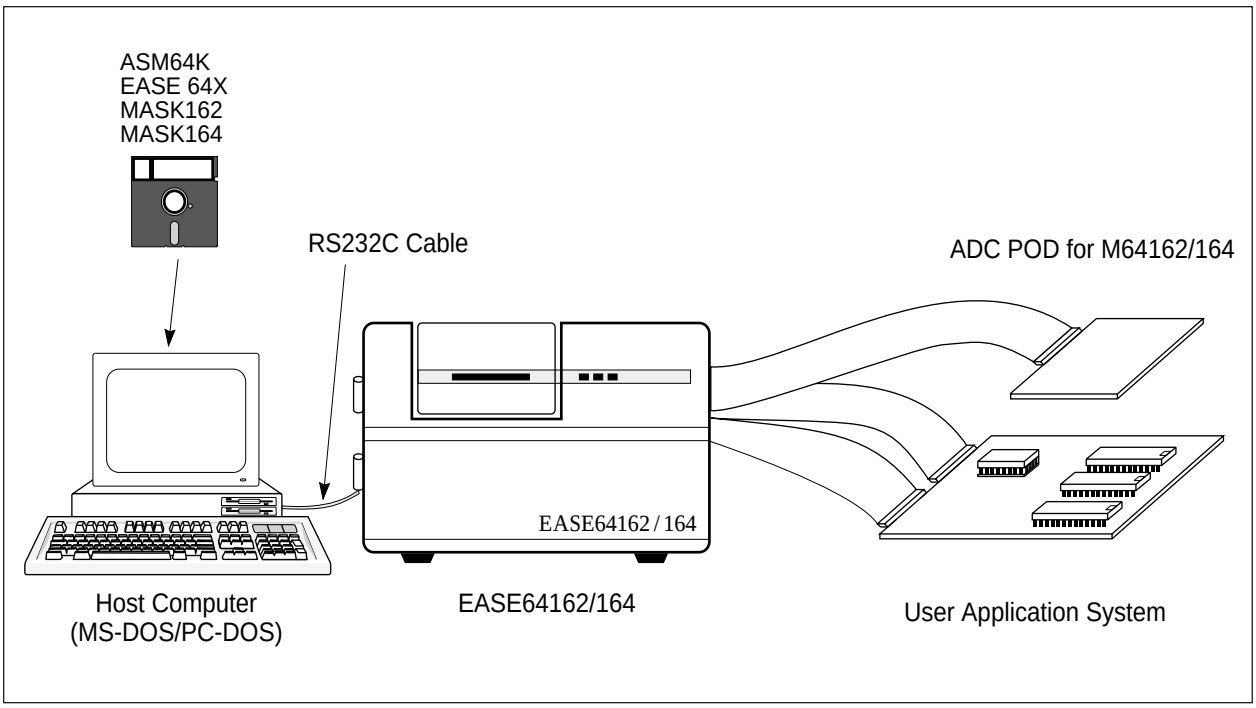
2.1.5. System Configuration

The system is used in the following configuration.



System Configuration Diagram

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2.2. Program Development With EASE64162/164

2.2.1. General Program Development and EASE64162/164

Figure 2-1 shows the general flow of program development (☞1).

First, one decides on the functions of the product to be developed, and evaluates which hardware and software should be designed to implement them. Specific considerations include which MPU to use, how to allocate MPU interrupts, how much ROM and RAM to add, etc. This is called the *functional design process*.

Next is the *specification design process*. Here the functions to be implemented are evaluated in detail, and the methods to use those functions in the final product are decided. Specifically, commands are decided upon and a command input specification is written. The specification generated by this process is usually called the functional specification.

The process of creating a program based on the functional specification is called the *program design process*. Algorithms, flowcharts, and a program specification are created. This process can also include coding (source program creation) and assembly. In other words, ASM64K is used in this process. This process also includes the creation of a mask option file with MASK162 or MASK164.

Next is the *debug process*. This is the process in which the EASE64162/164 especially excels (☞2). An object file and a mask option file created in the program design process is downloaded to the EASE64162/164, and by using the various functions of the EASE64162/164 emulator, program bug analysis, fixing, and testing are performed.

The last position of the overall program development process is occupied by the *testing process*. The complete program from the debug process is operated in the actual product, and operation according to the functional specification is verified with test programs, etc. If there are bugs in the operation, then the flow from the program design process on is repeated until there are no more bugs.

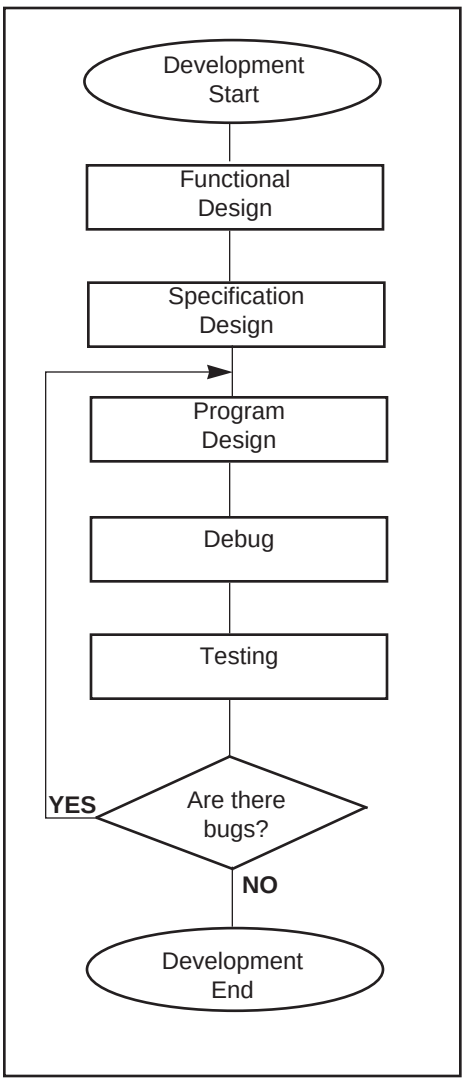

Figure 2-1. General Flow of Program Development

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☞ 1 The general flow and terminology given here are generally used, but other documents and manuals may have different expressions.

☞ 2 Refer to Chapter 3, “EASE64162/164 Emulator,” for details about the various function of the EASE64162/164 emulator.

2.2.2. From Source File To Object File

In order to perform debugging with the EASE64162/164 emulator, an object file for downloaded to the EASE64162/164 must be generated (☞ 3, 4).

Figure 2-2 shows the process of generating an object file from a source program file coded in assembly language (hereafter called a source file).

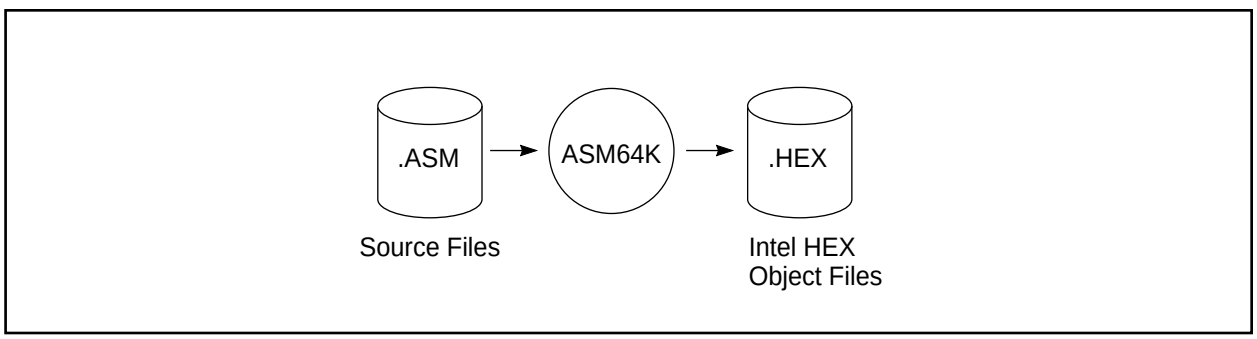

Figure 2-2. Process of Generating Object Files From Source Files

In the above figure, circles indicate operation of the ASM64K cross-assembler program, while cylinders indicate files generated by programs.

Object files that the EASE64162/164 emulator can handle are Intel HEX format object files that include symbol information, as shown in Figure 2-2.

☞ 3 Downloading means storing the contents of an object file in EASE64162/164 code memory with the EASE64X **LOD** command. Refer to Section 3.3.4.2.2, “Load/Save/Verify Commands,” for details on the **LOD** command.

☞ 4 Object files in this document refer to Intel HEX format object files that not include symbol information which the EASE64162/164 emulator can handle.

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2.2.3. Generating Mask Option Files

To perform debugging with the EASE64162/164 emulator, MSM64162 or MSM64164 mask option files must be created in addition to the object file described in the previous sections.

Figure 2-3 shows the process for generating mask option files.

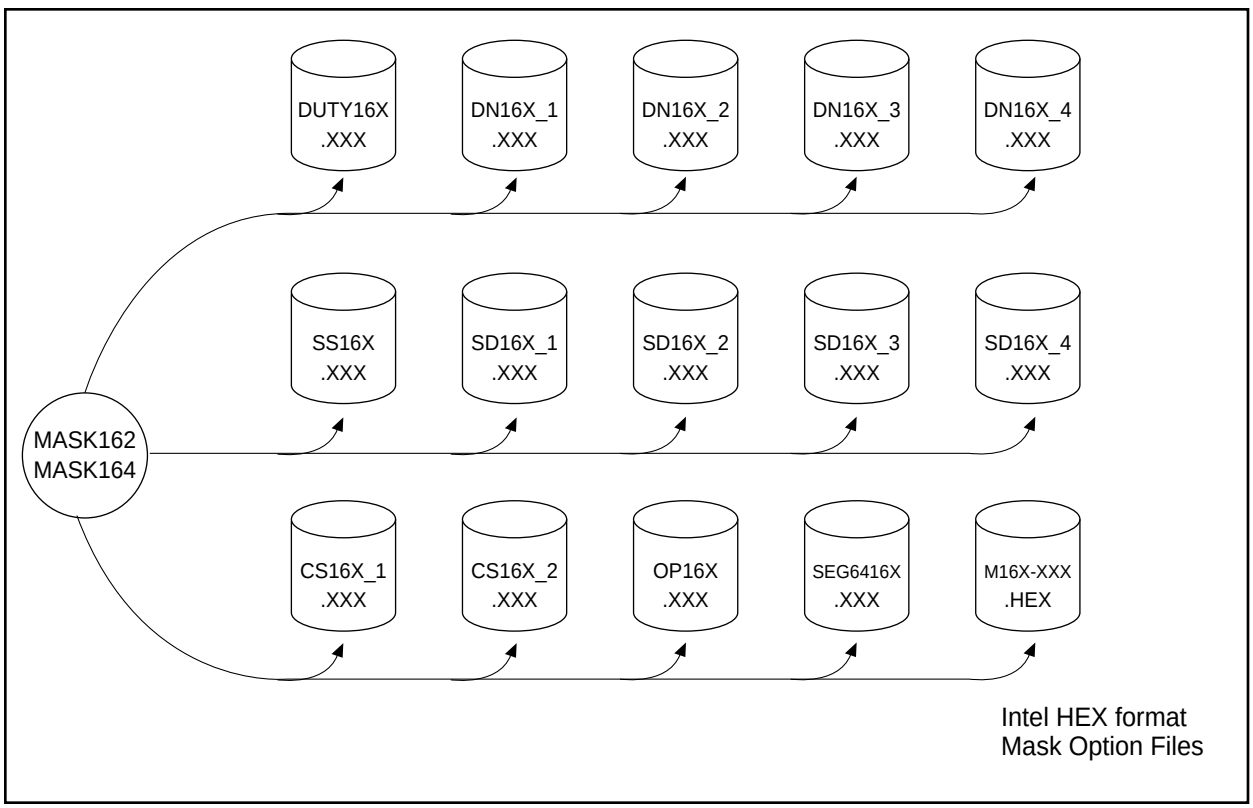

Figure 2-3. Process For Generating Mask Option Files

In the above figure, circles indicate operation of the MASK162 and MASK164 programs, while cylinders indicate files generated by the programs.

Based on mask option settings input by the operator, MASK162 and MASK164 outputs the fifteen files shown in Figure 2-3. The EASE64162/164 emulator can handle mask option files in Intel HEX format.

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2.2.4. Files Usable with the EASE64162/164 Emulator

The files usable with the EASE64162/164 emulator are described in the sections about files created by ASM64K and MASK162/MASK164. As described in those sections, there are two types of files that can be handled by the EASE64162/164 emulator. These are explained.

(1) Intel HEX files generated by ASM64K

These are object files generated by ASM64K from source files that consist of OLMS-64K mnemonics and various directives. Object files are read into code memory using the LOD command.

(2) Intel HEX files generated by MASK162/MASK164

These are mask option files generated by MASK162 and MASK164 from MSM64162 and MSM64164 mask option settings. Mask option files are read into the system memory of the EASE64162/164's MC68000 system controller using the LODM command.

If the "/S" option is added when the ASM64K assembler is executed, then the generated object file will include symbol information. However, EASE64162/164 cannot handle object files that include symbol information.

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Chapter 3

EASE64162/164 Emulator

This chapter explains the actual use of the EASE64162/164 emulation kit and the EASE64X debugger in detail.

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In this chapter...

Section 3.1 gives an overview of each group of functions that can be used with the EASE64162/164 emulation kit and the EASE64X debugger

Section 3.2 explains how to start the EASE64162/164. EASE64162/164 dipswitch settings (to set the communications mode with the host computer, etc.) are also explained in this section.

Section 3.3 explains in detail the actual use of EASE64X debugger commands with the EASE64162/164.

Section 3.3.1 describes the general input format of debugger commands and lists all debugger commands by function. This list also gives a reference page for each command, so it is convenient for use as a command index.

Sections 3.3.3 and 3.3.4 explain the history function and special-purpose keys respectively. These are provided to support efficient input of debugger commands.

Section 3.4 explains each debugger command in detail.

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3.1. EASE64162/164 Functions

3.1.1. Overview

Section 2.2 explained the program development process with the MSM64162 and MSM64164 microcontroller. This section gives an overview of the actual emulator functions used to debug prototype programs created by that process.

The most basic function of the emulator is to read and execute a user-created program (an Intel HEX format file generated by ASM64K). Here "execute" means to execute a program at the same speed (realtime) as the volume-production MSM64162 and MSM64164 with internal mask ROM. This is known as *emulation*, as distinguished from program simulation with large computers.

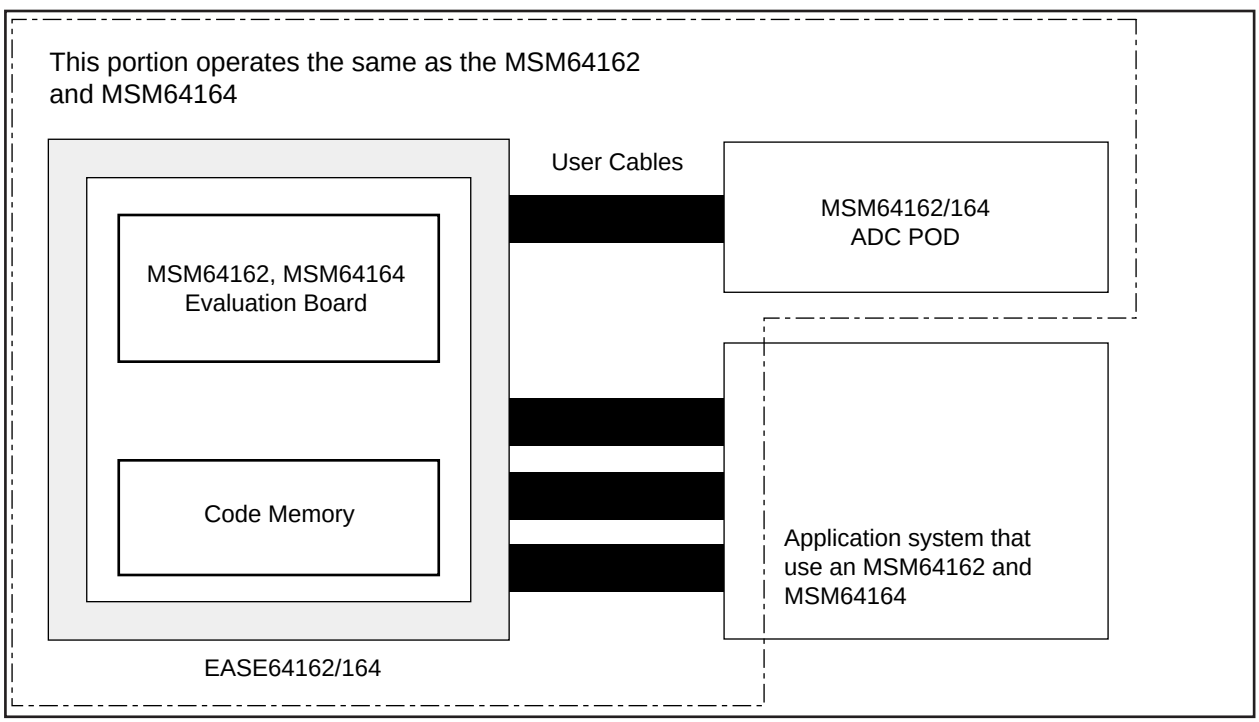

Figure 3-1

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The volume-production MSM64162 and MSM64164 microcontroller has mask ROM on-chip, but once mask ROM has been written it cannot be changed. However, program during the development stage is difficult to debug unless it is stored in rewritable memory (RAM).

Thus the EASE64162/164 has in internal 8K bytes program storage RAM. This RAM is called *code memory* . Refer to Figure 3-1 on the previous page.

EASE64162/164 executes programs in this code memory instead of mask ROM. When the user application system is being produced in volume, it will be mounted with an MSM64162 or MSM64164 microcontroller, but at the debug stage it is replaced with a connector in the user application system. This connector is attached to an EASE64162/164 user cable (Refer to Figure 3-1).

Within the EASE64162/164 is an internal evaluation board for emulating the functions of the MSM64162 and MSM64164. This evaluation board has the same CPU circuit and the same external pins as the MSM64162 and MSM64164 However, the CR oscillator for the A/D converter is implemented in the M64162/164 ADC POD.(☞1).

The main feature of the evaluation board is that it has no internal mask ROM, but it does have some special control circuitry and control pins. These additional circuits and pins are used to control execution of programs and reading of internal memory, registers, and flags.

Also, the contents of code memory instead of mask ROM are read and executed.

The evaluation board's external pins include the same pins as the volume-production chip (MSM64162, MSM64164). These are connected to the corresponding pins in the user application system through the user cables and pins for the CR oscillator of the A/D converter are provided on the M64162/164 ADC POD.

As a result, when viewed from the user application system, the pins on the user cable and M64162/164 ADC POD appears identical to the MSM64162 and MSM64164 (Refer to Figure 3-1).

☞ **1** The CPU circuit of the evaluation board is constructed from ordinary discrete components, so the electrical characteristics of the ports will differ from those of the MSM64162 and MSM64164.

The CR oscillator of the MSM64162 and MSM64164 A/D converter is assigned to the M64162/164 ADC POD. The CR oscillator of the MSM64164 mounted in the M641642/164 ADC POD has the same electrical characteristics as an MSM64164. The CR oscillation clock is input to the EASE64162/164 to perform A/D conversion.

The emulator operates with special hardware for the LCD drivers on the evaluation board in order to change the register assignments by the mask options. Therefore the display timing will differ from the MSM64162 and MSM64164.

That the basic function of the emulator is to read and execute programs was already explained, but effective debugging is not possible with just simple execution. For example, one must be able to start and stop program execution at specified addresses. One needs to display and change the states of data memory (internal RAM), registers, and flags after execution. Furthermore, instead of just stopping execution at a specified address, one needs the ability to set complex conditions for stopping after a specified time has elapsed or some address has been passed a specified number of times (pass count). To meet these needs, EASE64162/164 has many functions beyond its basic one. These features are explained one by one in the following sections.

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3.1.2. Changing Target Chips

The EASE64162/164 is an emulation kit designed for the MSM64162 and MSM64164. It operates in MSM64164 mode by default when started, but the target chip can be changed with the CHIP command. (☞1)

❑ Setting chip mode with the CHIP command

One of the EASE64X debugger commands, the CHIP command, changes the target chip. The EASE64162/164 chip mode can be changed with this command.

CHIP

The chip modes specified by the CHIP command set the EASE64162/164 as follows. (☞2)

Item	MSM64162 Mode	MSM64164 Mode
Code memory addresses	000~7DFH	000~0FDFH
Attribute memory addresses	000~7DFH	000~0FDFH
Instruction executed memory addresses	000~7DFH	000~0FDFH
Data memory	128 x 4 bits	256 x 4 bits
Port 4 data register (P4D)	Invalid	Valid
Port 40 control register (P40CON)	Invalid	Valid
Port 41 control register (P41CON)	Invalid	Valid
Port 42 control register (P42CON)	Invalid	Valid
Port 43 control register (P43CON)	Invalid	Valid
Serial port control register (SCON)	Invalid	Valid
Serial port buffer register (SBUF)	Invalid	Valid
Backup control register (BUPCON)	Bits 0~2 valid	Bit 0 valid
Buzzer frequency control register (BFCON)	Bit 0 valid	Bits 0~3 valid
Interrupt enable register 0 (IE0)	Bits 0, 2, 3 valid	Bits 0~3 valid
Interrupt request register 0 (IRQ0)	Bits 0, 2, 3 valid	Bits 0~3 valid
Time base counter interrupts	1 Hz, 4 Hz, 16 Hz, 32 Hz 256 Hz	0.1 Hz, 1 Hz, 16 Hz 32 Hz, 256 Hz
LCD drivers	L0~L23	L0~L33

When evaluating an MSM64162D with EASE64162/164, set the chip mode to MSM64162 mode. However, do not use functions that do not exist in the MSM64162D (high-speed clock, A/D converter CROSC1 oscillation mode, IN1 external clock input mode).

Refer to user's manual of your chip for details about each register.

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3.1.3. Emulation Functions

The EASE64162/164 has two modes for its emulation functions (program execution functions).

(1) Single-step mode (**STP** command)

In this mode, program execution stops after each step (one instruction) is executed. After each instruction is executed, the state of the evaluation chip is read and displayed on the CRT. Single-step mode is realized with the **STP** command.

SEE **STP**

(2) Realtime emulation mode (**G** command)

In this mode, program execution will continue until some specified break condition is satisfied or an **ESC** key is input. Realtime emulation mode is realized with the **G** command.

SEE **G**

❑ *Operating Clock*

The EASE64162/164 operates using a clock supplied from an internal oscillation circuit. Its operating frequency is set to 32.768 KHz in low-speed mode and 400 KHz in high-speed mode. To use other frequencies, replace the crystal on the crystal board or the resistor for CR oscillation on the CROSC board in the emulator.

For details, refer to Section 3.2.1, "Setting Operating Frequency."

- The allowable operating frequencies for the EASE64162/164 are 32.768 KHz~500 KHz.
- Depending on the manufacturer and frequency of the crystal, the capacitors and resistor for oscillation may also need to be changed.

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3.1.4. Realtime Trace Functions

One EASE64162/164's principal functions is realtime tracing. Realtime tracing occurs during program execution under realtime emulation mode. It stores the executed addresses, the data and addresses in data memory used, and the states of evaluation chip port pins, registers, and flags in memory provided for tracing. The memory provided for tracing is called *trace memory*.

The EASE64162/164 has trace memory for 8192 steps. It traces the following items.

Trace Contents
Executed address
State of all ports
A register and B register values
Data memory contents at specified address (☞1)
Stack pointer (SP) value
H register and L register values
Carry flag (C) value
Port 2 value
Port 3 value
Port 4 value (☞2)
Port 0 value (☞2)
Port 1 value (☞2)
Bank select register 0 (BSR0) value (☞2)
Bank select register 1 (BSR1) value (☞2)

☞ 1 The data memory contents at the one address specified by the CTDM command will be traced.

☞ 2 Tracing of port 4, port 0, port 1, bank select register 0, and bank select register 1 is selected by the CTO command.

SEE **FTR, ETR, RTR, DTR, STT, RTT, DTT, DTM, CTO, DTO, CTDM, DTDM**

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❑ *Controlling trace execution*

Realtime tracing can always be performed during program execution, but you may want to see trace contents for just a particular part of a program. EASE64162/164 provides two ways to specify the trace area.

(1) Specify trace area with *trace enable bits.*
(2) Specify a triggers with *trace start/stop bits.*

Details of each method are explained in the command details section 3-3. The following are related commands.

SEE **DTR, ETR, RTR, FTR, STT, RTT, DTT**

The trace pointer controls the address in trace memory to which data will be written. The trace pointer is actually a 13-bit counter which increments every time an instruction is executed under the conditions described in (1) and (2) above (refer to Figure 3-2).

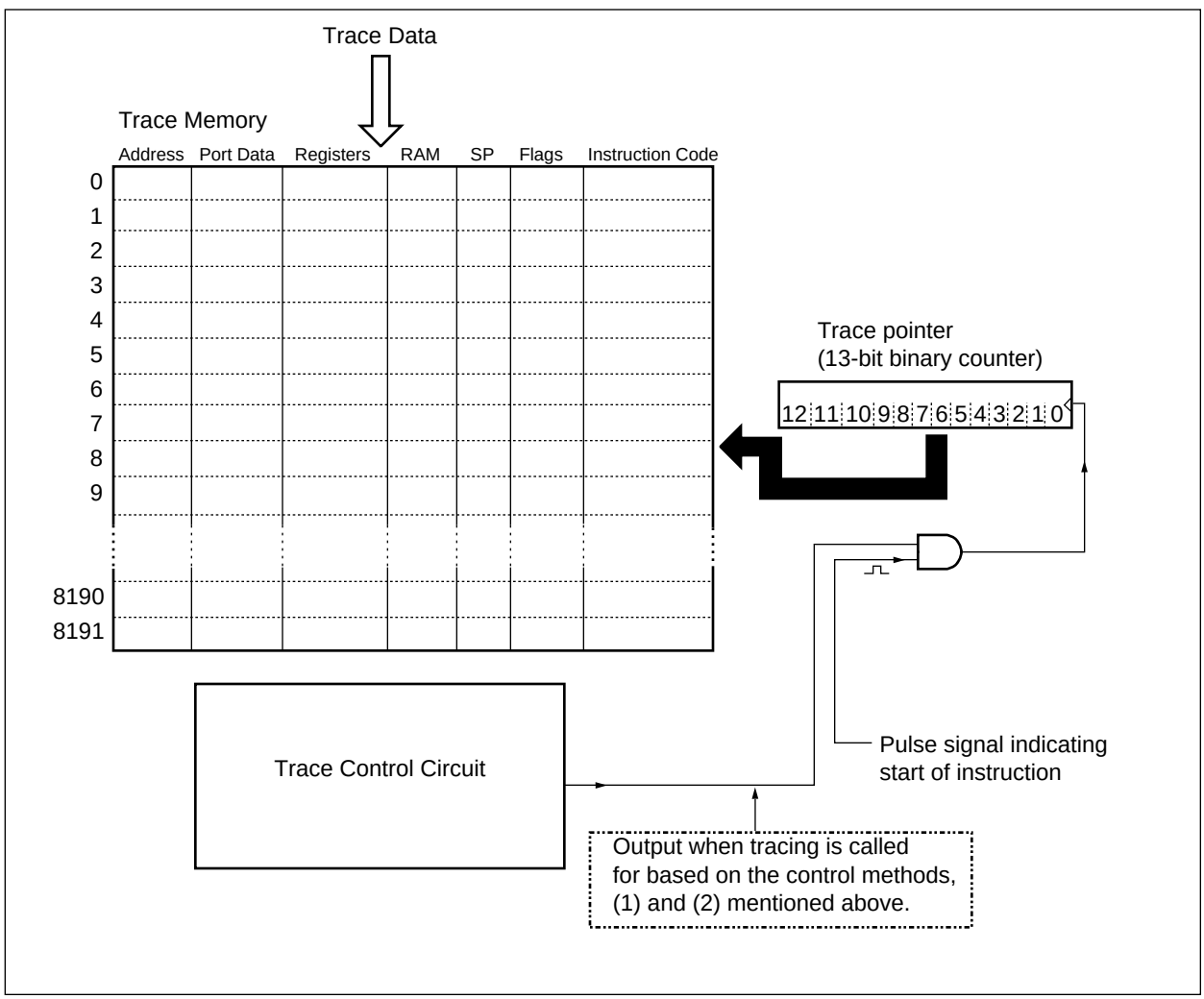

Figure 3-2. Trace Control Conceptual Diagram

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The trace pointer's value indicates the address in trace memory to which data will be written. The trace pointer is incremented at the start of each instruction while the conditions of the previously described control methods are satisfied. As a result, while trace conditions are satisfied, the trace memory addresses written are updated one by one as trace data is stored at each.

The trace pointer is a 13-bit counter, so its value will be between 0 and 1FFFH (in decimal, 0 and 8191). When the trace pointer exceeds 1FFFH and the next trace data arrives, the trace pointer overflows and becomes 0. In other words, when traced data exceeds 8192 steps, it will be overwritten in order from the oldest data in trace memory.

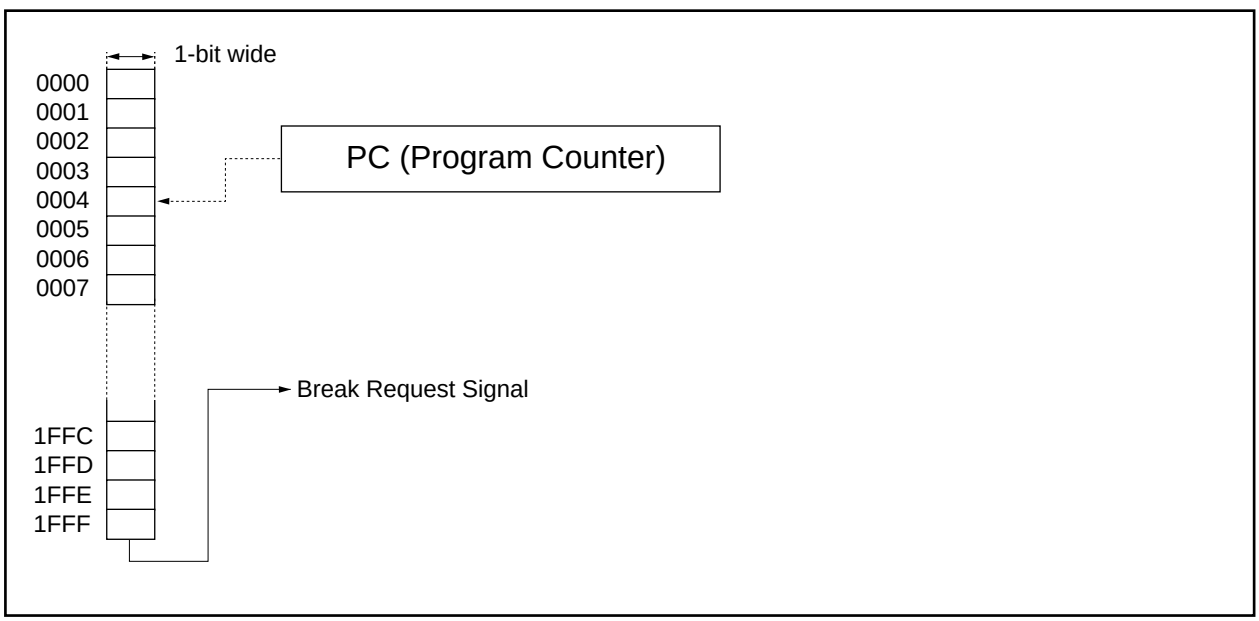
3.1.5. Break Functions

The following methods for breaking program execution are available with the EASE64162/164.

(a) Breakpoint bit breaks

The EASE64162/164 has a 1-bit wide memory that corresponds 1-for-1 with the entire program memory address space (0-1FFFH). This memory is called *breakpoint bits memory* or *breakpoint bits*.

Figure 3-3. Breakpoint Bits Conceptual Diagram



Breakpoint bits can be set to 1 or 0 with the FBP (Fill BreakPoint) command, EBP (Enable BreakPoint) command, and RBP (Reset BreakPoint) command. During emulation execution, the breakpoint bit corresponding to each executed address is referenced, and if "1," a break request signal is output (refer to Figure 3-3).

By using breakpoint bits, breakpoints can be set throughout the entire address space without a limit to their number. (In this manual breaks generated by breakpoint bits are called *breakpoint bit breaks* to clearly distinguish them from *address breaks*, which are generated by break addresses specified as break parameters of the **G** command.)

SEE **DBP, FBP, EBP, RBP, SBC, DBC**

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(b) Trace pointer overflow breaks

The EASE64162/164 can cause a break using overflow of the trace pointer. The trace pointer is a 13-bit counter that represents a location in trace memory. When the trace pointer exceeds 1FFFH (8192 steps), it overflows. The overflow of the trace pointer can be used as a break condition.

DTR, FTR, ETR, RTR, STT, RTT, DTT, SBC, DBC

(c) Cycle counter overflow breaks

The EASE64162/164 has a 32-bit counter that increments every step (called the *cycle counter*). The overflow of the cycle counter can be used as a break condition.

SCT, RCT, DCT, CCC, DCC, SBC, DBC

(d) ESC key breaks

Press the host computer's **ESC** key to forcibly stop G command execution (realtime emulation).

(e) Breaks specified during **G** command input

- Break at specified address (with pass count)
- Break when specified data matches data at a specified address in data memory
- Break when specified data matches data in A register or B register

G, CTDM, DTDM

(f) N area access breaks

The EASE64162/164 will forcibly break when it accesses an area that exceeds the maximum address for its respective chip modes (☞1). However, N area access breaks will not occur when code memory is expanded (EXPAND ON mode).

The maximum address of the program memory area differs for each chip mode. In MSM64162 mode it is 7DFH, and in MSM64164 mode it is FDFH.

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❑ *Break request mask function*

The break conditions explained in (a)-(c) above can be masked. As shown in Figure 3-4, each break condition can be selectively and independently masked using a register called the *break condition register.*

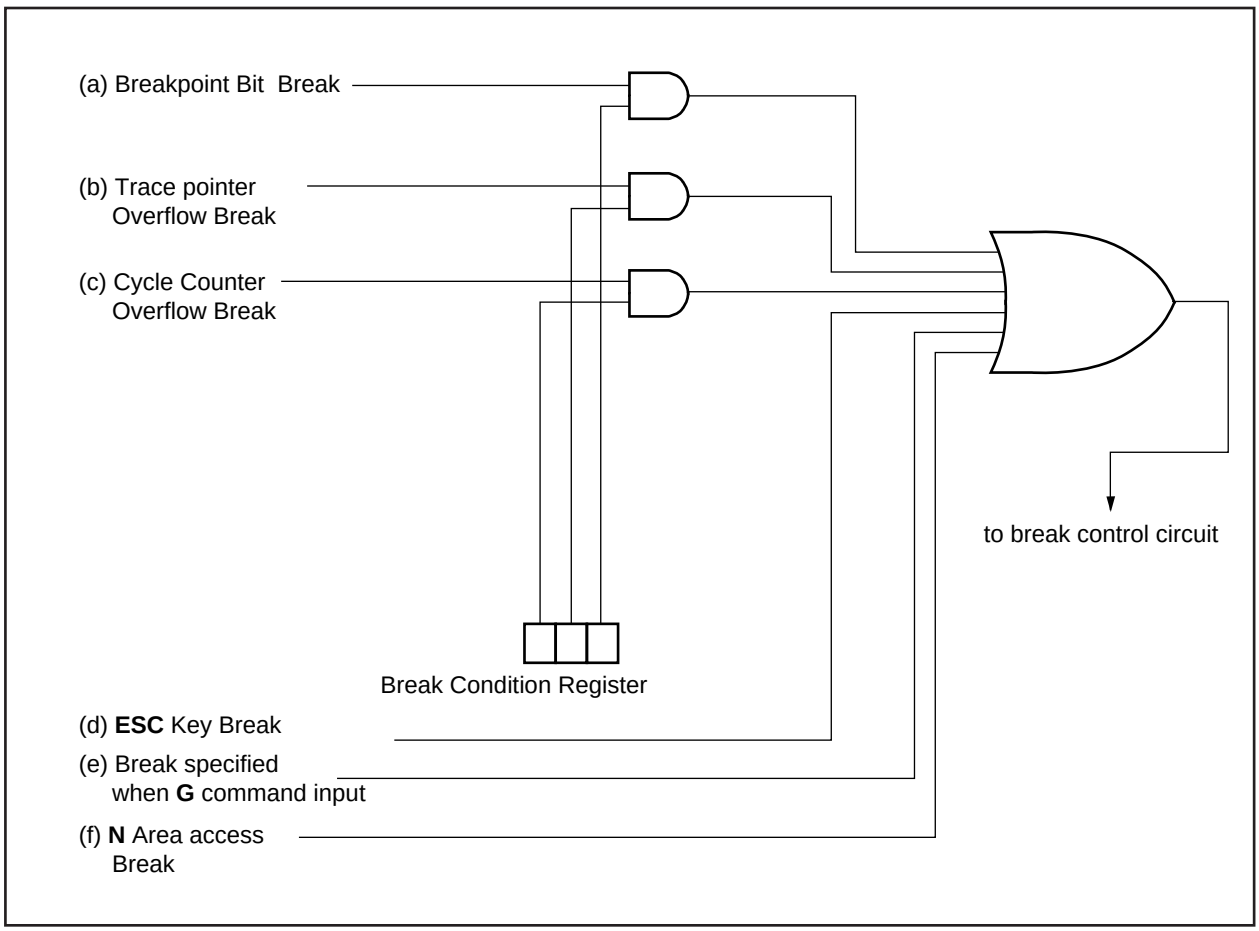

Figure 3-4. Break Masking

The order of bits in the break condition register of Figure 3-4 does not necessarily match the order of bits in the actual register. The purpose of the this figure is to shown how break conditions are masked, so the break conditions are listed in their order of appearance in the previous section.

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3.1.6. Performance/Coverage Functions

The EASE64162/164 has the following performance/coverage functions.

(a) Check for program areas not yet passed

The EASE64162/164 has a 8192 x 1-bit *instruction executed bits memory* (or *IE bit memory*) that corresponds 1-for-1 to code memory's entire address (0H-1FFFH). Whenever an instruction is executed, the contents of IE bit memory at the address corresponding to the instruction will be set to "1." By examining the contents of IE bit memory, one can see which program areas have not been passed (or debugged).

RIE, DIE

(b) Measuring elapsed time

Elapsed execution time for a specified block can be measured by using the EASE64162/164 internal 32-bit cycle counter (CC).

CCC, DCC, SCT, RCT, DCT

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3.1.7. EPROM Programmer

The EASE64162/164 has an internal EPROM programmer (EPROM writer). By using the EPROM programmer, EPROM contents can be transferred to code memory, and contents of a code memory area can be written to EPROM.

In addition, the EPROM programmer can be used to read mask option data (☞1).

The types of EPROM that the EPROM programmer can write are as follows:

2764, 27128, 27256, 27512, 27C64, 27C128, 27C256, 27C512

SEE **TPR, VPR, PPR, TYPE, TPRM, VPRM**

DO NOT USE THE EPROM PROGRAMMER FOR PURPOSES OTHER THAN DEBUGGING PROGRAMS. IF RELIABILITY IN WRITE CHARACTERISTICS IS NECESSARY, THEN USE AN EPROM PROGRAMMER DESIGNED FOR THAT PURPOSE.

☞ 1 Refer to Appendix 7, “Mounting EPROMs,” for information about how to mount EPROMs.

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3.1.8. Indicators

POWER indicator (red)

This indicator will light after EASE64162/164 power is turned on and correct operation begins.

RUN indicator (green)

This indicator will dark after EASE64162/164 power is turned on and correct operation begins. It will also light during while emulation is executing and while EPROM programmer commands are executing.

TPR, VPR, PPR, TPRM, VPRM, G, STP

PORT5V indicator (green)

This indicator will light when the user connector interface power supply is being supplied from the emulator's internal power supply.

PORT3V indicator (green)

This indicator will light when the user connector interface power supply is being supplied from an external power source (+3V ~ +5V).

CIPS

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3.2. EASE64162/164 Emulator Initialization

3.2.1. Setting Operating Frequency

As explained in Section 1.3, the EASE64162/164 operates with a clock supplied from an internal oscillation circuit (32.768 KHz or 400 KHz) when shipped. Oki Electric normally recommends that the EASE64162/164 be used as it is with these settings. Users who do not intend to change this setting can skip this section and proceed to section 3.2.2.

There are two methods for changing the clock settings.

(a) Oscillation clocks of crystal board and CROSC board in emulator

As explained in Section 1.2, the EASE64162/164 operates with a clock supplied from an internal oscillation circuit (32.768 KHz or 400 KHz) when shipped. The crystal for the internal oscillation circuit of low-speed mode is mounted on the internal crystal board. The oscillation resistor for the internal oscillation circuit of high-speed mode is mounted on the internal CROSC board. The crystal board and CROSC board can be removed by first taking off the crystal board cover on the EASE64162/164's right side (see Figures 3-5 and 3-6).

The crystal board can be made to oscillate for use by soldering on a commercial crystal and oscillation resistor and capacitors. The CROSC board can be made to oscillate for use by soldering on a commercial oscillation resistor. The CROSC board is supplied in two versions: 1.5V and 3.0V. Select a resistor that matches the power supply voltage of the target chip that you will use.

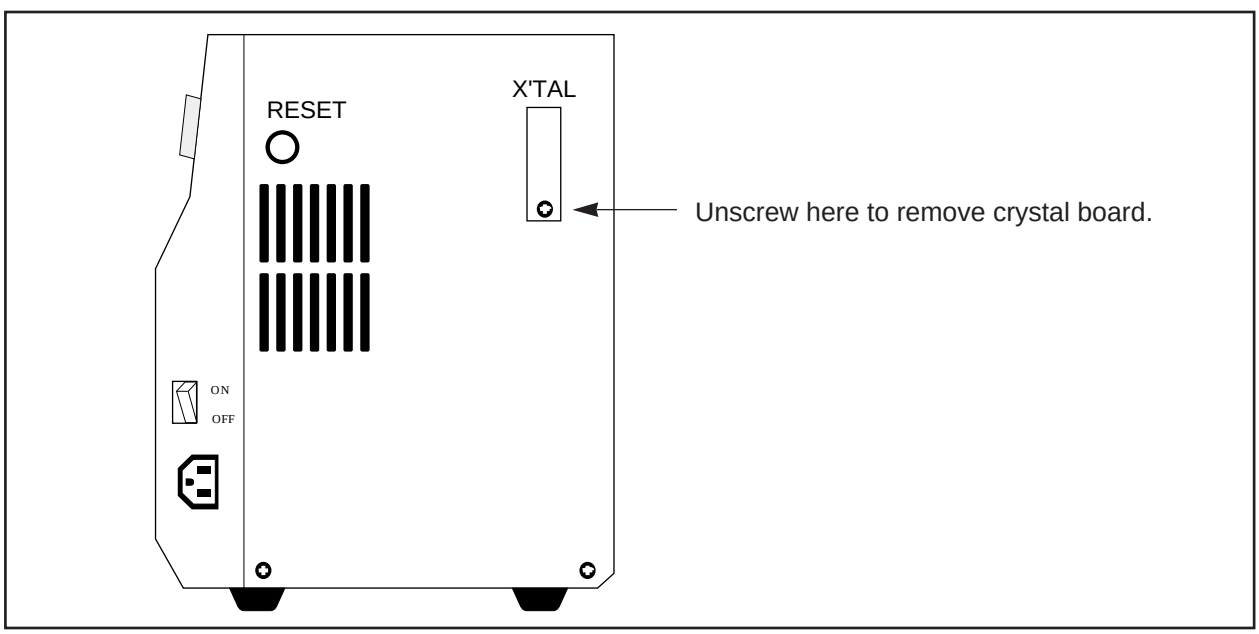

Figure 3-5. Removing Crystal Board (1)

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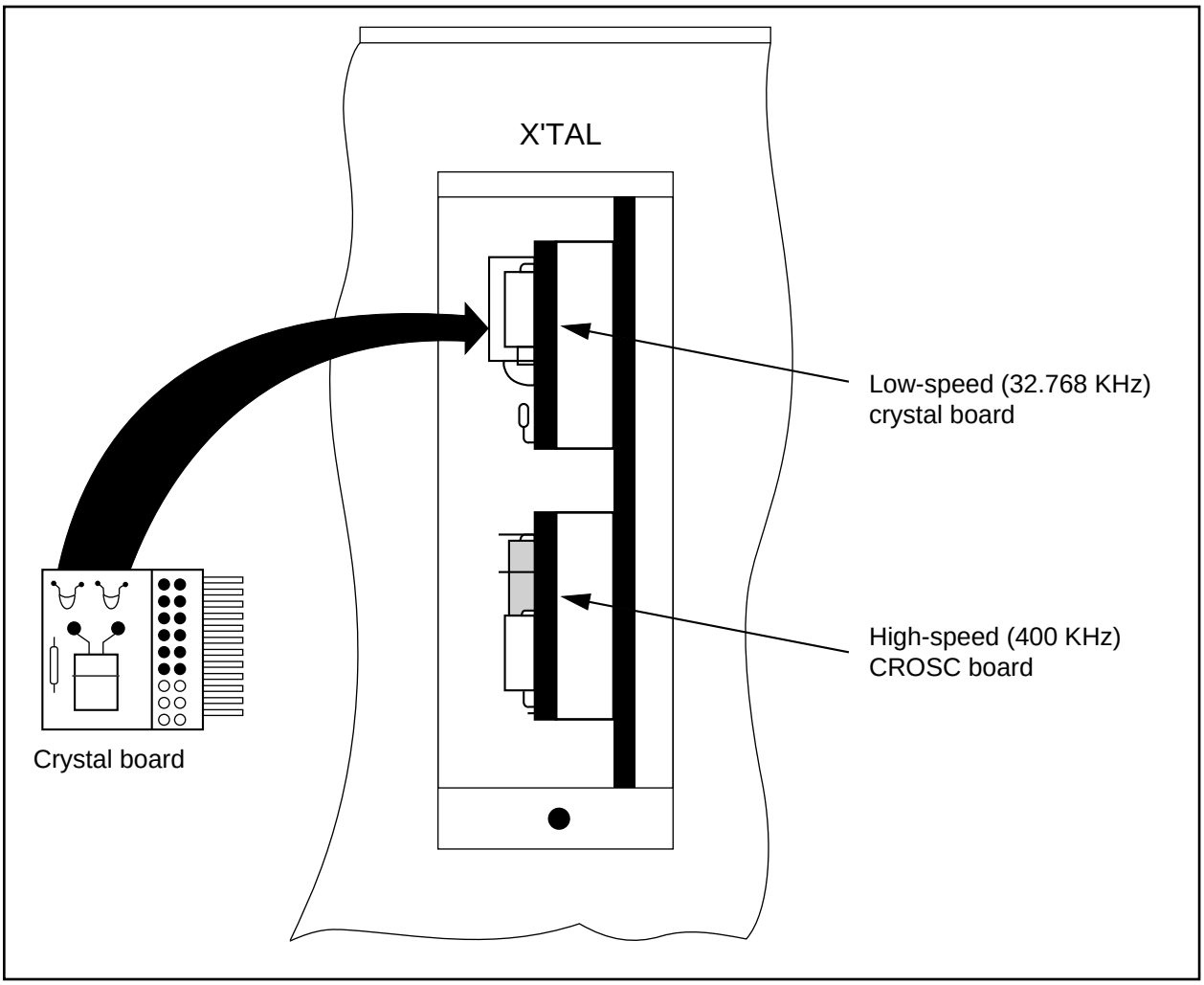

Figure 3-6. Removing Crystal Board (2)

As shown in Figure 3-6, the low-speed (32.768 KHz) crystal board and high-speed (400 KHz) CROSC board are internal to the EASE64162/164. The EASE64162/164 emulator's oscillation circuits are shown in Figures 3-7 and 3-8.

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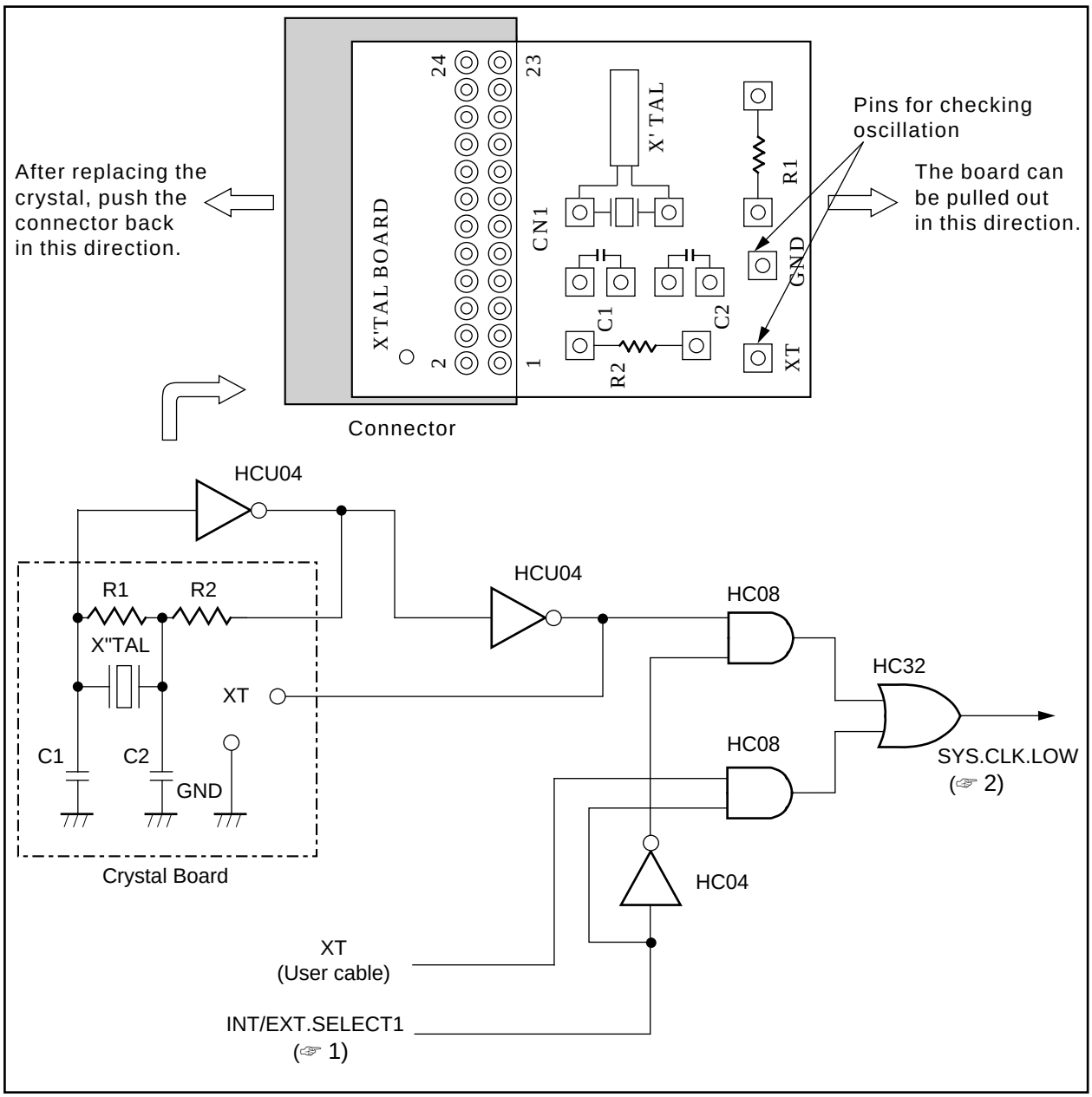

Figure 3-7. Crystal Board And Oscillation Circuit

☞ 1 The INT/EXT•SECLECT1 signal is switched by the CCLK command. It determines whether the oscillation source will be from the internal crystal board of from the user cable XT pin.

☞ 2 EASE64162/164 operates with this clock in low-speed mode.

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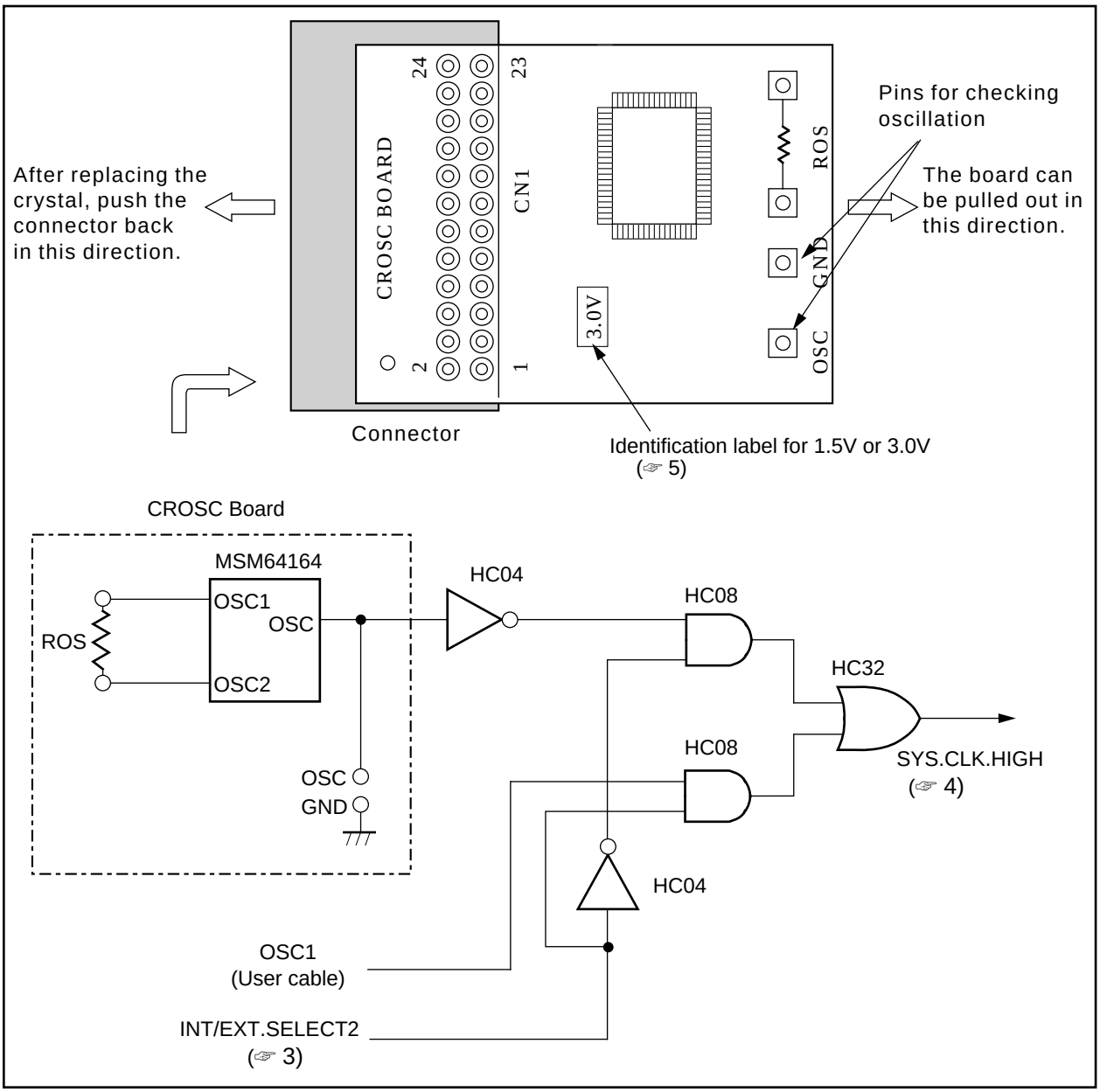

Figure 3-8. CROSC Board And Oscillation Circuit

☞ **3** The INT/EXT•SELECT2 signal is switched by the CCLK command. It determines whether the oscillation source will be from the internal crystal board of from the user cable OSC1 pin.

☞ **4** EASE64162/164 operates with this clock in high-speed mode.

☞ **5** The CROSC board is supplied in two versions: 1.5V and 3.0V. Select a resistor that matches the power supply voltage of the target chip that you will use.

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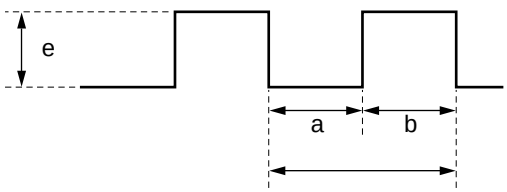
(b) User cable XT pin and OSC1 pin inputs

The emulator can be made to operate from clocks input on the user cable XT pin and OSC1 pin.

SEE **CCLK, DCLK**

Use a signal like that shown below for clocks input on the user cable XT pin and OSC1 pin.



Duty ratio a: b = 1:1
Frequency c = operating frequency
Voltage e= +4.75 to +5.0 V

If you are using the emulator by oscillating from the crystal on the crystal board, then always verify that it oscillates correctly. Depending on the crystal's type and manufacturer, it might not oscillate.

If you have changed the oscillation resistor (ROS) on the CROSC board, then always verify its oscillation. Depending on the resistor's value, it might not oscillate. Refer to the user's manual of each chip for the range of resistor values.

There is no high-speed clock with the MSM64162D. Please be aware of this if using the EASE64162/164 in MSM64162 mode to evaluate a MSM64162D.

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3.2.2. EASE64162/164 Switch Settings

There is a 7-bit dipswitch toward the top of the left panel of the EASE64162/164, labeled BAUD RATE SW (refer to Figure 3-9). The baud rate switch is explained below.

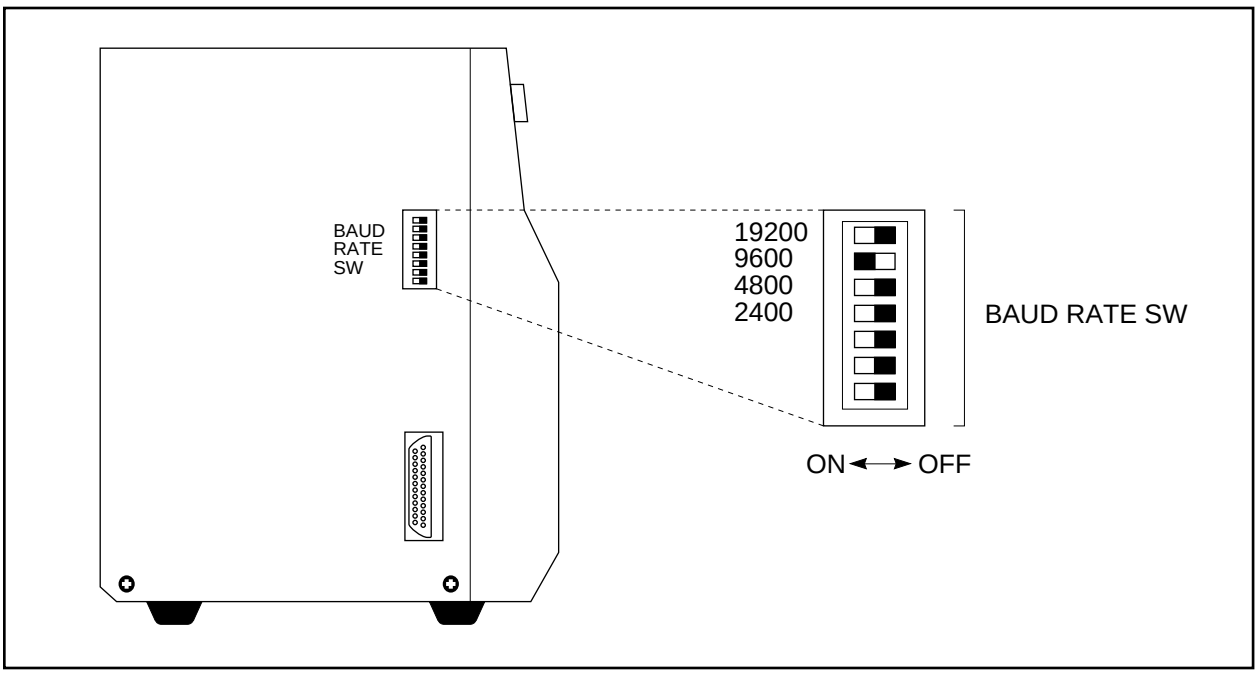

Figure 3-9. EASE64162/164 Dipswitch

[BAUD RATE SW]

These switches set the baud rate between EASE64162/164 and the host computer.

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❑ 19200~2400 baud rate switches

These switches set the baud rate of the RS232C interface. They are used to match the EASE64162/164 baud rate with that of the host computer.

EASE64162/164 is set as follows when shipped.

- Transfer format 8 bits, 1 stop bit, no parity
- Baud rate 9600 bps

The host computer must be set to match all the above EASE64162/164 parameters except for the baud rate (☞1). The baud rate can be set to a value 19200 bps to 2400 bps using the baud rate switches (refer to Table 3-1 below).

Table 3-1. Baud Rate Switch Settings

BPS / BAUD RATE SW	19200	9600	4800	2400
19200	ON	OFF	OFF	OFF
9600	OFF	ON	OFF	OFF
4800	OFF	OFF	ON	OFF
2400	OFF	OFF	OFF	ON

In Table 3-1:
ON Flip bit switch to the left.
OFF Flip bit switch to the right.

Oki if800 series computers are set using the SWITCH command.
PC9801 series computers are set using the SPEED command.
IBM-PC computers use the INT232C command (described in Section 3.2.5).

For details, refer to your host computer's user manual.

With the if800 series, after changing parameters with the SWITCH command, be sure to boot up the computer again by pushing the if800 reset button. Otherwise, the RS232C parameters will not be set correctly.

The EASE64162/164 settings must match the settings of the host computer connected to the RS232C cable. If the settings do not match, then the EASE64162/164 cannot operate.

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3.2.3. Connecting The MSM64162/164 ADC POD

The MSM64162/164 ADC POD provides the CR oscillator of the MSM64162 and MSM64164's A/D converter. There are two types of MSM64162/164 ADC POD: 1.5V and 3.0V. (☞1)

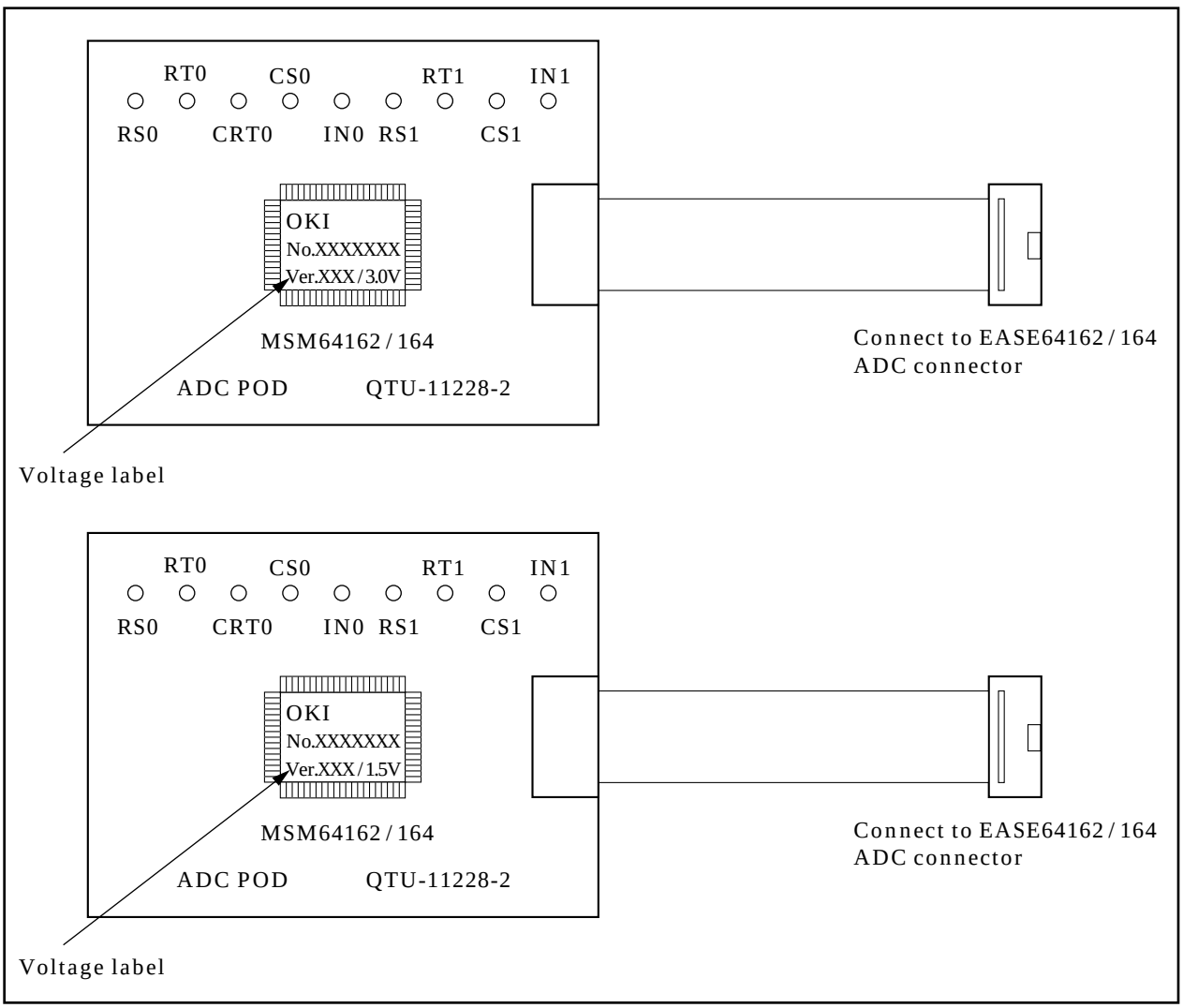

Figure 3-10. External Views Of MSM64162/164 ADC POD

Each of the pins shown in Figure 3-10 (RS0, RT0, CRT0, CS0, IN0, RS1, RT1, CS1, IN1) is identical to the corresponding MSM64162 and MSM64164 pin. Connect resistors and capacitors that match the oscillation modes. Refer to the user's manual of your target chip for specific interfacing details.

☞ 1 The CR oscillation characteristics differ for 1.5V and 3.0V. Select values that match the power supply voltage of the target chip.

! Be sure to connect the ADC POD with the emulator main unit's power supply switched off.

! Note that the MSM64162D chip does not have the four pins RS1, RT1, CS1, and IN1.

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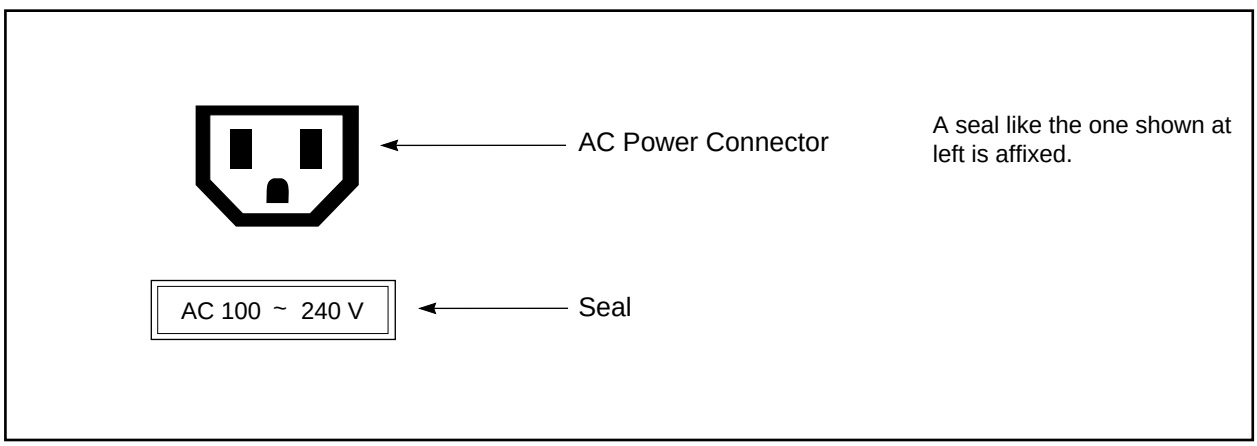
3.2.4. Confirming EASE64162/164 Power Supply Voltage

The EASE64162/164 has an internal power supply circuit that uses normal household power. The rated voltage of the power supply circuit is AC 100~240 V (50/60Hz).

The current voltage range setting is shown on a seal affixed below the AC power supply connector. Be sure that the AC power supply that you will use matches this range.



ABSOLUTELY DO NOT USE A POWER SUPPLY OTHER THAN AC 100-240 V. DOING SO COULD CAUSE A FIRE.

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3.2.5. Starting the EASE64162/164 Emulator

The procedure for starting the EASE64162/164 emulator is as follows.

(1) Verify that the following EASE64162/164 emulator (hereafter called the emulation kit) switches are set correctly.

- Baud rate switches

For details on switch settings, refer to Section 3.2.2, “EASE64162/164 Switch Settings.”

(2) Verify that the necessary cable types are connected to the emulation kit.

- Is the AC power supply connector connected to the AC power supply cable?
- Is the emulation kit connected to the host computer?
- Is the user cable connected (when interfacing to the user application system)?
- Is the M64162/164 ADC POD connected?

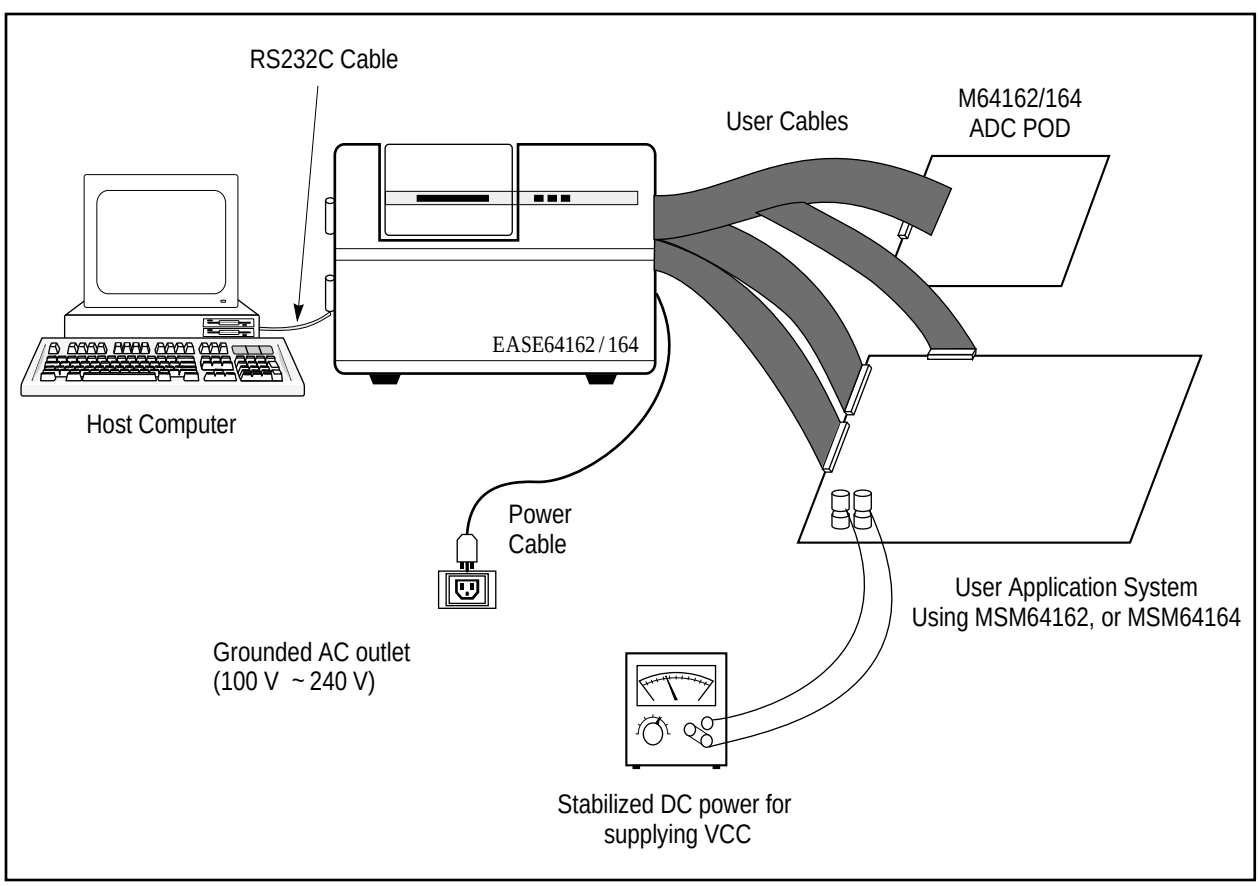

Figure 3-11. Cable Connection Diagram

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The system will start even if the user application system is not connected. In this case, do not connect the user cables.

Vcc is not supplied to the user application system from the user cables (however, GND is connected to the user application system through the user cables). If Vcc must be supplied to the user application system, then supply it from a separate power supply (refer to Figure 3-11).

(3) Turn on the host computer power supply, and start MS-DOS (PC-DOS).

Use MS-DOS or PC-DOS version 3.1 or later.

(4) Set the host computer's transfer parameters.

When the EASE64162/164 is shipped, its data transfer parameters are as follows.

Communication method	RS232C interface
Transfer speed	9600 bps
Transfer format	8 bits, 1 stop bit, no parity

Oki if800 series computers are set using the **SWITCH** command.

PC9801 series computers are set using the **SPEED** command.
For details, refer to the manual of the host computer.

With the if800 series after changing parameters with the **SWITCH** command, if the if800 reset button is pushed once more to boot up the computer again, then be sure to note that the RS232C parameters will not be set correctly.

IBM-PC computers use the INT232C program (described in step 5 below).

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(5) Invoke INT232C.
This step should be executed only if you are using an IBM-PC computer.
For other computers, skip this step and go to step 6.

INT232C is a TSR (Transient but Stay Resident) program. It sets the RS232C interface operating conditions of the IBM-PC/AT, and simultaneously enables interrupt signals.

Invoking this program once will place it in host computer memory, where it will reside until removed. The method for invoking and removing INT232C is shown below.

```
A>  INT232C [<options>[;<baud>,<parity>,<databits>,<stopbits>]] ↵
```

The brackets [ ] can be omitted. When omitted, the default values of the following explanations apply.

<options>

X	Perform XON/XOFF control (☞1).
M	Perform modem control.
*	Do not perform XON/XOFF or modem control.
R	Remove resident INT232C.

<baud>

Specifies the baud rate. Choose one of the following.

2400, 4800, 9600 (default)

<parity>

Specifies whether and what kind of parity checking to perform. Choose one of the following.

N	Do not perform parity checking (default).
O	Perform odd parity checking.
E	Perform even parity checking.

<databits>

Specifies the number of data bits. Choose one of the following.

7, 8 (default)

<stopbits>

Specifies the number of stop bits. Choose one of the following.

1 (default), 2

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EASE64162/164 does not perform XON/XOFF control. Therefore, only use '*****' or 'R" for the INT232C option. With any other settings, the EASE64X will not operate.

Example

A> INT232C * ↵
(This is the same as: **INT232C *;9600,N,8,1**

A> INT232C *;1200 ↵

A> INT232C R ↵

❏ *List of messages*

INT232C outputs the following messages.

- **INT232C has been removed from memory.**
- **INT232C has not been loaded.**
- **INT232C has already been loaded.**
- **INT232C has been loaded.**

(6) Start the EASE64X debugger.

The debugger executable file EASE64X.EXE can be started from the directory that stores it or from another directory.

(1) Starting from the directory that stores **EASE64X.EXE**

Input the following after the DOS prompt.

```
A> EASE64X ↵
```

(2) Starting from another directory

If the **PATH** environment variable includes the directory that contains **EASE64X.EXE**, then input is the same as in (1). If not specified by **PATH**, then the **EASE64X** debugger is invoked as follows.

```
A> pathname\EASE64X ↵
```

Here *pathname* is the absolute path name of the directory that contains **EASE64X.EXE**.

(7) The following message will be displayed on the console, and the system will wait for a reset switch input from emulation kit.

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```
EASE64X Debugger Ver. x.xx
Copyright (C) xxxx. OKI Electric Ind. Co., Ltd.
```

(8) Turn on the emulation kit power supply switch and the power supply of the user application system. The following message will be displayed on the host computer, and emulator system initialization will end.

```
Low-Power Series Emulator <<EASE64162/164>> Ver.X.XX
```

(9) A "*" prompt will be displayed, and the system will wait for command input.

```
*
```

(10) Debugger commands can now be input.

(1) For more information on the emulator's RS232C interface, refer to Section 3.2.2, "EASE64162/164 Switch Settings."
(2) The user application system cannot be supplied with Vcc taken from the emulator.
(3) Before turning on the emulator's power supply, verify that the connected AC power supply voltage is the same as the voltage shown on the AC power supply connector.
(4) If the emulator does not start, then refer to Appendix 6.
(5) Table 3-2 shows the various items initialized when EASE64162/164 is turned on, when the reset switch is pressed, when a RST command is executed, and when a RST E command is executed. A circle indicates that the item is initialized, while a dash indicates that it is not initialized. Also, when the reset switch is pressed, all open files will be closed.

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Table 3-2 Initialization

Item	Contents Initialized	Power Applied	Reset Switch Pressed	RST Command	RST E Command
Evaluation Board	Initializes to same state as when a reset is input to a microcontroller in the MSM64162/164.	O	O	O	O
Break Conditions	Only breakpoint bits are enabled.	O	–	–	–
Breakpoint Bits	All areas cleared to "0", disabling all breakpoint bit breaks.	O	–	–	–
Break Status	Cleared to state of no breaks generated.	O	O	O	–
Trace Pointer	Cleared to "0"	O	–	–	–
Trace Trigger	Trace trigger disabled; set to address tracing.	O	O	O	–
Trace Enable Bits	All areas set to 1, enabling trace enable bit tracing.	O	–	–	–
Cycle Counter	Set to default mode.	O	O	O	–
EPROM Programmer Setting	Set to type 27512	O	–	–	–
Reset Input from User Cable	Prohibited	O	–	–	–
Trace Object Settings	Set to BCF, BSR0, BEF, and BSR1.	O	–	–	–
Memory Expansion	Set to EXPAND OFF state.	O	–	–	–

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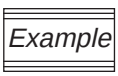
3.3. EASE64X Debugger Commands

3.3.1. Debugger Command Syntax

The explanations of this manual make use of the following symbols.

- UPPER CASE — Debugger command names are expressed with upper case letters.



DCM, LOD, G

- *Italics* — Italicized expressions indicate user-supplied information (changes according to operator input). The following italicized words are used.

parm	This indicates a general parameter that follows after a command name. It includes *fname*, *address*, *data*, *number*, and *mnemonic*, explained below.
fname	This indicates a file name, including drive name, path name, primary name, and extension. Except for the extension, a file name is handled with the exact same processing as a DOS file name. Extensions are handled differently depending on the command (when omitted for some commands, default extensions exist).
address	This indicates an address value input.
data	This indicates a data value input.
number *count*	A number is used to indicate a cycle counter value input, step *count*, etc. A *count* indicates input of a pass count value of **G** command breakpoints. Both are recognized as decimal numbers.
mnemonic	This indicates an optional string input from a set of strings that is determined by the command type.

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- Special symbols — These symbols have the following special meanings for explaining command syntax.

Δ	This indicates white space (☞1).
↵	This means a carriage return input.
{xxxx}	The xxxx means an optional string used within an explanation. The xxxx enclosed in { } means that it can be omitted.
___ (underline)	When text displayed automatically by the debugger and operator input are mixed on one line, the underlined portion indicates user input.

☞ 1 White space is a string consisting of one or more spaces (ASCII code 20H) and/or tabs (ASCII code 09H) in any order.

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3.3.1.1. Character Set

EASE64X debugger commands can make use of the following character set.

1. **Alphabetic characters (upper and lower case)**

   A B C D E F G H I J K L M
   N O P Q R S T U V W X Y Z
   a b c d e f g h i j k l m
   n o p q r s t u v w x y z

2. **Digits**

   0 1 2 3 4 5 6 7 8 9

3. **Delimiters**

   TAB space CR (☞ 2)

4. **Other special symbols**

   , ( ) – * >

☞ **2** TAB is ASCII code 09H; space is ASCII code 20H; CR (carriage return) is ASCII code 0DH.

! All characters usable with EASE64X debugger commands are included in this character set. However, any character can be coded in commend fields, described later.

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3.3.1.2. Command Format

❏ *Debugger Command Format*

command_name ∆ *parm, parm . . . , parm* ↵

Debugger commands consist of a command name followed by several parameters (*parm*). White space always delimits between the command name and *parm*. Commas (,) delimit between *parm* and *parm*. A command line is recognized as ending at the point a carriage return (↵) is input.

❏ *Comment Input*

The entire string following a semicolon (;) is recognized as a comment. It will be ignored during command parsing. For example, the entire input line below is a comment, so the emulator will perform no operation.

Example

```
* ;;;; This is an example of whole comment line ;;;;
```

❏ *Command Name Format*

Command names are strings consisting of 1-7 alphabetic characters. They express instructions given to the debugger. A command name's function is indicated by its first character. Second and following characters are keywords for memory and internal registers of the evaluation board or emulator.

D	**(Display)**	Data display commands
C	**(Change)**	Data change commands
E	**(Enable)**	Enable commands
F	**(Fill)**	Data fill commands
R	**(Reset)**	Reset commands
S	**(Set)**	Set commands
P	**(Program)**	Commands for writing data to EPROM
T	**(Transfer)**	Coommands for reading data from EPROM
V	**(Verify)**	Commands for comparing memory contents
G	**(Go)**	Execute (emulation) commands

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3.3.1.3 Command Summary

This section gives a summary table of all EASE64X commands.

Command Group Name			Page
No.	**Name**	Function	Reference page
	Syntax		
	Parameters / options		

Detailed explanations of each command are given in 3.3.4. The table of this section was created with the purpose of first giving a quick overview of the commands, and then in the future serving as a command index.

The tavle of this section follows the format below.

- No. — Sequence number
- Name — Name of the command
- Syntax — Syntax of the command
- Parameters and Options — Describes each of the parameters and options expressed in Command Syntax
- Reference Page — The reference page for a explanation in 3.3.4 “EASE64X Command Details”.

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	Evaluation Board Access Commands		Page
1	**CHIP**	Set target chip	3-61
	CHIP [Δ *mnemonic*] ↵		
	mnemonic : 64164, 64164		
2	**D**	Display contents of target chip registers	3-62
	D ↵ or D *mnemonic* ↵		
	mnemonic : PC, B, A, HL, XY, CY, SP, BSR0, BSR1, BCF, BEF, ,P0, ,P1D, ,P2D, ,P3D, ,P4D, ,SBUF, ,SCON, ,FCON, ,BDCON, ,BFCON, ,CAPR0, ,CAPR1, ,CAPCON, ,TBCR, ,DSPCON, CNTA, ,CNTB, ,ADCON0, ,ADCON1, ,IE0, ,IE1, ,IE2, ,IRQ0, ,IRQ1, ,IRQ2, ,BUPCON, ,MIEF	
3	**C**	Change contents of target chip registers	3-62
	C*mnemonic* Δ *data* ↵		
	mnemonic : PC (0 to 7DF or 0 to FDF) B (0 to F), A (0 to F), HL (0 to FF), XY (0 to FF), SP (0 to FF), BSR0 (0 to F), BSR1 (0 to F), BCF (0, 1), BEF (0, 1), P1D (0 to F), P2D (0 to F), P3D (0 to F), P4D (0 to F) ,CAPR0 (0 to FF), ,CAPR1 (0 to FF), ,CAPCON (0 to 1), ,CNTA (0 to 79999), ,CNTB (0 to 3FFF), ,ADCON0 (0 to 3), ,ADCON1 (0 to F), ,SBUF (0 to FF), ,SCON (0 to F), ,FCON (0, 1), ,BDCON (0 to F), ,BFCON (0, 1 or 0 to F), ,BUPCON (0 to 3 or 0, 1) ,TBCR (0 to F), ,DSPCON (0 to 3), ,IE0 (0 to F), ,IE1 (0 to F), ,IE2 (0, 1), ,IRQ0 (0 to F), ,IRQ1 (0 to F), ,IRQ2 (0 to F), ,MIEF (0, 1) ,P20CON (0 to F), ,P21CON (0 to F), ,P22CON (0 to F), ,P23CON (0 to F), ,P30CON (0 to F), ,P31CON (0 to F), ,P32CON (0 to F), ,P33CON (0 to F), ,P40CON (0 to F), ,P41CON (0 to F), ,P42CON (0 to F), ,P43CON (0 to F), ,P01CON (0 to F) (☞1)	

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	Evaluation Board Access Commands (cont.)		Page
4	**DDSPR**	Display Display Register	3-67
	DDSPR ↵		
5	**CDSPR**	Change Display Register	3-67
	CDSPR Δ *mnemonic* ↵		
	mnemonic : 0~20 . . . MSM64162 mode 0~30 . . . MSM64164 mode		

☞ 1

- The numbers in parentheses indicate the input data range for the corresponding *mnemonics*.
- The data range of PC is 0H~7DFH in MSM64162 mode and 0H~FDFH in MSM64164 mode.
- When TBCR is changed, it will be reset to 0 regardless of the specified data.
- The change data of CNTA is a decimal value.
- In MSM64162 mode, the following mnemonics are invalid.

  P4D, SBUF, SCON, P40CON, P41CON, P42CON, P43CON
- The data range of BFCON is 0H or 1H in MSM64162 mode and 0H~FH in MSM64164 mode.
- The data range of BUPCON is 0H~3H in MSM64162 mode and 0H or 1H in MSM64164 mode.
- The FCON register does not exist in the MSM64162D chip.
- If invalid data (5H, 6H, or 7H) is written to the ADCON1 register when evaluating a MSM64162D, then the emulator may operate incorrectly.

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	Code Memory Commands		Page
1	**DCM**	Display Code Memory	3-71
	DCM Δ *address* [, *address*] ↵ or DCM Δ * ↵		
	address : 0 to 7DF . . . MSM64162 mode 0 to FDF . . . MSM64164 mode * : displays entire address range		
2	**CCM**	Change Code Memory	3-73
	CCM Δ *address* ↵		
	address : 0 to 7DF . . . MSM64162 mode 0 to FDF . . . MSM64164 mode		
3	**FCM**	Fill Code Memory	3-75
	FCM Δ *address* , *address* [, *data*] ↵ or FCM Δ * [, *data*] ↵		
	address : 0 to 7DF . . . MSM64162 mode 0 to FDF . . . MSM64164 mode * : fills entire address range *data* : 0 to FF		
4	**LOD**	Load Disk file program into Code Memory	3-77 3-81
	LOD Δ *fname* ↵		
	fname : [*Pathname*] *filename* [*extension*]		
5	**SAV**	Save Code Memory into Disk file	3-78 3-81
	SAV Δ *fname* [Δ *address , address*] ↵		
	address : 0 to 7DF . . . MSM64162 mode 0 to FDF . . . MSM64164 mode *fname* : [*Pathname*] *filename* [*extension*]		

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Code Memory Commands (cont.)			Page
6	**VER**	Verify Disk file with Code Memory	3-79 3-81
	VER Δ *fname* [Δ *address* , *address*] ↵		
	address : 0 to 7DF . . . MSM64162 mode 0 to FDF . . . MSM64164 mode *fname* : [*Pathname*] *filename* [*extension*]		
7	**ASM**	Line Assembler Command This command stores the code it generates in code memory.	3-82
	ASM Δ *address* ↵		
	address : 0 to 7DF . . . MSM64162 mode 0 to FDF . . . MSM64164 mode		
8	**DASM**	Disassembler Command This command disassembles program memory contents of a specified address range.	3-84
	DASM Δ *address* [, *address*] ↵ or DASM Δ ***** ↵		
	address : 0 to 7DF . . . MSM64162 mode 0 to FDF . . . MSM64164 mode ***** : displays entire address range		

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	Data Memory Commands		Page
1	**DDM**	Display Data Memory	3-87
	DDM Δ *address* [, *address*] ↵ or DDM Δ * ↵		
	address : 780 to 7FF . . . MSM64162 mode 700 to 7FF . . . MSM64164 mode * : displays entire address range		
2	**CDM**	Change Data Memory	3-89
	CDM Δ *address* ↵		
	address : 780 to 7FF . . . MSM64162 mode 700 to 7FF . . . MSM64164 mode		
3	**FDM**	Fill Data Memory	3-91
	FDM Δ *address* , *address* [, *data*] ↵ or FDM Δ * [, *data*] ↵		
	address : 780 to 7FF . . . MSM64162 mode 700 to 7FF . . . MSM64164 mode * : fills entire address range *data* : 0 to FF		

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	Emulation Commands		Page
1	**STP**	Step Execution	3-94
	STP [Δ *number*] [, *address*] ↵ or STP Δ ***** ↵		
	address : 0 to 7DF . . . MSM64162 mode 0 to FDF . . . MSM64164 mode ***** : executes 65535 steps *number* : 1 to 65535		
2	**G**	Realtime Emulation (continuous execution)	3-97
	G [Δ *address*] [, *parm*] ↵		
	parm : *address* [, *address* . . . , *address*] RAM (*data–count*) BAR (*data–count*) *address* (*count*) *address* : 0 to 7DF . . . MSM64162 mode 0 to FDF . . . MSM64164 mode		

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	Break Commands		Page
1	**DBC**	Display Break Condition Register	3-103
	DBC ↵		
2	**SBC**	Set Break Condition Register	3-103
	SBC ↵		
3	**DBS**	Display Break Status	3-109
	DBS ↵		
4	**DBP**	Display Break Point Bits	3-105
	DBP Δ *address* [, *address*] ↵		
	address : 0 to 7DF . . . MSM64162 mode 0 to FDF . . . MSM64164 mode		
5	**EBP**	Enable Break Point Bits	3-106
	EBP Δ *address* [, *address . . .* , *address*] ↵		
	address : 0 to 7DF . . . MSM64162 mode 0 to FDF . . . MSM64164 mode		
6	**RBP**	Reset Break Point Bits	3-105
	RBP Δ *address* [, *address . . .* , *address*] ↵		
	address : 0 to 7DF . . . MSM64162 mode 0 to FDF . . . MSM64164 mode		

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Break Commands			Page
7	**FBP**	Fill Break Point Bits	3-107
	FBP Δ *address* , *address* [, *data*] ↵ or FBP Δ ***** [, *data*] ↵		
	address : 0 to 7DF . . . MSM64162 mode 0 to FDF . . . MSM64164 mode ***** : fills entire address range *data* : 0, 1		

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	Trace Commands		Page
1	**DTM**	Display Trace Memory	3-112
	DTM Δ -*number*$_{-step}$ Δ *number*$_{step}$ ↵ or DTM Δ *number*$_{TP}$ Δ *number*$_{step}$ ↵ or DTM Δ * ↵		
	number$_{-step}$: number of steps to go back (1~8192) *number*$_{step}$: number of steps to display (1~8192) *number*$_{TP}$: value of TP at which to start display (0~8191) * : Display the entire area of trace memory		
2	**CTO**	Change Trace Object	3-118
	CTO ↵		
3	**DTO**	Display Trace Object	3-118
	DTO ↵		
4	**CTDM**	Change Trace Data Memory	3-117
	CTDM [Δ *address*]↵		
	address : 780 to 7FF . . . MSM64162 mode 700 to 7FF . . . MSM64164 mode		
5	**DTDM**	Display Trace Data Memory	3-117
	DTDM ↵		
6	**STT**	Set Trace Trigger	3-120
	STT ↵		

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Trace Commands (continued)			Page
7	**DTT**	Display Trace Trigger	3-118
	DTT ↵		
8	**RTT**	Reset Trace Trigger	3-118
	RTT ↵		
9	**DTR**	Display Trace Enable Bits	3-124
	DTR Δ *address* [, *address . . .* , *address*] ↵ or DTR Δ ***** ↵		
	address : 0 to 7DF . . . MSM64162 mode 0 to FDF . . . MSM64164 mode ***** : displays entire address range		
10	**ETR**	Enable Trace Enable Bits	3-125
	ETR Δ *address* [, *address . . .* , *address*] ↵		
	address : 0 to 7DF . . . MSM64162 mode 0 to FDF . . . MSM64164 mode		
11	**RTR**	Reset Trace Enable Bits	3-125
	RTR Δ *address* [, *address . . .* , *address*] ↵		
	address : 0 to 7DF . . . MSM64162 mode 0 to FDF . . . MSM64164 mode		
12	**FTR**	Fill Trace Enable Bits	3-126
	FTR Δ *address* , *address* [, *data*] ↵ or FTR Δ ***** [, *data*] ↵		
	address : 0 to 7DF . . . MSM64162 mode 0 to FDF . . . MSM64164 mode ***** : fills entire address range *data* : 0, 1		

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Trace Commands (continued)			Page
13	**DTP**	Display Trace Pointer	3-128
	DTP ↵		
14	**RTP**	Reset Trace Pointer	3-128
	RTP ↵		

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Reset Commands			Page
1	**RST**	Reset System and Evaluation Chip	3-130
	RST ↵ Reset the system. RST Δ E ↵ Reset the evaluation chip.		
2	**URST**	Set User Reset Terminal (on user cable)	3-132
	URST [Δ *mnemonic*]↵		
	mnemonic : ON, OFF		

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	Performance/Coverage Commands		Page
1	**DCC**	Display Cycle Counter	3-137
	DCC ↵		
2	**CCC**	Change Cycle Counter	3-138
	CCC Δ [-]*number* ↵		
	number : 0 to 4294967295		
3	**SCT**	Set Cycle Counter Trigger	3-134
	SCT ↵		
4	**DCT**	Display Cycle Counter Trigger	3-134
	DCT↵		
5	**RCT**	Reset Cycle Counter Trigger	3-134
	RCT ↵		
6	**DIE**	Display Instruction Executed Bits	3-139
	DIE Δ *address* [, *address*] or DIE Δ * ↵		
	address : 0 to 7DF . . . MSM64162 mode 0 to FDF . . . MSM64164 mode * : displays entire address range		
7	**RIE**	Reset Instruction Executed Bits	3-139
	RIE ↵		

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	EPROM Programmer Commands		Page
1	**TYPE**	Set EPROM Type	3-142
	TYPE Δ *mnemonic* ↵		
	mnemonic : 64, 128, 256, 512		
2	**PPR**	Program EPROM	3-143
	PPR Δ *address*$_{Code}$, *address*$_{Code}$ [, *address*$_{EPROM}$]↵ or PPR Δ * ↵		
	address $_{Code}$: 0 to 7DF . . . MSM64162 mode 0 to FDF . . . MSM64164 mode *: programs entire address range *address* $_{EPROM}$: EPROM write address		
3	**TPR**	Transfer EPROM into Code Memory	3-145
	TPR Δ *address*$_{Code}$, *address*$_{Code}$ [, *address*$_{EPROM}$]↵ TPR Δ * ↵		
	address $_{Code}$: 0 to 7DF . . . MSM64162 mode 0 to FDF . . . MSM64164 mode *: transfers entire address range *address* $_{EPROM}$: EPROM transfer address		
4	**VPR**	Verify EPROM with Code Memory	3-147
	VPR Δ *address*$_{Code}$, *address*$_{Code}$ [, *address*$_{EPROM}$]↵ VPR Δ * ↵		
	address $_{Code}$: 0 to 7DF . . . MSM64162 mode 0 to FDF . . . MSM64164 mode *: verifies entire address range *address* $_{EPROM}$: EPROM comparison address		

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Mask Option File Commands			Page
1	**LODM**	Load Disk file Mask Option into System memory	3-150
	LODM Δ *fname* ↵		
	fname : [*Pathname*] *filename* [*Extension*]		
2	**VERM**	Verify Disk file with System Memory	3-151
	VERM Δ *fname* ↵		
	fname : [*Pathname*] *filename* [*Extension*]		
3	**PPRM**	Program Mask Option Data into EPROM	3-153
	PPRM ↵		
4	**TPRM**	Transfer EPROM into System Memory	3-154
	TPRM ↵		
5	**VPRM**	Verify EPROM with System Memory	3-155
	VPRM ↵		

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	Commands for Automatic Command Execution		Page
1	**BATCH**	Batch Processing	3-158
	BATCH Δ *fname* ↵		
	fname : [*Pathname*] *filename* [*Extension*]		
2	**PAUSE**	Pause Command Input	3-159
	PAUSE ↵		

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Other Commands			Page
1	**LIST**	Listing (Redirect the Console output to Disk file)	3-161
	LIST Δ *fname* ↵		
	fname : [*Pathname*] *filename* [*Extension*]		
2	**NLST**	No Listing (Cancel the Console output Redirection)	3-162
	NLST ↵		
3	**>**	Call OS Shell	3-163
	>DOS command ↵		
4	**CCLK**	Display/Change Clock Mode	3-164
	CCLK [Δ *mnemonic*] ↵		
	HIN, HOUT, LIN, LOUT		
5	**CIPS**	Display/Change Interface Power Supply	3-165
	CIPS [Δ *mnemonic*] ↵		
	mnemonic : INT, EXT		
6	**EXPAND**	Expand Code Memory	3-166
	EXPAND [Δ *mnemonic*] ↵		
	mnemonic : ON, OFF		
7	**EXIT**	Terminate the Debugger and Exit to OS	3-168
	EXIT ↵		

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3.3.2. History Functions

EASE64X has a function for saving previous command line input (☞1). This function is known as the history function.

When using the debugger, occasionally you will want to input the same command as one several previous, or the same command except with different parameters. This is when the history function is especially powerful.

(1) Current line buffer and history buffer

EASE64X has a current line buffer for editing the current command line input and a history buffer for saving command lines.

The command line buffer is a 72-character buffer for command line input. The history buffer is a 72-character by 20-line buffer for storing command line input in order.

There are two types of history buffers. One is for normal command line input, and one is for command line input during execution of the **ASM** command.

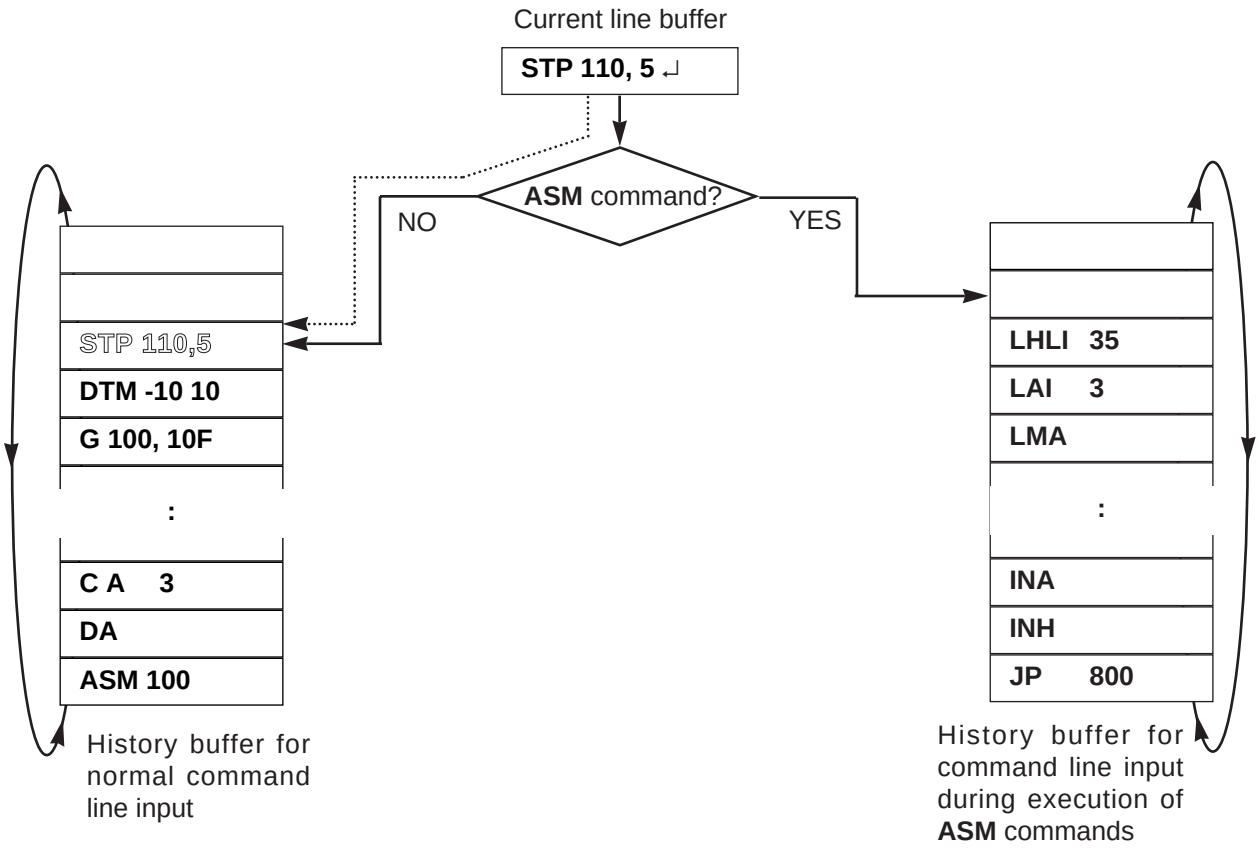

Figure 2-5. Current Line Buffer and History Buffer

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A command line input by an operator is first stored in the current line buffer. Simultaneous to the operator pressing a carriage return, the contents of the current line buffer are stored in the history buffer. Each time a command line is input, its contents are stored in order in the history buffer.

The history buffer is configured as a ring. The oldest input line (the command line input 20 lines before the current command line input) is overwritten. As a result, the previous 20 lines of command line input will always be stored.

The operator can read the contents of the history buffer into the current line buffer at any time during command line input.

Note that input from a file called by the **BATCH** command will not be stored in the history buffer.

❑ Using history functions

This somewhat covers the same material as Section 3-3-3, “Special Keys For Raising Command Input Efficiency,” but the history functions are utilized with the ↑ key (or **CTRL + K**) and the ↓ key (or **CTRL + J**).

Pressing the ↑ key will read the immediately previous command line input from the history buffer into the command line buffer and display it on the console. Then each time the ↑ key is pressed, the next previous command line input will be read and displayed.

Converse to the ↑ key, the ↓ key reads the command line input immediately afterward from the history buffer and displays it on the console.

After the operator has edited the displayed current line buffer contents with the special keys for command line editing, as explained in the next section, he can enter it as the new command line input by pressing the ↵ key. At this time, the current line buffer will be executed to its end as the command line input, regardless of the cursor position on the line.

Of course, the contents of the current line buffer can be executed if only the ↵ key is pressed without any editing.

EASE64X command line input is input from the console after the EASE64X output prompt “*****”, and during **ASM** command execution.

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3.3.3. Special Keys For Raising Command Input Efficiency

EASE64X provides special editing keys, as mentioned in the previous section on the history function, for raising efficiency of current line buffer editing. There are a total of 12 special keys. They can effectively create new command line inputs. The special keys and their control functions are explained below.

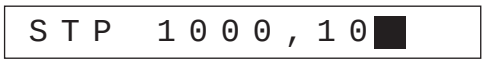
(1) **CTRL+A** and **CTRL+Z**

CTRL+A moves the cursor to the first location of the current line buffer.

CTRL+Z moves the cursor to the last location of the current line buffer.

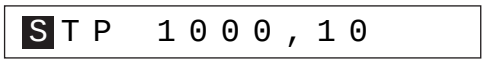
Example

Contents of current line buffer before editing



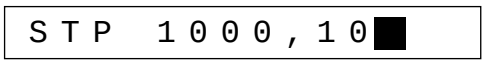
CTRL + A pressed

Contents of current line buffer after editing



CTRL + Z pressed

Contents of current line buffer after editing



(2) **CTRL+B** and **CTRL+F**

CTRL+B searches for a string *consisting of letters and digits only* from the current cursor location in the current line buffer toward the first location. In other words, it recognizes characters other than letters and digits as string delimiters.

If a string is detected, then the cursor will be moved to its first location. If no string could be detected, then the cursor will be moved to the first location of the current line buffer.

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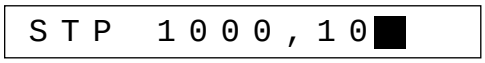
CTRL+F searches for a string *consisting of letters and digits only* from the current cursor location in the current line buffer toward the last location. In other words, it recognizes characters other than letters and digits as string delimiters.

If a string is detected, then the cursor will be moved to its first location. If no string could be detected, then the cursor will be moved to the last location of the current line buffer.

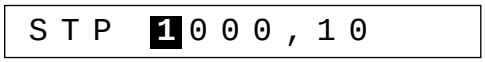
Example

Contents of current line buffer before editing



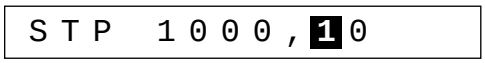
CTRL + B pressed
CTRL + B pressed

Contents of current line buffer after editing



CTRL + F pressed

Contents of current line buffer after editing



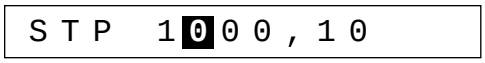
(3) **CTRL+H** (or ←) and **CTRL+L** (or →)

CTRL+H moves the cursor one location to the left of its current location in the current line buffer.

CTRL+L moves the cursor one location to the right of its current location in the current line buffer.

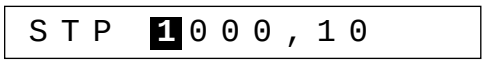
Example

Contents of current line buffer before editing



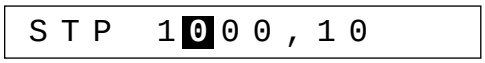
CTRL + H or ← pressed

Contents of current line buffer after editing



CTRL + L or → pressed

Contents of current line buffer after editing



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(4) **CTRL+K** (or ↑) and **CTRL+J** (or ↓)

CTRL+K (or ↑) and **CTRL+J** (or ↓) read history buffer contents into the current line buffer, as explained in the previous section. For details, refer to the previous Section 3.3.2, “History Function.”

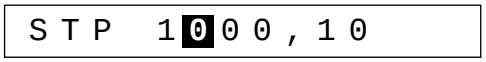
(5) **CTRL+D** and **CTRL+X**

CTRL+D deletes current line buffer contents from the current cursor position to the last location, and then moves the cursor to the end of the line.

CTRL+X deletes the current line buffer contents, and then moves the cursor to the start of the buffer.

Example

Contents of current line buffer before editing

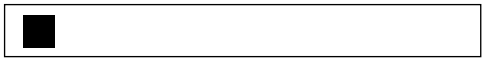


CTRL + D pressed

Contents of current line buffer after editing

CTRL + X pressed

Contents of current line buffer after editing



(6) **CTRL+R** (or **INS**) and **DEL**

CTRL+R (or **INS**) inserts a single blank character at the current cursor position in the current line buffer.

DEL deletes a singles character at the current cursor position in the current line buffer. The cursor position does not change.

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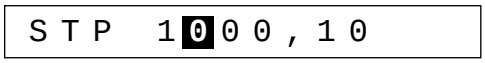
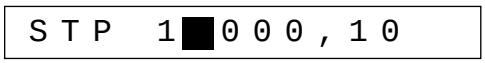
Example

Contents of current line buffer before editing



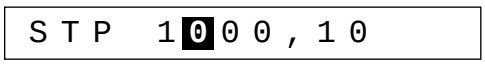
CTRL + R or **INS** pressed

Contents of current line buffer after editing



DEL pressed

Contents of current line buffer after editing



If you will use EASE64X with an IBM PC-AT, then add the appropriate ANSI escape sequence driver from your DOS system disk to CONFIG.SYS. If you forget to do so, then you will not be able to use the special editing keys.

Host Computer	ANSI Escape Sequence Driver Name
IBM PC-AT	ANSI.SYS

To use the ↑, ↓ , ← , → , **INS** and **DEL** keys, set your host computer's key table to the same key code settings as in the table on the next page. If the settings do not match, then the danger exists that a special key function will operate differently. NEC PC-9801 change the key table file to **KEY.TBL** using the MS-DOS utility program **KEY.EXE**.

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The table below shows the special editing keys and how they affect the contents of the current line buffer. It also shows the EASE64X internal processing code (in hexadecimal) for each key. Check the settings of your host computer's key table, and if they do not match these settings, then change them to match.

In the table, "line" means the current line buffer.

Editing Key	*Control Function*	*Code*
CTRL + A	Moves the cursor to the start of the current line buffer.	01H
CTRL + B	Searches for string of letters and digits only from the current cursor location to the first location, and moves the cursor to the start of the string.	02H
CTRL + D	Deletes all characters from the current cursor location to the last location.	04H
CTRL + F	Searches for string of letters and digits only from the current cursor location to the first location, and moves the cursor to the start of the string.	06H
CTRL + J or ↓	Reads the next command line input from the history buffer into the current line buffer and displays it.	0AH
CTRL + K or ↑	Reads the previous command line input from the history buffer into the current line buffer and displays it.	0BH
CTRL + H or ←	Moves the current cursor position one to the left.	08H
CTRL + L or →	Moves the current cursor position one to the right.	0CH
CTRL + X	Deletes the current line buffer, and moves the cursor to the first location.	18H
CTRL + Z	Moves the cursor to the end of the current line buffer.	1AH
CTRL + R or **INS**	Inserts a single blank at the current cursor location.	12H
DEL	Deletes a character at the current cursor location.	7FH

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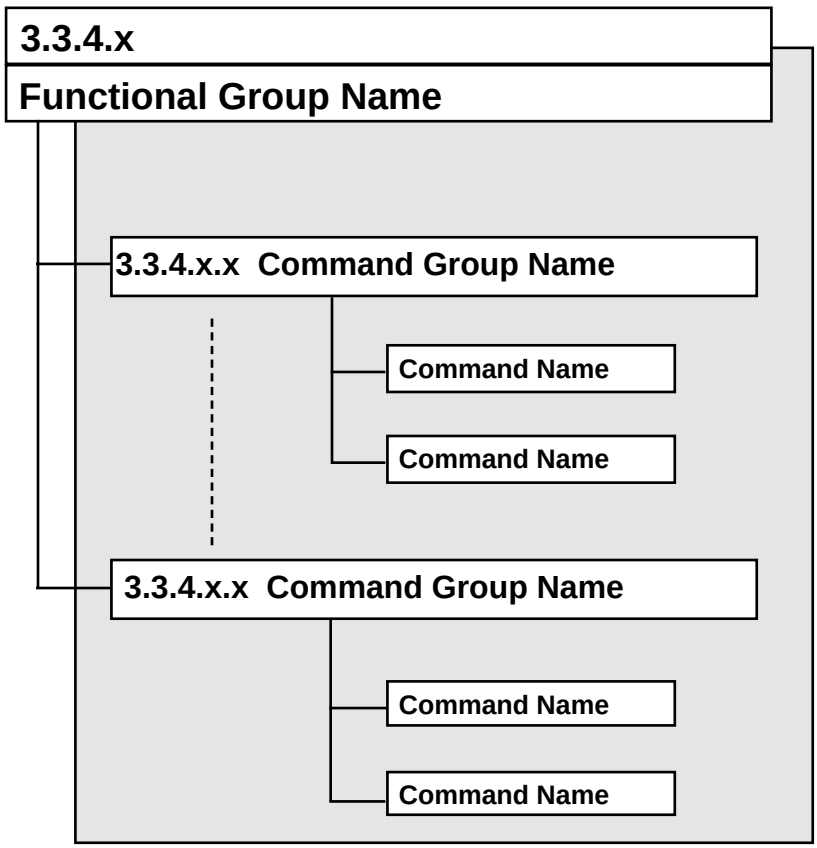
3.3.4 Command Details

This chapter explains the EASE64X commands organized by function.

A list of contents like the one shown below is given at the start of each functional grouping. At the top is a two-line title box outlining the name of the functional group. Below it are the names of the command groups covered by the functional group, outlined in one-line title boxes. Under each command group are the names of the commands it covers.



The header of each page shows the name of the command explained on that page in boldface and enclosed in a rectangle. This is provided for convenience when looking up command explanations.

Each command is explained in the order of input format, description, and execution example. These are given under the following respective title lines.

Input Format

Description

Execution Example

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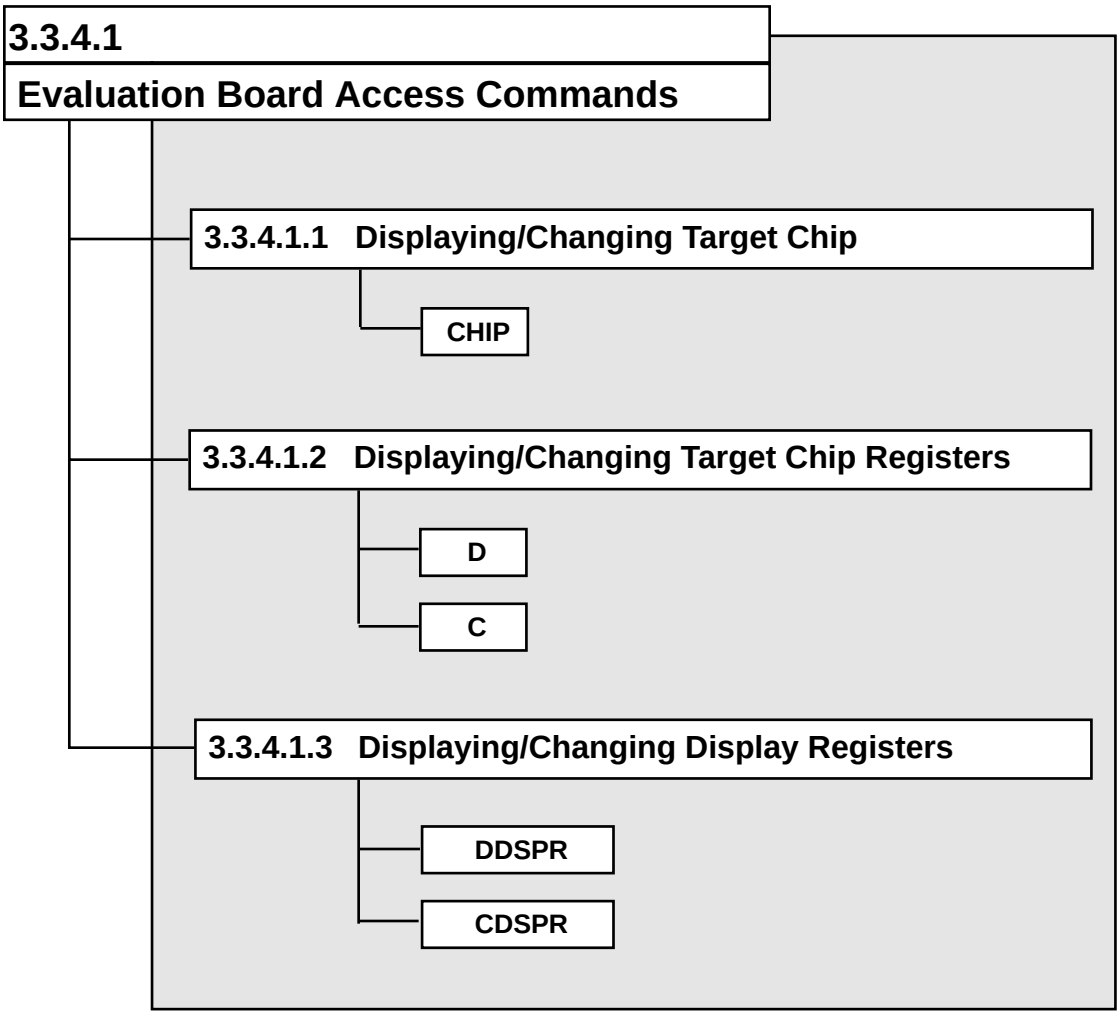

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3.3.4.1.1 Displaying/Changing Target Chip

CHIP

Input Format

CHIP [Δ *mnemonic*] ↵

mnemonic : 64162
64164

Description

The EASE64162/164 can operate in a MSM64162 mode and a MSM64164 mode (☞ 1). The CHIP command sets the EASE64162/164 operating mode with mnemonic. If mnemonic is omitted, then the current operating chip mode will be displayed.

The EASE64162/164 resets its evaluation board after the CHIP command is input. The CHIP command will display the following on the CRT.

```
* CHIP 64162

            * * * * *  EVA BOARD RESET  * * * * *
```

☞ 1 To evaluate an MSM64162D, set the chip mode to MSM64162 mode.

Execution Example

```
* CHIP
        MSM64164 MODE

* CHIP 64162
        *** EVA BOARD RESET ***
```

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D, C

3.3.4.1.2 Displaying/Changing Target Chip Registers

D, C

Input Format

D [*mnemonic*] ↵ ◄····· *Display command*

C *mnemonic* [Δ *data*] ↵ ◄····· *Change command*

mnemonic : *mnemonic of a register*

Description

The **D** command displays the contents of the register specified by *mnemonic.* A register *mnemonic* is one of the mnemonics shown in Table 3-3. If no mnemonic is input, then contents of all registers will be displayed.

The **C** command changes the contents of the register specified by *mnemonic.* The format of *mnemonic* is the same as for the **D** command. A list of *mnemonics* is shown in Table 3-3. The data differs for each register; Table 3-3 shows the *data* range of each.

mnemonic : *old-data OLD ---->*
(☞ 1)

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Here *mnemonic* expresses the mnemonic of the register that is to have its current contents changed. The *old-data* will be the current contents of the SFR or register. At this point the operator enters new data (*data*) and inputs a carriage return.

mnemonic : *old-data OLD* ---> *data* ↵

When the emulator waiting for input data for a change, the following key input is value in addition to data.

↵ (carriage return only) The C command terminates

The following mnemonics are write-only registers. If selected, then old-data will not be displayed.

P20CON, P21CON, P22CON, P23CON
P30CON, P31CON, P32CON, P33CON
P40CON, P41CON, P42CON, P43CON
P01CON

The MSM64162/164 mask option specifications can set P5 and P6, but their contents cannot be displayed or changed by EASE64162/164 with a debugger command.

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Table 3-3(a). List of registers mnemonics

	Register Name	Mnemonic	Input Data Range In MSM64162 Mode	Input Data Range In MSM64162 Mode
	Program Counter	PC	0 to 7DF	0 to FDF
	B Register	B	0 to F	0 to F
	A Register	A	0 to F	0 to F
	HL Register	HL	0 to FF	0 to FF
	XY Register	XY	0 to FF	0 to FF
	Carry Flag	CY	0, 1	0, 1
	Stack Pointer	SP	80 to FF	0 to FF
	Bank Select Register 0	BSR0	0 to 7	0 to 7
	Bank Select Register 1	BSR1	0 to 7	0 to 7
	Bank Common Flag	BCF	0, 1	0, 1
	Bank Enable Flag	BEF	0, 1	0, 1
(☞ 3)	Backup Control Register	BUPCON	0 to 3	0, 1
(☞ 2)	Serial Port Buffer Register	SBUF		0 to FF
(☞ 2)	Serial Control Register	SCON		0 to F
(☞ 8)	Frequency Control Register	FCON	0, 1	0, 1
	Buzzer Control Register	BDCON	0 to F	0 to F
(☞ 3)	Buzzer Frequency Control Register	BFCON	0, 1	0 to F
	Capture Control Register	CAPCON	0 to F	0 to F
(☞ 4)	Capture Register 0	CAPR0		
(☞ 4)	Capture Register 1	CAPR1		
(☞ 5)	Time Base Counter Register	TBCR	0 to F	0 to F
	Display Control Register	DSPCON	0 to 2	0 to 2
	A/D Converter Control Register 0	ADCON0	o to 3	o to 3
(☞ 9)	A/D Converter Control Register 1	ADCON1	0 to F	0 to F
(☞ 6)	Counter A Register	CNTA	0 to 79999	0 to 79999
	Counter B Register	CNTB	0 to 3FFF	0 to 3FFF
(☞ 4)	Port 0 Register	P0		
	Port 1 Register	P1D	0 to F	0 to F
	Port 2 Register	P2D	0 to F	0 to F
	Port 3 Register	P3D	0 to F	0 to F
(☞ 2)	Port 4 Register	P4D		0 to F
(☞ 7)	Port 20 Control Register	P20CON	0 to F	0 to F
	Port 21 Control Register	P21CON	0 to F	0 to F
	Port 22 Control Register	P22CON	0 to F	0 to F
	Port 23 Control Register	P23CON	0 to F	0 to F
	Port 30 Control Register	P30CON	0 to F	0 to F
	Port 31 Control Register	P31CON	0 to F	0 to F
	Port 32 Control Register	P32CON	0 to F	0 to F
	Port 33 Control Register	P33CON	0 to F	0 to F
(☞ 2)	Port 40 Control Register	P40CON		0 to F
(☞ 2)	Port 41 Control Register	P41CON		0 to F
(☞ 2)	Port 42 Control Register	P42CON		0 to F

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Table 3-3(b). List of registers mnemonics

	Register Name	Mnemonic	Input Data Range In MSM64162 Mode	Input Data Range In MSM64162 Mode
(☞ 2)	Port 43 Control Register	P43CON		0 to F
	Port 01 Control Register	P01CON	0 to 7	0 to 7
(☞ 3)	Interrupt Enable Register 0	IE0	0 to F	0 to F
	Interrupt Enable Register 1	IE1	0 to F	0 to F
	Interrupt Enable Register 2	IE2	0, 1	0, 1
(☞ 3)	Interrupt Request Register 0	IRQ0	0 to F	0 to F
	Interrupt Request Register 1	IRQ1	0 to F	0 to F
	Interrupt Request Register 2	IRQ2	0 to 3	0 to 3
	Master Interrupt Enable Flag	MIEF	0, 1	0, 1

☞ 2 In MSM64162 mode, the mnemonics *SCON, SBUF, P4D, and P40CON~P43CON* are invalid

☞ 3 The bit configurations in MSM64162 mode and MSM64164 mode differ. Refer to the chips' user's manuals for details.

☞ 4 *CAPR0, CAPR1,* and *P0* are read-only registers, so the change command is invalid with them.

☞ 5 When *TBCR* is changed, it will be reset to 0 regardless of the change data specified.

☞ 6 The change data for *CNTA* is a decimal value.

☞ 7 *P20CON~P23CON, P30CON~P33CON, P40CON~P43CON,* and *P01CON* are write-only registers, so the display command is invalid with them.

☞ 8 The *FCON* register does not exist in the MSM64162D chip.

☞ 9 If invalid data (5, 6, or 7) is written to the *ADCON1* register when evaluating a MSM64162D, then the emulator may operate incorrectly.

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D, C

Execution Example

```
* DA
A :0

* CA
A :0 OLD  ---> 8

* CHL E4

* DHL
HL :E4

* CHIP
MSM64164 MODE

* D                MSM64164 mode
PC   :0000  P0     :F   CNTA   :80000
A    :8     P1D    :0   CNTB   :C000
B    :0     P2D    :F   ADCON0 :C
HL   :E4    P3D    :F   ADCON1 :0
XY   :00    FCON   :E   IE0    :0
CY   :0     BDCON  :0   IE1    :0
SP   :FF    BFCON  :0   IE2    :E
BSR0 :0     CAPRO  :0   IRQ0   :0
BSR1 :0     CAPR1  :0   IRQ1   :0
BCF  :0     CAPCON :0   IRQ2   :C
BEF  :0     TBCR   :0   BUPCON :E
MIEF :E     DSPCON :C
P4D  :F     SCON   :0   SBUF   :00


* CHIP 64162

*** EVA BOARD RESET ***

* D                MSM64162 mode

PC   :0000  P0     :F   CNTA   :80000
A    :0     P1D    :0   CNTB   :C000
B    :0     P2D    :F   ADCON0 :C
HL   :00    P3D    :F   ADCON2 :0
XY   :00    FCON   :E   IE0    :2
CY   :0     BDCON  :0   IE1    :0
SP   :FF    BFCON  :E   IE2    :E
BSR0 :0     CAPR0  :0   IRQ0   :2
BSR1 :0     CAPR1  :0   IRQ1   :0
BCF  :0     CAPCON :0   IRQ2   :C
BEF  :0     TBCR   :0   BUPCON :8
MIEF :E     DSPCON :C
```


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3.3.4.1.3 Displaying/Changing Display Registers

CDSPR

Input Format

CDSPR [Δ *number*] ↵

Description

The CDSPR command changes the values of the display registers (DSPR00~DSPR30). (☞ 1)

The number range differs for MSM64162 mode and MSM64164 mode. In MSM64162 mode, its range is 00 to 20 (decimal). In MSM64164 mode, its range is 00 to 30 (decimal).

DSPR00 = old-data OLD --->

Here old-data is the current value of the corresponding display register. The inputs new data (data) and a carriage return. The data is a value 0H to FH.

DSPR00 = old-data OLD ---> *data* NEW ↵
DSPR00 = old-data OLD ---> ◄····· *input data for next parameter*

When the carriage return is input, processing moves to the next parameter. If there is no next parameter, then the CDSR command terminates.

If number is specified, then changes will begin from the specified display register.

When the emulator is waiting for input data for a change, the following three key inputs are valid in addition to data.

"Δ ↵" (space followed by carriage return) Display contents of next display register without changing the current data, and wait for new input data.

"– ↵"- (minus followed by carriage return) Display contents of previous display register without changing the current data, and wait for new input data.

"↵" (carriage return only) Terminate the CDSPR command.

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CDSPR, DDSPR

Execution Example

```
* CDSPR
  DSPR00 = 0  OLD  ---> 8
  DSPR01 = 0  OLD  ---> 4
  DSPR02 = 0  OLD  ---> F
  DSPR03 = 0  OLD  --->    NOT CHANGE          :Input Δ↵
  DSPR04 = 0  OLD  ---> -                      :Input -↵
  DSPR03 = 0  OLD  ---> 1
  DSPR04 = 0  OLD  --->                        :Input ↵

* CDSPR 5
  DSPR05 = 0  OLD  ---> 7
  DSPR06 = 0  OLD  ---> A
  DSPR07 = 0  OLD  --->
```


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DDSPR

Input Format

DDSPR ↵

Description

The DDSPR command displays all display register values (DSPR00~DSPR30).(☞ 1)

Execution Example

```
* DDSPR --------->  MSM64162 mode

          0 1 2 3 4 5 6 7 8 9
  DSPR0   8 4 F 1 0 7 A 0 0 0
  DSPR1   0 0 0 0 0 0 0 0 0 0
  DSPR2   0

* CHIP 64164
  *** EVA BOARD RESET ***

* DDSPR ---------->  MSM64164 mode

          0 1 2 3 4 5 6 7 8 9
  DSPR0   0 0 0 0 0 0 0 0 0 0
  DSPR1   0 0 0 0 0 0 0 0 0 0
  DSPR2   0 0 0 0 0 0 0 0 0 0
  DSPR3   0
```

☞ 1 In MSM64162 mode, display registers DSPR00~DSPR20 are valid. In MSM64164 mode, display registers DSPR00~DSPR30 are valid.

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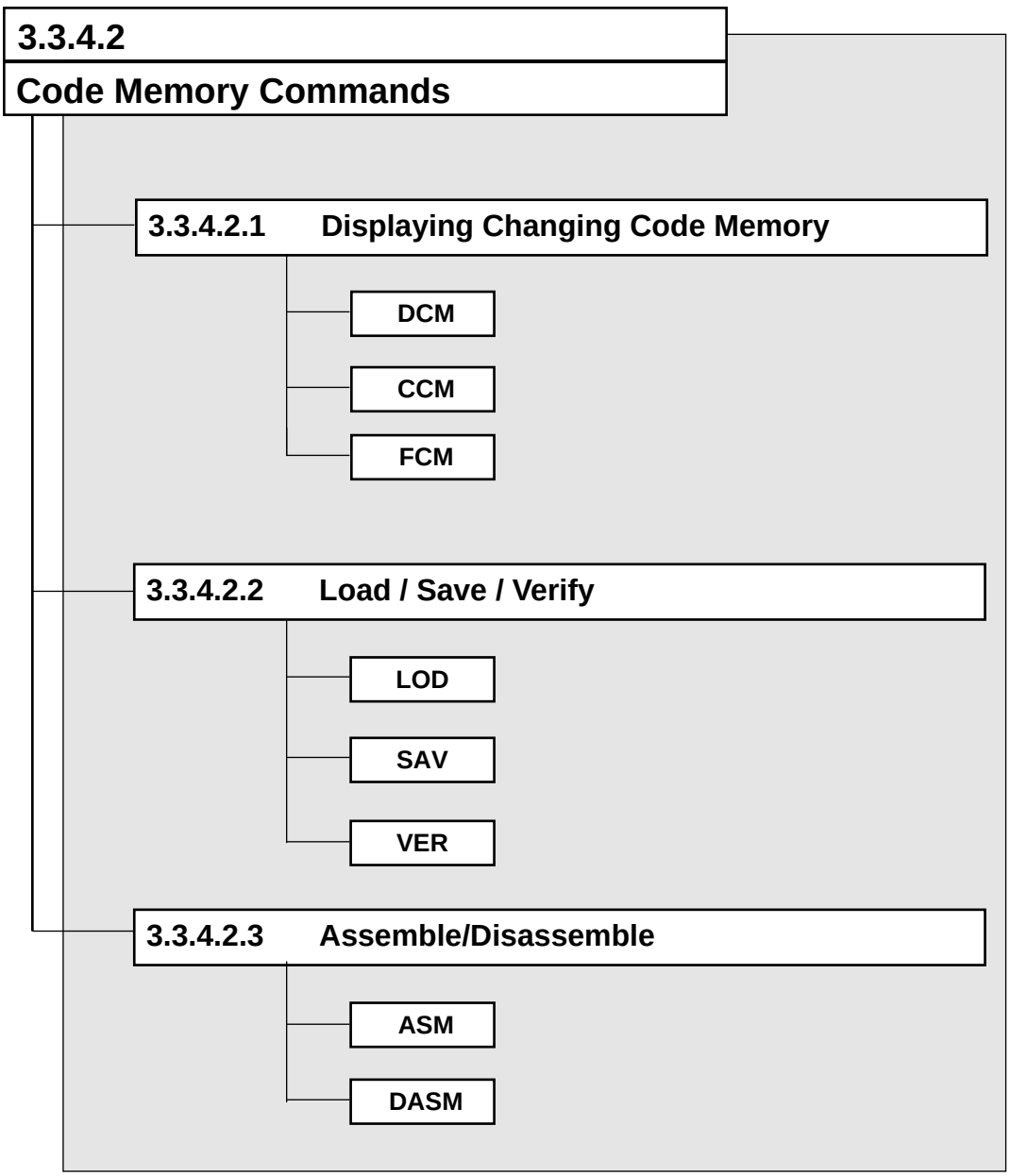

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3.3.4.2.1 Displaying/Changing Code Memory

DCM

Input Format

DCM Δ *address* [, *address*] ↵
or
DCM Δ ***** ↵

address	:	0~7DF (MSM64162 mode) 0~FDF (MSM64164 mode)
*****	:	display entire address range

Description

The **DCM** command displays the contents of code memory.

The *address* expresses an address in code memory space for which the contents are to be displayed. It is a value 0H to 7DFH when in MSM64162 mode, or 0H to FDFH when in MSM64164 mode.

The DCM command can be forcibly terminated by pressing the ESC key.

Display contents are one of the following, depending on input format.

address	Displays the contents of one address.
address, address	Displays the range from the first address to the second address.
*****	Displays the entire area of code memory (☞1).

☞ **1** The entire area of code memory changes with the mode. When in MSM64162 mode, it is 0H to 7DFH. When in MSM64164 mode, it is 0H to FDFH.

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DCM

Execution Example

```
* DCM 0,2F

           0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F
  LOC=0000 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
  LOC=0010 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
  LOC=0020 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00


* DCM 1A
  LOC=001A 00


* DCM *  --------->  MSM64164 mode

           0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F
  L0C=0000 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
  LOC=0010 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
  LOC=0020 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
  LOC=0030 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
  L0C=0040 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
  LOC=0050 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
  LOC=0060 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
  LOC=0070 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
           0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F
  L0C=0080 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
       .
       .
       .
       .
  LOC=0FD0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
```


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CCM

Input Format

CCM Δ *address* ↵

address : 0~7DF (MSM64162 mode)
0~FDF (MSM64164 mode)

Description

The **CCM** command changes the contents of code memory.

The *address* expresses a code memory address. It is a value 0H to 7DFH when in MSM64162 mode, or 0H to FDFH when in MSM64164 mode.

When the carriage return is input, the emulator will output the following message and wait for data input.

LOC = address old-data OLD --->

Here *address* is the code memory address at which contents are to be changed. The *old-data* is the current contents of code memory. The user inputs new *data* followed by a carriage return. The data is the value to change the contents to. It is in the range 0H to FFH.

LOC = *address old-data* OLD ---> *data* NEW ↵
LOC = *address old-data* OLD ---> ◄····· input data for next parameter

When the carriage return is input, processing will move to the next parameter. If there is no next parameter, then the CCM command will terminate.

When the emulator is waiting for input data for a change, the following three key inputs are valid in addition to data.

"Δ ↵" (space followed by carriage return)	Display contents of next code memory address without changing the current data, and wait for new input data.
"– ↵"- (minus followed by carriage return)	Display contents of previous code memory address without changing the current data, and wait for new input data.
"↵" (carriage return only)	Terminate the CDSPR command.

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CCM

Execution Example

```
* CCM 200
  LOC=0200  00 OLD  ---> 11 NEW
  LOC=0201  00 OLD  ---> 23 NEW
  LOC=0202  00 OLD  ---> E4 NEW
  LOC=0203  00 OLD  ---> A1 NEW
  LOC=0204  00 OLD  --->   NOT CHANGE                 :INPUT Δ ↵
  LOC=0205  00 OLD  ---> 4 NEW
  LOC=0206  00 OLD  ---> -                            :INPUT - ↵
  LOC=0205  04 OLD  ---> 33 NEW
  LOC=0206  00 OLD  ---> BB NEW
  LOC=0207  00 OLD  --->                              :INPUT ↵


* DCM 200,20F

             0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F
  LOC=0200  11 23 E4 A1 00 33 BB 00 00 00 00 00 00 00 00 00
```


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FCM

Input Format

FCM Δ *address, address* [, *data*] ↵
or
FCM Δ ***** [, *data*] ↵

address	:	0~7DF (MSM646162 mode)
		0~FDF (MSM646164 mode)
*	:	display entire address range
data	:	0~FF

Description

The **FCM** command changes the contents of code memory.

The address expresses a code memory address. It is a value 0H to 7DFH when in MSM64162 mode, or 0H to FDFH when in MSM64164 mode. The data is a the value of the change data. Its range is 0H to FFH.

The changes are classified by input format as follows.

address, address, data	Fill entire range from first address to second address with the data value.
address, address	Fill entire range from first address to second address with "0."
, data	Fill entire code memory area with the data value.
*	Fill entire code memory area with “0.” (☞1)

☞ **1** The entire area of code memory changes with the mode. When in MSM64162 mode, it is 0H to 7DFH. When in MSM64164 mode, it is 0H to FDFH.

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FCM

Execution Example

```
* FCM 50,8F,E4


* DCM 50,8F
             0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F
  LOC=0050  E4 E4 E4 E4 E4 E4 E4 E4 E4 E4 E4 E4 E4 E4 E4 E4
  LOC=0060  E4 E4 E4 E4 E4 E4 E4 E4 E4 E4 E4 E4 E4 E4 E4 E4
  LOC=0070  E4 E4 E4 E4 E4 E4 E4 E4 E4 E4 E4 E4 E4 E4 E4 E4
  LOC=0080  E4 E4 E4 E4 E4 E4 E4 E4 E4 E4 E4 E4 E4 E4 E4 E4


* FCM 50,6F


* DCM 50,8F
             0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F
  LOC=0050  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
  LOC=0060  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
  LOC=0070  E4 E4 E4 E4 E4 E4 E4 E4 E4 E4 E4 E4 E4 E4 E4 E4
  LOC=0080  E4 E4 E4 E4 E4 E4 E4 E4 E4 E4 E4 E4 E4 E4 E4 E4


* FCM *,AA


* DCM 50,8F
             0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F
  LOC=0050  AA AA AA AA AA AA AA AA AA AA AA AA AA AA AA AA
  LOC=0060  AA AA AA AA AA AA AA AA AA AA AA AA AA AA AA AA
  LOC=0070  AA AA AA AA AA AA AA AA AA AA AA AA AA AA AA AA
  LOC=0080  AA AA AA AA AA AA AA AA AA AA AA AA AA AA AA AA


* FCM *


* DCM 50,8F
             0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F
  LOC=0050  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
  LOC=0060  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
  LOC=0070  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
  LOC=0080  00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
```


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3.3.4.2.2 Load/Save/Verify

LOD

Input Format

LOD Δ *fname* ↵

fname : [*Pathname*] *filename* [*Extension*]

Description

The **LOD** command loads the contents of an object file output by ASM64K into code memory. For this command, an object file is an Intel HEX format file generated by ASM64K.

If the extension is omitted, then ".HEX" (Intel HEX format file) will be the default.

The input filename can have a path specification. If the path is omitted, then the file in the current directory will be loaded. If the extension is omitted, then the the file with the default extension will be loaded.

The object file generated by the ASM64K cross-assembler includes code information obtained by converting the OLMS-64K instruction mnemonics and directives in the source program file, and symbol information obtained from the symbol definitions in the source program file. Do not specify the /S option for assembly that will generate symbol information because EASE64X does not handle symbol information.

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SAV

SAV

Input Format

SAV Δ *fname* [Δ *address* , *address*] ↵

fname : [*Pathname*] *filename* [*Extension*]

Description

The **SAV** command saves the contents of the specified range of code memory to a disk file.

The input filename can have a path specification. If the path is omitted, then a file in the current directory will be saved. If the extension is omitted, then the default extension (HEX) will be appended to the file.

The address, address represents the area of code memory to be saved. If omitted, then the entire code memory area will be saved. (☞ 1)

☞ **1** The entire area of code memory changes with the mode. When in MSM64162 mode, it is 0H to 7DFH. When in MSM64164 mode, it is 0H to FDFH.

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VER

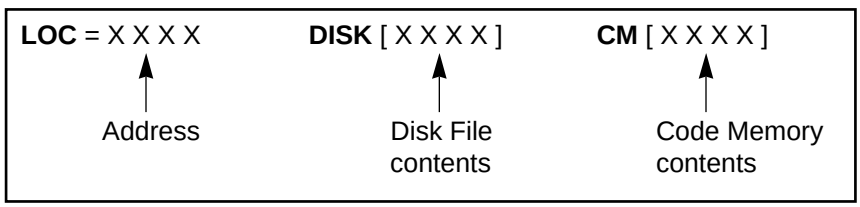
Input Format

VER Δ *fname* [Δ *address* , *address*] ↵

fname : [*Pathname*] *filename* [*Extension*]

Description

The **VER** command compares the contents of the specified disk file with the contents of code memory. When a difference is found, the address and the contents of the disk file and of code memory will be displayed as shown below.



The input filename can have a path specification. If the path is omitted, then a file in the current directory will be verified. If the extension is omitted, then the default extension (HEX) will be appended to the file.

The address, address represents the area of disk file and of code memory to be compared. When in MSM64162 mode, the address range is 0H to 7DFH. When in MSM64164 mode, the address range is 0H to FDFH. If address, address is omitted, then the entire code memory area will be compared. (☞1).

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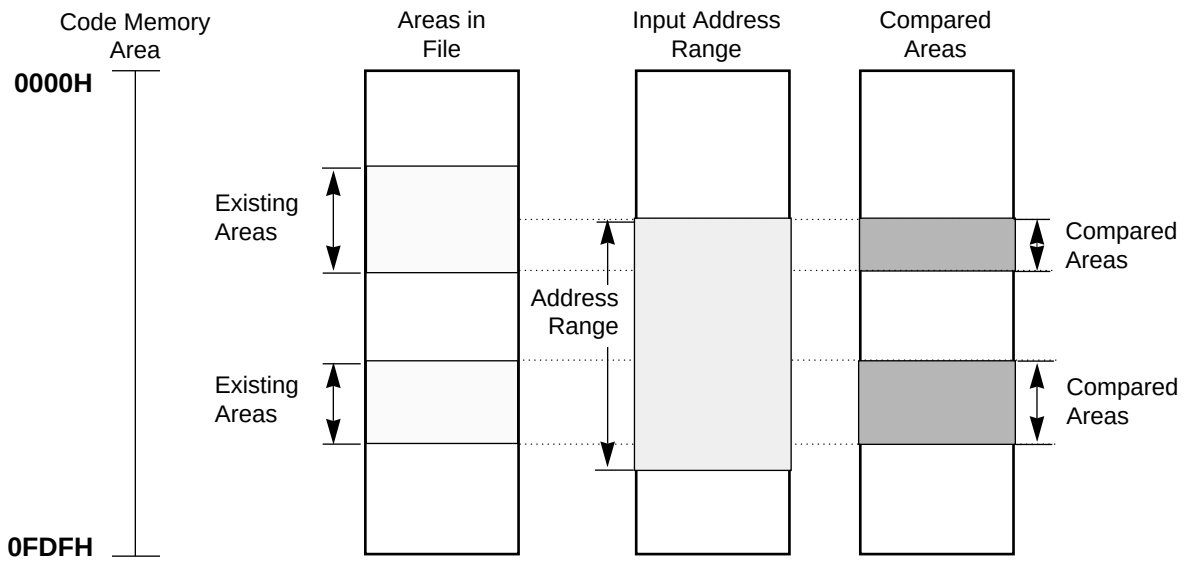
VER

1 As shown below, comparison between the disk file and code memory will be performed on the overlap of disk file areas containing data and the “address, address” address range specified with the **VER** command.



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Execution Example

```
* LOD T1

   FILE OPENED NORMALLY.  FILE TYPE : INTELLEC HEX

  ***** LOAD COMPLETED , NEXT ADDRESS =  0300   *****

* VER T1
  ***** VERIFY COMPLETED *****


* CCM 100

  LOC=0100  BE OLD  ---> 12 NEW
  LOC=0101  A7 OLD  ---> 34 NEW
  LOC=0102  11 OLD  ---> 45 NEW
  LOC=0103  90 OLD  ---> 56 NEW
  LOC=0104  36 OLD  ---> 78 NEW
  LOC=0105  00 OLD  ---> A1 NEW
  LOC=0106  01 OLD  ---> 22 NEW
  LOC=0107  C4 OLD  --->

* VER T1 0,7FF

  LOC = 0100   DISK [ BE ]   CM [ 12 ]
  LOC = 0101   DISK [ A7 ]   CM [ 34 ]
  LOC = 0102   DISK [ 11 ]   CM [ 45 ]
  LOC = 0103   DISK [ 90 ]   CM [ 56 ]
  LOC = 0104   DISK [ 36 ]   CM [ 78 ]
  LOC = 0105   DISK [ 00 ]   CM [ A1 ]
  LOC = 0106   DISK [ 01 ]   CM [ 22 ]
 ***** VERIFY COMPLETED *****

* SAV T1CH 0,2FF

 ***** SAVE COMPLETED *****
```

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ASM

3.3.4.2.3 Assemble/Disassemble Commands

ASM

Input Format

ASM Δ *address* ↵

address : 0~7DF (MSM64162 mode)
0~FDF (MSM64164 mode)

Description

The ASM command converts OLMS-64K series instruction statements (directives, mnemonics, and operands) into object code using an assembler based on ASM64K, and then stores that object code in code memory.(☞ 1).

The address expresses a code memory address. It is a value 0H to 7DFH when in MSM64162 mode, or 0H to FDFH when in MSM64164 mode.

When the carriage return is input, the emulator displays the following message and waits for data input.

address ***** ◄ wait for instruction statement input

At this point the operator can input code that follows the format below.

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(1) The maximum number of characters that can be input on one line is 29.
(2) After an instruction statement and carriage return are input, the emulator displays the assembled object code and then waits for input at the next address.
(3) The ASM command terminates with an "END."
(4) Spaces or tabs can be used as delimiters.
(5) All MSM64162, MSM64164 mnemonics and operands can be used.
(6) Character constants (such as 'A') and string constants (such as "ABC") cannot be coded in operands.
(7) A semicolon ";" is used to code a comment.
(8) The default radix for immediate values used in operands is 10 (decimal values). To use a radix other than 10, input as shown in the following table.

When a hexadecimal constant's first character would normally be a letter (A~F), a '0' (zero) needs to be inserted as the first character to distinguish it from a symbol.

Radix	***Syntax***	***Examples***
Binary (radix 2)	Append a 'B' after the number.	01010101B
Octal (radix 8)	Append an 'O' after the number.	777O
Decimal (radix 10)	Append a 'D' or nothing after the number.	10D, 10
Hexadecimal (radix 16)	Append a 'H' after the number.	0ABH

(9) The following assembler directives can be used.

Directive Type	***Directives Allowed***
Address control	**ORG**
Data definition	**DB**
Assembly control	**END**

(10) The history function can be used. The ASM command has a 20-line buffer, separate from the debugger's history buffer, for use as an assembler-only history function. This buffer's contents are preserved even after the ASM command terminates, so when the ASM command is started again, the previously input 20 lines can easily be brought up for editing using the arrow keys. This feature can simplify input.

Comments input with the ASM command cannot be displayed with the DASM command.

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DASM

DASM

Input Format

DASM Δ *address* [, *address*] ↵
or
DASM Δ ***** ↵

address	:	0~7DF (MSM64162 mode) 0~FDF (MSM64164 mode)
*****	:	disassemble entire address range

Description

The DASM command disassembles the contents of code memory and displays the results on the console (☞1).

The address expresses an address in code memory. It is a value 0H to 7DFH when in MSM64162 mode, or 0H to FDFH when in MSM64164 mode.

The DASM command can be forcibly terminated by pressing the ESC key.

Display contents are one of the following, depending on input format.

address	Displays the contents of one address.
address, address	Displays the range from the first address to the second address.
*****	Displays the entire area of code memory.

☞ **1** Comments input with the ASM command cannot be displayed with the DASM command.

☞ **2** The entire area of code memory changes with the mode. When in MSM64162 mode, it is 0H to 7DFH. When in MSM64164 mode, it is 0H to FDFH.

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Execution Example

```
* ASM 100
 LOC = 0100 50 C0     * LHLI 0C0H
 LOC = 0102 6F        * LMA
 LOC = 0200           * ORG 200H
 LOC = 0200           * LHLI 03FH
 LOC = 0202           * END

* DASM 100
 LOC=0100   50C0     LHLI   C0

* DASM 100,103
 LOC=0100   50C0     LHLI   C0
 LOC=0102   6F       LMA
 LOC=0103   00       NOP
```

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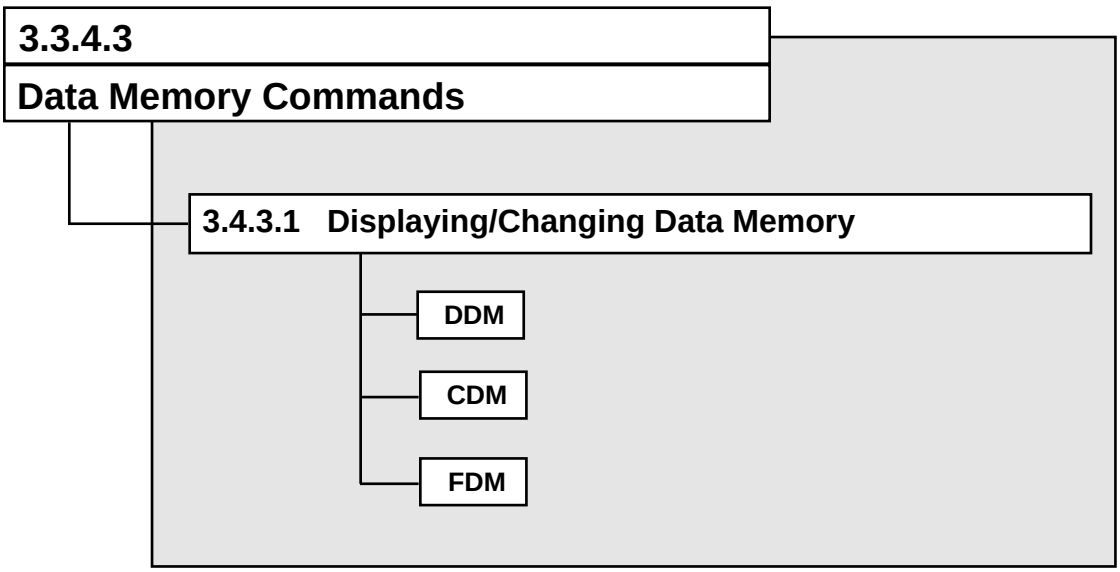

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3.3.4.3.1 Displaying/Changing Data Memory

DDM

Input Format

DDM Δ *address* [, *address*] ↵
or
DDM Δ ***** ↵

address	:	780~7FF (MSM64162 mode)
		700~7FF (MSM64164 mode)
*****	:	display entire address range

Description

The **DDM** command displays the contents of data memory.

The *address* is a value 780H~7FFFH in MSM64162 mode and 700H~7FFH in MSM64164 mode.

The **DDM** command can be forcibly terminated by pressing the ESC key.

Display contents are one of the following, depending on input format.

address	Displays the contents of one address.
address, address	Displays the range from the first address to the second address.
*****	Displays the entire area of data memory (☞ 1).

☞ **1** The entire area displayed differs for each chip mode. In MSM64162 mode, the area 780H to 7FFH is displayed. In MSM64164 mode, the area 700H to FFFH is displayed.

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DDM

Execution Example

```
* DDM 780,79F
           F E D C B A 9 8 7 6 5 4 3 2 1 0
  LOC=0780  0 1 0 B 0 0 2 2 0 0 0 6 0 0 2 0
  LOC=0790  0 1 1 9 1 4 4 0 0 3 1 6 4 4 0 8

* DDM 79F
  LOC=079F  0

* DDM 790
  LOC=0790  8

* DDM *  -------->  MSM64164 mode
           F E D C B A 9 8 7 6 5 4 3 2 1 0
  LOC=0700  0 9 0 0 1 1 1 0 0 D 0 0 0 A 0 0
  LOC=0710  0 2 0 0 0 7 2 8 5 2 0 0 0 1 4 3
  LOC=0720  1 0 0 C 8 B 0 0 0 1 0 9 C 1 0 4
  LOC=0730  2 5 0 8 0 8 0 2 0 3 C 4 0 8 0 A
  LOC=0740  8 1 0 0 0 E 0 4 0 1 0 0 0 6 0 B
  LOC=0750  4 2 0 A 0 8 0 0 0 0 1 3 0 0 1 6
  LOC=0760  0 9 0 0 2 0 0 0 0 5 4 1 0 A 0 0
  LOC=0770  0 2 8 2 0 8 0 4 0 1 8 2 0 C 8 A

           F E D C B A 9 8 7 6 5 4 3 2 1 0
  LOC=0780  0 1 0 B 0 0 2 2 0 0 0 6 0 0 2 0
  LOC=0790  0 1 1 9 1 4 4 0 0 3 1 6 4 4 0 8
  LOC=07A0  0 2 0 0 0 4 0 0 4 A 0 1 0 1 0 4
  LOC=07B0  F F 0 0 1 0 0 8 0 8 0 4 4 4 0 7
  LOC=07C0  0 2 C 4 8 0 4 3 0 7 1 0 0 1 8 0
  LOC=07D0  0 9 0 C 2 0 6 0 8 4 0 B 0 0 0 1
  LOC=07E0  1 C 8 0 0 0 1 3 0 D 1 A 0 2 0 0
  LOC=07F0  1 0 0 4 1 0 0 8 0 0 0 E 0 1 0 5
```


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CDM

Input Format

CDM Δ *address* ↵

address : 780~7FF (MSM64162 mode)
700~7FF (MSM64164 mode)

Description

The **CDM** command changes the contents of data memory.

When the carriage return is input, the emulator will output the following message and wait for data input.

LOC = *address* *old-data* OLD --->

Here *address* is the data memory address at which contents are to be changed. The *old-data* is the current contents of data memory. The user inputs new data followed by a carriage return. The data is the value to change the contents to. It is in the range 0H to FH.

LOC = *address* *old-data* OLD ---> *data* NEW ↵
LOC = *address* *old-data* OLD ---> ← input next parameter

When the carriage return is input, processing will move to the next parameter. If there is no next parameter, then the **CDM** command will terminate.

When the emulator is waiting for input data for a change, the following three key inputs are valid in addition to data.

"Δ ↵"	(space followed by carriage return)	Display contents of next data memory address without changing the current data, and wait for new input data.
"– ↵"	(minus followed by carriage return)	Display contents of previous data memory address without changing the current data, and wait for new input data.
"↵"	(carriage return only)	Terminate the **CDM** command.

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CDM

Execution Example

```
* DDM 750,75F
            F E D C B A 9 8 7 6 5 4 3 2 1 0
  LOC=0750  4 2 0 A 0 8 0 0 0 0 1 3 0 0 1 6

* CDM 750
  LOC=0750  6 OLD ---> 0 NEW
  LOC=0751  1 OLD ---> 5 NEW
  LOC=0752  0 OLD ---> 0 NEW
  LOC=0753  0 OLD ---> -                  :INPUT – ↵
  LOC=0752  0 OLD ---> E NEW
  LOC=0753  0 OLD ---> A NEW
  LOC=0754  3 OLD ---> F NEW
  LOC=0755  1 OLD ---> 2 NEW
  LOC=0756  0 OLD --->   NOT CHANGE       :INPUT Δ ↵
  LOC=0757  0 OLD ---> C NEW
  LOC=0758  0 OLD ---> 9 NEW
  LOC=0759  0 OLD --->                    :INPUT ↵

* DDM 750,75F
            F E D C B A 9 8 7 6 5 4 3 2 1 0
  LOC=0750  4 2 0 A 0 8 0 9 C 0 2 F A E 5 0
```


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FDM

Input Format

FDM Δ *address, address* [, *data*] ↵
or
FDM Δ ***** [, *data*] ↵

address	:	780~7FF (MSM64162 mode)
		700~7FF (MSM64164 mode)
*****	:	display entire address range
data	:	0~F

Description

The **FDM** command changes the contents of data memory.

The *address* expresses a data memory address. The address is a value 780H~7FFFH in MSM64162 mode and 700H~7FFH in MSM64164 mode.
The data is the value of the change data. Its range is 0H to FH.

The changes are classified by input format as follows.

address, address, data	Fill entire range from first address to second address with the data value.
address, address	Fill entire range from first address to second address with "0."
*****, *data*	Fill entire code memory area with the data value.
*****	Fill entire code memory area with “0.” (☞ 1).

☞ **1** The address is a value 780H~7FFFH in MSM64162 mode and 700H~7FFH in MSM64164 mode.

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FDM

Execution Example

```
* FDM 700,7FF,A

* DDM 750,76F
            F E D C B A 9 8 7 6 5 4 3 2 1 0
  LOC=0750  A A A A A A A A A A A A A A A A
  LOC=0760  A A A A A A A A A A A A A A A A

* FDM 760,76F

* DDM 750,76F
            F E D C B A 9 8 7 6 5 4 3 2 1 0
  LOC=0750  A A A A A A A A A A A A A A A A
  LOC=0760  0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

* FDM *,1

* DDM 750,76F
            F E D C B A 9 8 7 6 5 4 3 2 1 0
  LOC=0750  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
  LOC=0760  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

* FDM *

* DDM 750,76F
            F E D C B A 9 8 7 6 5 4 3 2 1 0
  LOC=0750  0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
  LOC=0760  0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
```


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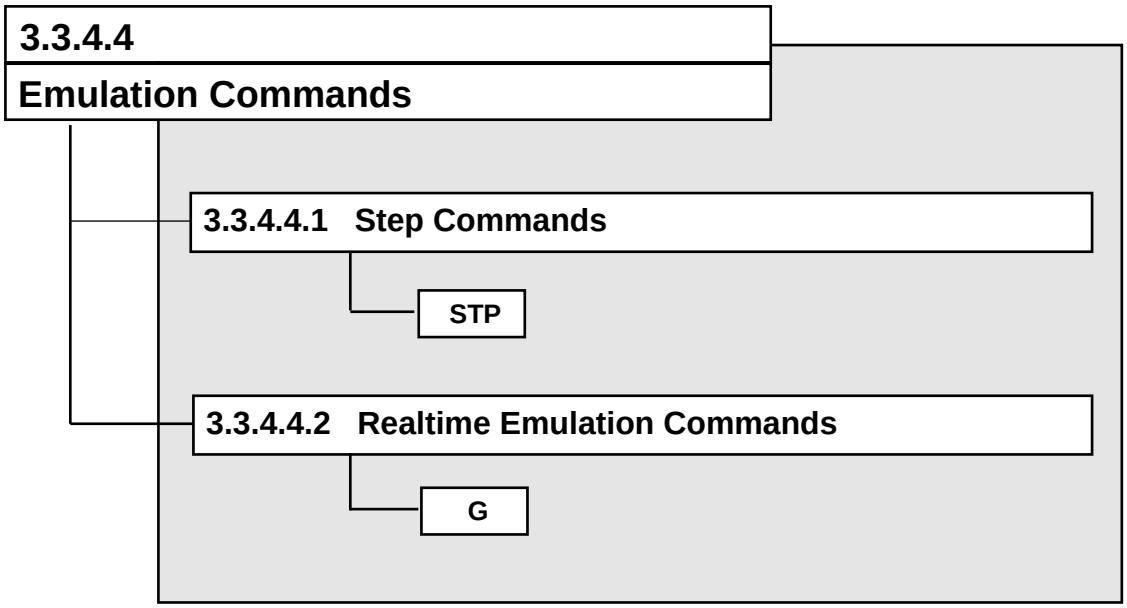

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STP

3.3.4.4.1 Step Commands

STP

Input Format

STP [Δ *count*] [, *address*] ↵
or
STP Δ ***** ↵

address	:	0~7DF (MSM64162 mode)
		0~FDF (MSM64164 mode)
count	:	1~65535
*****	:	execute 65535 steps

Description

The **STP** command executes a user program in code memory one instruction at a time.

The address expresses the first address of the user program at which step execution is to start. It is a value 0H to 7DFH when in MSM64162 mode, or 0H to FDFH when in MSM64164 mode.

If address is omitted, then step execution will start from the address indicated by the current program counter (PC). If "*****" is input, then 65535 steps will be executed from the current program counter (PC).

The count is a decimal value from 1 to 65535. It indicates the number of steps to be executed. If count is omitted, then step execution will be performed for just one instruction and the command will terminate.

The **STP** command stops user program execution after each instruction. At each stop, it displays the address and mnemonic of the executed instruction, and then displays the states of the registers and ports after execution.

The **STP** command does not display instructions skipped by the skip instructions. When the condition for skipping an instruction is met (multiply-accumulate instruction, increment instruction, etc.), the step ends after skipping the next instruction.

The **STP** command can be forcibly terminated by pressing the ESC key. (☞ 1)

☞ **1** Termination by the ESC key cannot be performed while in halt mode.

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STP

When the carriage return is input, the emulator will display the following header, followed by register and port values for each step.

B Δ A Δ H Δ L Δ X Δ Y Δ C Δ P0 Δ P1D Δ P2D Δ P3D Δ P4D Δ SP (☞ 2)

The header is displayed every 10 steps. Register and port data are shown as numbers only where they change. They are displayed as '.' where they have not changed from the previous step. However, the data immediately after a header is always displayed as numbers. (☞ 3)

The register and port contents displayed and the corresponding headers are shown below.

B	B register
A	A register
H	H register
L	L register
X	X register
Y	Y register
C	Carry flag
P0	Port 0 register
P1D	Port 1 register
P2D	Port 2 register
P3D	Port 3 registe
P4D	Port 4 registe
SP	Stack pointer

☞ 2 P4D is not displayed in MSM64162 mode.

☞ 3 Values are displayed for registers and ports after each instruction is executed.

! When an AIS instruction is executed after an ADCS or SUBCS instruction, the skip function of the AIS instruction is not allowed. However, when executed as a single instruction with the STP command, the skip function of the AIS instruction will no longer be disallowed.

! The time base counter value is preserved between instructions even with the STP command. However, while operation of timers and counters synchronized to the microprocessor's internal clock is guaranteed, operation when synchronized to an external clock is not guaranteed.

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STP

Execution Example

```
* STP 3,0
                                B A H L X Y C P0 P1D P2D P3D P4D SP
LOC=0000  13    SBC             0 1 0 2 0 0 0  F  0   F   F   F  FF
LOC=0001  2D0F  LMAD  0F00      . . . . . . .  .  .   .   .   .  ..
LOC=0003  95    LAI   5         . 5 . . . . .  .  .   .   .   .  ..


* STP 5
                                B A H L X Y C P0 P1D P2D P3D P4D SP
LOC=0004  2D36  LMAD  36        0 5 0 2 0 0 0  F  0   F   F   F  FF
LOC=0006  9A    LAI   A         . A . . . . .  .  .   .   .   .  ..
LOC=0007  2D36  LMAD  36        . . . . . . .  .  .   .   .   .  ..
LOC=0009  247C  RMBD  7C,0      . . . . . . .  .  .   .   .   .  ..
LOC=000B  2B31  SMBD  31,3      . . . . . . .  .  .   .   .   .  ..
```


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3.3.4.4.2 Realtime Emulation Commands

G

Input Format

G Δ [*address*] [, *parm*] ↵

parm	:	*address* [, *address* . . . , *address*]
		address (*count*)
	:	RAM (*data* – *count*)
	:	BAR (*data* – *count*)
address	:	0~7DF (MSM64162 mode)
(☞ 1)		0~FDF (MSM64164 mode)
count	:	1~65535
data	:	0~FF, X

Description

The **G** command performs realtime emulation (continuous execution) of a user program in code memory.

The address expresses the first address of the user program at which realtime emulation is to start. It is a value 0H to 7DFH when in MSM64162 mode, or 0H to FDFH when in MSM64164 mode.

If the first address is omitted, then realtime emulation will start from the *address* indicated by the current program counter (PC). If a start address is specified for realtime emulation, then both the entire instruction executed memory and the trace pointer will be reset '0.'

The condition that will break realtime emulation is entered in *parm*. There are four break conditions, shown on the next page. If *parm* is omitted, then realtime emulation will continue to execute until a break condition break occurs (☞ 2).

The **G** command can be forcibly terminated by pressing the ESC key.(☞ 3)

☞ **1** Be sure to input the first address of an instruction within the code memory area for *address*. Breaks will not occur if other addresses are input.

☞ **2** Refer to section 3.3.4.5, "Break Commands," regarding break conditions.

☞ **3** Breaks by the ESC key are not performed while in halt mode.

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G

(1) Address break (specified as individual addresses)

address [, *address* ..... , *address*]

A break will occur when an instruction at any of the addresses specified by address is executed. A maximum of 20 addresses can be entered at one time. The address is a value 0H to 7FDH when in MSM64162 mode, or 0H to FDFH when in MSM64164 mode. It should be the address of the first byte of an instruction.

(2) Address pass count break

address (*count*)

A break will occur when the instruction at the address specified by address is executed count times. The address is a value 0H to 7DFH when in MSM64162 mode, or 0H to FDFH when in MSM64164 mode. It should be the address of the first byte of an instruction. The count is a decimal value 1-65535.

(3) Data memory match break

RAM *(data - count)*

A break will occur when the specified data is written count times to data memory. RAM indicates data memory; the actual data memory address for matching is specified with the CTDM command (☞ 4).

The data is a value 0H to FFH, and can be specified as either 4 bits or 8 bits (☞ 5).
The count is a decimal value 1-65535.)

☞ **4** Refer to Section 3.4.6, "Trace Commands," regarding the CTDM command. If the address specified with the CTDM command does not match the data memory address specified in the addressing of an instruction, then no break will occur.

☞ **5** The input methods for 4-bit and 8-bit data differ as follows.

• 8-bit

RAM (3E-16) Break when 3EH is written 16 times to the specified data memory with an 8-bit move instruction or 8-bit calculation instruction.

• 8-bit (high nibble is FH)

RAM (F5-6) Break when the number of times F5H is written to the specified data memory with an 8-bit move instruction or 8-bit calculation instruction, and the number of times 5H is written with another instruction, totals 6.

• 4-bit

RAM (X3-10) Break when 3H is written 10 times to the specified data memory. The 'X' indicates a 4-bit input. However, if the data memory address specified with the CTDM command is an odd address, then data writes with 8-bit move instructions or 8-bit calculation instructions will not be counted.

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(4) BA register match break

BAR (*data* - *count*)

A break will occur when the data specified by data is written to the BA register count times. The data is a value 0H to FFH, and can be specified as either 4 bits or 8 bits (☞ 6). The count is a decimal value 1-65535.

☞ 6 The input methods for 4-bit and 8-bit data differ as follows.

• 8-bit

BAR (1F-5) Break when 1FH is written 5 times to the BA register with an 8-bit move instruction or 8-bit calculation instruction.

• 4-bit

BAR (X3-3) Break when 3H is written 3 times to the A register. Specification for the B register only is not possible.

When the carriage return is input, the emulator will display the following message.

```
RESET TRACE POINTER
*** EMULATION GO ***
```

However, the "RESET TRACE POINTER" message will be output only when a user program start address has been specified.

When this message is output, all instruction executed bits and the trace pointer will be set to '0,' and execution will begin.

There are two ways to break once realtime emulation of a program is begun by a G command. The first is to specify parameters with the command input, as described above. The second is to use the break condition register. G command break conditions are listed below.

(1) Break when ESC key is pressed.
(2) Break when one of the conditions specified by *parm* in G command input is satisfied.
(3) Break when the following break conditions are enabled.
  (a) Break upon execution of an address at which the breakpoint bit is set to '1.'
  (b) Break when the trace pointer overflows.
  (c) Break when the cycle counter overflows.
(4) Break when the execution address exceeds 07DFH in MSM64162 mode or 0FDFH in MSM64164 mode.

If one of the above conditions is satisfied, then the emulator will display the following message after the instruction at the address that caused the break condition is executed.

```
***** Break Status *****
[Break PC = Break-address Next PC = Next-address]
[Next Trace Pointer = Trace-Pointer]
```

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G

The *Break Status* is one of the break conditions.

SEE DBS command

The Break-address is the address of the user program where the realtime emulation break occurred. The Next-address is the first address of the instruction that is to be executed after the Break-address. The Trace-Pointer is the trace pointer value at the point the break occurred.

The Break-address and Next-address are hexadecimal data. The Trace-Pointer is decimal data.

When a break condition is fulfilled during a skip, the break will be saved. The break will be performed after the skip completes.

However, if an instruction at a break address set as an address break or breakpoint break is skipped, then the break will not be saved. No break will be performed after the skip completes.

If an interrupt is generated when a break condition is fulfilled, then the break will be saved. The break will be performed after the interrupt transfer cycle completes.

The time base counter value is preserved after a break occurs until execution begins again. However, while operation of timers and counters synchronized to the microprocessor's internal clock is guaranteed, operation when synchronized to an external clock is not guaranteed.

When a break occurs in high-speed clock mode, the time base counter value will not be the same as it would for low-speed clock mode even under the same break conditions because the clocks are asynchronous.

If a warning message (Warning 2) is displayed after a G command break, then the duty setting of the LCD driver display control register (DSPCON) is different from the duty setting of the mask options previously loaded. You should verify the duty settings. (When power is first applied, the mask option duty setting is 1/4 duty.)

With the MSM64162/MSM64162D/MSM64164, the skip function of an AIS instruction will be disabled in a program where the AIS instruction is executed following either ADCS and ADCS@XY instructions, and SUBCS and SUBCS@XY instructions. With the EASE64162/164 emulator, however, if a break is set to occur immediately after execution of either ADCS and ADCS@XY instructions, or SUBCS and SUBCS@XY instructions, and execution is set to resume starting with the AIS instruction, then the skip function of the AIS instruction will not be disabled.

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Execution Example

```
* G 0,100
      RESET TRACE POINTER
   *** EMULATION GO ***
  ** ADDRESS MATCH BREAK **
  [ BREAK PC=0100    NEXT PC=0102 ]
  [ NEXT TRACE POINTER=0021 ]

* G 0
      RESET TRACE POINTER
   *** EMULATION GO ***
  ** ESC KEY BREAK **
  [ BREAK PC=010B    NEXT PC=010C ]
  [ NEXT TRACE POINTER=2857 ]

* G 0,16F(15)
      RESET TRACE POINTER
   *** EMULATION GO ***
  ** ADDRESS PASS COUNT BREAK **
  [ BREAK PC=016F    NEXT PC=0000 ]
  [ NEXT TRACE POINTER=5520 ]

* G 0,RAM(3C-2)
      RESET TRACE POINTER
   *** EMULATION GO ***
  ** DATA MEMORY PASS COUNT BREAK **
  [ BREAK PC=0108    NEXT PC=010A ]
  [ NEXT TRACE POINTER=1311 ]

* G 0,BAR(XC-4)
      RESET TRACE POINTER
   *** EMULATION GO ***
  ** BA DATA PASS COUNT BREAK **
  [ BREAK PC=0108    NEXT PC=0109 ]
  [ NEXT TRACE POINTER=0259 ]
```

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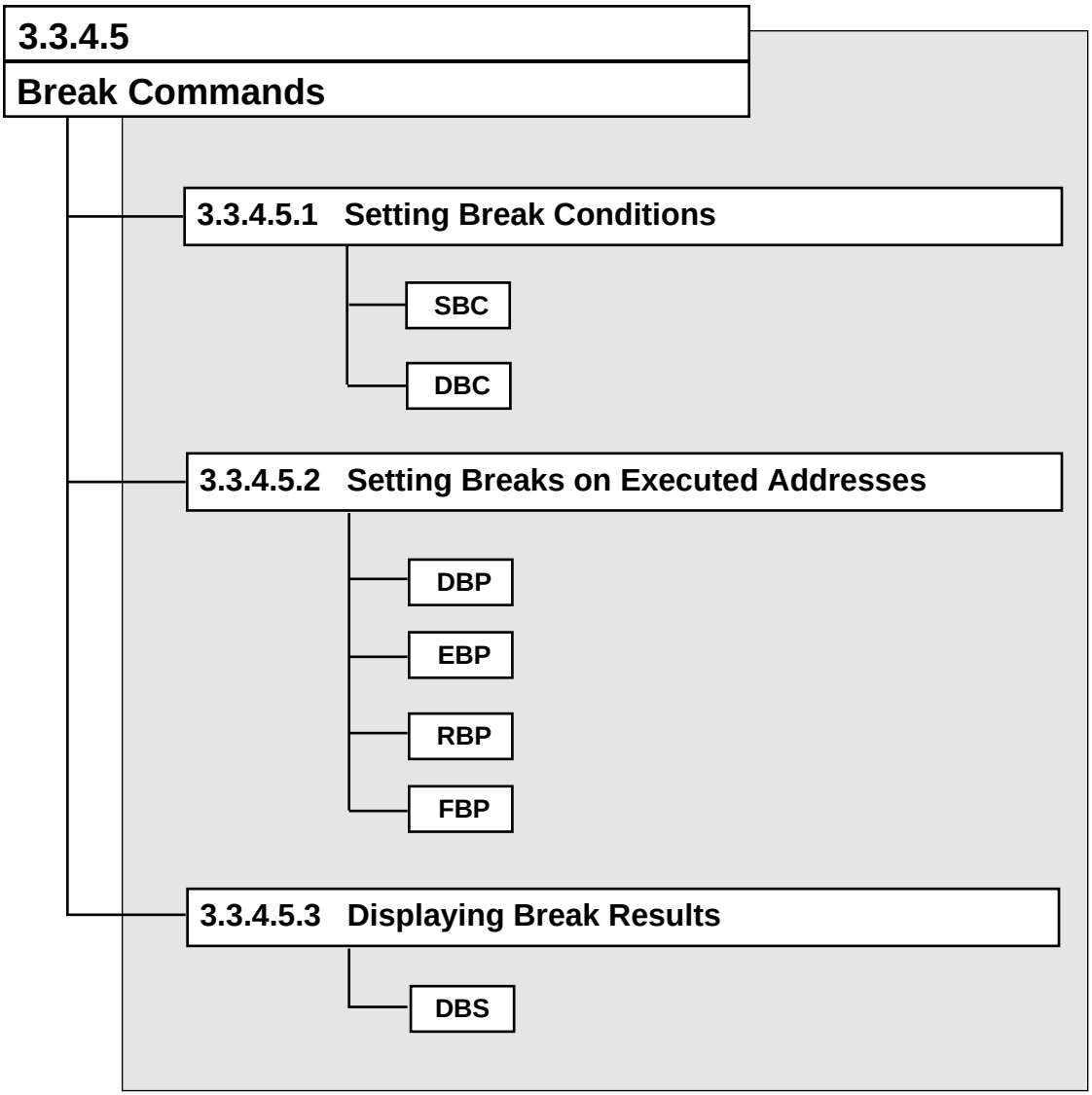

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3.3.4.5.1 Setting Break Conditions

SBC, DBC

Input Format

SBC ↵

DBC ↵

Description

The SBC command sets break conditions.

When the carriage return is input, input mode will be entered for each break condition.

```
BREAK POINT BREAK (Y/N)_
```

The operator sets or cancels each break condition by entering a 'Y' or 'N' at the underscore.

```
BREAK POINT BREAK (Y/N)  Y
CYCLE COUNTER OVER-FLOW BREAK (Y/N)  N
TRACE POINTER OVER-FLOW BREAK (Y/N)
                                        Input next parameter
```

When each carriage return is input, processing moves to the next parameter. If there is no next parameter, then the **SBC** command will terminate.

When the emulator is waiting for input data for a change, the following two key inputs are valid.

"Δ ↵"	(space followed by carriage return)	Process the next parameter without changing the current data. If there is no next parameter, then the SBC command will terminate.
"↵"	(carriage return only)	Terminate the SBC command.

The **DBC** command displays currently specified break conditions.

ALL BREAK CONDITIONS RESET	All break conditions have been canceled.
BREAK POINT BREAK	Breaks on breakpoint bits are set.
TRACE POINTER OVER-FLOW BREAK	Breaks on trace pointer overflow are set.
CYCLE COUNTER OVER-FLOW BREAK	Breaks on cycle counter overflow are set.

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SBC, DBC

Execution Example

```
* DBC
       BREAK POINT BREAK

* SBC
      BREAK POINT BREAK (Y/N)Y
      CYCLE COUNTER OVER-FLOW BREAK (Y/N)Y
      TRACE POINTER OVER-FLOW BREAK (Y/N)Y

* DBC
       BREAK POINT BREAK
       CYCLE COUNTER OVER-FLOW BREAK
       TRACE POINTER OVER-FLOW BREAK

* SBC
      BREAK POINT BREAK (Y/N)N
      CYCLE COUNTER OVER-FLOW BREAK (Y/N)N
      TRACE POINTER OVER-FLOW BREAK (Y/N)N

* DBC
       ALL BREAK CONDITION RESET
```


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3.3.4.5.2 Setting Breaks on Executed Addresses

DBP

Input Format

DBP Δ *address* [, *address*] ↵
or
DBP Δ ***** ↵

address	:	0~7DF (MSM64162 mode) 0~FDF (MSM64164 mode)
*****	:	display entire address range

Description

The **DBP** command displays the contents of breakpoint bit memory (☞1).

The address is a value 0H to 7DFH when in MSM64162 mode, or 0H to FDFH when in MSM64164 mode.

The DBP command can be forcibly terminated by pressing the ESC key.

Breaks will be performed at addresses where the breakpoint bit is '1.' Breaks will not be performed at addresses where the breakpoint bit is '0.'

Display contents are one of the following, depending on input format.

address	Displays the contents of one address.
address, address	Displays the range from the first address to the second address.
*****	Displays the entire area of breakpoint bit memory. (☞2).

☞ 1 Breakpoint bits correspond one-for-one with addresses in code memory. They are used to cause breaks at specified locations in a user program when executed with the G command.

A breakpoint bit is enabled when the breakpoint bit is '1.' However, the only breakpoint bits that can generate breaks are those corresponding to the address of the first byte of an instruction code in the user program.

Breakpoint bits are enabled as realtime emulation break conditions only when "BREAK POINT BREAK" is set as a break condition.

☞ 2 The entire area of breakpoint bit memory changes with the mode. When in MSM64162 mode, it is 0H to 7DFH. When in MSM64164 mode, it is 0H to FDFH.

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DBP, EBP, RBP, FBP

EBP

Input Format

EBP Δ *address* [, *address* . . . *address*] ↵

address : 0~7DF (MSM64162 mode)
0~FDF (MSM64164 mode)

Description

The **EBP** command sets breakpoint bits to '1.'

The address expresses an address to be set to “1.” It is a value 0H to 7DFH when in MSM64162 mode, or 0H to FDFH when in MSM64164 mode. Up to ten address values can be input with one command.

RBP

Input Format

RBP Δ *address* [, *address* . . . *address*] ↵

address : 0~7DF (MSM64162 mode)
0~FDF (MSM64164 mode)

Description

The **RBP** command resets breakpoint bits to '0.'

The address expresses an address to be set to “0.” It is a value 0H to 7DFH when in MSM64162 mode, or 0H to FDFH when in MSM64164 mode. Up to ten address values can be input with one command.

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FBP

Input Format

FBP Δ *address* , *address* [, *data*] ↵
or
FBP Δ ***** [, *data*] ↵

address	:	0~7DF (MSM64162 mode) 0~FDF (MSM64164 mode)
*****	:	display entire address range
data	:	0, 1

Description

The FBP command changes the contents of a specified range of breakpoint bit memory.

The address expresses a breakpoint bit memory address. It is a value 0H to 7DFH when in MSM64162 mode, or 0H to FDFH when in MSM64164 mode. The data is a the value of the change data. Its can be '0' or '1.'

The changes are classified by input format as follows.

address, address, data	Fill entire range from first address to second address with the data value.
address, address	Fill entire range from first address to second address with "0."
*****, *data*	Fill entire breakpoint bit memory area with the data value.
*****	Fill entire breakpoint bit memory area with ”0.” (☞ 1)

☞ **1** The entire area of breakpoint bit memory changes with the mode. When in MSM64162 mode, it is 0H to 7DFH. When in MSM64164 mode, it is 0H to FDFH.

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DBP, EBP, RBP, FBP

Execution Example

```
* FBP

* DBP 40,7F
           0 1 2 3 4 5 6 7 8 9 A B C D E F
  LOC=0040 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
  LOC=0050 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
  LOC=0060 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
  LOC=0070 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

* FBP 40,55,1

* DBP 40,7F
           0 1 2 3 4 5 6 7 8 9 A B C D E F
  LOC=0040 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
  LOC=0050 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0
  LOC=0060 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
  LOC=0070 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

* EBP 60,68,6F,73,79

* DBP 40,7F
           0 1 2 3 4 5 6 7 8 9 A B C D E F
  LOC=0040 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
  LOC=0050 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0
  LOC=0060 1 0 0 0 0 0 0 0 1 0 0 0 0 0 0 1
  LOC=0070 0 0 0 1 0 0 0 0 0 1 0 0 0 0 0 0

* RBP 68,73

* DBP 40,7F
           0 1 2 3 4 5 6 7 8 9 A B C D E F
  LOC=0040 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
  LOC=0050 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0
  LOC=0060 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1
  LOC=0070 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0
```


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3.3.4.5.3 Displaying Break Results

DBS

Input Format

DBS ↵

Description

The **DBS** command displays the break condition from realtime emulation.

ESC KEY BREAK	Break on ESC key input.
BREAK STATUS NOT FOUND	System has just been initialized or no program has been executed.
BREAK POINT BREAK	Break on a breakpoint bit.
TRACE POINTER OVER-FLOW BREAK	Break on trace pointer overflow.
CYCLE COUNTER OVER-FLOW BREAK	Break on cycle counter overflow.
ADDRESS MATCH BREAK	Break on address match.
ADDRESS PASS COUNT BREAK	Break on address pass count.
DATA MEMORY PASS COUNT BREAK	Break on data memory pass count.
BA DATA PASS COUNT BREAK	Break on BA register pass count.
N AREA BREAK	Break when address exceeded 7DFH in MSM64162 mode or FDFH in MSM64614 mode.

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DBS

Execution Example

```
* G 0,100
    RESET TRACE POINTER
   *** EMULATION GO ***
  ** ADDRESS MATCH BREAK **
  [ BREAK PC=0100    NEXT PC=0102 ]
  [ NEXT TRACE POINTER=0194 ]

* DBS
  ** ADDRESS MATCH BREAK **

* G 0
  RESET TRACE POINTER
 *** EMULATION GO ***
** ESC KEY BREAK **
[ BREAK PC=0109    NEXT PC=010A ]
 [ NEXT TRACE POINTER=0025 ]

* DBS
 ** ESC KEY BREAK **

* EBP 100

* G 0
  RESET TRACE POINTER
 *** EMULATION GO ***
** BREAK POINT BREAK **
[ BRAEAK PC=0100   NEXT PC=0102 ]
 [ NEXT TRACE POINTER=0194 ]

* DBS
  ** BREAK POINT BREAK **
```


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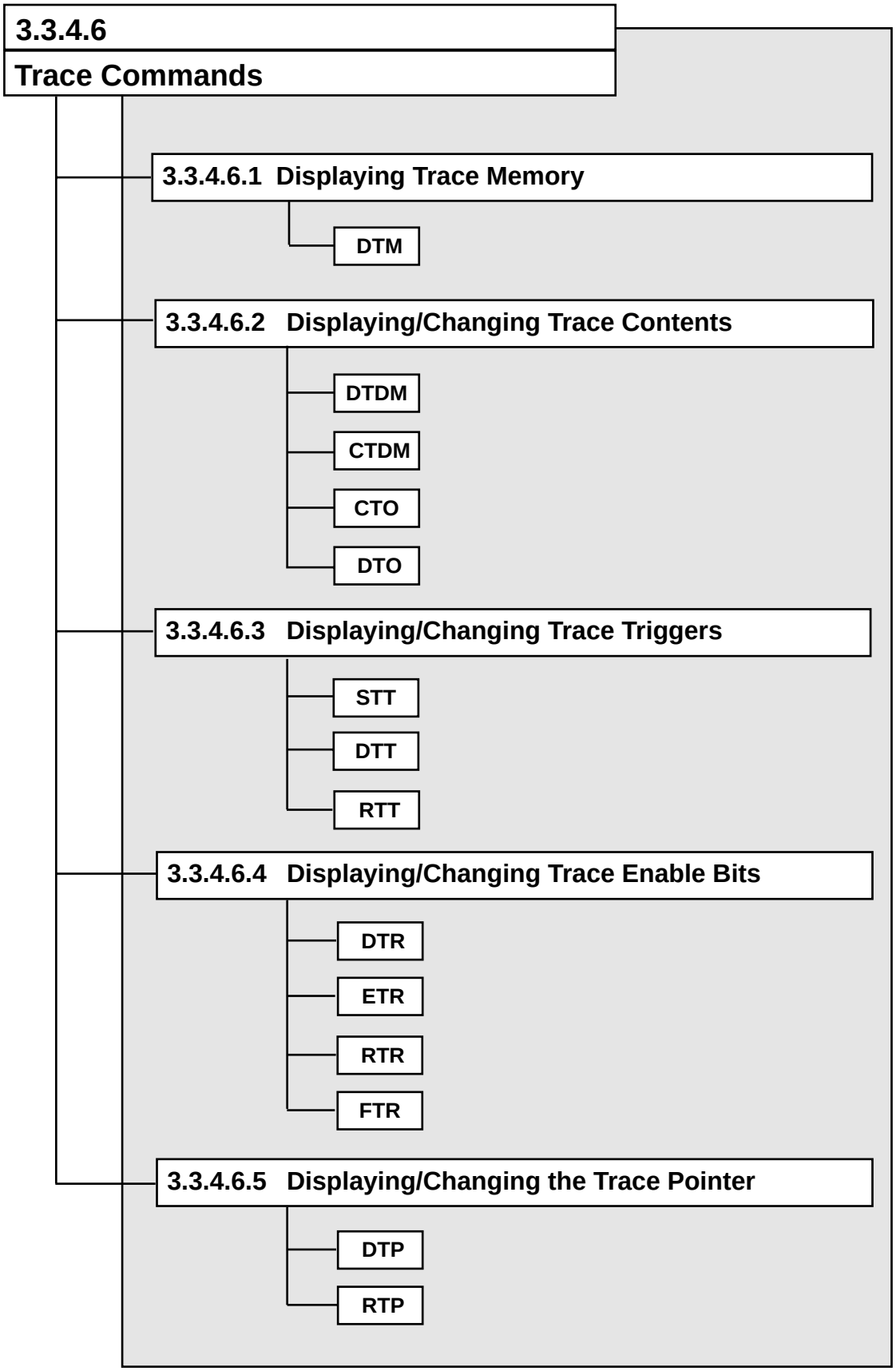

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DTM

3.3.4.6.1 Displaying Trace Memory

DTM

Input Format

DTM Δ *parm* ↵

parm	:	- $number_{-step}$, $number_{step}$
	:	$number_{Tp}$, $number_{step}$
	:	*

Description

The DTM command displays the contents of trace memory as specified by parm. Trace memory is an 8192 x 64-bit RAM area.

The $number_{step}$ indicates the number of steps to display as a decimal number 1-8192. The $number_{-step}$ indicates the number of steps back from the current trace pointer value (called TP below). The $number_{TP}$ indicates the TP value at which to start the trace display as a decimal number 0-8191 (☞ 1).

The * indicates that the contents of TP to TP-1 should be displayed if the trace pointer has overflowed, or the contents of 0 to TP-1 should be displayed if it has not.

Trace memory stores various information from realtime emulation. An operator can debug more efficiently be viewing this information.

As shown below, trace memory is configured as a ring, so during realtime emulation trace memory will be overwritten in order from the oldest contents first.

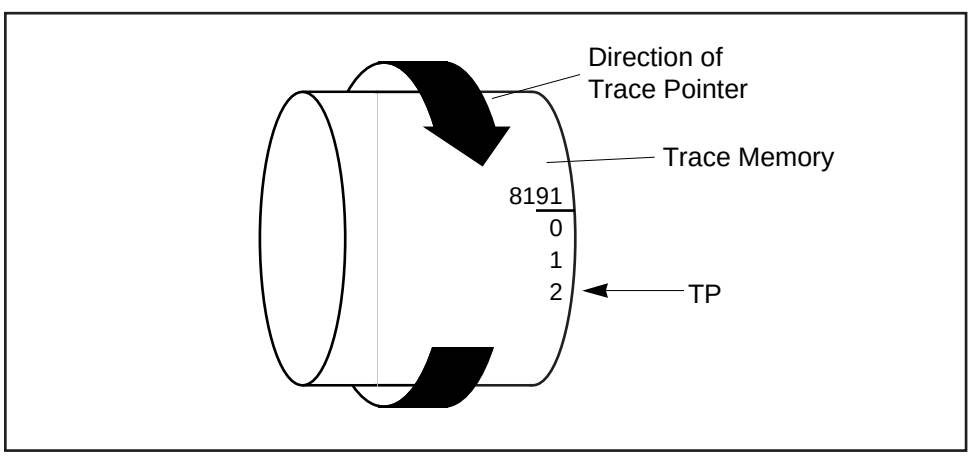

Figure 3-11. Trace Pointer Example

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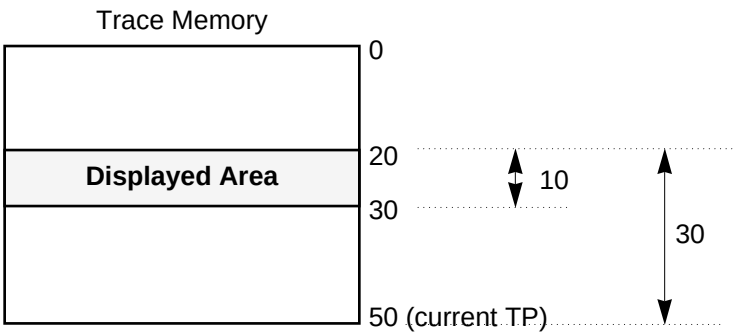
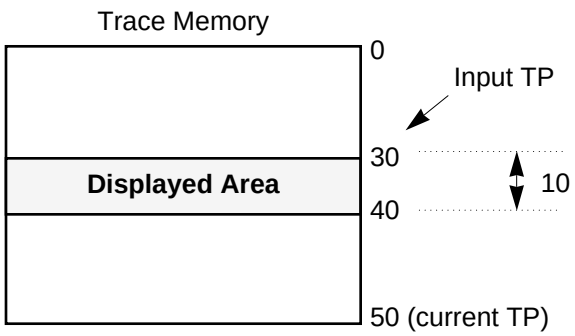
Examples of *-number*$_{-step}$, *number*$_{step}$ input and *number*$_{Tp}$, *number*$_{step}$ input are shown below. Assume that the current TP is 50.

Example DTM -30, 10



Example DTM 30, 10



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DTM

After the parameters are correctly input and a carriage return is pressed, a header in the format below will be displayed, followed by the trace memory contents for each trace pointer value.

```
  BA Δ HL Δ C Δ SP Δ R(address) Δ P2 Δ P3 Δ BC Δ BE Δ BS01 Δ
TP
```

The header is displayed every 10 steps. Trace data is shown as numbers only where it changes. It is displayed as '.' where it has not changed from the previous step. However, the trace data immediately after a header is always displayed as numbers. The address will be displayed as the data memory address specified by the CTDM command (☞ 2).

The above header is the initial display state. It can be changed with the CTO command as shown below.

(1) If BCF, BSR0, BEF, BSR1 are selected

```
  BA Δ HL Δ C Δ SP Δ R(address) Δ P2 Δ P3 Δ BC Δ BE Δ BS01 Δ
TP
```

(2) If P4, P0 are selected (☞ 3)

```
  BA Δ HL Δ C Δ SP Δ R(address) Δ P2 Δ P3 Δ P4 Δ P0 Δ TP
```

(3) If P4, P1 are selected (☞ 3)

```
  BA Δ HL Δ C Δ SP Δ R(address) Δ P2 Δ P3 Δ P4 Δ P1 Δ TP
```

The trace contents displayed and the corresponding headers are shown below.

B	B register
A	A register
H	H register
L	L register
C	Carry flag
SP	Stack pointer
R(address)	Data memory at address
P2	Port 2
P3	Port 3
BC	BCF flag
BE	BEF flag
BS01	BSR0 register and BSR1 register
P4	Port 4
P0	Port 0
P1	Port 1

Tracing of the BCF flag, BEF flag, BSR0 register, BSR1 register and Port 4, Port 0 or Port 4,Port 1 is selected with the CTO command.

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1 Keep in mind the following points when displaying the contents of trace memory.

- If trace memory has not overflowed, then trace data will be stored in trace memory from 0 to the current TP. Accordingly, if the input TP or number of back steps is greater than the current TP, then trace memory from 0 will be displayed. If the number of steps input is greater than the number of steps stored in trace memory, then only steps with stored data will be displayed.

- If trace memory has overflowed, then trace data will be stored in the entire trace memory (0-8191), regardless of the current TP. Accordingly, if the number of back steps is greater than the current TP, then data before a TP of 0 (8191, 8190, 8189, ...) will be displayed.

2 The data memory address to be traced is specified with the CTDM command. Data memory tracing traces write data each time it is written to the specified address in data memory. Usually the value of the upper 4 bits of the data memory trace will be FH, but when data is written with an 8-bit move instruction or 8-bit calculation instruction the full 8 bits of write data will be traced. Data memory tracing will not be performed when the data memory address specified by an instruction's addressing does not match the address specified by the CTDM command.

3 Port 4 will not be displayed if MSM64162 mode is selected.

! When trace data being displayed changes, it is traced with a one-instruction delay.

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DTM

Execution Example

```
* CTO
      (1) BCF,BSR0,BEF,BSR1
      (2) P4,P0
      (3) P4,P1
            TRACE OBJECT ---> 1
      ** RESET TRACE POINTER **

* G 0,100
    RESET TRACE POINTER
   *** EMULATION GO ***
  ** ADDRESS MATCH BREAK **
  [ BREAK PC=0100    NEXT PC=0102 ]
   [ NEXT TRACE POINTER=0012 ]


* DTM 0,11
                          BA HL C SP R(700) P2 P3 BC BE BS01 TP
  LOC=0000 13   SBC       DA 00 0 EF DC      F  F  1  0   70 0000
  LOC=0001 95   LAI  5    .. .. . .. ..      .  .  .  .   .. 0001
  LOC=0002 2D36 LMAD 36   .5 .. . .. ..      .  .  .  .   .. 0002
  LOC=0004 9A   LAI  A    .. .. . .. ..      .  .  .  .   .. 0003
  LOC=0005 2D36 LMAD 36   .A .. . .. ..      .  .  .  .   .. 0004
  LOC=0007 2D0F LMAD 0F   .. .. . .. ..      .  .  .  .   .. 0005
  LOC=0009 247C RMBD 7C,0 .. .. . .. ..      .  .  .  .   .. 0006
  LOC=000B 2B31 SMBD 31,1 .. .. . .. ..      .  .  .  .   .. 0007
  LOC=000D 287C SMBD 7C,0 .. .. . .. ..      .  .  .  .   .. 0008
  LOC=000F 2809 SMBD 09,0 .. .. . .. ..      .  .  .  .   .. 0009
                          BA HL C SP R(700) P2 P3 BC BE BS01 TP
  LOC=0011 A900 JP   0100 DA 00 0 EF DC      F  F  1  0   70 0010
```


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3.3.4.6.2 Displaying/Changing Trace Contents

DTDM, CTDM

Input Format

DTDM ↵
CTDM [Δ *address*] ↵
address : 780~7FF (MSM64162 mode)
700~7FF (MSM64164 mode)

Description

The **DTDM** command displays the data memory address being traced. When the carriage return is input, the emulator will output the following message.

TRACE DATA MEMORY ADDRESS ---> *address*

The address is the data memory address being traced.

The **CTDM** command sets the address to trace. The *address* is the address to trace. It is a value 780H to 7FFH when in MSM64162 mode, or 700H to 7FFH when in MSM64164 mode. If it is omitted, then the emulator will output the following message and wait for data input.

TRACE DATA MEMORY ADDRESS : *old-data* OLD --->

Here old-data is the data memory address currently set. The operator inputs a new address and a carriage return. The new address should be a value 780H to 7FFH when in MSM64162 mode, or 700H to 7FFH when in MSM64164. If a carriage return only is input, then the **CTDM** command will terminate without changing the data address.

When the emulator is waiting for input data for a change, the following key input is valid in addition to a new address.

"↵" (carriage return only) Terminate the **CTDM** command.

If a data memory match break is specified as a break parameter of the G command, then the object of the match will be data memory address specified with the CTDM command.

Execution Example

```
* DTDM
  TRACE DATA MEMORY ADDRESS ---> 0700

* CTDM
  TRACE DATA MEMORY ADDRESS : 0700 OLD ---> 790 NEW

* DTDM
  TRACE DATA MEMORY ADDRESS ---> 0790
```


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DTO, CTO

Input Format

DTO ↵
CTO ↵

Description

The **CTO** command selects one of three sets of trace objects traced in 8 bits of trace memory. These trace objects are listed below.

- BCF, BSR0, BEF, BSR1
- P4, P0
- P4, P1

The **DTO** command displays the currently set trace objects.

The **CTO** command sets the trace objects. When the carriage return is input, the emulator outputs the following message and waits for data.

(1) BCF, BSR0, BEF, BSR1
(2) P4, P0
(3) P4, P1
TRACE OBJECT --->

Here the user inputs a 1 or 3, followed by a carriage return.

When the emulator is waiting for input, the following key input is valid in addition to 1 or 3.

"↵" (carriage return only) Terminate the CTO command.

- When the trace objects are changed with the CTO command, the TP (trace pointer) will be reset to '0.'
- After a system reset, the trace objects will be set to BCR, BSR0, BEF, and BSR1.

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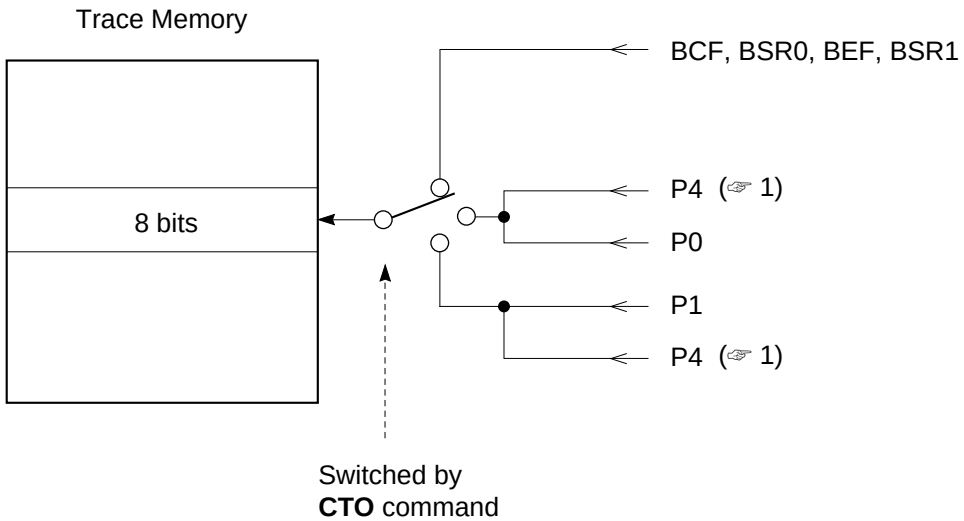

☞ 1 In MSM64162 mode P4 (port 4) data is not traced and is not displayed by the DTM command. P4 is also not displayed by the CTO command.

Execution Example

```
* DTO
  TRACE OBJECT ---> BCF,BSR0,BEF,BSR1

* CTO
  (1) BCF,BSR0,BEF,BSR1
  (2) P4,P0
  (3) P4,P1
         TRACE OBJECT ---> 2
 ** RESET TRACE POINTER **

* DTO
  TRACE OBJECT ---> P4,P0
```


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STT, DTT, RTT

3.3.4.6.3 Displaying/Changing Trace Triggers

STT

Input Format

STT ↵
DTT ↵
RTT ↵

The **STT** command sets the trace start address and trace stop address for trigger tracing.

The **DTT** command displays the trace trigger settings.

The **RTT** command cancels trigger tracing, and enables address tracing.

Description

There are two conditions for executing a trace.

(1) Address tracing

With address tracing, tracing is performed upon execution of addresses where the trace enable bit is set to '1.' The trace enable bit must be set at the address of the first byte of each instruction to be traced (☞ 1).

(2) Trigger tracing

When the STT command sets a trace start address and trace stop address, the trace start bit and trace stop bit at those respective addresses will be set to '1.' With trigger tracing, tracing starts when an address with the trace start bit set to '1' is passed. Tracing then stops when an address with the trace stop bit set to '1' is passed (☞ 2).

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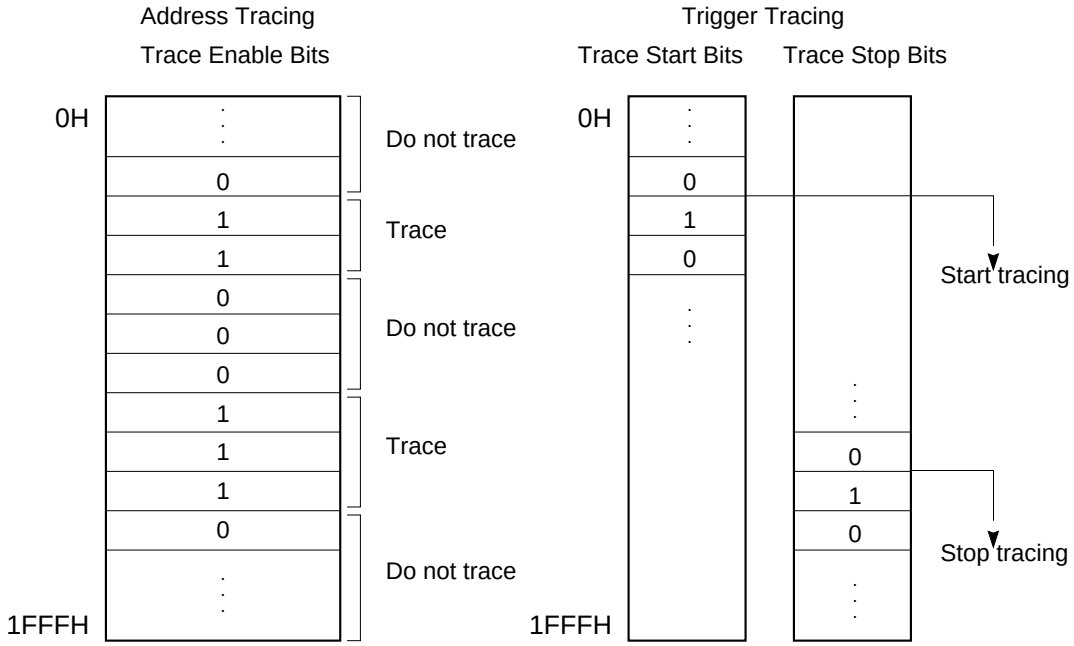
STT, DTT, RTT

Selection of address tracing or trigger tracing is performed with the STT and RTT commands.

- Select address tracing --- Execute **RTT** command, disabling trigger tracing.
- Select trigger tracing ----- Execute **STT** command, enabling trigger tracing.

The concepts of address tracing and trigger tracing are shown below.



Address tracing will be selected when the system is reset.

1 Trace enable bits correspond one-for-one with addresses in code memory. They enable tracing when address tracing is being executed. Trace enable bits need to be set to '1' at the address of the first byte of each instruction to be traced.

2 Trace start bits and trace stop bits both correspond one-for-one with addresses in code memory. They set the start and stop addresses for tracing when trigger tracing is being executed. Trace start bits and trace stop bits need to be set to '1' at the address of the first byte of their respective instructions. The contents of the address where the trace start bit is '1' will be traced, but the contents of the address where the trace stop bit is '1' will not be traced. If the start address set with the **G** command is identical to the trace start address, then tracing will start when the trace start address is passed the second time.

When the carriage return of an STT command is input, the emulator will output the following message and wait for input.

START ADDRESS : *old-address* OLD --->

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STT, DTT, RTT

Here old-address is the currently set trace start address. The operator inputs the new address at which trace execution is to start, followed by a carriage return. The address is a value 0H to 7DFH when in MSM64162 mode, or 0H to FDFH when in MSM64164 mode. When the carriage return is input, the emulator moves to input mode for the next parameter.

When the emulator is waiting for input, the following two key inputs are valid in addition to an address.

"Δ ↵"	(space followed by carriage return)	Proceed to process next parameter without changing the start address.
"↵"	(carriage return only)	Terminate the STT command without changing the start address.

After input of the start address is complete, the emulator outputs the following message and waits for data input.

STOP ADDRESS : *old-address* OLD --->

Here old-address is the currently set trace stop address. The operator inputs the new address at which trace execution is to stop, followed by a carriage return. The address is a value 0H to 7DFH when in MSM64162 mode, or 0H to FDFH when in MSM64164 mode.

When the emulator is waiting for input, the following two key inputs are valid in addition to an address.

"Δ ↵"	(space followed by carriage return)	For both key inputs, terminate the **STT** command without changing the stop address.
"↵"	(carriage return only)	

When the **STT** command terminates, the trace start bit will be set to '1' at the address set as the start address, the trace stop bit will be set to '1' at the address set as the stop address, and then the emulator will wait for the next command to be input. Both the start address and stop address need to be set at the first byte of an instruction code.

After execution of an **STT** command, the trace triggers will remain valid until an **RTT** command is executed.

The **DTT** command outputs the following message when its carriage return is input.

START ADDRESS : *start-address*
STOP ADDRESS : *stop-address*

Here start-address will be the address at which to start trace execution, and stop-address will be the address at which to stop trace execution.

The **RTT** command cancels trigger tracing and enables address tracing when its carriage return is input. However, if an **STT** command has been executed before the **RTT** command input, then the start address and stop address set by that **STT** command will be saved. Later when another **STT** command is input, if just a carriage return is input, then trigger tracing will be enabled and tracing will execute from the saved start address to the saved stop address.

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Execution Example

```
* STT
  START ADDRESS 0000 OLD  ---> 100 NEW
  STOP  ADDRESS 0100 OLD  ---> 200 NEW

* DTT
  START ADDRESS 0100
  STOP  ADDRESS 0200

* G 0,300
    RESET TRACE POINTER
   *** EMULATION GO ***
  ** ADDRESS MATCH BREAK **
  [ BREAK PC=0300    NEXT PC=0301 ]
   [ NEXT TRACE POINTER=0256 ]

* RTT
```


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DTR, ETR, RTR, FTR

3.3.4.6.4 Displaying/Changing Trace Enable Bits

DTR

Input Format

DTR Δ address [, address] ↵
or
DTR Δ * ↵

address : 0~7DF (MSM64162 mode)
0~FDF (MSM64164 mode)

Description

The **DTR** command displays the contents of trace enable bit memory.

Trace enable bits correspond one-for-one with code memory addresses. When address tracing is selected, the user can control trace execution by manipulating the trace enable bits.

When address tracing is selected and a user program is executed, the emulator examines the trace enable bit at the address of each executed instruction code. If a trace enable bit is '1,' then the trace information at that time will be written to trace memory. Thus, the user can write only the trace information he needs into trace memory by setting the appropriate trace enable bits to '1.'

Only trace enable bits set at the first byte of an instruction code are effective.

The address is a value 0H to 7DFH when in MSM64162 mode, or 0H to FDFH when in MSM64164 mode.

The **DTR** command can be forcibly terminated by pressing the ESC key.

Tracing will be performed at addresses where the trace enable bit is '1.' Tracing will not be performed at addresses where the trace enable bit is '0.'

Display contents are one of the following, depending on input format.

address	Displays the contents of one address.
address, address	Displays the range from the first address to the second address.
*	Displays the entire area of trace enable bit memory (☞ 1).

☞ 1 The entire area of trace enable bit memory changes with the mode. When in MSM64162 mode, it is 0H to 7DFH. When in MSM64164 mode, it is 0H to FDFH.

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ETR

Input Format

ETR Δ *address* [, address . . . , address] ↵

address : 0~7DF (MSM64162 mode)
0~FDF (MSM64164 mode)

Description

The **ETR** command sets trace enable bits to '1.'

The address expresses an address to be set to '1.' It is a value 0H to 7DFH when in MSM64162 mode, or 0H to FDFH when in MSM64164 mode. Up to ten address values can be input with one command.

RTR

Input Format

RTR Δ *address* [, address . . . , address] ↵

address : 0~7DF (MSM64162 mode)
0~FDF (MSM64164 mode)

Description

The **RTR** command resets trace enable bits to '0.'

The address expresses an address to be set to '0.' It is a value 0H to 7DFH when in MSM64162 mode, or 0H to FDFH when in MSM64164 mode. Up to ten address values can be input with one command.

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DTR, ETR, RTR, FTR

FTR

Input Format

FTR Δ *address , address* [, *data*] ↵
or
FTR Δ ***** [, *data*] ↵

address	:	0~7DF (MSM64162 mode) 0~FDF (MSM64164 mode)
*****	:	display entire address range
data	:	0, 1

Description

The address expresses a trace enable bit memory address. It is a value 0H to 7DFH when in MSM64162 mode, or 0H to FDFH when in MSM64164 mode. The data is a the value of the change data. Its can be '0' or '1.'

The changes are classified by input format as follows.

address, address, data	Fill entire range from first address to second address with the data value.
address, address	Fill entire range from first address to second address with "0."
*****, *data*	Fill entire trace enable bit memory area with the data value.
*****	Fill entire trace enable bit memory area with "0." (☞ 1)

☞ **1** The entire area of trace enable bit memory changes with the mode. When in MSM64162 mode, it is 0H to 7DFH. When in MSM64164 mode, it is 0H to FDFH.

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Execution Example

```
* FTR *

* DTR 30,60
            0 1 2 3 4 5 6 7 8 9 A B C D E F
  LOC=0030  0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
  LOC=0040  0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
  LOC=0050  0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
  LOC=0060  0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

* FTR 30,4A,1

* DTR 30,60
            0 1 2 3 4 5 6 7 8 9 A B C D E F
  LOC=0030  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
  LOC=0040  1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0
  LOC=0050  0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
  LOC=0060  0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

* ETR 50,5A,63,6F

* DTR 30,60
            0 1 2 3 4 5 6 7 8 9 A B C D E F
  LOC=0030  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
  LOC=0040  1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0
  LOC=0050  1 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0
  LOC=0060  0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 1

* RTR 5A,63

* DTR 30,60
            0 1 2 3 4 5 6 7 8 9 A B C D E F
  LOC=0030  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
  LOC=0040  1 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0
  LOC=0050  1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
  LOC=0060  0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1
```


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3.3.4.6.5 Displaying/Changing the Trace Pointer

DTP, RTP

Input Format

DTP ↵ Display trace pointer

RTP ↵ Clear trace pointer

Description

The **DTP** command displays the contents of the current trace pointer (TP). The value is displayed as decimal data.

The **RTP** command clears the trace pointer value to 0. The trace pointer is also initialized to 0 when power is turned on, when a start address is specified with a **G** command, or when the trace objects are changed with the **CTO** command.

Execution Example

```
* DTP
  TRACE POINTER ---> 5039

* RTP
  ** RESET TRACE POINTER **

* DTP
  TRACE POINTER ---> 0000
```


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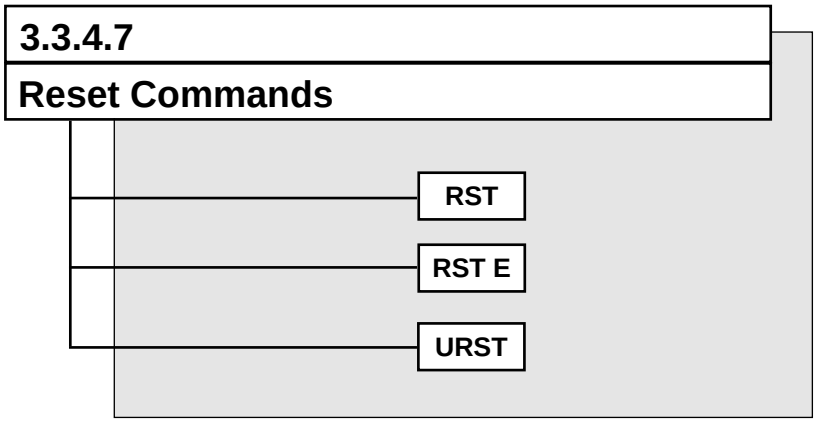
3.3.4.7 Reset Commands



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RST

RST

Input Format

RST ↵

Description

The RST command resets the EASE64162/164 as follows.

Cycle counter	Reset to 0.
Break status register	Invalidate all break status.
Trigger trace start address	Disabled.
Trigger trace stop address	Disabled.
Trace mode	Set to address trace mode.
Cycle counter start address	Disabled.
Cycle counter stop address	Disabled.
Instruction executed memory	All reset to 0.
Evaluation board	Reset to same as when MSM64164 is reset.

Execution Example

```
* RST
  Low-Power Series Emulator << EASE64162/164 >>  Ver 2.24
```

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RST E

Input Format

RST ∆ E ↵

Description

The **RST E** command resets the evaluation board.

After this command is executed, the evaluation board will be reset to the same state as when the MSM64162 or MSM64164 is reset. For details about the state after reset, refer to the user's manual of the chip.

Execution Example

```
* RST E
  **** EVA BOARD RESET ****
```


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URST

URST

Input Format

URST [Δ *mnemonic*] ↵

Description

The URST command sets whether the $\overline{\text{RESET}}$ pin input of the user cable is enabled or not.

One of the following parameters is entered for mnemonic.

ON : Inputs from $\overline{\text{RESET}}$ pin during realtime emulation are enabled.
OFF : Inputs from $\overline{\text{RESET}}$ pin are disabled.

If mnemonic is omitted, then the current setting will be displayed. After a system reset, inputs from the $\overline{\text{RESET}}$ pin are disabled.

Execution Example

```
* URST
  USER RESET DISABLE

 * URST ON

* URST
  USER RESET ENABLE

* URST OFF

* URST
  USER RESET DISABLE
```

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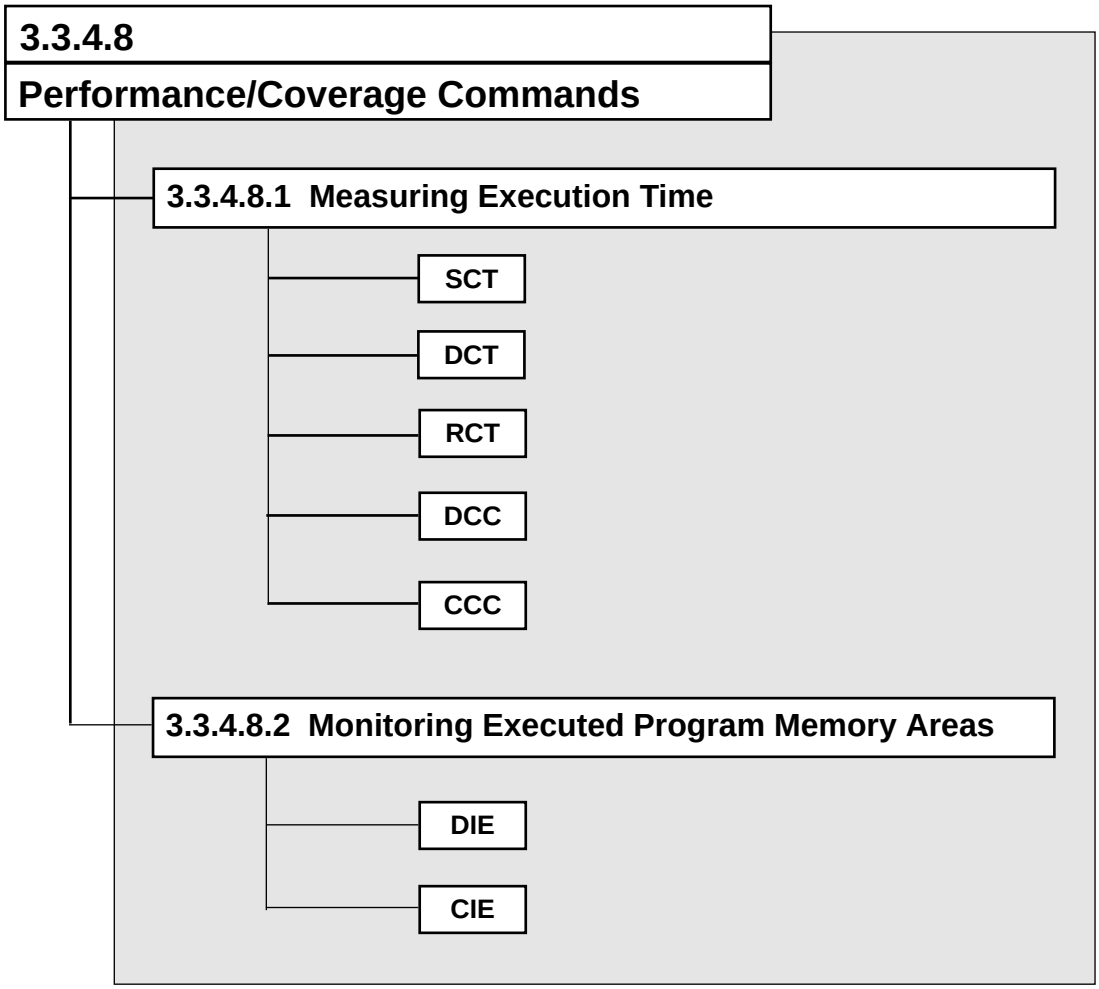
3.3.4.8
Performance/Coverage Commands
3.3.4.8.1 Measuring Execution Time
SCT
DCT
RCT
DCC
CCC
3.3.4.8.2 Monitoring Executed Program Memory Areas
DIE
CIE

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SCT, DCT, RCT

3.3.4.8.1 Measuring Execution Time

SCT

Input Format

SCT ↵
DCT ↵
RCT ↵

Description

The **SCT** command specifies the addresses where cycle counter counting is to start and stop. This command allows program execution time to be measured by incrementing the cycle counter during **G** command execution (☞ 1).

The cycle counter is a 32-bit binary counter, so it can count up to a maximum of 4,294,967,295. Program execution breaks on cycle counter overflow are also possible.

The **DCT** command displays the cycle counter start and stop addresses.

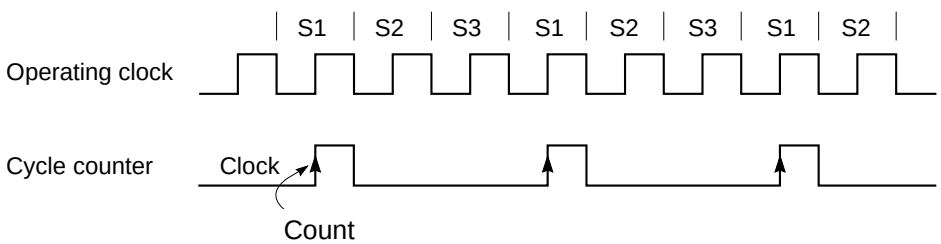
The **RCT** command disables the cycle counter start and stop addresses and stops cycle counter counting.

When the **SCT** command sets a cycle counter start address and cycle counter stop address, the cycle counter start bit and cycle counter stop bit at those respective addresses will be set to '1.' After **G** command program execution starts, cycle counting starts when an address with the cycle counter start bit set to '1' is passed. Cycle counting then stops when an address with the cycle counter stop bit set to '1' is passed (☞ 2).

☞ 1 The cycle counter is incremented each machine cycle. Program execution time can be calculated with the following formula.

Program execution time = 1/frequency x 3 x cycle counter value

Below is a timing diagram of cycle counter counting.



☞ 2 Cycle counter start bits and cycle counter stop bits both correspond one-for-one with addresses in code memory. They set the start and stop addresses for cycle counter counting. Cycle counter start bits and cycle counter stop bits need to be set to '1' at the address of the first byte of their respective instructions. The cycle counter will not be incremented at the address where the cycle counter stop bit is set to '1.'

! The cycle counter is not incremented in hold mode.

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When the carriage return of an **SCT** command is input, the emulator will output the following message and wait for input.

START ADDRESS : *old-address* OLD --->

Here old-address is the currently set cycle counter start address. The operator inputs the new address at which cycle counter counting is to start, followed by a carriage return. The address is a value 0H to 7DFH when in MSM64162 mode, or 0H to FDFH when in MSM64164 mode. When the carriage return is input, the emulator moves to input mode for the next parameter.

When the emulator is waiting for input, the following two key inputs are valid in addition to an address.

"Δ ↵"	(space followed by carriage return)	Proceed to process next parameter without changing the start address.
"↵"	(carriage return only)	Terminate the SCT command without changing the start address.

After input of the start address is complete, the emulator outputs the following message and waits for data input.

STOP ADDRESS : *old-address* OLD --->

Here old-address is the currently set cycle counter stop address. The operator inputs the new address at which cycle counter counting is to stop, followed by a carriage return. The address is a value 0H to 7DFH when in MSM64162 mode, or 0H to FDFH when in MSM64164 mode.

When the emulator is waiting for input, the following two key inputs are valid in addition to an address.

"Δ ↵"	(space followed by carriage return)	For both key inputs, terminate the SCT command without changing the stop address.
"↵"	(carriage return only)	

When the **SCT** command terminates, the cycle counter start bit will be set to '1' at the address set as the start address, the cycle counter stop bit will be set to '1' at the address set as the stop address, and then the emulator will wait for the next command to be input. Both the start address and stop address need to be set at the first byte of an instruction code.

After execution of an **SCT** command, the cycle counter settings will remain valid until an RCT command is executed.

The **DCT** command outputs the following message when its carriage return is input.

START ADDRESS : *start-address*
STOP ADDRESS : *stop-address*

Here start-address will be the address at which to start cycle counter counting, and stop-address will be the address at which to stop cycle counter counting.

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SCT, DCT, RCT

The **RCT** command cancels the start and stop addresses set by the previous **SCT** command when its carriage return is input. However, the start address and stop address set by that **SCT** command will be saved. Later when another **SCT** command is input, if just a carriage return is input, then cycle counter counting will be performed from the saved start address to the saved stop address.

Execution Example

```
* SCT
  START ADDRESS 0000 OLD ---> NOT CHANGE
  STOP  ADDRESS 0000 OLD ---> 100 NEW

* DCT
  START ADDRESS 0000
  STOP  ADDRESS 0100

* CCC
  CYCLE COUNTER STATUS : 0000000000

* G 0,100
      RESET TRACE POINTER
   *** EMULATION GO ***
  ** ADDRESS MATCH BREAK **
  [ BREAK PC=0100    NEXT PC=0101 ]
   [ NEXT TRACE POINTER=0257 ]

* DCC
  CYCLE COUNTER STATUS : 0000000256

* RCT
```

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DCC

Input Format

DCC ↵

Description

The DCC command displays the contents of the cycle counter. When the carriage return is entered, the emulator will output the following message.

CYCLE COUNTER STATUS : *number*

The number is the cycle counter value displayed in decimal.

Execution Example

```
* DCC
  CYCLE COUNTER STATUS : 0000000256
```


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CCC

CCC

Input Format

CCC [-] *number* ↵
data : 0–4294967295

Description

The **CCC** command changes the cycle counter contents to the value indicated by *number*. The *number* should be a decimal value 0 to 4,294,967,295. If a minus sign '-' is input before *number*, then the cycle counter will be set to the value of *number* subtracted from 4,294,967,295.

Execution Example

```
* CCC 19
  CYCLE COUNTER STATUS : 0000000019

* CCC -1
  CYCLE COUNTER STATUS : 4294967294
```

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3.3.4.8.2 Monitoring Executed Program Memory Areas

DIE, RIE

Input Format

DIE Δ *address* [, *address*] ↵
or
DIE Δ ***** ↵

address	:	0~7DF (MSM64162 mode) 0~FDF (MSM64164 mode)
*****	:	display entire address range

RIE ↵

Description

The **DIE** command displays the contents of instruction executed bit memory.

Instruction executed bits correspond one-for-one with code memory addresses. While realtime emulation of a user program executes, the instruction executed bits at the same addresses as executed instruction codes will be set to '1.' After realtime emulation, using the **DIE** command to view the contents of instruction executed memory can show ranges which user program executed.

When a start address is specified with the G command, all instruction executed bit memory will be reset to 0.

The address is a value 0H to 7DFH when in MSM64162 mode, or 0H to FDFH when in MSM64164 mode.

The **DIE** command can be forcibly terminated by pressing the ESC key.

Addresses where the instruction executed bits are '1' indicate addresses where the user program was executed. Addresses where the instruction executed bits are '0' indicate addresses where the user program was not executed.

Display contents are one of the following, depending on input format.

address	Displays the contents of one address.
address, address	Displays the range from the first address to the second address.
*****	Displays the entire area of instruction executed bit memory (☞ 1).

☞ **1** The entire area of instruction executed bit memory changes with the mode. When in MSM64162 mode, it is 0H to 7DFH. When in MSM64164 mode, it is 0H to FDFH.

The **RIE** command resets the entire contents of instruction executed bit memory to '0.'

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DIE, RIE

Execution Example

```
* RIE

* G 32,4E
      RESET TRACE POINTER
   *** EMULATION GO ***
  ** ADDRESS MATCH BREAK **
  [ BREAK PC=004E    NEXT PC=004F ]
   [ NEXT TRACE POINTER=0029 ]

* DIE 20, 5F

           0 1 2 3 4 5 6 7 8 9 A B C D E F
  LOC=0020  0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
  LOC=0030  0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1
  LOC=0040  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0
  LOC=0050  0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
```

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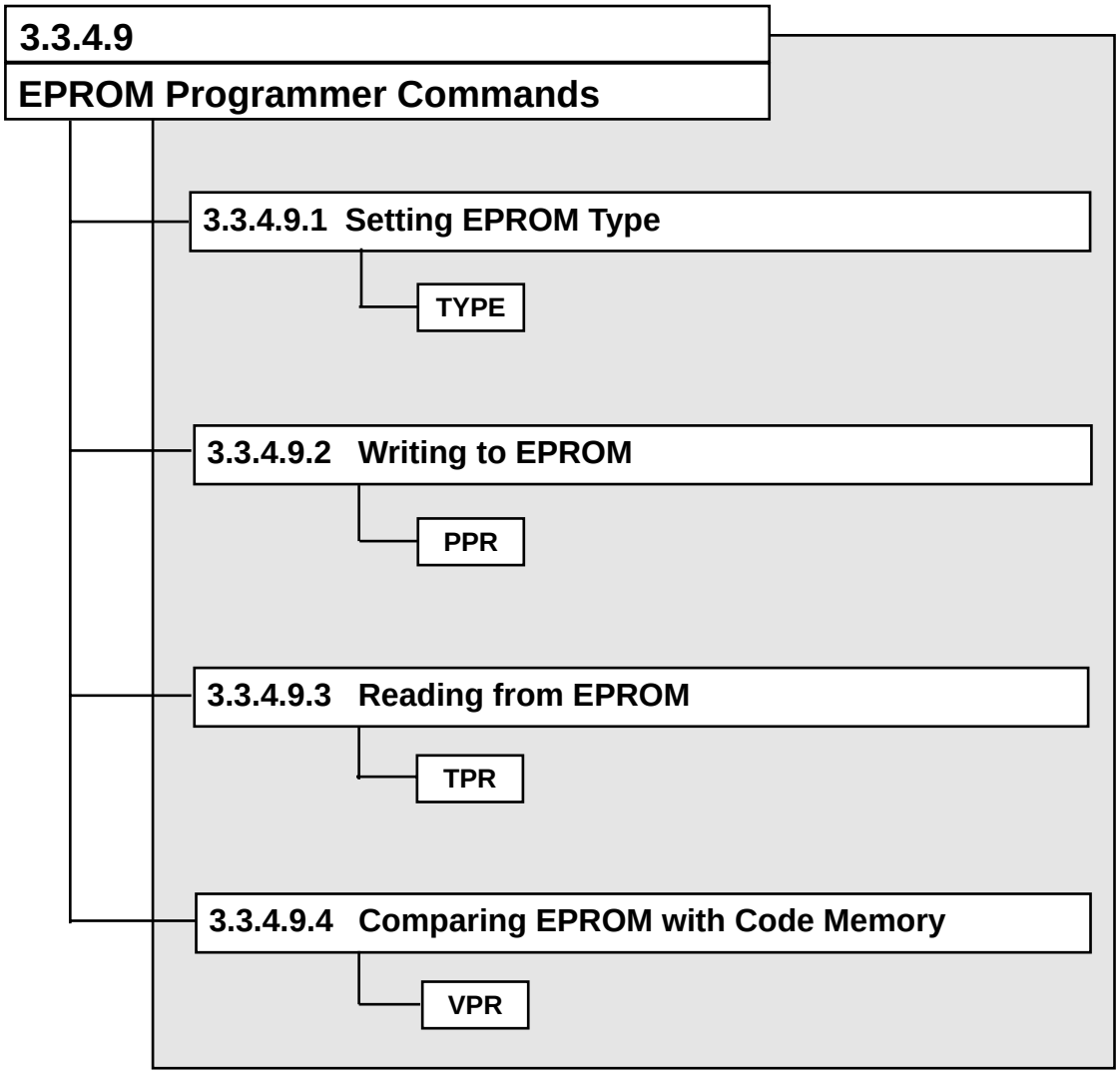

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TYPE

3.3.4.9.1 Setting EPROM Type

TYPE

Input Format

TYPE Δ [*parm*] ↵

parm : *mnemonic*

Description

The **TYPE** command sets the type of EPROM that will be used in the EPROM programmer. The mnemonic indicates the EPROM type.

Usable EPROM types are one of the following.

Intel products and other EPROMs that are written at high speed with the Intelligent Programming method.

The following can be input for mnemonic.

EPROM Type	mnemonic
2764	64
27128	128
27256	256
27512	512

If mnemonic is omitted, then the currently set EPROM type will be displayed. The setting will be "27512" after power is turned on.

Execution Example

```
* TYPE
  EPROM TYPE --->27512

* TYPE 256

* TYPE
  EPROM TYPE --->27256
```

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3.3.4.9.2 Writing to EPROM

PPR

Input Format

PPR Δ *address*$_{code}$, *address*$_{code}$ [, *address*$_{EPROM}$] ↵
or
PPR Δ ***** ↵

address$_{code}$	:	0~7DF (MSM64162 mode) 0~FDF (MSM64164 mode)
*****	:	writes entire address range
address$_{EPROM}$	:	EPROM write start address

Description

The **PPR** command writes the contents of the specified code memory area to the EPROM starting at the specified *address*$_{EPROM}$.

Each *address*$_{code}$ is a value 0H to 7DFH when in MSM64162 mode, or 0H to FDFH when in MSM64164 mode. The *address*$_{code}$, *address*$_{code}$ specifies the range of code memory to be written. If an '*****' is input, then a range of code memory that corresponds to the EPROM type will be set (☞ 1).

The *address*$_{EPROM}$ is the EPROM's starting address for writing. If this address is omitted, then writing will start from EPROM address 0.

Input continues until a carriage return is entered. Then the following message will be output.

EPROM TYPE ---> *type*
START PROGRAMMING [Y/N] ---> _

Here *type* indicates the currently set EPROM type. If the EPROM type displayed is the same as the EPROM type that the user wants to write, then enter "Y↵" at the underscore. If they are different, then input "N↵" and set the EPROM type again with the TYPE command.

When "Y↵" is input at the underscore, the EASE64162/164 "RUN" indicator will light, and the data write will start. If the data write completes normally, then the "RUN" indicator will go off, the PPR command will terminate, and the emulator will wait for another command input.

☞ **1** The range of code memory written to EPROM when '*****' is input changes with the mode. When in MSM64612 mode, it is 0H to 7DFH. When in MSM64164 mode, it is 0H to FDFH.

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PPR

Execution Example

```
* PPR 0,1FF,0
  EPROM TYPE ---> 27512
  START PROGRAMMING [Y/N] --->Y

* TYPE 128

* PPR *,0
  EPROM TYPE ---> 27128
  START PROGRAMMING [Y/N] --->Y
```


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3.3.4.9.3 Reading from EPROM

TPR

Input Format

TPR Δ *address*$_{code}$, *address*$_{code}$ [, *address*$_{EPROM}$] ↵

or

TPR Δ ***** ↵

Description

address$_{EPROM}$	:	EPROM address
address$_{code}$	:	0~7DF (MSM64162 mode) 0~FDF (MSM64164 mode)
*****	:	transferred entire address range

The **TPR** command reads EPROM contents in the specified range and transfers them to the specified code memory area.

Each *address*$_{code}$ represents a code memory address. It is a value 0H to 7DFH in MSM64162 mode or 0H to FDFH in MSM64164 mode.(☞ 1) The *address*$_{code}$, *address*$_{code}$ specifies the range of code memory to be transferred.

The *address*$_{EPROM}$ is the starting address in EPROM to be read. If this address is omitted, then reading will start from EPROM address 0. If an '*****' is input, then the entire area of the EPROM from address 0 will be transferred to code memory. (☞ 2).

Input continues until a carriage return is entered. Then the following message will be output.

```
EPROM TYPE ---> type
START READING [Y/N] ---> _
```

Here *type* indicates the currently set EPROM type. If the EPROM type displayed is the same as the EPROM type that the user wants to read, then enter "Y↵" at the underscore. If they are different, then input "N↵" and set the EPROM type again with the **TYPE** command.

When "Y↵" is input at the underscore, the EASE64162/164 "RUN" indicator will light, and the data transfer will start. If the data transfer completes normally, then the "RUN" indicator will go off, the TPR command will terminate, and the emulator will wait for another command input.

☞ **1** The valid address range for each EPROM type is shown below.

EPROM Type	address range
2764	0 ~ 1FFF
27128	0 ~ 3FFF
27256	0 ~ 7FFF
27512	0 ~ FFFF

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TPR

The range of code memory transferred from EPROM when '*****' is input changes with the mode. When in MSM64162 mode, it is 0H to 7DFH. When in MSM64164 mode, it is 0H to FDFH.

Execution Example

```
* TPR 0,2FF,0
  EPROM TYPE ---> 27512
  START READING [Y/N] --->Y

* TPR *
  EPROM TYPE ---> 27512
  START READING [Y/N] --->Y
```

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3.3.4.9.4 Comparing EPROM with Code Memory

VPR

Input Format

VPR Δ *address*$_{code}$, *address*$_{code}$ [, *address*$_{EPROM}$] ↵

or

VPR Δ ***** ↵

Description

address$_{code}$	:	0~7DF (MSM64162 mode) 0~FDF (MSM64164 mode)
*****	:	compared entire address range
address$_{EPROM}$	:	EPROM comparison start address

The **VPR** command compares the contents of the specified range of code memory with the contents of the EPROM starting at the specified address, and displays any differences on the console.

Each *address*$_{code}$ is a code memory address 0H to 7DFH when in MSM64162 mode, or 0H to FDFH when in MSM64164 mode. The *address*$_{code}$, *address*$_{code}$ specifies the range of code memory to be compared. If an '*****' is input, then a range of code memory that corresponds to the EXPAND mode will be set (☞ 1).

The *address*$_{EPROM}$ is the EPROM's starting address for comparison. If this address is omitted, then comparison will start from EPROM address 0.

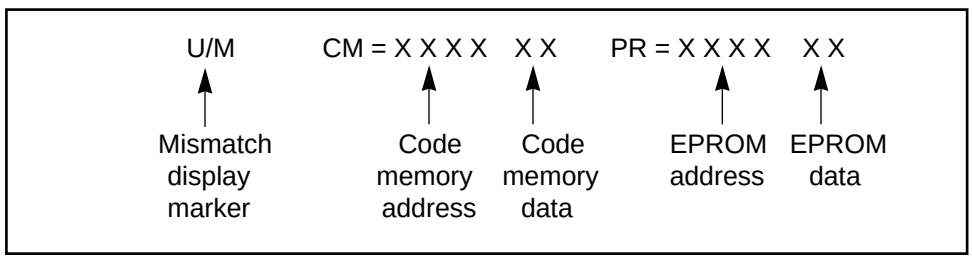
Input continues until a carriage return is entered. Then the following message will be output.

EPROM TYPE ---> *type*
START READING [Y/N] ---> _

Here *type* indicates the currently set EPROM type. If the EPROM type displayed is the same as the EPROM type that the user wants to compare, then enter "Y↵" at the underscore. If they are different, then input "N↵" and set the EPROM type again with the **TYPE** command.

When "Y↵" is input at the underscore, the EASE64162/164 "RUN" indicator will light, and the data comparison will start. If the data comparison completes normally, then the "RUN" indicator will go off, the **VPR** command will terminate, and the emulator will wait for another command input.

When compare errors are encountered, they will be displayed on the console in the following format.



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VPR

The range of code memory compared with EPROM when '*****' is input changes with the mode. When in MSM64162 mode, it is 0H to 7DFH. When in MSM64164 mode, it is 0H to FDFH.

Execution Example

```
* TPR *
  EPROM TYPE ---> 27512
  START READING [Y/N] --->Y

* CCM 100
  LOC=0100  E4 OLD  ---> 23 NEW
  LOC=0101  E4 OLD  ---> 65 NEW
  LOC=0102  E4 OLD  --->

* VPR 0,FDF,0
  EPROM TYPE ---> 27512
  START READING [Y/N] --->Y


   U/M    CM = 0100 23   PR = 0100 E4
   U/M    CM = 0101 65   PR = 0101 E4
```


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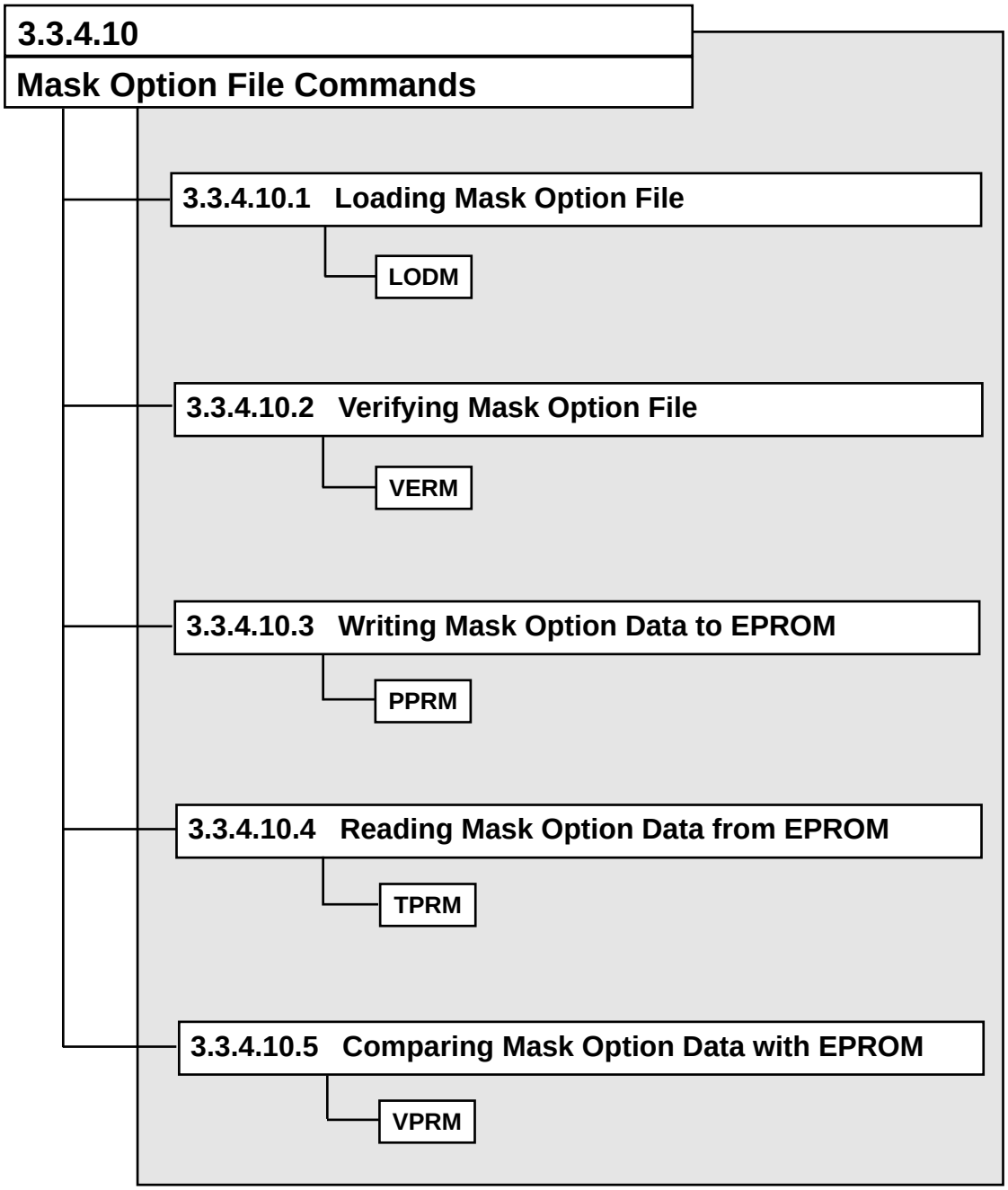
3.3.4.10
Mask Option File Commands
3.3.4.10.1 Loading Mask Option File
LODM
3.3.4.10.2 Verifying Mask Option File
VERM
3.3.4.10.3 Writing Mask Option Data to EPROM
PPRM
3.3.4.10.4 Reading Mask Option Data from EPROM
TPRM
3.3.4.10.5 Comparing Mask Option Data with EPROM
VPRM

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LODM

3.3.4.10.1 Loading Mask Option File

LODM

Input Format

LODM Δ *fname* ↵

fname : [*Pathname*] *filename* [*Extension*]

Description

The **LODM** command loads the contents of a mask option file output by MASK162 or MASK164 into the system controller's system memory. A mask option file is an Intel HEX format file generated by MASK162 or MASK164. (☞ 1)

If the file extension is omitted, then "HEX" (Intel HEX format file) will be the default.

The input file name can have a path specification. If the path is omitted, then the file in the current directory will be loaded. If the extension is omitted, then the file with the default extension appended will be loaded.

☞ 1

- Refer to the MASK162 User's Manual or MASK164 User's Manual for details about mask option files.
- If a program is executed when no mask option file has been loaded into system memory, then LCD driver display will not be performed correctly.

! If mask option data for 1/2 duty is loaded, then a warning message (Warning 1) will be displayed after the load completes. The EASE64162/164 emulator cannot output a 1/2-bias waveform when 1/2 duty is specified. For details, refer to Chapter 4, "Debugging Notes".

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3.3.4.10.2 Verifying Mask Option File

VERM

Input Format

VERM Δ *fname* ↵

fname : [*Pathname*] *filename* [*Extension*]

Description

The **VERM** command compares the contents of the specified mask option file with mask option data stored the system controller's system memory. If a mismatch in contents is found, then the address of the mismatch and the contents of both the mask option file and system memory will be displayed as follows.

LOC =	xxxx	DISK [xx]	SM [xx]
	↑	↑	↑
	Address	Contents of mask option file	Contents of system memory

The input file name can have a path specification. If the path is omitted, then the file in the current directory will be compared.

If the extension is omitted, then the file with the default extension (HEX) appended will be compared.

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LODM, VERM

Execution Example

```
* LODM M164_000

   FILE OPENEND NORMALLY.   FILE TYPE : INTELLEC HEX
  ***** LOAD COMPLETED *****

* VERM M164_000

  ***** VERIFY COMPLETED *****
```


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3.3.4.10.3 Writing Mask Option Data to EPROM

PPRM

Input Format

PPRM ↵

Description

The **PPRM** command writes an EPROM with the mask option data in the system controller's system memory. The EPROM address range to be written is always from 0H to BFFH.

When the carriage return is entered after the above input format, the emulator will output the following message.

EPROM TYPE ---> *type*
START PROGRAMMING [Y/N] ---> _

Here *type* indicates the currently set EPROM type. If the EPROM type displayed is the same as the EPROM type that the user wants to write, then enter "Y↵" at the underscore. If they are different, then input "N↵" and set the EPROM type again with the TYPE command.

When "Y↵" is input at the underscore, the EASE64162/164 "RUN" indicator will light, and the data write will start. If the data write completes normally, then the "RUN" indicator light will go off, the PPRM command will terminate, and the emulator will wait for another command input.

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TPRM

3.3.4.10.4 Reading Mask Option Data from EPROM

TPRM

Input Format

TPRM ↵

Description

The **TPRM** command transfers mask option data on an EPROM into the system controller's system memory. The EPROM address range to be transferred is always from 0H to BFFH.

When the carriage return is entered after the above input format, the emulator will output the following message.

EPROM TYPE ---> *type*
START READING [Y/N] ---> _

Here *type* indicates the currently set EPROM type. If the EPROM type displayed is the same as the EPROM type that the user wants to write, then enter "Y↵" at the underscore. If they are different, then input "N↵" and set the EPROM type again with the TYPE command.

When "Y↵" is input at the underscore, the EASE64162/164 "RUN" indicator will light, and the data transfer will start. If the data transfer completes normally, then the "RUN" indicator light will go off, the TPRM command will terminate, and the emulator will wait for another command input.

If mask option data for 1/2 duty is transferred, then a warning message (Warning 1) will be displayed after the load completes. The EASE64162/164 emulator cannot output a 1/2-bias waveform when 1/2 duty is specified. For details, refer to Chapter 4, "Debugging Notes".

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3.4.10.5 Comparing Mask Option Data with EPROM

VPRM

Input Format

VPRM ↵

Description

The **VPRM** command compares an EPROM with the mask option data in the system controller's system memory. The EPROM address range to be compared is always from 0H to BFFH.

When the carriage return is entered after the above input format, the emulator will output the following message.

EPROM TYPE ---> *type*
START READING [Y/N] ---> _

Here *type* indicates the currently set EPROM type. If the EPROM type displayed is the same as the EPROM type that the user wants to write, then enter "Y↵" at the underscore. If they are different, then input "N↵" and set the EPROM type again with the TYPE command.

When "Y↵" is input at the underscore, the EASE64162/164 "RUN" indicator will light, and the data comparison will start. If the data comparison completes normally, then the "RUN" indicator light will go off, the VPRM command will terminate, and the emulator will wait for another command input.

If a comparison error is found, then the emulator will display the following on the console.

U/M	PR =	xxxx	xx	SM	xx
↑		↑	↑		↑
Mismatch display marker		EPROM address	EPROM data		System memory data

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PPRM, TPRM, VPRM

Execution Example

```
* LODM M164_000

   FILE OPENED NOMALLY.   FILE TYPE : INTELLEC HEX
  ***** LOAD COMPLETED *****

* PPRM
  EPROM TYPE ---> 27512
   START PROGRAMMING [Y/N] --->Y

* VPRM
  EPROM TYPE --->27512
  START READING [Y/N] --->Y

*TPRM
  EPROM TYPE --->27512
  START READING [Y/N] --->Y
```


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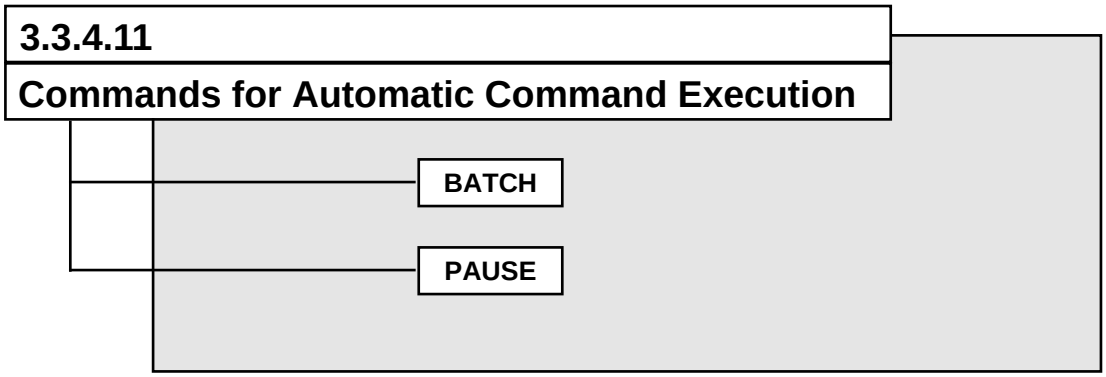
3.3.4.11 Commands for Automatic Command Execution



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BATCH

BATCH

Input Format

BATCH Δ *fname* ↵

fname : [*Pathname*] *filename* [*Extension*]

Description

The **BATCH** command automatically executes the contents of the specified *fname* as emulator commands.

The input file name can have a path specification. If the path is omitted, then the file will be taken in the current directory.

If the file extension is omitted, then a default extension (CMD) will be appended. To specify a file without an extension, append a period '.' after the filename.

In addition to emulator commands, the batch file can also contain assembler mnemonics input within the **ASM** command.

Automatic execution is performed until the end of the file.

Only one batch file can be open. Therefore, even if a **BATCH** command is included within a batch file, it will be ignored.

Execution Example

```
* BATCH E4
       Batchfile: E4 opened

* DTR 0,30

            0 1 2 3 4 5 6 7 8 9 A B C D E F
  LOC=0000  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
  LOC=0010  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
  LOC=0020  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
  LOC=0030  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

* DTO
  TRACE OBJECT ---> BCF,BSR0,BEF,BSR1

* DCC
  CYCLE COUNTER STATUS : 0000000000

* TYPE
  EPROM TYPE --->27512

*
*       Batchfile: E4 closed
```

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PAUSE

Input Format

PAUSE ↵

Description

The **PAUSE** command waits for keyboard input when executed. By placing a **PAUSE** command in a batch file, automatic command execution can be temporarily suspended. The input wait state will be released upon input from the keyboard, or if the emulator reset switch is pressed.

Execution Example

```
* PAUSE

* PAUSE
 Low-Power series Emulator << EASE64162/164 >> Ver 2.24
```


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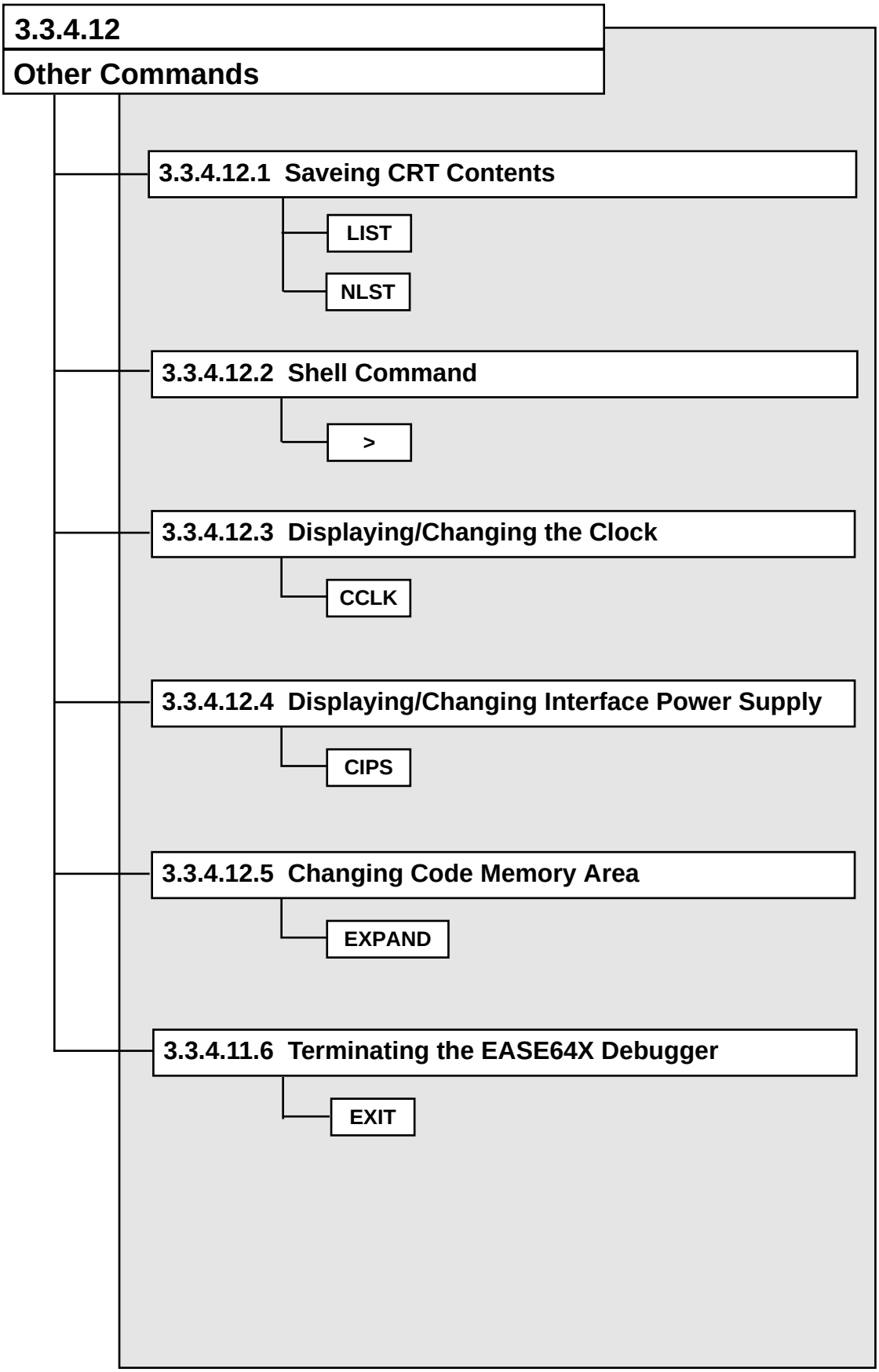

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3.3.4.12.1 Saving CRT Contents

LIST

Input Format

LIST Δ *fname* ↵

fname : [*Pathname*] *filename* [*Extension*]

Description

The **LIST** command stores the contents displayed to the console in the specified file.

The input file name can have a path specification. If the path is omitted, then the file will be created in the current directory. If a file of the same name exists in the specified directory, then that file will be deleted and a new file will be created.

If the file extension is omitted, then a default extension (LST) will be appended.

While a file is being created by a **LIST** command, another **LIST** command cannot be used (only one list file can be opened).

The LIST command becomes valid immediately after it has been input. When any of the following occurs, the **LIST** command becomes invalid and the list file is closed.

- An NLST command is input.
- The EASE64X debugger terminates.
- The EASE64162/164 base unit's reset switch is pressed.

Execution Example

```
* LIST SAMP1
      Listfile: FILENAME.LST opened

* DTR 0, 30
            0 1 2 3 4 5 6 7 8 9 A B C D E F
  LOC=0000  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
  LOC=0010  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
  LOC=0020  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
  LOC=0030  1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
```


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NLST

NLST

Input Format

NLST ↵

Description

The **NLST** command terminates a previous **LIST** command. It will close the list file opened by the **LIST** command.

Contents are stored in the list file until the **NLST** command.

Execution Example

```
* NLST
        Listfile: SAMP1.LST closed
```

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3.3.4.12.2 Shell Command

>

Input Format

>DOS *command* ↵

Description

The shell function invokes the MS-DOS command processor COMMAND.COM as a child process of the EASE64X debugger. The string input after this command will be passed to COMMAND.COM and executed.

After the MS-DOS command terminates, the EASE64X debugger will again wait for a command to be input.

In order to realize the shell function, the free area of the system being used must have sufficient space for invoked programs. The resident portion of EASE64X.EXE consumes about 90K bytes. Thus, for a program to be invoked after the shell command has been executed, it must have fewer bytes than the original free area less the size of the newly loaded COMMAND.COM.

Execution Example

```
* >COPY A:SAMP1. LST B:
```


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CCLK

3.3.4.12.3 Displaying/Changing the Clock

CCLK

Input Format

CCLK [Δ *mnemonic*] ↵
mnemonic : HIN, HOUT, LIN, LOUT

Description

The **CCLK** command switches the clock supplied to the evaluation board. One of the following is entered for mnemonic.

HIN : High-speed clock on CROSC board.
HOUT : High-speed clock from user cable OSC1 pin.
LIN : Low-speed clock on crystal board.
LOUT : Low-speed clock from user cable XT pin.

The EASE64162/164 clock will be set to internal clocks (HIN, LIN) when power is turned on (☞ 1).

If mnemonic is omitted, then the current setting will be displayed.

☞ 1 Refer to Section 3.2.1, "Setting Operating Frequency," regarding the crystal board, CROSC board, and their peripheral circuits.

! The high-speed clock function does not exist in the MSM64162D chip. Please keep this in mind when evaluating the MSM64162 with EASE64162/164.

Execution Example

```
* CCLK
  HIGH CLOCK --->  IN
  LOW  CLOCK --->  IN

* CCLK HOUT

* CCLK
  HIGH CLOCK --->  OUT
  LOW  CLOCK --->  IN

* CCLK LOUT

* CCLK
  HIGH CLOCK --->  OUT
  LOW  CLOCK --->  OUT
```

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3.3.4.12.4 Displaying/Changing Interface Power Supply

CIPS

Input Format

CIPS [Δ *mnemonic*] ↵

Description

The **CIPS** command changes the interface power supply of the user connector. The mnemonic is one of the following.

INT : Supply the user connector interface power supply from the emulator's internal power supply (5V) (☞ 1).

EXT : Supply the user connector interface power supply from the user connector VDD pin (☞ 2).

When the emulator is turned on, the EASE64162/164 user connector interface power supply will be supplied from the emulator's internal power supply (5V).

If mnemonic is omitted, then the current setting will be displayed.

☞ **1** The EASE64162/164 "PORT5V" indicator will light up, and the "PORT3V" indicator will go off.

☞ **2** Supply a voltage from 3V to 5V to the user connector VDD pin. The EASE64162/164 "PORT3V" indicator will light up, and the "PORT5V" indicator will go off.

Execution Example

```
* CIPS
   INTERFACE POWER SUPPLY --->  INTERNAL

* CIPS EXT
* CIPS
   INTERFACE POWER SUPPLY --->  EXTERNAL
```


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EXPAND

3.3.4.12.5 Changing Code Memory Area

EXPAND

Input Format

EXPAND [Δ *mnemonic*] ↵

Description

The **EXPAND** command switches the EASE64162/164 code memory area.

The mnemonic is one of the following.

ON : Make code memory area 8192 bytes(☞ 1).
OFF : Make code memory area 2016 bytes or 4064 bytes.

When power is turned on, the EASE64162/164 code memory area will be set to 4064 bytes (MSM64164 mode).

If mnemonic is omitted, then the current setting will be displayed.

☞ **1** When the code memory area is changed to 8192 bytes, code memory addresses will be expanded to 0H~1FFFH, and command parameter input values will be changed as shown in Table 3-4.

☞ **2** The setting will be 2016 bytes in MSM64162 mode and 4064 bytes in MSM64164 mode.

Execution Example

```
* EXPAND
  CODE MEMORY AREA :  4Kbyte

* EXPAND ON

* EXPAND
  CODE MEMORY AREA :  8Kbyte
```

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Table 3-4. Command Parameter Changes

Command	Parameter
CPC [Δ *data*] ↵	*data* : 0H to 1FFFH
DCM Δ *address* [, *address*] ↵	*address* : 0H to 1FFFH
CCM Δ *address* ↵	*address* : 0H to 1FFFH
FCM Δ *address* , *address* [, *data*] ↵	*address* : 0H to 1FFFH
SAV Δ *fname* [Δ *address* , *address*] ↵	*address* : 0H to 1FFFH
VER Δ *fname* [Δ *address* , *address*] ↵	*address* : 0H to 1FFFH
ASM Δ *address* ↵	*address* : 0H to 1FFFH
DASM Δ *address* [, *address*] ↵	*address* : 0H to 1FFFH
STP [Δ *number*] [, *address*] ↵	*address* : 0H to 1FFFH
G [Δ *address*] [, *parm*] ↵	*address* : 0H to 1FFFH
DBP Δ *address* [, *address*] ↵	*address* : 0H to 1FFFH
EBP Δ *address* [, *address . . .* , *address*] ↵	*address* : 0H to 1FFFH
FBP Δ *address* [*address* [, *data*]] ↵	*address* : 0H to 1FFFH
DTR Δ *address* [, *address*] ↵	*address* : 0H to 1FFFH
ETR Δ *address* [, *address . . .* , *address*] ↵	*address* : 0H to 1FFFH
FTR Δ *address* [Δ *address* [, *data*]] ↵	*address* : 0H to 1FFFH
DIE Δ *address* [, *address*] ↵	*address* : 0H to 1FFFH
PPR Δ $address_{code}$, $address_{code}$ [, $address_{EPROM}$] ↵	$address_{code}$: 0H to 1FFFH
TPR Δ $address_{code}$, $address_{code}$ [, $address_{EPROM}$] ↵	$address_{code}$: 0H to 1FFFH
VPR Δ $address_{code}$, $address_{code}$ [, $address_{EPROM}$] ↵	$address_{code}$: 0H to 1FFFH
STT ↵ START ADDRESS: *old-address OLD* ---> *address* ↵ STOP ADDRESS: *old-address OLD* ---> *address* ↵	*address* : 0H to 1FFFH
SCT ↵ START ADDRESS: *old-address OLD* ---> *address*↵ STOP ADDRESS: *old-address OLD* ---> *address*↵	*address* : 0H to 1FFFH

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EXIT

3.3.4.12.6 Terminating the EASE64X Debugger

EXIT

Input Format

EXIT ↵

Description

The **EXIT** command terminates the EASE64X debugger.

If a list file has been opened by the **LIST** command, then it will be closed before the debugger terminates.

Execution Example

```
* EXIT
A>
```

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Chapter 4

Debugging Notes

This chapter provides some notes about debugging with the EASE64162/164 system.

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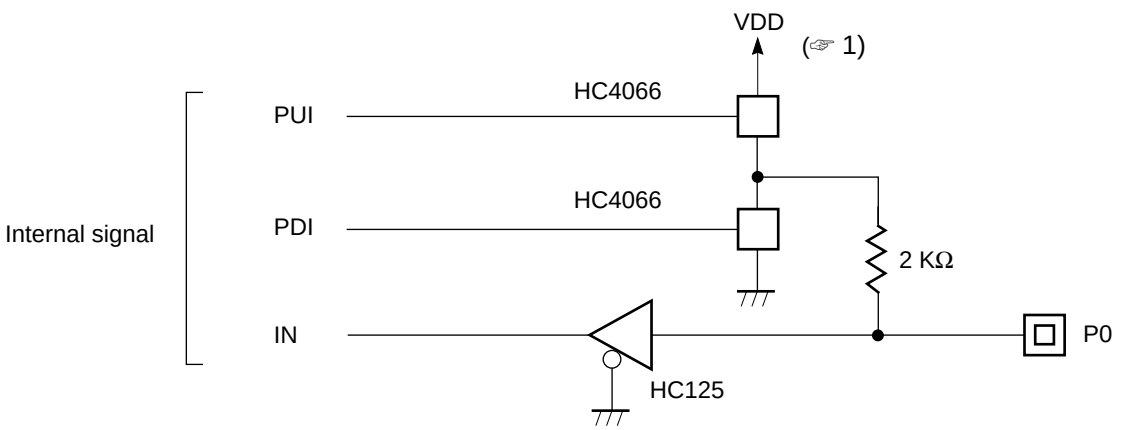
4.1. Debugging Notes

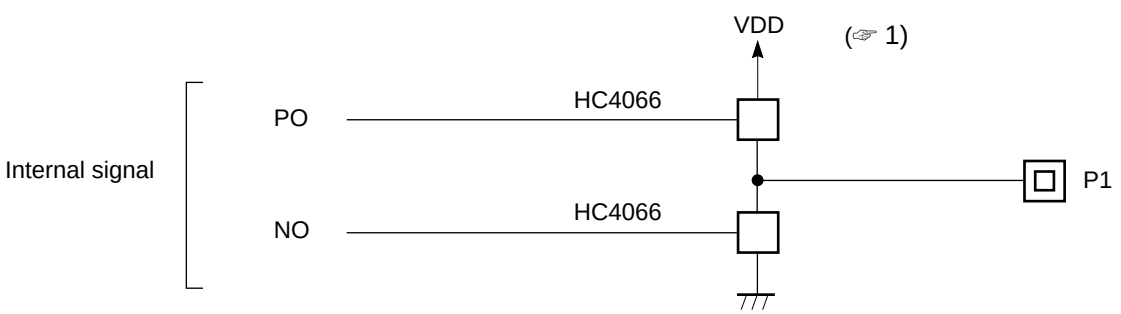
4.1.1. Ports

The input/output of the port pins, BD pin, and $\overline{\text{RESET}}$ pin are as shown below. Their input/output characteristics differ from those of the MSM64162 and MSM64164.

(1) P0 (input port)



(2) P1 (output ports)



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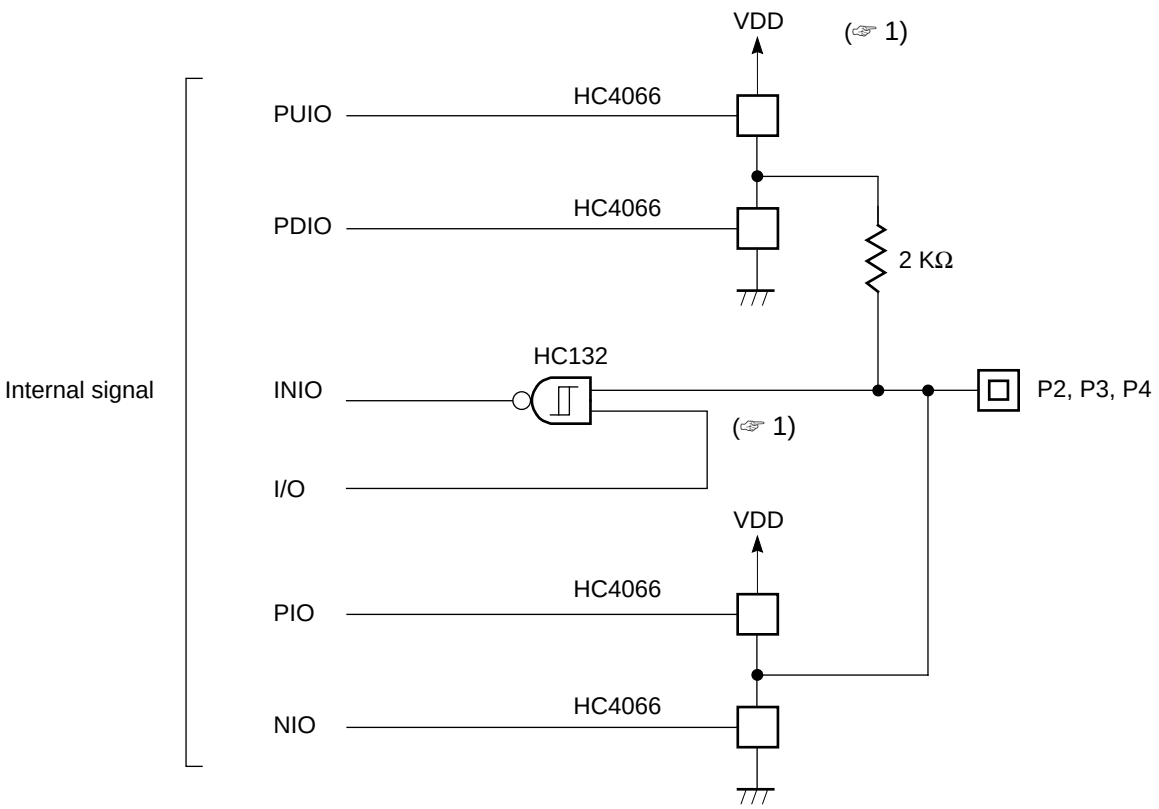
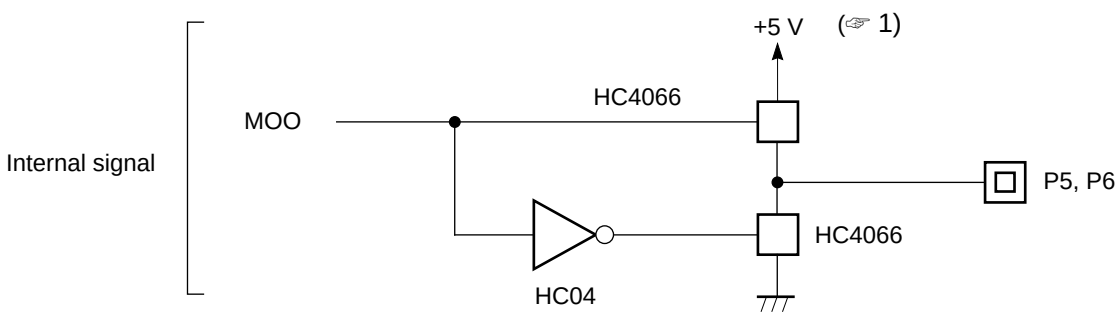
(3) P2, P3, P4 (input/output ports)



(4) P5, P6 (mask option output ports)



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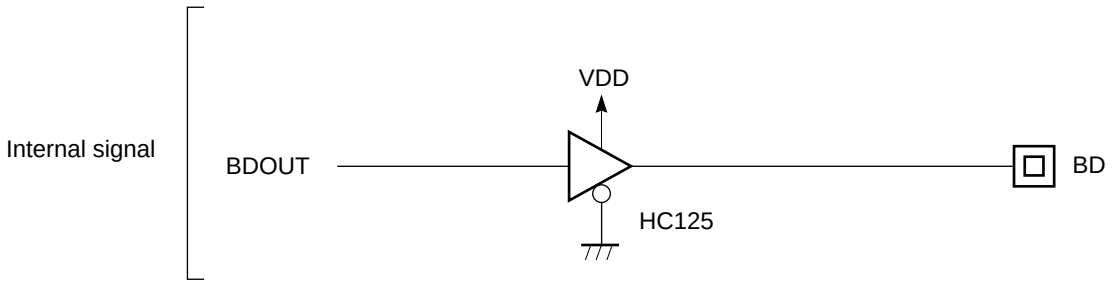
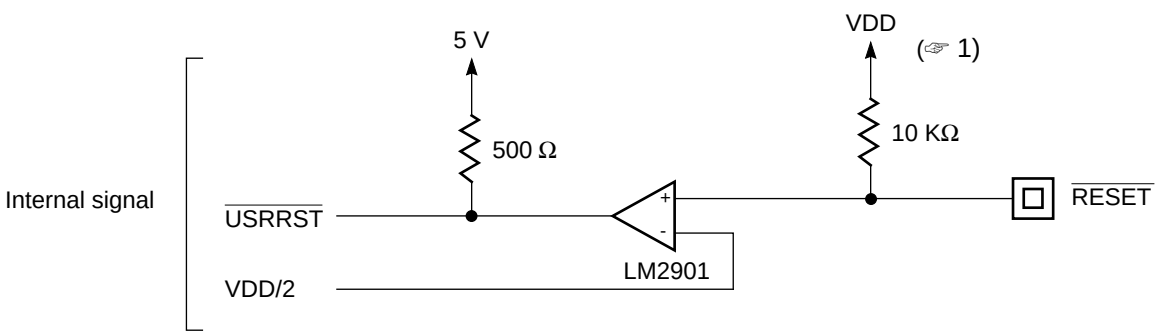
(5) BD (buzzer driver)



(6) $\overline{\text{RESET}}$ (reset input) (☞ 2)



☞ **1** From 3V to 5V is applied to VDD. The VDD supply is switched by the **CIPS** command: it will be the emulation kit internal 5V supply if **CIPS INT** is input, or it will be the VDD supply of user connector pins 36 and 37 if **CIPS EXT** is input. A voltage 3V to 5V can be input to the VDD pin.

☞ **2** The $\overline{\text{RESET}}$ pin is effective when specified to be on by the **URST** command. If an “L” level is input on this pin during realtime emulation, then the evaluation board will reset.

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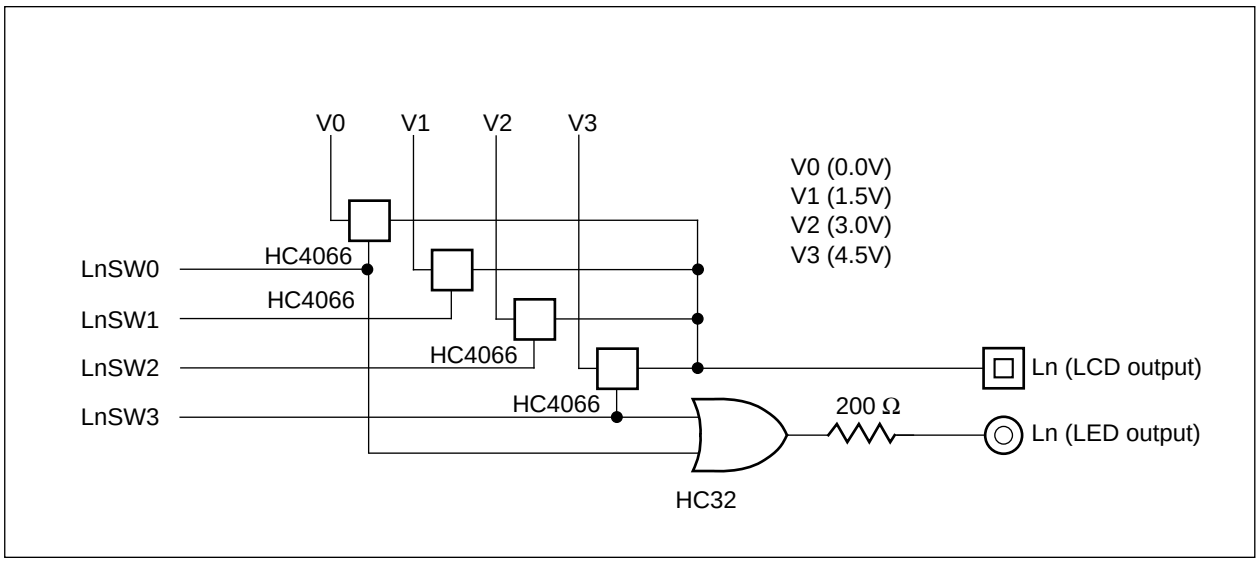
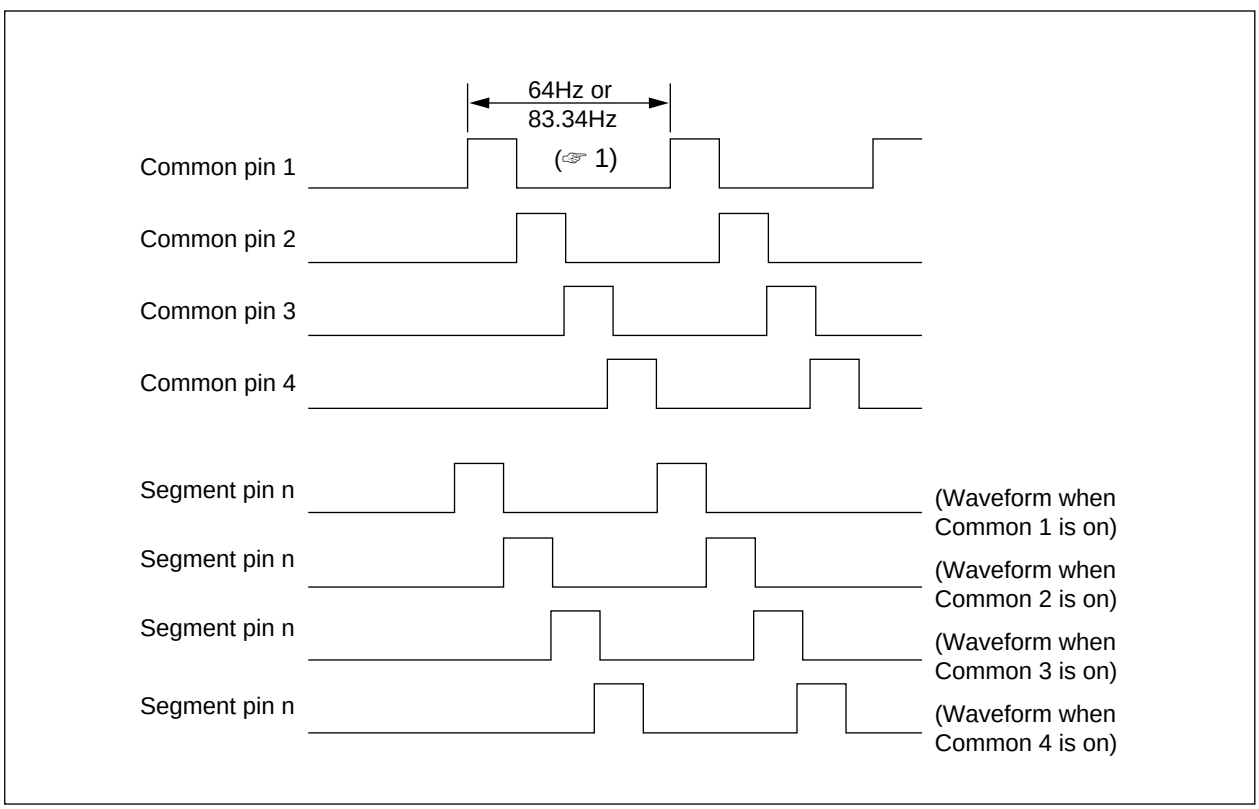
4.1.2. LCD Drivers

(1) Output Characteristics

The LCD driver outputs are configured as shown below. Their input/output characteristics differ from those of the MSM64162 and MSM64164.



The LED output above is used to implement LEDs (light emitting diodes) to evaluate the LCD portion. It outputs the following signals.



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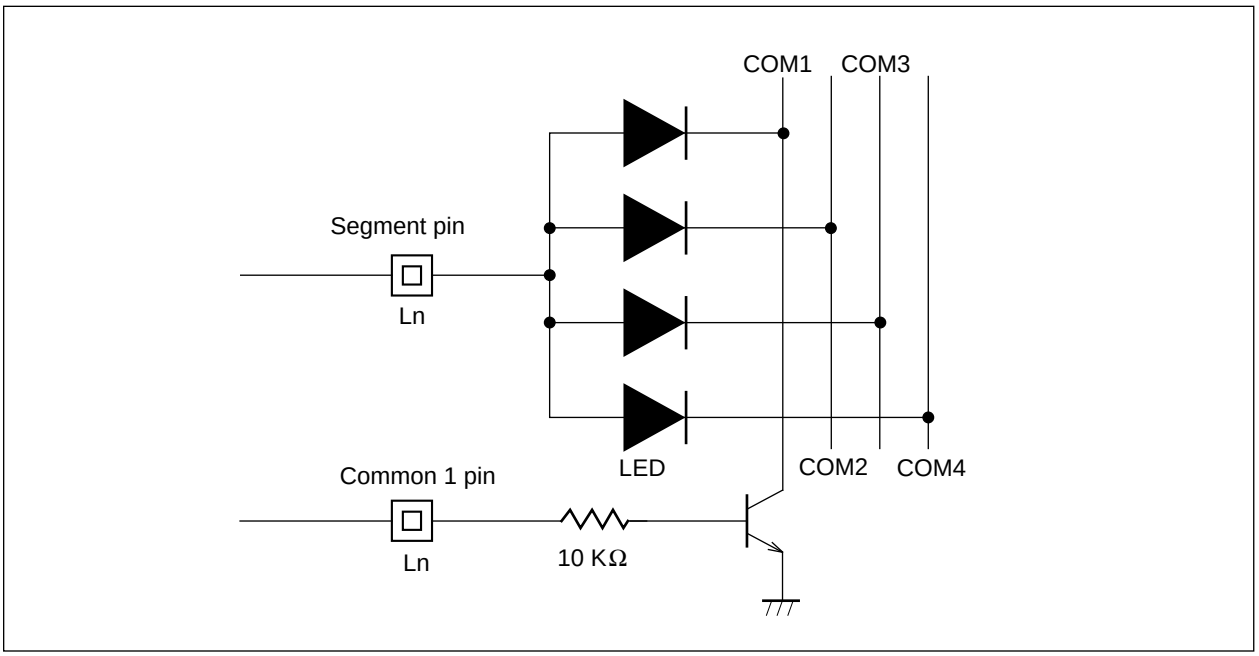
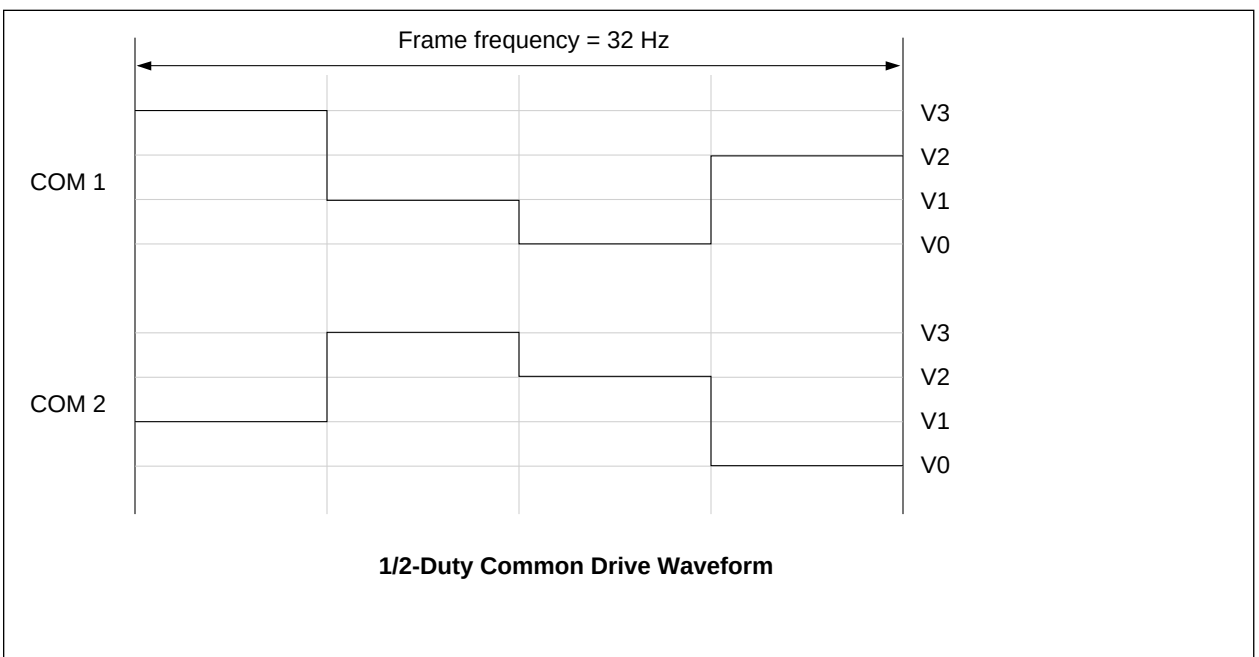
To evaluate the timing of an LED turning on, build a circuit like the following.



Connection Example For LED Timing Evaluation

If the current flowing through in one LED is assumed to be 1.25 mA with this circuit, then the collector current of the common pin transistor will be up to 37.5 mA (at 1/4 duty), so a transistor that can drive high current is necessary.

1 Frequency will be 64 Hz when 1/4 duty or 1/2 duty is selected, or 83.34 Hz when 1/3 duty is selected.



1/2-Duty Common Drive Waveform

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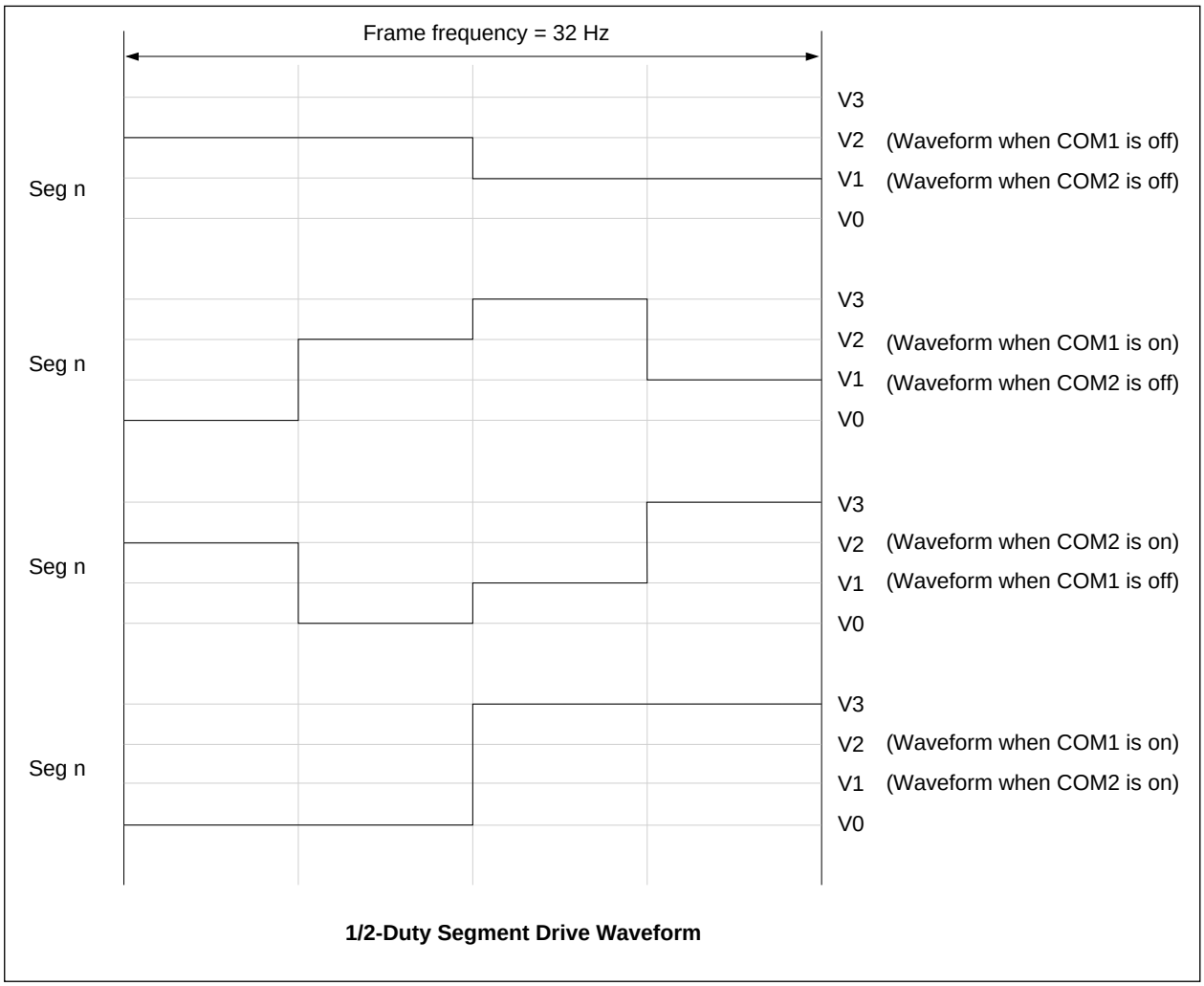

1/2-Duty Segment Drive Waveform

(2) Display registers for LCD drivers

In the MSM64162/MSM64164, the display registers and bits that are not specified as either segment or common ports by LCD driver mask option data (☞ 2) cannot be read or written. However, in the EASE64162/164 emulator, all bits of display registers can be read and written, regardless of mask option data.

Therefore, an application program that utilizes the unused display register bits as a RAM area will not work with the MSM64162/MSM64164. Also, the MSM64162/MSM64164 will always read these bits as 1, but the EASE64162/164 will read them as undefined (but 0 after reset).

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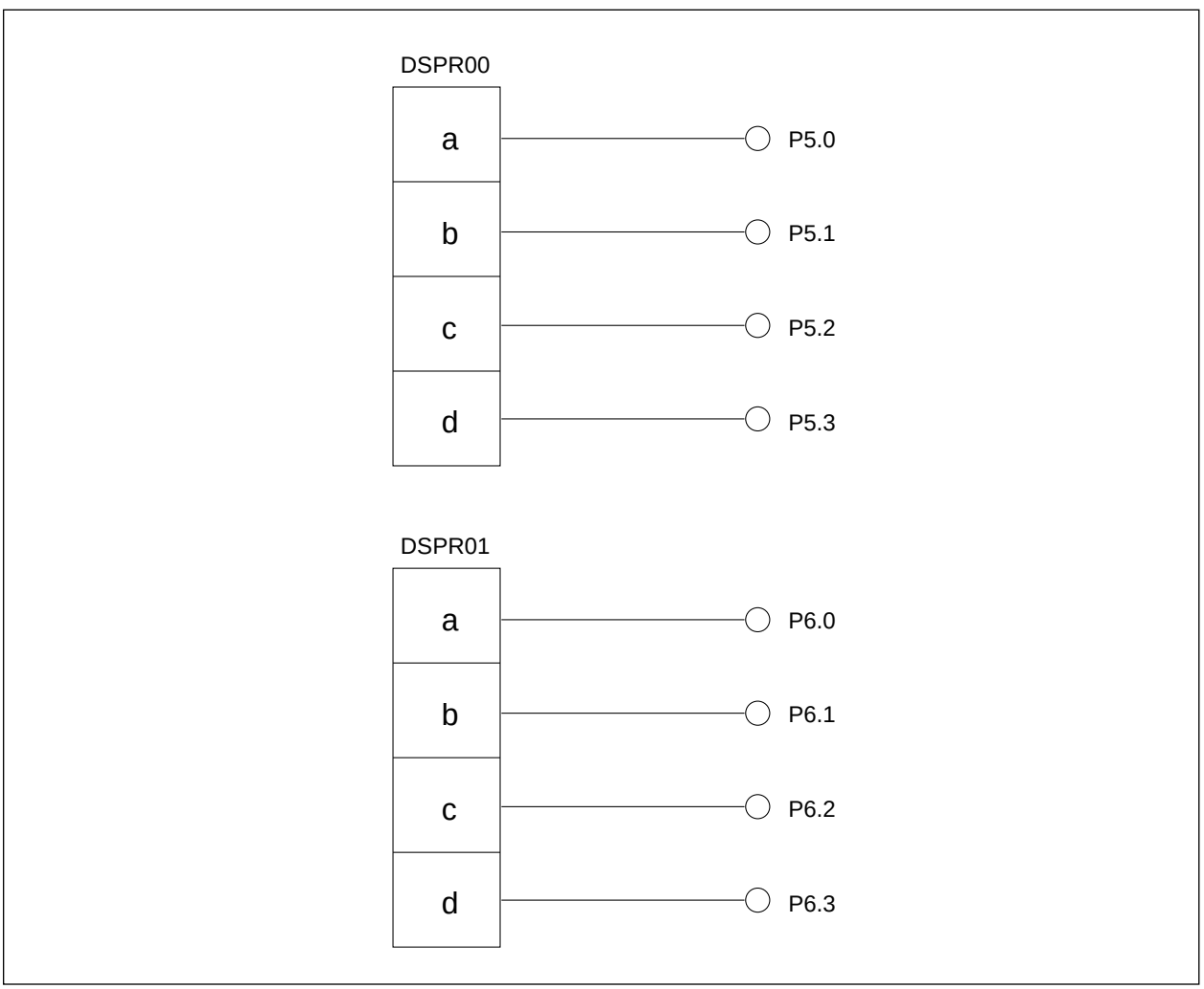
(3) Clearing display registers by user reset

The EASE64162/164 can initialize the evaluation board with a user reset (☞ 3), but the display registers for LCD drivers are not initialized by user resets.

(4) Output port selection by mask option

Eight pins of LCD driver outputs (L16~L23 for MSM64162, L26~L33 for MSM64164) can be set as output ports by mask option. In the MSM64162/MSM64164 these 8 pins can match up in any way with the 8 bits of Display Register 0 and Display Register 1 (DSPR00, DSPR01), but in the EASE64162/164 emulator the matching is fixed to output to the user connector as shown below.



☞ 2 Mask option data is created by the mask option generators MASK162 and MASK164.

☞ 3 A user reset initializes the evaluation board by the input of an "L" level on the user connector RESET pin during realtime emulation.

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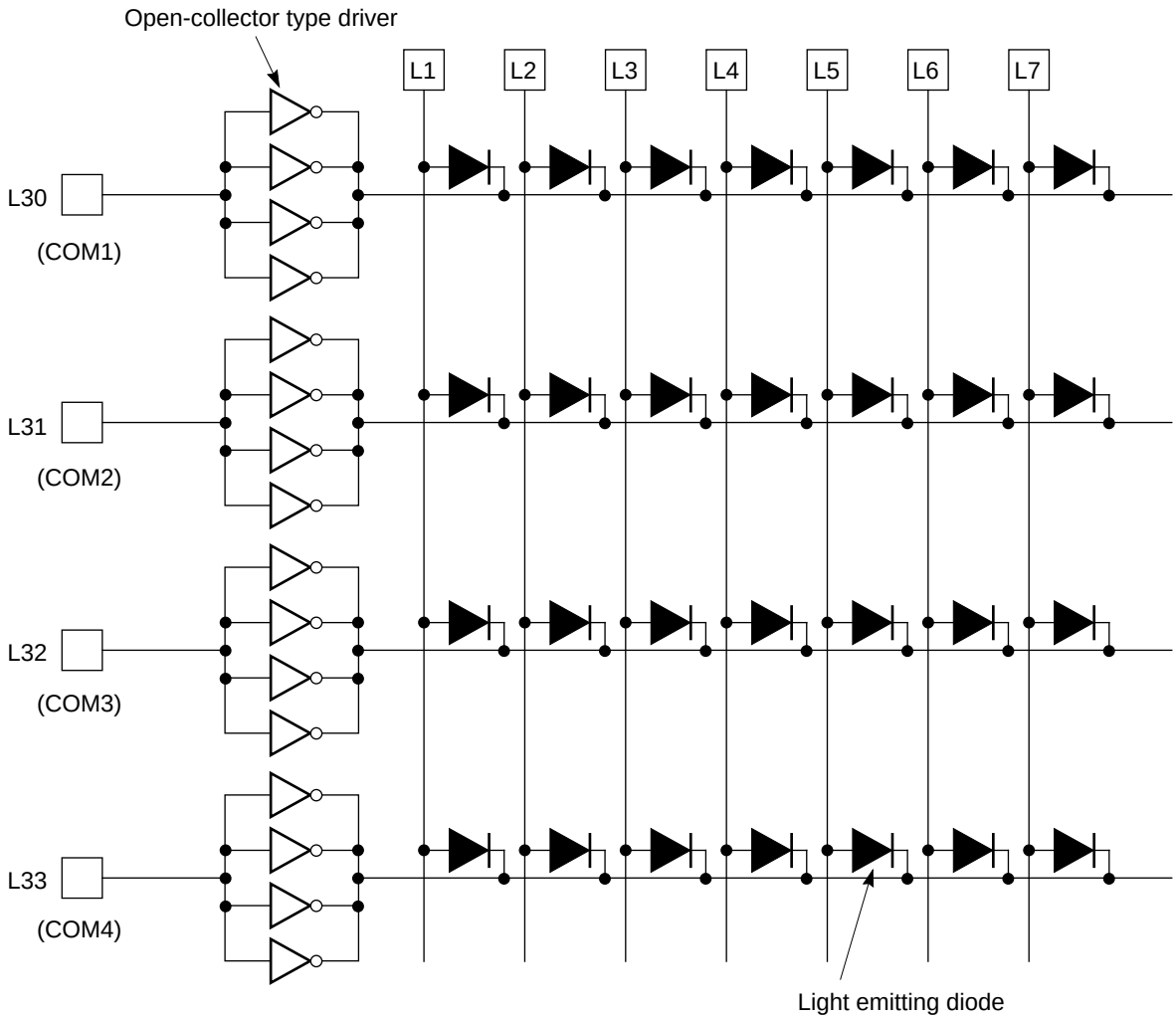

Circuit Example For LED Timing Evaluation

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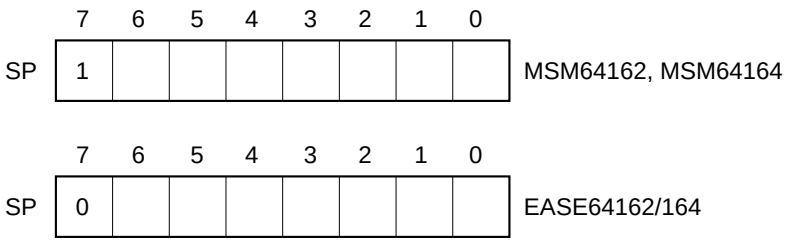
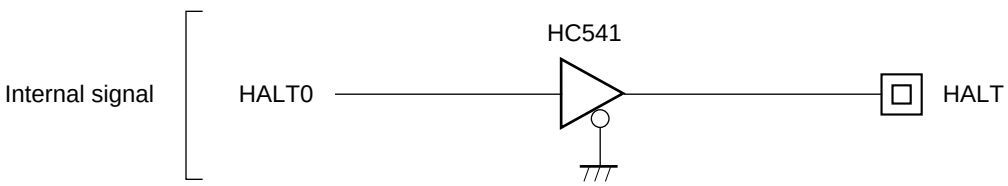
4.1.3. Stack Pointer

The most significant bit of the MSM64162 and MSM64164 stack pointer is always 1, but the most significant bit of the EASE64162/164 stack pointer is always 0.



4.1.4. HALT Pin

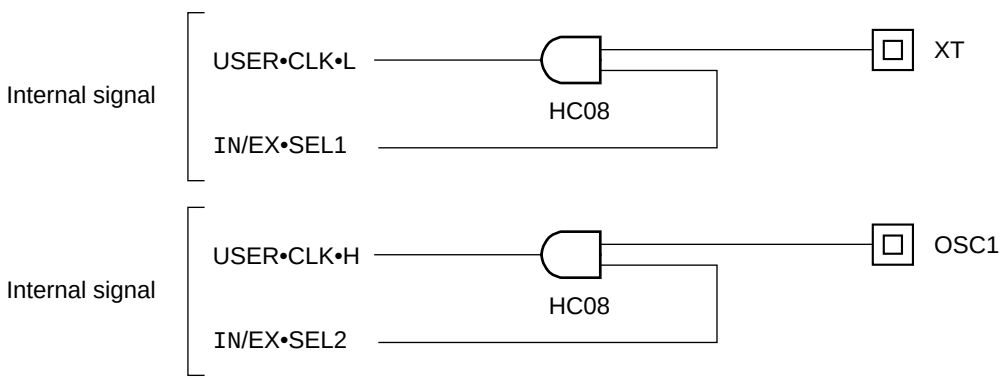
The user connector HALT pin is a monitoring pin that outputs an “H” level in halt mode. The peripheral circuitry of the HALT pin is shown below.



HALT Pin Peripheral Circuit

4.1.5. XT and OSC1 Pins

The user connector XT pin and OSC1 pin are used respectively for input of a low-speed and high-speed clock. The interface power supply voltage must be 5V. The peripheral circuitry of the XT pin and OSC1 pin is shown below.



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4.1.6 ADC POD

(1) Connecting to emulator base unite

Be sure that the emulator power supply is off when connecting the ADC POD to the emulator base unit. If the power supply is on, then even when the ADC POD is connected, A/D conversion will not be performed.
Also be sure that the serial number and version on the ADC POD voltage label (☞ 1) match those of the label on the back of the emulator base unit (☞ 2) before connecting them. If the serial numbers and versions are different, then A/D conversion might not be performed.

(2) CR oscillation clock

The CR oscillation clock for the ADC POD is supplied by the emulator's internal evaluation board, except when the SFR A/D conversion run/stop select bit (EADC) is 1. Therefore the evaluation board's internal counter B (CNTB0 ~ 3) will count regardless of whether emulation is executing or stopped.

☞ 1 Refer to section 3.2.3, "Connecting the MSM64162/164 ADC POD."

☞ 2 Refer to Appendix 1, "EASE64162/164 External Views."

4.1.7 DASM Command

The pairs of instructions shown below result in identical instruction codes. When the debugger's DASM command encounters one of these codes, it will display the mnemonic shown on the left.

NOP	and	AIS0	(both result in code 0H)
INA	and	AIS1	(both result in code 1H)
LAM	and	LAMM0	(both result in code 70H)
XAM	and	XAMM0	(both result in code 71H)

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4.1.8 Breaks

(1) If a break condition is fulfilled during a skip, then the break will be saved until after the skip operation completes. (operation is the same even with the STP command.) However, if a break address instruction is skipped at an address break or breakpoint break, then the break will not be saved, and no break will occur when the skip completes.

(2) If a break condition is fulfilled during an interrupt transfer cycle, then the break will occur after the interrupt transfer cycle completes. The break PC will be the interrupt vector address.

(3) The value of the time base counter when a break occurs in high-speed clock mode will not always be the same even under the same conditions because the high-speed clock and low-speed clock are asynchronous. Furthermore, when EASE64162/164 is operated with the high-speed clock, interrupt timing may differ between break (emulation) operation and step command execution.

(4) With the MSM64162/MSM64162D/MSM64164, the skip function of an AIS instruction will be disabled in a program where the AIS instruction is executed following either ADCS and ADCS@XY instructions, or SUBCS and SUBCS@XY instructions. With the EASE64162/164 emulator, however, if a break is set to occur immediately after execution of either ADCS and ADCS@XY instructions, or SUBCS and SUBCS@XY instructions, and execution is set to resume starting with the AIS instruction, then the skip function of the AIS instruction will not be disabled. Likewise, the skip function of the AIS instruction will not be disabled with a STP command.

4.1.9 MSM64162D

The MSM64162D, when evaluated with EASE64162/164, will be evaluated in MSM64162 mode, but be aware that you can still use functions that do not exist in the MSM64162D chip (high-speed clock, A/D converter CROSC oscillation mode, IN1 external clock input mode). If those functions are used when evaluating a MSM64162D, then chip operation will not be guaranteed.

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Appendix

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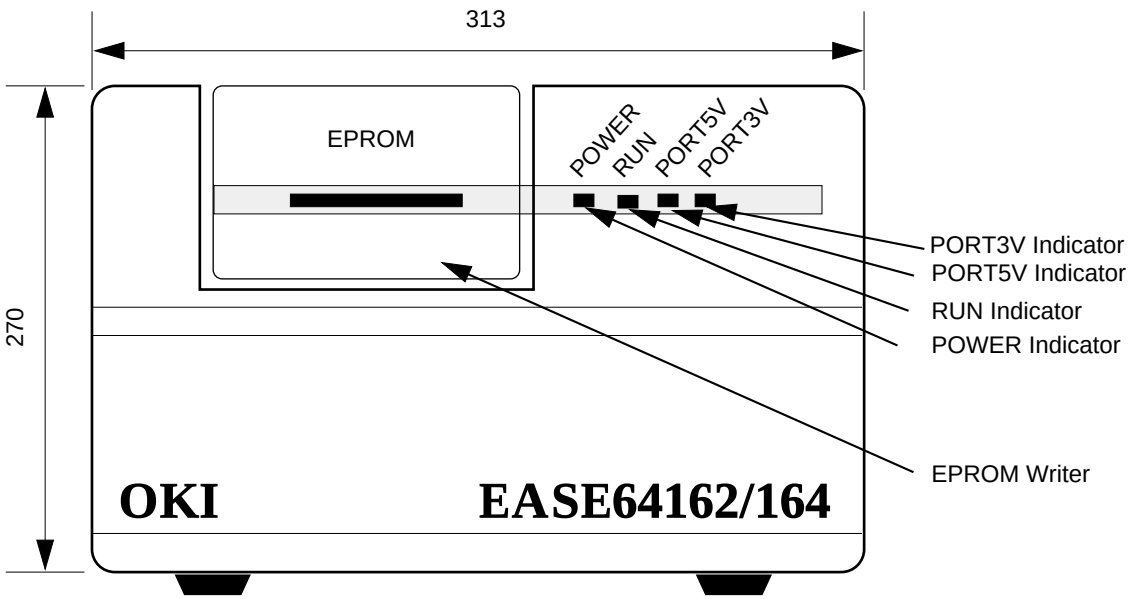
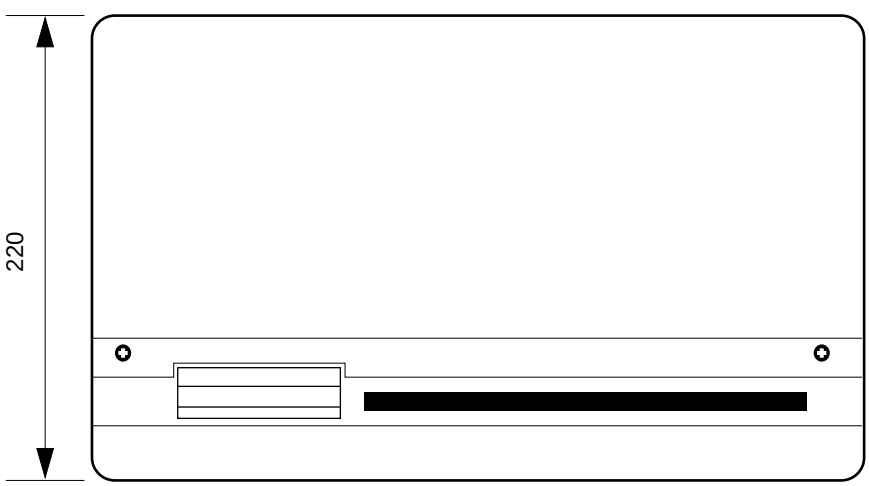
A.1. EASE64162/164 External Views



Front View



Top View

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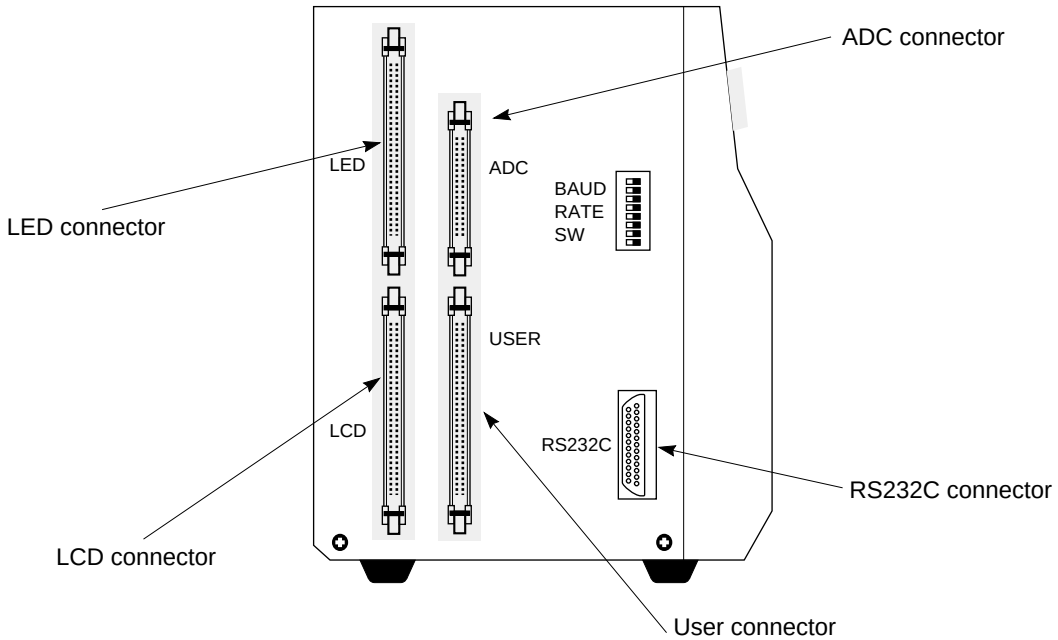
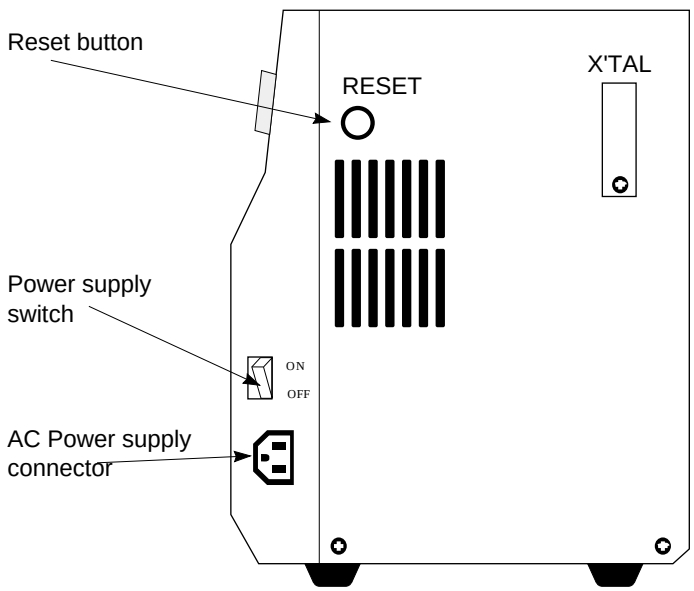


Left View



Right View

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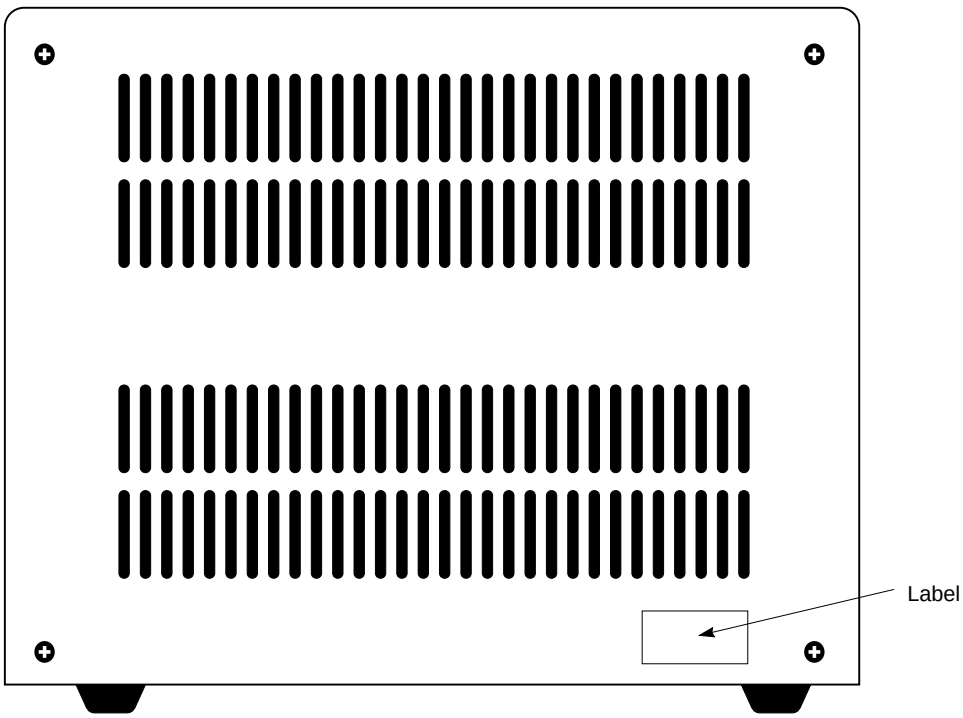

Rear View

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A.2. User Cable Configuration

Figure A-1 shows the configuration of the accessory user cables (two 40-pin cables). Table A-1 gives the connector part number for the user cable.

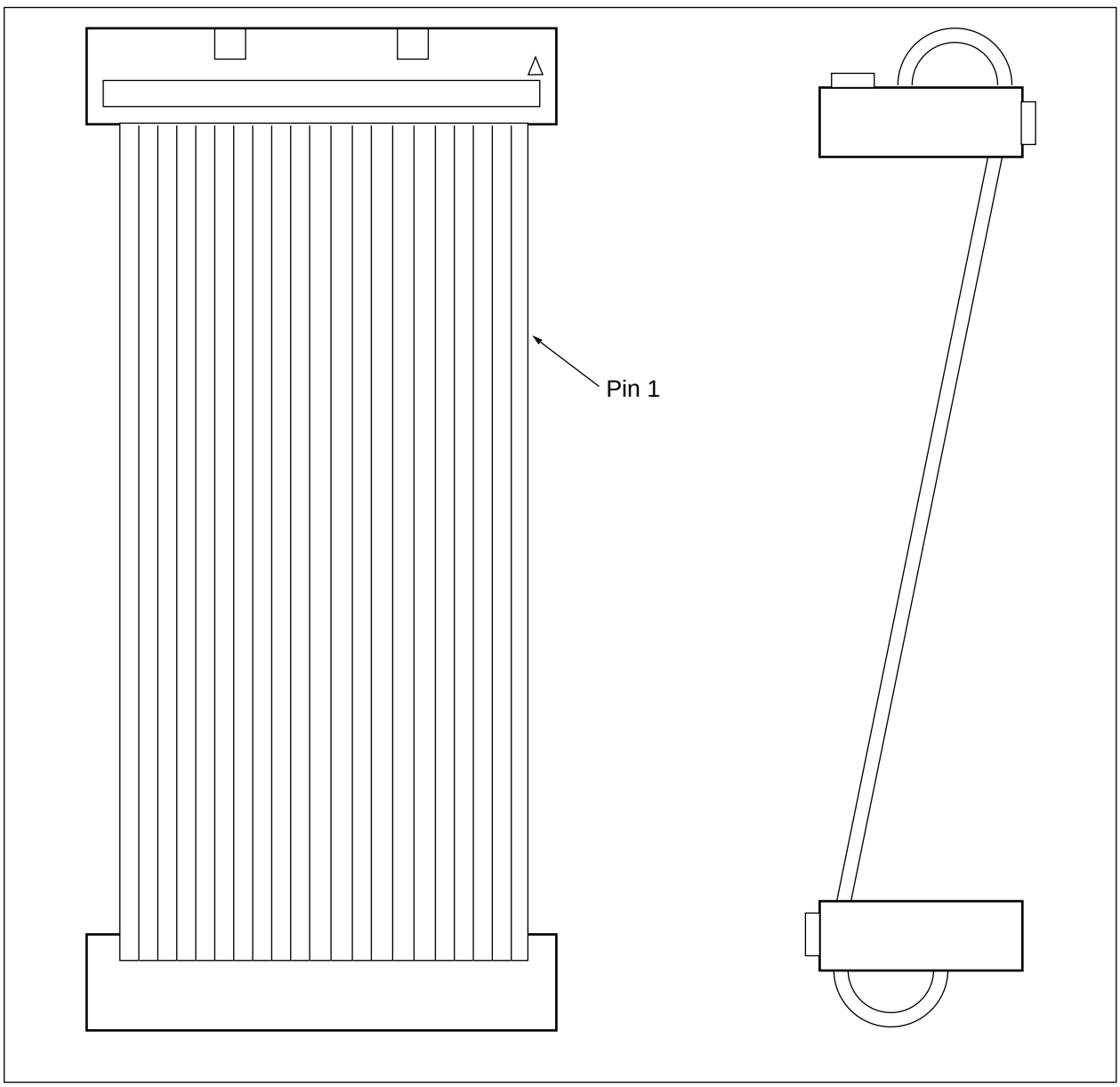

Figure A-1. User Cable Configuration

Table A-1. User Cable Connector Part Number Information

Cable	Maker	Connector Model
User Cable (40-pin)	Hirose Electric	HIF3BA-40D-2.54R

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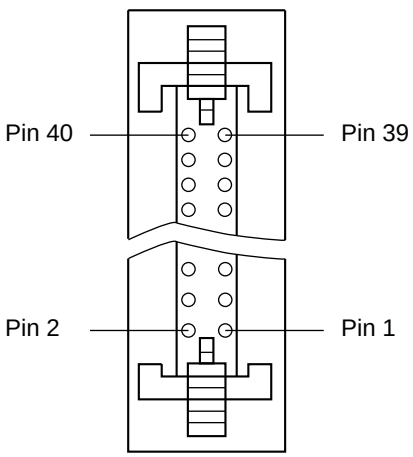
A.3. Pin Layout of User Connectors

(1) User Connectors



- As shown at left, the user connector is a 40-pin connector with pin 1 at lower right.
- The voltage level of the user connector interface power supply can be switched by the CIPS command to either an internal power supply voltage (5V) or an externa power supply voltage (3V~5V). However, the switching of the interface power supply has no relationship with the selection of the 1.5V or 3.0V versions of the MSM64162/164 ADC POD and CROSC board.
- The HALT pin is a monitoring pin that outputs an “H” level in halt mode.

  The P5.0~P5.3 pins and P6.0~P6.3 pins will be output pins when the LCD driver pins (L26~L33 or L16~L23) are set by mask option as output ports. They will output the contents of the display registers (DSPR00, DSPR01).

- When ON is specified by the URST command, the $\overline{\text{RESET}}$ pin becomes valid. When it is valid, an "L" level input during realtime emulation will reset the evaluation board.
- When LOUT is specified by the CCLK command, the XT pin becomes valid. When it is valid, the XT pin inputs a low-speed clock.
- When HOUT is specified by the CCLK command, the OSC1 pin becomes valid. When it is valid, the OSC1 pin inputs a high-speed clock.
- When the user connector interface power supply is set to be an external power supply by the CIPS command, supply a voltage from 3V to 5V on the VDD pin.

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User Connector Pin List

Pin Number	Signal Name	Pin Number	Signal Name
1	P2.0	21	BD
2	P2.1	22	P5.0 (DSPR00 a)
3	P2.2	23	P5.1 (DSPR00 b)
4	P2.3	24	P5.2 (DSPR00 c)
5	P3.0	25	P5.3 (DSPR00 d)
6	P3.1	26	P6.0 (DSPR01 a)
7	P3.2	27	P6.1 (DSPR01 b)
8	P3.3	28	P6.2 (DSPR01 c)
9	P4.0	29	P6.3 (DSPR01 d)
10	P4.1	30	—
11	P4.2	31	$\overline{\text{RESET}}$
12	P4.3	32	HALT
13	P0.0	33	XT
14	P0.1	34	OSC1
15	P0.2	35	—
16	P0.3	36	VDD
17	P1.0	37	VDD
18	P1.1	38	—
19	P1.2	39	GND
20	P1.3	40	GND

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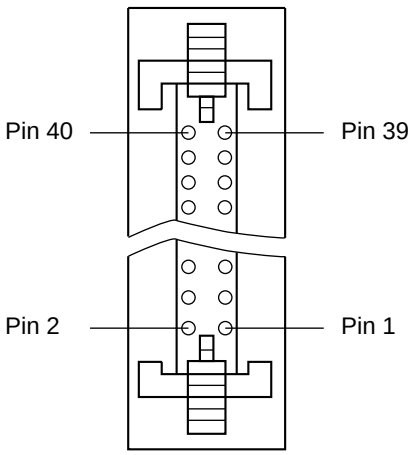
(2) LCD connector



- As shown at left, the LCD connector is a 40-pin connector with pin 1 at lower right.
- The LCD connector corresponds to the L0~L33 pins of the MSM64162 and MSM64164. It outputs LCD driver signals 0V to 4.5V.

LCD Connector Pin List

Pin Number	Signal Name	Pin Number	Signal Name
1	L0	21	L20
2	L1	22	L21
3	L2	23	L22
4	L3	24	L23
5	L4	25	L24
6	L5	26	L25
7	L6	27	L26
8	L7	28	L27
9	L8	29	L28
10	L9	30	L29
11	L10	31	L30
12	L11	32	L31
13	L12	33	L32
14	L13	34	L33
15	L14	35	—
16	L15	36	—
17	L16	37	—
18	L17	38	—
19	L18	39	—
20	L19	40	—

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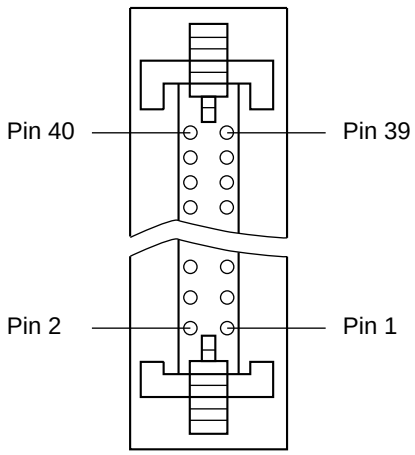
(3) LED connector



- As shown at left, the LED connector is a 40-pin connector with pin 1 at lower right.
- The LED connector corresponds to thend L0~L33 pins of the MSM64162 and MSM64164. It outputs LED driver signals 0V to 5V.

LED Connector Pin List

Pin Number	Signal Name	Pin Number	Signal Name
1	L0	21	L20
2	L1	22	L21
3	L2	23	L22
4	L3	24	L23
5	L4	25	L24
6	L5	26	L25
7	L6	27	L26
8	L7	28	L27
9	L8	29	L28
10	L9	30	L29
11	L10	31	L30
12	L11	32	L31
13	L12	33	L32
14	L13	34	L33
15	L14	35	—
16	L15	36	—
17	L16	37	—
18	L17	38	—
19	L18	39	GND
20	L19	40	GND

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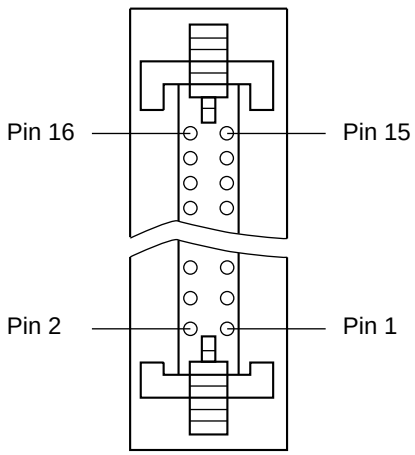
(4) ADC connector



* The ADC connector is a 16-pin connector with pin 1 at the lower right.

* The ADC connector connects to the accessory ADC POD.

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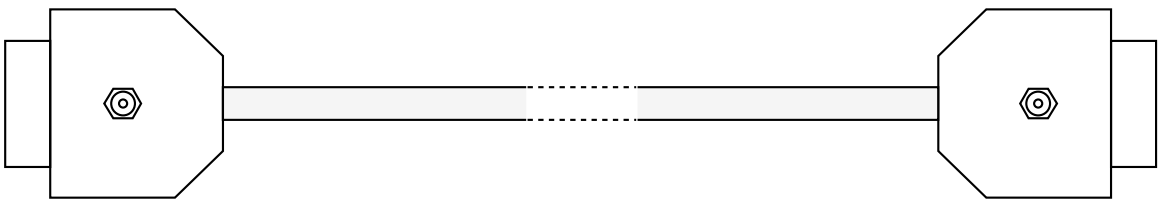
A.4. RS232C Cable Configuration

(1) For NEC PC9801and OKI if800 series computers



Emulator Serial Port			Host Computer Serial Port	
Signal name	*Terminal No.*		*Terminal No.*	*Signal name*
F.GND	**1**	———	**1**	**F.GND**
RxD	**2**	———	**2**	**TxD**
TxD	**3**	———	**3**	**RxD**
CTS	**4**	———	**4**	**RTS**
RTS	**5**	———	**5**	**CTS**
DTR	**6**	———	**6**	**DSR**
S. GND	**7**	———	**7**	**S.GND**
CD	**8**	———	**8**	**CD**
	:		:	
DSR	**20**	———	**20**	**DTR**

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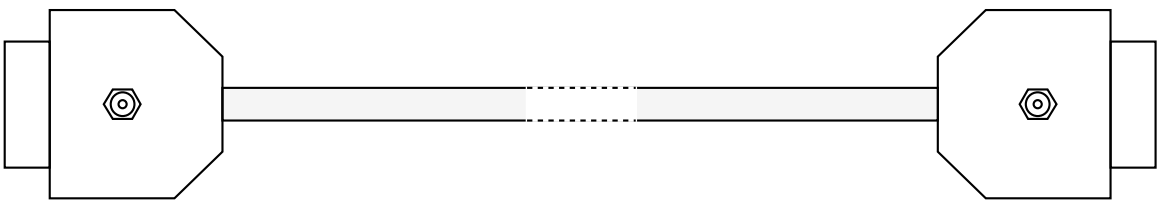
(2) For IBM PC/AT computers



Emulator Serial Port

Host Computer Serial Port

Signal Name	*Pin Number*		*Pin Number*	*Signal Name*
F.GND	**1**		**1**	**CD**
RxD	**2**		**2**	**RxD**
TxD	**3**		**3**	**TxD**
CTS	**4**		**4**	**DTR**
RTS	**5**		**5**	**S. GND**
DTR	**6**		**6**	**DSR**
S. GND	**7**		**7**	**RTS**
CD	**8**		**8**	**CTS**
DSR	**20**		**9**	

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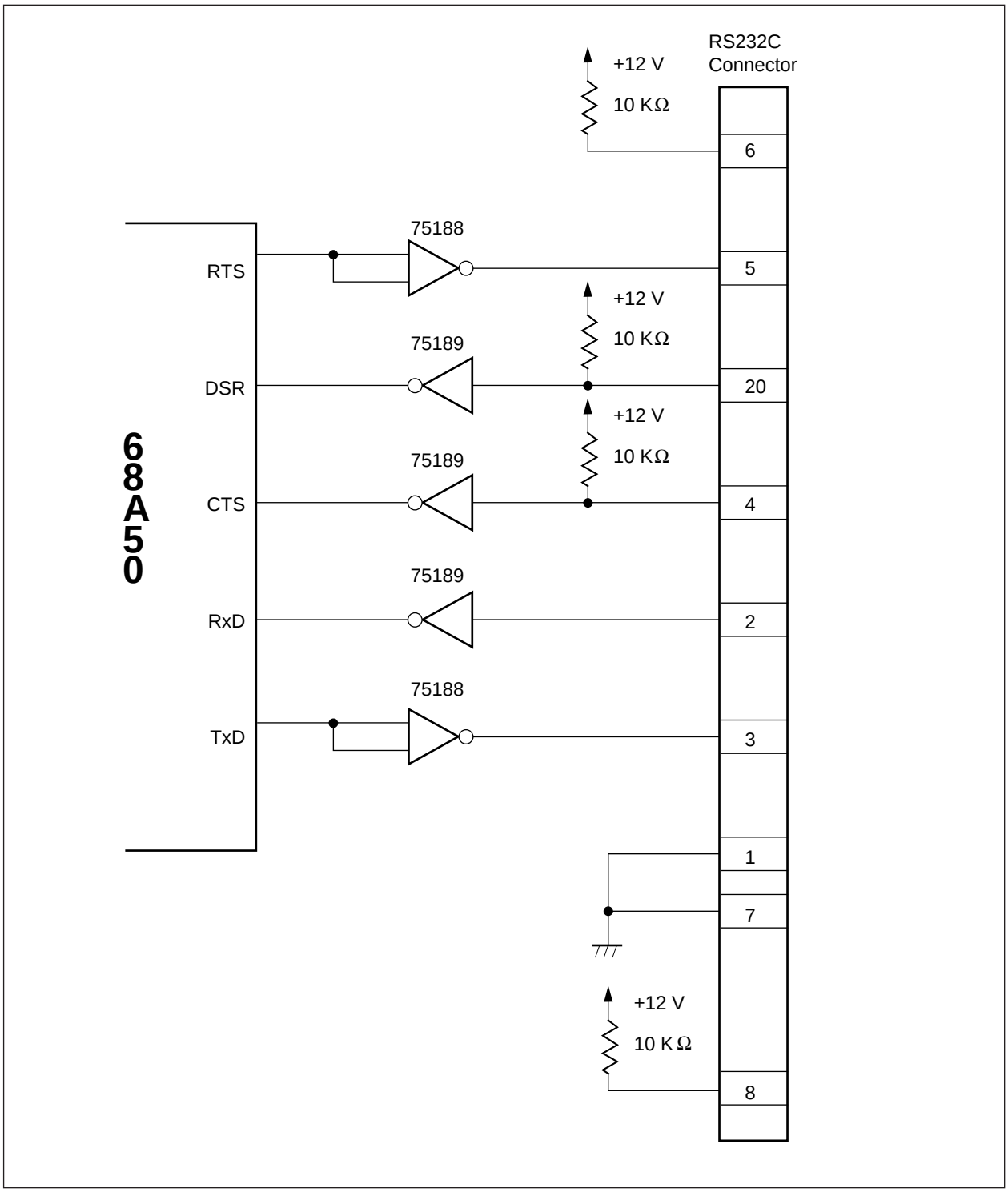
A.5. Emulator RS232C Interface Circuit



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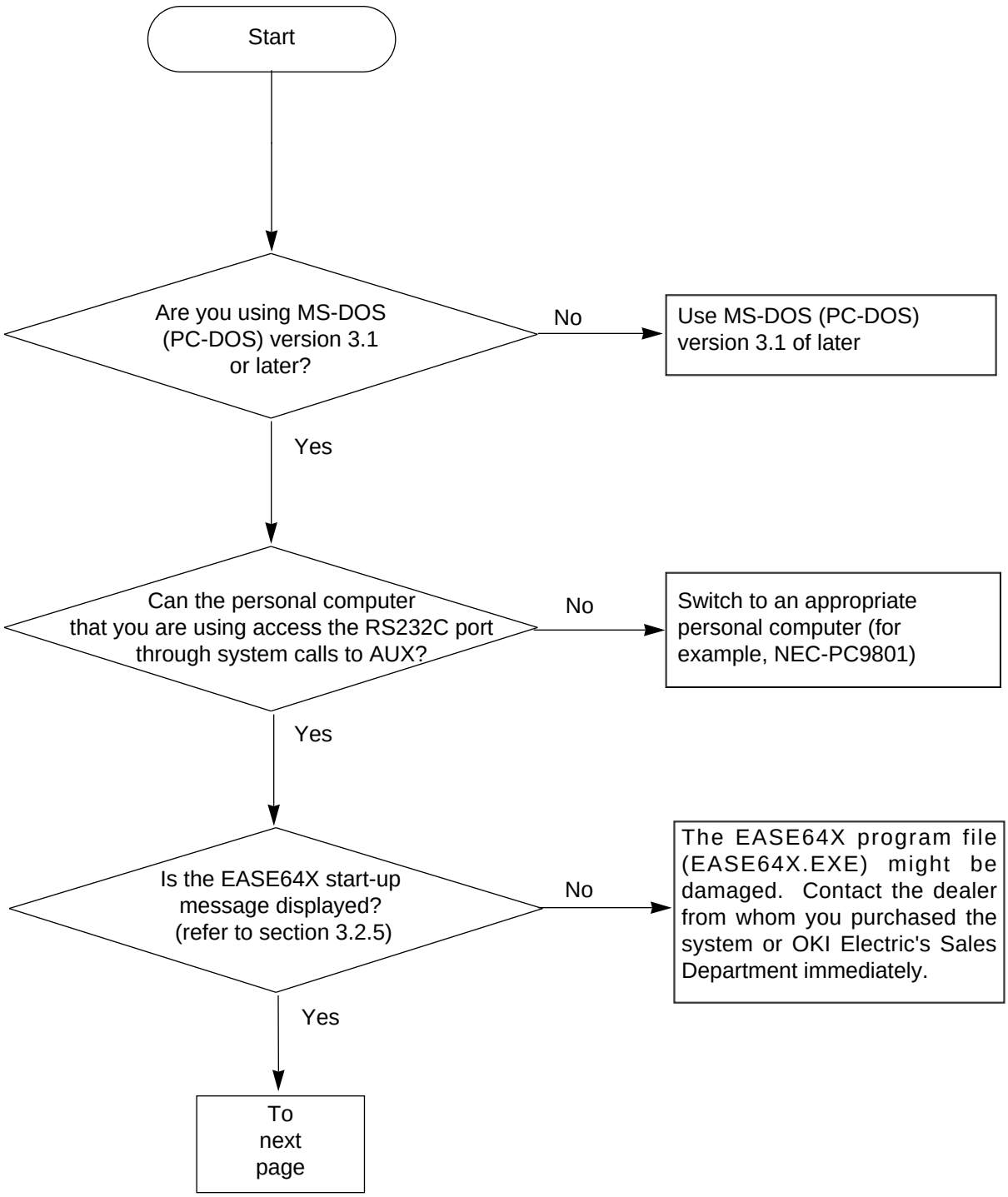
A.6. If EASE64162/164 Won't Start



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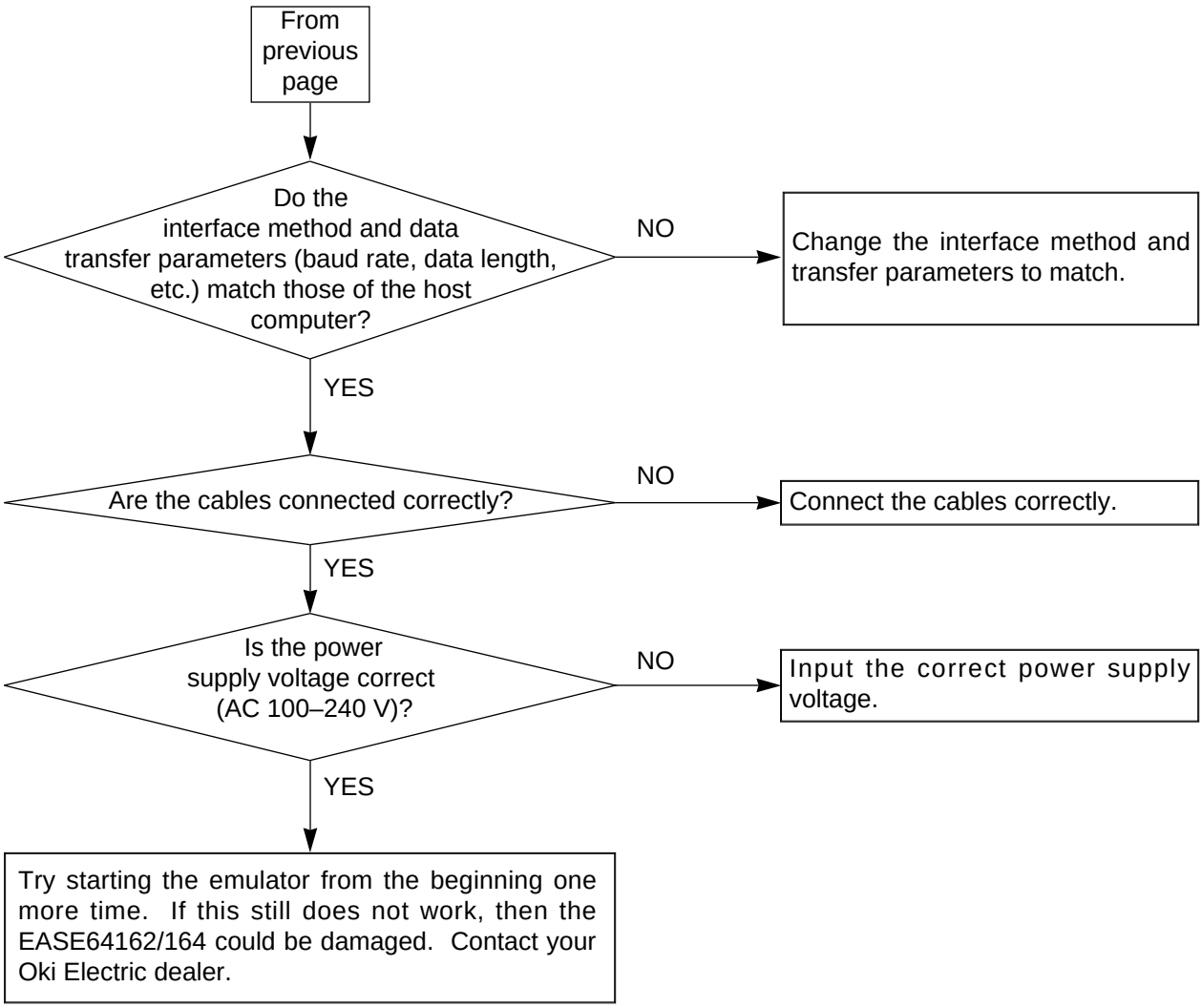
From previous page
Do the interface method and data transfer parameters (baud rate, data length, etc.) match those of the host computer?
NO
Change the interface method and transfer parameters to match.
YES
Are the cables connected correctly?
NO
Connect the cables correctly.
YES
Is the power supply voltage correct (AC 100–240 V)?
NO
Input the correct power supply voltage.
YES
Try starting the emulator from the beginning one more time. If this still does not work, then the EASE64162/164 could be damaged. Contact your Oki Electric dealer.

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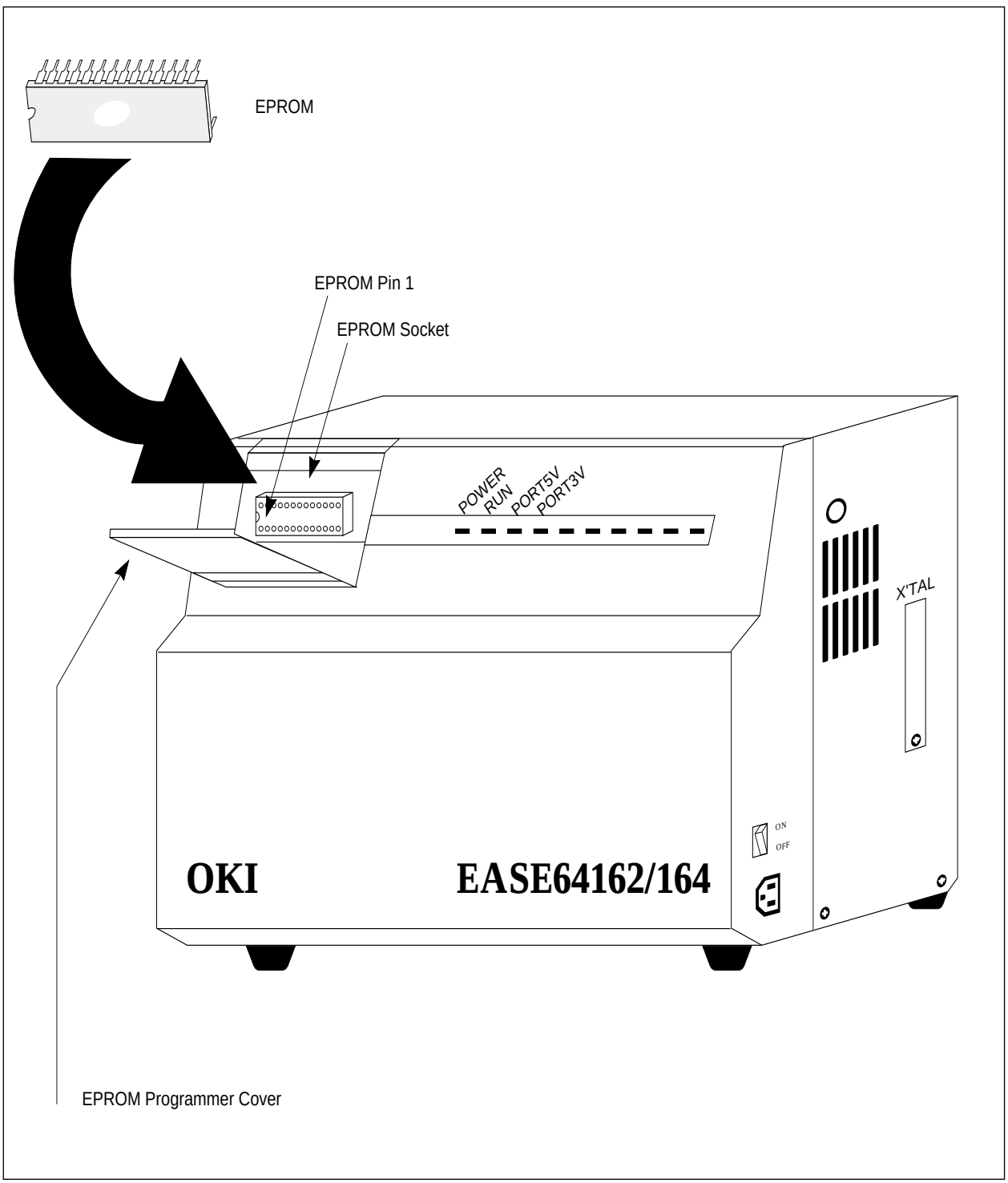
A.7. Mounting EPROMs

Follow the procedure below to insert an EPROM into the EASE64162/164's EPROM socket.

(1) Open the EPROM programmer cover in the upper left of the EASE64162/164, as shown below.



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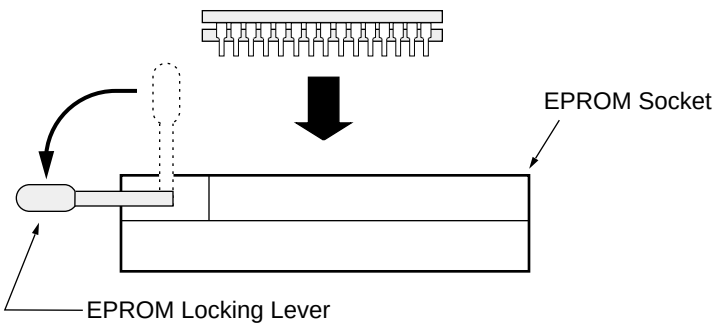
(2) Next, set the EPROM to be written or read in the EPROM socket, as shown below.



To set the EPROM, insert the EPROM in the EPROM socket while the EPROM locking lever is up, and then flip the EPROM locking lever to the horizontal position.

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A.8. Error Messages

**** Error 1: Data address error ****

The input address was not an allowable value.

**** Error 2: Data error ****

The input data value was not an allowable value.

**** Error 3: Illegal format ****

The command syntax contains an error.

**** Error 4: Command not found ****

The input command does not exist.

**** Error 5: Break status not found ****

The break status does not exist.

**** Error 6: Trace data not ready ****

No data has been traced into trace memory.

**** Error 7: File not found ****

The input file name cannot be found.

**** Error 8: Command input too long ****

The number of characters input exceeds 256.

**** Error 9: EPROM abnormal ****

Programming of the EPROM was not performed correctly.

**** Error 10: File not found ****

The specified file name cannot be found.

**** Error 11: Illegal file ****

The specified file is not in Intel HEX format.

**** Error 12: Illegal file ****

The specified HEX file contains an error.

**** Error 13: Abort ****

Communications were terminated abnormally.

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**** Error 14: Cannot create file ****

The specified file cannot be created.

**** Error 15: Disk full ****

The disk is full.

**** Error 16: File write error ****

The specified file cannot be written correctly.

**** Error 17: File read error ****

The specified file cannot be read correctly.

**** Error 18: File open error ****

The specified file cannot be opened.

**** Error 19: File close error ****

The specified file cannot be closed.

**** Error 20: Illegal code accepted ****

The emulator received an illegal code.

**** Error 21: Communication buffer overflow ****

An abnormal condition occurred during communication.

**** Error 22: Already diagnostic sequence ****

A batch file is already open.

**** Error 23: List file already open ****

A list file is already open.

**** Error 24: List file already closed ****

No list file is open.

**** Warning 1: The 1/2 bias signal cannot be output ****

A 1/2 bias waveform cannot be output.

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**** Warning 2: The LCD driver duty disagreed with mask option ****

The LCD duty setting differs from the loaded mask option data.

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A.9. Command Summary

Evaluation Board Access Commands			Page
1	**CHIP**	Set target chip	3-61
	CHIP [Δ *mnemonic*] ↵		
	mnemonic : 64164, 64164		
2	**D**	Display contents of target chip registers	3-62
	D ↵ or D *mnemonic* ↵		
	mnemonic : PC, B, A, HL, XY, CY, SP, BSR0, BSR1, BCF, BEF, ,P0, ,P1D, ,P2D, ,P3D, ,P4D, ,SBUF, ,SCON, ,FCON, ,BDCON, ,BFCON, ,CAPR0, ,CAPR1, ,CAPCON, ,TBCR, ,DSPCON, CNTA, ,CNTB, ,ADCON0, ,ADCON1, ,IE0, ,IE1, ,IE2, ,IRQ0, ,IRQ1, ,IRQ2, ,BUPCON, ,MIEF	
3	**C**	Change contents of target chip registers	3-62
	C*mnemonic* Δ *data* ↵		
	mnemonic : PC (0 to 7DF or 0 to FDF), B (0 to F), A (0 to F), HL (0 to FF), XY (0 to FF), SP (0 to FF), BSR0 (0 to F), BSR1 (0 to F), BCF (0, 1), BEF (0, 1), P1D (0 to F), P2D (0 to F), P3D (0 to F), P4D (0 to F), ,CAPR0 (0 to FF), ,CAPR1 (0 to FF), ,CAPCON (0 to 1), ,CNTA (0 to 79999), ,CNTB (0 to 3FFF), ,ADCON0 (0 to 3), ,ADCON1 (0 to F), ,SBUF (0 to FF), ,SCON (0 to F), ,FCON (0, 1), ,BDCON (0 to F), ,BFCON (0, 1 or 0 to F), ,BUPCON (0 to 3 or 0, 1), ,TBCR (0 to F), ,DSPCON (0 to 3), ,IE0 (0 to F), ,IE1 (0 to F), ,IE2 (0, 1), ,IRQ0 (0 to F), ,IRQ1 (0 to F), ,IRQ2 (0 to F), ,MIEF (0, 1), ,P20CON (0 to F), ,P21CON (0 to F), ,P22CON (0 to F), ,P23CON (0 to F), ,P30CON (0 to F), ,P31CON (0 to F), ,P32CON (0 to F), ,P33CON (0 to F), ,P40CON (0 to F), ,P41CON (0 to F), ,P42CON (0 to F), ,P43CON (0 to F), ,P01CON (0 to F)	
	(☞1)		

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Evaluation Board Access Commands (cont.)			Page
4	**DDSPR**	Display Display Register	3-67
	DDSPR ↵		
5	**CDSPR**	Change Display Register	3-67
	CDSPR Δ *mnemonic* ↵		
	mnemonic : 0~20 . . . MSM64162 mode 0~30 . . . MSM64164 mode		

☞ 1

- The numbers in parentheses indicate the input data range for the corresponding *mnemonics*.
- The data range of PC is 0H~7DFH in MSM64162 mode and 0H~FDFH in MSM64164 mode.
- When TBCR is changed, it will be reset to 0 regardless of the specified data.
- The change data of CNTA is a decimal value.
- In MSM64162 mode, the following mnemonics are invalid.

  P4D, SBUF, SCON, P40CON, P41CON, P42CON, P43CON
- The data range of BFCON is 0H or 1H in MSM64162 mode and 0H~FH in MSM64164 mode.
- The data range of BUPCON is 0H~3H in MSM64162 mode and 0H or 1H in MSM64164 mode.
- The FCON register does not exist in the MSM64162D chip.
- If invalid data (5H, 6H, or 7H) is written to the ADCON1 register when evaluating a MSM64162D, then the emulator may operate incorrectly.

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	Code Memory Commands		Page
1	**DCM**	Display Code Memory	3-71
	DCM Δ *address* [, *address*] ↵ or DCM Δ * ↵		
	address : 0 to 7DF . . . MSM64162 mode 0 to FDF . . . MSM64164 mode * : displays entire address range		
2	**CCM**	Change Code Memory	3-73
	CCM Δ *address* ↵		
	address : 0 to 7DF . . . MSM64162 mode 0 to FDF . . . MSM64164 mode		
3	**FCM**	Fill Code Memory	3-75
	FCM Δ *address* , *address* [, *data*] ↵ or FCM Δ * [, *data*] ↵		
	address : 0 to 7DF . . . MSM64162 mode 0 to FDF . . . MSM64164 mode * : fills entire address range *data* : 0 to FF		
4	**LOD**	Load Disk file program into Code Memory	3-77 3-81
	LOD Δ *fname* ↵		
	fname : [*Pathname*] *filename* [*extension*]		
5	**SAV**	Save Code Memory into Disk file	3-78 3-81
	SAV Δ *fname* [Δ *address , address*] ↵		
	address : 0 to 7DF . . . MSM64162 mode 0 to FDF . . . MSM64164 mode *fname* : [*Pathname*] *filename* [*extension*]		

	Code Memory Commands (cont.)		Page
6	**VER**	Verify Disk file with Code Memory	3-79 3-81
	VER Δ *fname* [Δ *address* , *address*] ↵		
	address : 0 to 7DF . . . MSM64162 mode 0 to FDF . . . MSM64164 mode *fname* : [*Pathname*] *filename* [*extension*]		
7	**ASM**	Line Assembler Command This command stores the code it generates in code memory.	3-82
	ASM Δ *address* ↵		
	address : 0 to 7DF . . . MSM64162 mode 0 to FDF . . . MSM64164 mode		
8	**DASM**	Disassembler Command This command disassembles program memory contents of a specified address range.	3-84
	DASM Δ *address* [, *address*] ↵ or DASM Δ * ↵		
	address : 0 to 7DF . . . MSM64162 mode 0 to FDF . . . MSM64164 mode * : displays entire address range		

	Data Memory Commands		Page
1	**DDM**	Display Data Memory	3-87
	DDM Δ *address* [, *address*] ↵ or DDM Δ * ↵		
	address : 780 to 7FF . . . MSM64162 mode 700 to 7FF . . . MSM64164 mode * : displays entire address range		
2	**CDM**	Change Data Memory	3-89
	CDM Δ *address* ↵		
	address : 780 to 7FF . . . MSM64162 mode 700 to 7FF . . . MSM64164 mode		
3	**FDM**	Fill Data Memory	3-91
	FDM Δ *address* , *address* [, *data*] ↵ or FDM Δ * [, *data*] ↵		
	address : 780 to 7FF . . . MSM64162 mode 700 to 7FF . . . MSM64164 mode * : fills entire address range *data* : 0 to FF		

	Emulation Commands		Page
1	**STP**	Step Execution	3-94
	STP [Δ *number*] [, *address*] ↵ or STP Δ * ↵		
	address : 0 to 7DF . . . MSM64162 mode 0 to FDF . . . MSM64164 mode * : executes 65535 steps *number* : 1 to 65535		
2	**G**	Realtime Emulation (continuous execution)	3-97
	G [Δ *address*] [, *parm*] ↵		
	parm : *address* [, *address* . . . , *address*] RAM (*data–count*) BAR (*data–count*) *address* (*count*) *address* : 0 to 7DF . . . MSM64162 mode 0 to FDF . . . MSM64164 mode		

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	Break Commands		Page
1	**DBC**	Display Break Condition Register	3-103
	DBC ↵		
2	**SBC**	Set Break Condition Register	3-103
	SBC ↵		
3	**DBS**	Display Break Status	3-109
	DBS ↵		
4	**DBP**	Display Break Point Bits	3-105
	DBP Δ *address* [, *address*] ↵		
	address : 0 to 7DF . . . MSM64162 mode 0 to FDF . . . MSM64164 mode		
5	**EBP**	Enable Break Point Bits	3-106
	EBP Δ *address* [, *address . . .* , *address*] ↵		
	address : 0 to 7DF . . . MSM64162 mode 0 to FDF . . . MSM64164 mode		
6	**RBP**	Reset Break Point Bits	3-105
	RBP Δ *address* [, *address . . .* , *address*] ↵		
	address : 0 to 7DF . . . MSM64162 mode 0 to FDF . . . MSM64164 mode		

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Break Commands			Page
7	**FBP**	Fill Break Point Bits	3-107
	FBP Δ *address* , *address* [, *data*] ↵ or FBP Δ * [, *data*] ↵		
	address : 0 to 7DF . . . MSM64162 mode 0 to FDF . . . MSM64164 mode * : fills entire address range *data* : 0, 1		

	Trace Commands		Page
1	**DTM**	Display Trace Memory	3-112
	DTM Δ -*number*$_{-step}$ Δ *number*$_{step}$ ↵ or DTM Δ *number*$_{TP}$ Δ *number*$_{step}$ ↵ or DTM Δ * ↵		
	number$_{-step}$: number of steps to go back (1~8192) *number*$_{step}$: number of steps to display (1~8192) *number*$_{TP}$: value of TP at which to start display (0~8191) * : Display the entire area of trace memory		
2	**CTO**	Change Trace Object	3-118
	CTO ↵		
3	**DTO**	Display Trace Object	3-118
	DTO ↵		
4	**CTDM**	Change Trace Data Memory	3-117
	CTDM [Δ *address*]↵		
	address : 780 to 7FF . . . MSM64162 mode 700 to FDF . . . MSM64164 mode		
5	**DTDM**	Display Trace Data Memory	3-117
	DTDM ↵		
6	**STT**	Set Trace Trigger	3-120
	STT ↵		

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Trace Commands (continued)			Page
7	**DTT**	Display Trace Trigger	3-118
	DTT ↵		
8	**RTT**	Reset Trace Trigger	3-118
	RTT ↵		
9	**DTR**	Display Trace Enable Bits	3-124
	DTR Δ *address* [, *address . . .* , *address*] ↵ or DTR Δ *↵		
	address : 0 to 7DF . . . MSM64162 mode 0 to FDF . . . MSM64164 mode * : displays entire address range		
10	**ETR**	Enable Trace Enable Bits	3-125
	ETR Δ *address* [, *address . . .* , *address*] ↵		
	address : 0 to 7DF . . . MSM64162 mode 0 to FDF . . . MSM64164 mode		
11	**RTR**	Reset Trace Enable Bits	3-125
	RTR Δ *address* [, *address . . .* , *address*] ↵		
	address : 0 to 7DF . . . MSM64162 mode 0 to FDF . . . MSM64164 mode		
12	**FTR**	Fill Trace Enable Bits	3-126
	FTR Δ *address* , *address* [, *data*] ↵ or FTR Δ * [, *data*] ↵		
	address : 0 to 7DF . . . MSM64162 mode 0 to FDF . . . MSM64164 mode * : fills entire address range *data* : 0, 1		

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Trace Commands (continued)			Page
13	**DTP**	Display Trace Pointer	3-128
	DTP ↵		
14	**RTP**	Reset Trace Pointer	3-128
	RTP ↵		

Reset Commands			Page
1	**RST**	Reset System and Evaluation Chip	3-130
	RST ↵ Reset the system. RST Δ E ↵ Reset the evaluation chip.		
2	**URST**	Set User Reset Terminal (on user cable)	3-132
	URST [Δ *mnemonic*]↵		
	mnemonic : ON, OFF		

	Performance/Coverage Commands		Page
1	**DCC**	Display Cycle Counter	3-137
	DCC ↵		
2	**CCC**	Change Cycle Counter	3-138
	CCC Δ [-]*number* ↵		
	number : 0 to 4294967295		
3	**SCT**	Set Cycle Counter Trigger	3-134
	SCT ↵		
4	**DCT**	Display Cycle Counter Trigger	3-134
	DCTz		
5	**RCT**	Reset Cycle Counter Trigger	3-134
	RCT ↵		
6	**DIE**	Display Instruction Executed Bits	3-139
	DIE Δ *address* [, *address*] or DIE Δ * ↵		
	address : 0 to 7DF . . . MSM64162 mode 0 to FDF . . . MSM64164 mode * : displays entire address range		
7	**RIE**	Reset Instruction Executed Bits	3-139
	RIE ↵		

	EPROM Programmer Commands		Page
1	**TYPE**	Set EPROM Type	3-142
	TYPE Δ *mnemonic* ↵		
	mnemonic : 64, 128, 256, 512		
2	**PPR**	Program EPROM	3-143
	PPR Δ *address*$_{Code}$, *address*$_{Code}$ [, *address*$_{EPROM}$]↵ or PPR Δ * ↵		
	address $_{Code}$: 0 to 7DF . . . MSM64162 mode 0 to FDF . . . MSM64164 mode * : programs entire address range *address* $_{EPROM}$: EPROM write address		
3	**TPR**	Transfer EPROM into Code Memory	3-145
	TPR Δ *address*$_{Code}$, *address*$_{Code}$ [, *address*$_{EPROM}$]↵ TPR Δ * ↵		
	address $_{Code}$: 0 to 7DF . . . MSM64162 mode 0 to FDF . . . MSM64164 mode * : transfers entire address range *address* $_{EPROM}$: EPROM transfer address		
4	**VPR**	Verify EPROM with Code Memory	3-147
	VPR Δ *address*$_{Code}$, *address*$_{Code}$ [, *address*$_{EPROM}$]↵ VPR Δ * ↵		
	address $_{Code}$: 0 to 7DF . . . MSM64162 mode 0 to FDF . . . MSM64164 mode * : verifies entire address range *address* $_{EPROM}$: EPROM comparison address		

	Mask Option File Commands		Page
1	**LODM**	Load Disk file Mask Option into System memory	3-150
	LODM Δ *fname* ↵		
	fname : [*Pathname*] *filename* [*Extension*]		
2	**VERM**	Verify Disk file with System Memory	3-151
	VERM Δ *fnamez*		
	fname : [*Pathname*] *filename* [*Extension*]		
3	**PPRM**	Program Mask Option Data into EPROM	3-153
	PPRM ↵		
4	**TPRM**	Transfer EPROM into System Memory	3-154
	TPRM ↵		
5	**VPRM**	Verify EPROM with System Memory	3-155
	VPRM ↵		

	Commands for Automatic Command Execution		Page
1	**BATCH**	Batch Processing	3-158
	BATCH Δ *fname* ↵		
	fname : [*Pathname*] *filename* [*Extension*]		
2	**PAUSE**	Pause Command Input	3-159
	PAUSE ↵		

	Other Commands		Page
1	**LIST**	Listing (Redirect the Console output to Disk file)	3-161
	LIST Δ *fname* ↵		
	fname : [*Pathname*] *filename* [*Extension*]		
2	**NLST**	No Listing (Cancel the Console output Redirection)	3-162
	NLST ↵		
3	**>**	Call OS Shell	3-163
	>DOS command ↵		
4	**CCLK**	Display/Change Clock Mode	3-164
	CCLK [Δ *mnemonic*] ↵		
	HIN, HOUT, LIN, LOUT		
5	**CIPS**	Display/Change Interface Power Supply	3-165
	CIPS [Δ *mnemonic*] ↵		
	mnemonic : INT, EXT		
6	**EXPAND**	Expand Code Memory	3-166
	EXPAND [Δ *mnemonic*] ↵		
	mnemonic : ON, OFF		
7	**EXIT**	Terminate the Debugger and Exit to OS	3-168
	EXIT ↵		