OKI Semiconductor

MK31VT832-10YC

8,388,608 Word x 32 Bit SYNCHRONOUS DYNAMIC RAM MODULE (1BANK):

DESCRIPTION

The Oki MK31VT832-10YC is a fully decoded, 8,388,608 x 32bit synchronous dynamic random access memory composed of four 64Mb DRAMs (8Mx8) in TSOP packages mounted with decoupling capacitors on a 100-pin glass epoxy Dual-in-Line Package supports any application where high density and large capacity of storage memory are required, like for example PCs or servers.

FEATURES

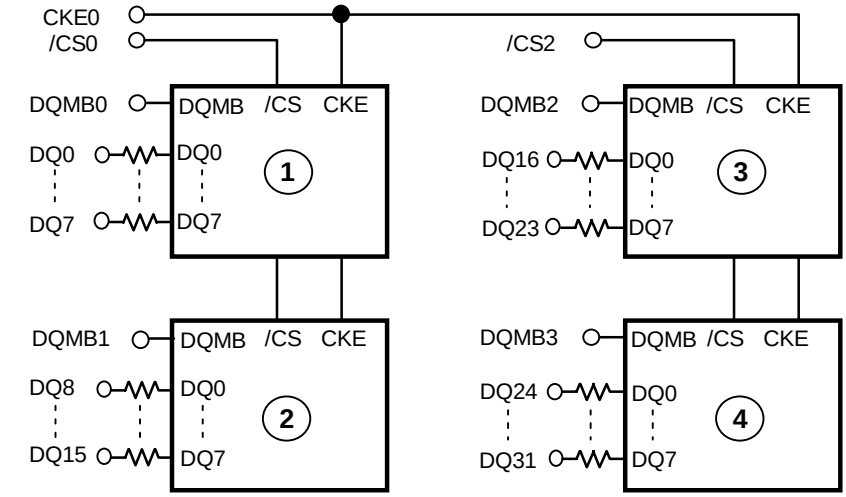
- 8-Meg Word x 32-Bit (1Bank 4 Byte) organization
- 100-pin Dual Inline Memory Module
- 10Ω Damping Resister for DQ and CLK Pins
- Single 3.3V power supply, ±0.3V tolerance
- Input :LVTTL compatible
- Output :LVTTL compatible
- Refresh : 4,096 cycles/64 ms
- Programmable data transfer mode
  - /CAS latency (2, 3)
  - Burst length (2, 4, 8)
  - Data scramble(sequential, interleave)
- /CAS before /RAS auto-refresh, Self-refresh capability
- Serial Presence Detect (SPD) With EEPROM

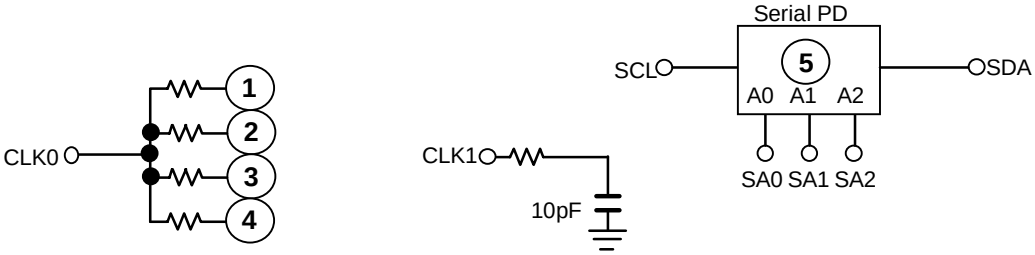
PRODUCT ORGANIZATION

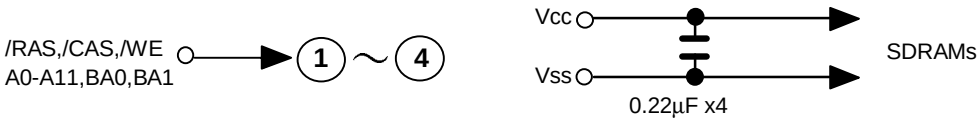
Product Name	Operation Frequency (Max.)	Access Time (Max.)	
		t_{AC2}	t_{AC3}
MK31VT832 - 10YC	100 MHz	9.0ns	9.0ns

Note. Specification are subject to change without notice.

BLOCK DIAGRAM

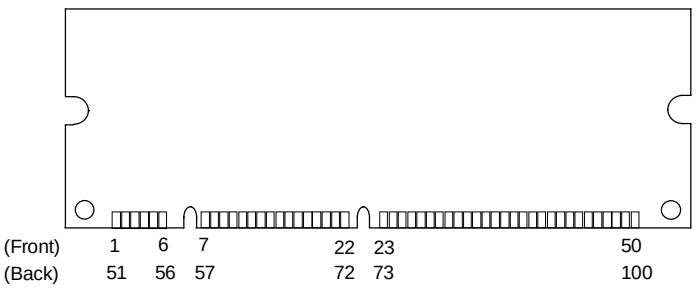






Note. The Value of all resistors is 10Ω .

MODULE OUTLINE



PIN CONFIGURATION

Front side		Back side	
Pin No.	Pin name	Pin No.	Pin name
1	VSS	51	VSS
2	DQ0	52	DQ8
3	DQ1	53	DQ9
4	DQ2	54	DQ10
5	DQ3	55	DQ11
6	VCC	56	VCC
7	DQ4	57	DQ12
8	DQ5	58	DQ13
9	DQ6	59	DQ14
10	DQ7	60	DQ15
11	DQMB0	61	DQMB1
12	VSS	62	VSS
13	A0	63	A1
14	A2	64	A3
15	A4	65	A5
16	A6	66	A7
17	A8	67	A9
18	A10	68	BA0
19	BA1	69	A11
20	NC	70	NC
21	VCC	71	VCC
22	NC	72	/RAS
23	NC	73	/CAS
24	NC	74	NC
25	CLK0	75	CLK1

Front side		Back side	
Pin No.	Pin name	Pin No.	Pin name
26	VSS	76	VSS
27	CKE0	77	NC
28	/WE	78	NC
29	/CS0	79	NC
30	/CS2	80	NC
31	VCC	81	VCC
32	NC	82	NC
33	NC	83	NC
34	NC	84	NC
35	NC	85	NC
36	VSS	86	VSS
37	DQMB2	87	DQMB3
38	DQ16	88	DQ24
39	DQ17	89	DQ25
40	DQ18	90	DQ26
41	DQ19	91	DQ27
42	VCC	92	VCC
43	DQ20	93	DQ28
44	DQ21	94	DQ29
45	DQ22	95	DQ30
46	DQ23	96	DQ31
47	VSS	97	VSS
48	SDA	98	SA0
49	SCL	99	SA1
50	VCC	100	SA2

Pin Name	Function	Pin Name	Function
VCC	Power Supply (3.3V)	/WE	Write Enable
VSS	Ground (0V)	DQMB#	Data Input / Output Mask
CLK#	System Clock	DQ#	Data Input / Output
/CS#	Chip Select	SDA	Data I/O for SPD
CKE#	Clock Enable	SCL	CLK input for SPD
A0-A11	Address	SA#	Socket Position Address for SPD
BA0, BA1	Bank Select Address	NC	No Connection
/RAS	Row Address Strobe		
/CAS	Column Address Strobe		

SERIAL PRESENCE DETECT

Byte No.	SPD Hex Value	Remark	Notes
0	80	Defines the number of bytes written into SPD memory	128 byte
1	08	Total number of bytes of SPD memory	256 byte
2	04	Fundamental memory type	SDRAM
3	0C	Number of rows	12 rows
4	09	Number of columns	9 columns
5	01	Number of module banks	1 bank
6	20	Data width of this assembly	32 bits
7	00	... Data width continuation	0
8	01	Voltage interface level	LVTTL
9	A0	Cycle time (CL=3)	CL=3 t_{CC3}=10ns
10	90	Access time from CLK (CL=3)	CL=3 t_{AC3}=9ns
11	00	DIMM configuration type	None Parity
12	80	Refresh rate / type	Normal / Self
13	08	Primary SDRAM width	x8
14	00	Error checking SDRAM width	
15	01	Minimum CLK delay	t_{CCD}: 1 CLK
16	0E	Burst lengths supported	2, 4, 8
17	04	Number of banks on each SDRAM	4 banks
18	06	/CAS latency	2, 3
19	01	/CS latency	0
20	01	/WE latency	0
21	00	SDRAM module attributes	
22	06	SDRAM device attributes : General	
23	F0	Cycle time (CL=2)	CL=2 t_{CC2}=15ns
24	90	Access time from CLK (CL=2)	CL=2 t_{AC2}=9ns
25	00	Cycle time (CL=1)	Not support
26	00	Access time from CLK (CL=1)	Not support
27	1E	Minimum ROW pulse width	t_{RP}=30ns
28	14	/RAS to /RAS bank delay	t_{RRD}=20ns
29	1E	/RAS to /CAS delay	t_{RCD}=30ns
30	3C	Minimum /RAS precharge time	t_{RAS}=60ns
31	08	Density of each bank on module	32MB
32	30	Command and address signal input setup time	3ns
33	10	Command and address signal input hold time	1ns
34	30	Data signal input setup time	3ns
35	10	Data signal input hold time	1ns
36-61	00-00	Superset Information	R.F.U
62	02	SPD data revision code	0.2
63	32	Checksum for byte 0-62	
64-71	41,45,20,20,20,20,20,20	Manufacturer's JEDEC ID code	
72	01 / 06	Manufacturing location	
73-90	4D,4B,33,31,56,54,38,33,32, 2D,31,30,59,43,20,20,20,20	Manufacturer's part number	MK31VT832-10YC
91, 92	20, 20	Revision code	
93-125	00-00	R.F.U	
126	66	Intel specification frequency	66MHz
127	06	Intel specification /CAS latency	CL=2, 3
128-255	FF-FF	Unused storage locations	

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.5 to Vcc+0.5	V
Vcc supply voltage	Vcc, VccQ	-0.5 to 4.6	V
Storage temperature	T_{stg}	- 55 to 150	°C
Power dissipation	P_{D*}	4	W
Short circuit current	I_{OS}	50	mA
Operating temperature	T_{opr}	0 to 70	°C

*: Ta=25°C

Recommended Operating Conditions

(Voltages referenced to Vss = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	Vcc, VccQ	3.0	3.3	3.6	V
Input high voltage	V_{IH}	2.0	-	Vcc+0.3	V
Input low voltage	V_{IL}	-0.3	-	0.8	V

Capacitance

(Vcc=3.3V ± 0.3V, Ta=25°C f=1MHz)

Parameter	Symbol	Max.	Unit
Input capacitance(A0-A11, /RAS, /CAS, /WE)	C_{IN1}	20	pF
Input capacitance(/CS0, /CS2)	C_{IN2}	20	pF
Input capacitance(DQMB0-DQMB3)	C_{IN3}	5	pF
Input capacitance(CKE0)	C_{IN4}	20	pF
I/O capacitance(DQ0-DQ31)	$C_{I/O}$	7	pF
Input capacitance(CLK0, CLK1)	C_{CLK}	50	pF

DC CHARACTERISTICS

(Vcc=3.3V ± 0.3V, Ta = 0 to 70 °C)

Parameter	Symbol	Condition		Module Spec.		Unit	Note
		CKE	Others	Min.	Max.		
Output High Voltage	V_{OH}	-	I_{OH} = -2.0mA	2.4	-	V	
Output Low Voltage	V_{OL}	-	I_{OL} = 2.0mA	-	0.4	V	
Input Leakage Current	I_{LI}	-	-	-40	40	µA	
Output Leakage Current	I_{LO}	-	-	-10	10	µA	
Average Power Supply Current (Operating)	I_{CC1}	CKE ≥ V_{IH}	t_{CC}=min. t_{RC}=min. No Burst	-	460	mA	1, 2
Power Supply Current (Stand by)	I_{CC2}	CKE ≥ V_{IH}	t_{CC}=min.	-	160	mA	3
Average Power Supply Current (Clock Suspension)	I_{CC3S}	CKE ≤ V_{IL}	t_{CC}=min.	-	60	mA	2
Average Power Supply Current (Active Stand by)	I_{CC3}	CKE ≥ V_{IH}, /CS ≥ V_{IH}	t_{CC}=min.	-	320	mA	3
Power Supply Current (Burst)	I_{CC4}	CKE ≥ V_{IH}	t_{CC}=min.	-	620	mA	1, 2
Power Supply Current (Auto-Refresh)	I_{CC5}	CKE ≥ V_{IH}	t_{CC}=min. t_{RC}=min.	-	740	mA	2
Average Power Supply Current (Self-Refresh)	I_{CC6}	CKE ≤ 0.2V	t_{CC}=min.	-	8	mA	
Average Power Supply Current (Power down)	I_{CC7}	CKE ≤ V_{IL}	t_{CC}=min.	-	8	mA	

Notes: 1. Measured with the output open.
2. Address and data can be changed once or not be changed during one cycle.
3. Address and data can be changed once or not be changed during two cycle.

MODE SET ADDRESS KEYS

/CAS Latency				Burst Type		Burst Length				
A6	A5	A4	CL	A3	BT	A2	A1	A0	BT=0	BT=1
0	0	0	Reserved	0	Sequential	0	0	0	Reserved	Reserved
0	0	1	Reserved	1	Interleave	0	0	1	2	2
0	1	0	2			0	1	0	4	4
0	1	1	3			0	1	1	8	8
1	0	0	Reserved			1	0	0	Reserved	Reserved
1	0	1	Reserved			1	0	1	Reserved	Reserved
1	1	0	Reserved			1	1	0	Reserved	Reserved
1	1	1	Reserved			1	1	1	Reserved	Reserved

Note: A7, A8, A10, A11, BA0, BA1 and All should stay "L" during mode set cycle.

POWER ON SEQUENCE

1. With inputs in NOP state, turn on the power supply and enter the system clock.
2. After the VCC voltage has reached the specified level, take a pause of 200μs or more with the input being NOP.
3. Enter the precharge all bank command.
4. Apply CBR auto-refresh eight or more times.
5. Enter the mode register setting command.

AC CHARACTERISTIC

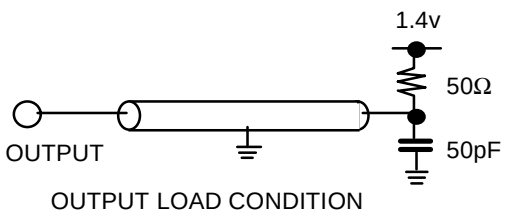
(Vcc=3.3V ± 0.3V, Ta = 0 to 70 °C)

NOTE 1, 2

Parameter		Symbol	Module Spec.		Unit	Note
			Min.	Max.		
Clock Cycle Time	CL=3	t_{CC}	10	-	ns	
	CL=2		15	-	ns	
Access Time from Clock	CL=3	t_{AC}	-	9	ns	3, 4
	CL=2		-	9	ns	3, 4
Clock "H" Pulse Time		t_{CH}	3	-	ns	
Clock "L" Pulse Time		t_{CL}	3	-	ns	
Input Setup Time		t_{SI}	3	-	ns	
Input Hold Time		t_{HI}	1	-	ns	
Output Low Impedance Time from Clock		t_{OLZ}	3	-	ns	
Output High Impedance Time from Clock		t_{OHZ}	-	8	ns	
Output Hold from Clock		t_{OH}	3	-	ns	3
/RAS Cycle Time		t_{RC}	90	-	ns	
/RAS Precharge Time		t_{RP}	30	-	ns	
/RAS Active Time		t_{RAS}	60	100,000	ns	
/RAS to /CAS Delay Time		t_{RCD}	30	-	ns	
Write Recovery Time		t_{WR}	15	-	ns	
/RAS to /RAS Bank Active Delay Time		t_{RRD}	20	-	ns	
Refresh Time		t_{REF}	-	64	ms	
Power-down Exit Set-up Time		t_{PDE}	t_{SI}+1CLK	-	ns	
Input Level Transition Time		t_T	-	3	ns	
/CAS to /CAS Delay Time (Min)		l_{CCD}	1		Cycle	
Clock Disable Time from CKE		l_{CKE}	1		Cycle	
Data Output High Impedance Time from DQMB		l_{DOZ}	2		Cycle	
Data Input Mask Time from DQMB		l_{DOD}	0		Cycle	
Data Input Time from Write Command		l_{DWD}	0		Cycle	
Data Output High Impedance Time from Precharge Command		l_{ROH}	2		Cycle	
Active Command Input Time from MODE Register Set Command Input (Min)		l_{MRD}	3		Cycle	
Write Command Input Time from Output		l_{OWD}	2		Cycle	

NOTES:

1) AC measurements assume t_T=1ns.
2) The reference level for timing of input signals is 1.4V.
3) This parameter is measured with a load circuit equivalent to 1 TTL load and 50pF (R_{Load} is 50ohm).
4) An access time is measured at 1.4V.
5) If t_T is longer than 1ns, the reference level for timing of input signals are V_{IH} and V_{IL}.



OUTPUT LOAD CONDITION

FUNCTION TRUTH TABLE (Table1) (1/2)

Current State	/CS	/RAS	/CAS	/WE	BA	ADDR	Action
Idle	H	X	X	X	X	X	NOP
	L	H	H	H	X	X	NOP
	L	H	H	L	BA	X	ILLEGAL [2]
	L	H	L	X	BA	CA	ILLEGAL [2]
	L	L	H	H	BA	RA	Row Active
	L	L	H	L	BA	A10	NOP [4]
	L	L	L	H	X	X	Auto-Refresh or Self-Refresh [5]
	L	L	L	L	L	OP Code	Mode Register write
Row Active	H	X	X	X	X	X	NOP
	L	H	H	X	X	X	NOP
	L	H	L	H	BA	CA, A10	Read
	L	H	L	L	BA	CA, A10	Write
	L	L	H	H	BA	RA	ILLEGAL [2]
	L	L	H	L	BA	A10	Precharge
	L	L	L	X	X	X	ILLEGAL
Read	H	X	X	X	X	X	NOP (Continue Row Active after Burst ends)
	L	H	H	H	X	X	NOP (Continue Row Active after Burst ends)
	L	H	H	L	BA	X	Reserved
	L	H	L	H	BA	CA, A10	Term Burst, start new Burst Read [3]
	L	H	L	L	BA	CA, A10	Term Burst, start new Burst Write [3]
	L	L	H	H	BA	RA	ILLEGAL [2]
	L	L	H	L	BA	A10	Term Burst, execute Row Precharge
	L	L	L	X	X	X	ILLEGAL
Write	H	X	X	X	X	X	NOP (Continue Row Active after Burst ends)
	L	H	H	H	X	X	NOP (Continue Row Active after Burst ends)
	L	H	H	L	BA	X	Reserved
	L	H	L	H	BA	CA, A10	Term Burst, start new Burst Read [3]
	L	H	L	L	BA	CA, A10	Term Burst, start new Burst Write [3]
	L	L	H	H	BA	RA	ILLEGAL [2]
	L	L	H	L	BA	A10	Term Burst, execute Row Precharge [3]
	L	L	L	X	X	X	ILLEGAL
Read with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End and enter Row Precharge)
	L	H	H	H	X	X	NOP (Continue Burst to End and enter Row Precharge)
	L	H	H	L	BA	X	ILLEGAL [2]
	L	H	L	H	BA	CA, A10	ILLEGAL [2]
	L	H	L	L	X	X	ILLEGAL
	L	L	H	X	BA	RA, A10	ILLEGAL [2]
	L	L	L	X	X	X	ILLEGAL
Write with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End and enter Row Precharge)
	L	H	H	H	X	X	NOP (Continue Burst to End and enter Row Precharge)
	L	H	H	L	BA	X	ILLEGAL [2]
	L	H	L	H	BA	CA, A10	ILLEGAL [2]
	L	H	L	L	X	X	ILLEGAL
	L	L	H	X	BA	RA, A10	ILLEGAL [2]
	L	L	L	X	X	X	ILLEGAL

FUNCTION TRUTH TABLE (Table1) (2/2)

Current State	/CS	/RAS	/CAS	/WE	BA	ADDR	Action
Precharge	H	X	X	X	X	X	NOP → Idle after t_{RP}
	L	H	H	H	X	X	NOP → Idle after t_{RP}
	L	H	H	L	BA	X	ILLEGAL [2]
	L	H	L	X	BA	CA	ILLEGAL [2]
	L	L	H	H	BA	RA	ILLEGAL [2]
	L	L	H	L	BA	A10	NOP [4]
	L	L	L	X	X	X	ILLEGAL
Write Recovery	H	X	X	X	X	X	NOP
	L	H	H	H	X	X	NOP
	L	H	H	L	BA	X	ILLEGAL [2]
	L	H	L	X	BA	CA	ILLEGAL [2]
	L	L	H	H	BA	RA	ILLEGAL [2]
	L	L	H	L	BA	A10	ILLEGAL [2]
	L	L	L	X	X	X	ILLEGAL
Row Active	H	X	X	X	X	X	NOP → Row Active after t_{RCD}
	L	H	H	H	X	X	NOP → Row Active after t_{RCD}
	L	H	H	L	BA	X	ILLEGAL [2]
	L	H	L	X	BA	CA	ILLEGAL [2]
	L	L	H	H	BA	RA	ILLEGAL [2]
	L	L	H	L	BA	A10	ILLEGAL [2]
	L	L	L	X	X	X	ILLEGAL
Refresh	H	X	X	X	X	X	NOP → Idle after t_{RC}
	L	H	H	X	X	X	NOP → Idle after t_{RC}
	L	H	L	X	X	X	ILLEGAL
	L	L	H	X	X	X	ILLEGAL
	L	L	L	X	X	X	ILLEGAL
Mode Resister Access	H	X	X	X	X	X	NOP
	L	H	H	H	X	X	NOP
	L	H	H	L	X	X	ILLEGAL
	L	H	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	ILLEGAL

ABBREVIATIONS

RA = Row Address BA = Bank Address NOP = No Operation command

CA = Column Address AP = Auto Precharge

Notes:

1. All inputs will be enabled when CKE is set high for at least 1 cycle prior to the inputs.
2. Illegal to bank in specified state, but may be legal in some cases depending on the state of bank selection.
3. Satisfy the timing of I_{CCD} and t_{WR} to prevent bus contention.
4. NOP to bank precharging or in idle state. Precharges activated bank by BA or A10.
5. Illegal if any bank is not idle.

FUNCTION TRUTH TABLE (CKE) (Table2)

Current State(n)	CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	ADDR	Action
Self Refresh	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit Self Refresh → ABI
	L	H	L	H	H	H	X	Exit Self Refresh → ABI
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Self Refresh)
Power Down	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit Power Down → ABI
	L	H	L	H	H	H	X	Exit Power Down → ABI
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL [6]
	L	L	X	X	X	X	X	NOP (Continue power down mode)
All Banks idle [6] (ABI)	H	H	X	X	X	X	X	Refer to Table 1
	H	L	H	X	X	X	X	Enter Power Down
	H	L	L	H	H	H	X	Enter Power Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	H	L	X	ILLEGAL
	H	L	L	L	L	H	X	Enter Self Refresh
	H	L	L	L	L	L	X	ILLEGAL
	L	L	X	X	X	X	X	NOP
Any State Other than Listed Above	H	H	X	X	X	X	X	Refer to Operations in Table 1
	H	L	X	X	X	X	X	Begin Clock Suspend Next Cycle
	L	H	X	X	X	X	X	Enable Clock of Next Cycle
	L	L	X	X	X	X	X	Continue Clock Suspension

Notes:

6. Power-down and self refresh can be entered only when all the banks are in an idle state.