OKI

ML670100 EVA BOARD

User's Guide (preliminary)

Oki ARM7TDMI Emulation Kit

Third edition: Aug 1998

ARM POWERED ™

Oki Electric Industry Co.,Ltd.

Notes

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Contents

1 Read Me First

This Chapter lists the procedures to be followed when the Oki ARM7TDMI Emulation Kit is first unpacked. Read it thoroughly before applying power to the Oki ML670100 evaluation board.

1.1 Using this Product Safely and Properly

This User's Guide uses various labels and icons that serve as your guides to operating this product safely and properly so as to prevent death, personal injury, and property damage. The following table lists these labels and their definitions.

Labels

 **Warning**	**This label indicates precautions that, if ignored or otherwise not completely followed, could lead to death or serious personal injury.**
 **Caution**	**This label indicates precautions that, if ignored or otherwise not completely followed, could lead to personal injury or property damage.**

Icons

A triangular icon draws your attention to the presence of a hazard. The illustration inside the triangular frame indicates the nature of the hazard--in this example, an electrical shock hazard.

A circular icon with a solid background illustrates an action to be performed. The illustration inside this circle indicates this action--in this example, disconnecting the power supply.

A circular icon with a crossbar indicates a prohibition. The illustration inside this circle indicates the prohibited action--in this example, disassembly.

1.2 Important Safety Notes

Please read this page before using the product.

Warning	
Use only the specified voltage. Using the wrong voltage risks fire and electrical shock.	
At the first signs of smoke, an unusual smell, or other problems, disconnect the power plug and unplug all external power cords. Continued use risks fire and electrical shock.	
Do not use the product in an environment exposing it to moisture or high humidity. Such exposure risks fire and electrical shock.	
Do not pile objects on top of the product. Such pressure risks fire and electrical shock.	
At the first signs of breakdown, immediately stop using the product, disconnect the power plug, and unplug all external power cords. Continued use risks fire and electrical shock.	

Please read this page before using the product.

Caution

Do not use this product on an unstable or inclined base as it can fall or overturn, producing injury.

Do not use this product in an environment exposing it to excessive vibration, strong magnetic fields, or corrosive gases. Such factors can loosen or even disconnect cable connectors, producing a breakdown.

Do not use this product in an environment exposing it to temperatures outside the specified range, direct sunlight, or excessive dust. Such factors risk fire and breakdown.

Use only the cables and other accessories provided. Using non-compatible parts risks fire and breakdown.

Always observe the specified order for turning equipment on and off. Using the incorrect order risks fire and breakdown.

Do not use the cables and other accessories provided with other systems. Such improper usage risks fire.

Always turn off the power before connecting or disconnecting cables or other accessories. Such improper usage risks fire and breakdown.

1.3 Notations

This User's Guide uses the following labels for material that complements the main text.

[Caution]	This notation introduces material requiring special attention.
[Reference]	This notation introduces related material found elsewhere in this User's Guide.
[Example]	This notation introduces an example illustrating the discussion.
(See Note n.)	This notation introduces a reference to a numbered note providing supplementary information lower on the same page.
[Note n]	This notation introduces a numbered note providing supplementary information.

1.4 For Further Information

Thank you for choosing the Oki ARM7TDMI Emulation Kit.

Please direct any questions or comments that you may have to your Oki distributor or the nearest Oki Electric Sales Office.

1.5 Packing List

When you first unpack your Oki ARM7TDMI Emulation Kit, check that the package contains all the components shown in the following Figure.

Although every effort has been made to minimize damage and eliminate mistakes, please report any damage or missing parts to your Oki distributor or the nearest Oki Electric Sales Office.

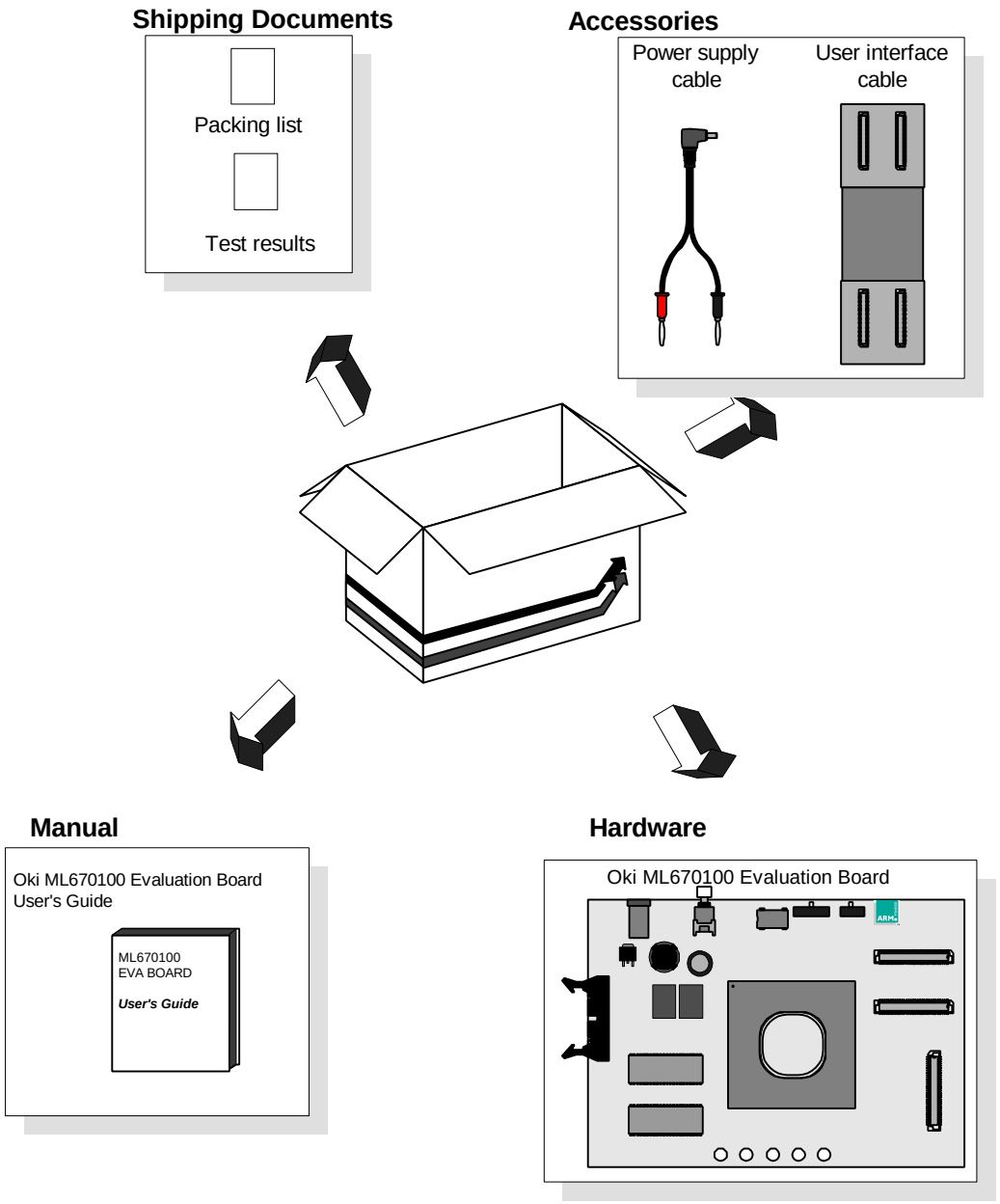
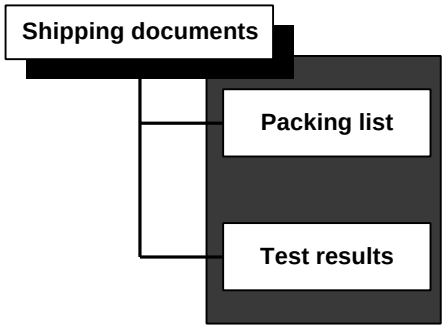
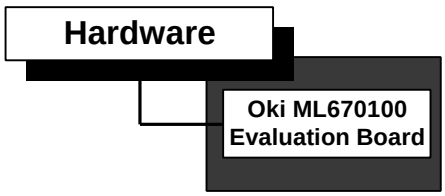


Figure 1-1 Package Contents

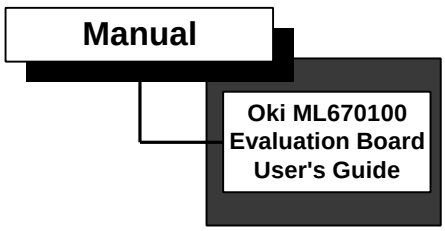


This document lists the contents of the Oki ARM7TDMI Emulation Kit. Check the package contents against this list.

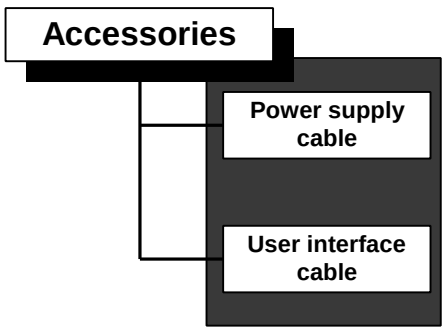
This document reports the results of tests conducted on the Oki ML670100 evaluation board prior to shipping.



This board is the key component of the kit.



Oki ARM7TDMI Emulation Kit User's Guide: This document, the manual that you are now reading, describes the Oki ARM7TDMI Emulation Kit in full.



This cable is for connecting the Oki ML670100 evaluation board to the system power supply (5 V DC +/- 5%).

This cable is for communicating between the Oki ML670100 evaluation board and the user application program.

2 Overview

This Chapter provides an overview of the Oki ML670100 evaluation board, its components, and its functions.

2.1 What is it?

The Oki ML670100 evaluation board is part of the Oki ARM7TDMI Emulation Kit for developers debugging and evaluating embedded systems built around the Oki ML670100 32-bit single-chip microcontroller.

The board links to the ARM Software Development Support Toolkit via an EmbeddedICE or Multi-ICE Interface Unit from ARM Limited to form a complete debugging system for user application programs.

The board contains an evaluation chip that emulates the target device, the Oki ML670100 microcontroller. This chip features the same CPU core, memory spaces, onboard peripherals, and I/O pins (See Note 1.) as the ML670100. Instead of running the user application program from a built-in ROM, however, it uses RAM as a rewritable emulation memory.

The following Figure gives a block diagram for this board.

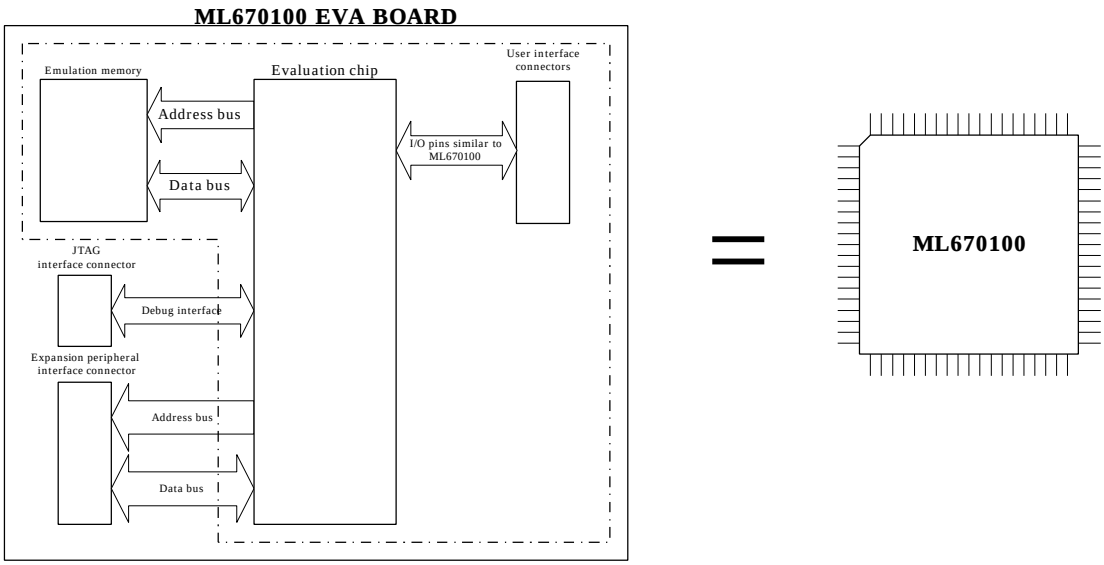


Figure 2-1 Oki ML670100 Eva Board Block Diagram

[Note 1]

The only onboard ML670100 peripheral that the board cannot emulate is PIO8. For further details, see Chapter 6 "Important Usage Notes."

The board provides access to the evaluation chip's I/O pins via the user interface connectors. Connect these to the user application program with the supplied user interface cable for debugging while connected to the embedded system.

2.2 Program Development Support System Components

The following Figure lists the components making up the Oki ARM7TDMI program development support system.

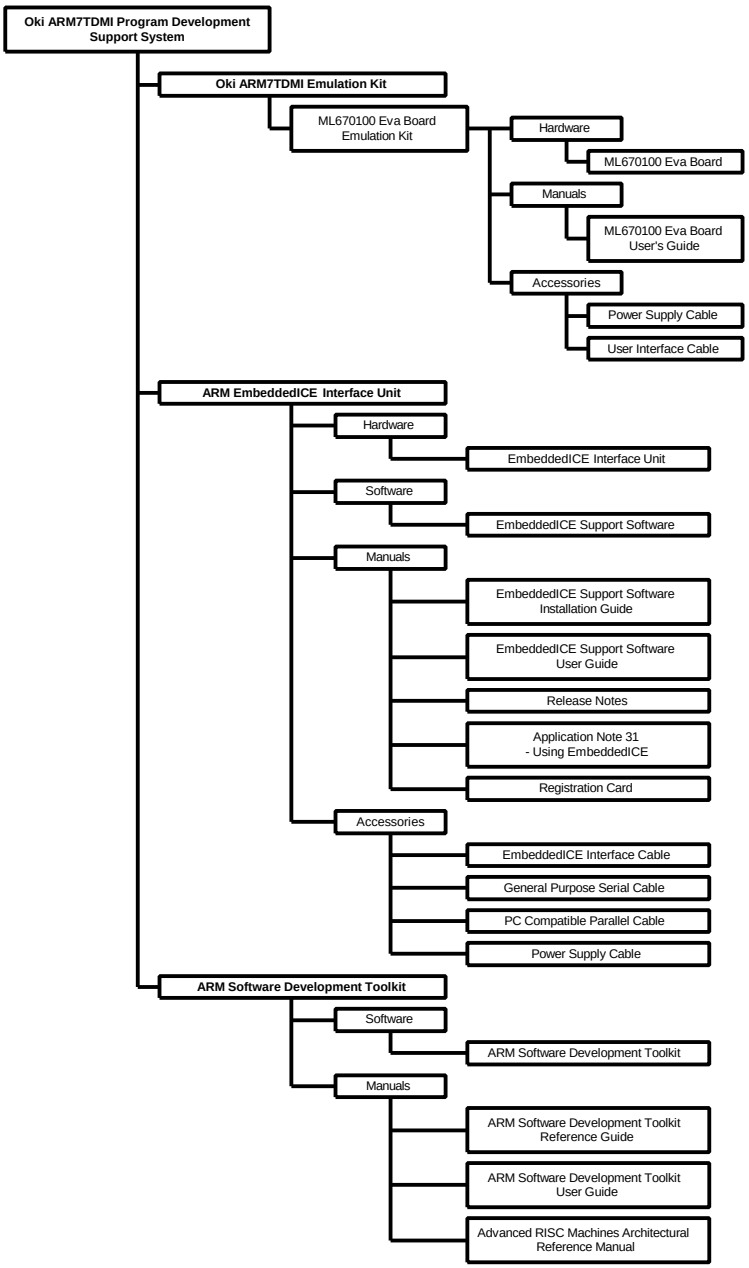


Figure 2-2 Program Development Support System Components

Oki ARM7TDMI Program Development Support System

This term covers all hardware and software provided by Oki Electric and ARM Limited. For further details, see the Oki ARM7TDMI Program Development Support System Reference Manual.

Oki ARM7TDMI Emulation Kit

This term covers all support hardware and software used in program development for the ARM7TDMI core. The Oki ML670100 evaluation board falls into this category.

Oki ML670100 evaluation board Emulation Kit

This term covers all support hardware, software, and accessories used in program development for the Oki ML670100 32-bit single-chip microcontroller.

Oki ML670100 evaluation board

This hardware is for real-time evaluation of the Oki ML670100 32-bit single-chip microcontroller and Oki's general-purpose peripherals. This and other documentation sometimes refers to it simply as the board.

Power Supply Cable

This cable is for connecting the Oki ML670100 evaluation board to the system power supply (5 V DC ±5%).

ARM EmbeddedICE Interface Unit

This hardware provides an interface between the ARM Software Development Support Toolkit and the Oki ML670100 evaluation board.

EmbeddedICE Support Software

This consists of the debugger, armsd, shipped on 3.5-inch floppy disks in either MS-DOS or UNIX® format.

EmbeddedICE Support Software Installation Guide

This guide explains how to install the appropriate version of the debugger, armsd, for the EmbeddedICE version.

EmbeddedICE Support Software User Guide

This guide describes controlling the EmbeddedICE Interface Unit from the debugger, armsd.

Release Notes

These describe safety precautions for the EmbeddedICE Interface Unit.

Registration Card

This is for registering the EmbeddedICE Interface Unit.

ARM Software Development Support Toolkit (ARM SDT)

This package contains the ARM Project Manager and other tools for ARM software development. It is available on CD–ROM or MO disc. This and other documentation sometimes abbreviates the Software Development Toolkit portion to SDT.

ARM Software Development Support Toolkit Reference Guide

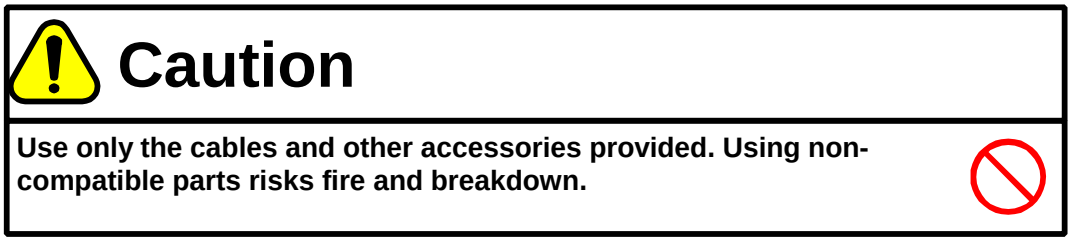
This is the reference manual for the ARM SDT. It describes the functions of the various tools, calling syntax for standard procedures, and file formats. This and other documentation sometimes abbreviates the title to “ARM SDT Reference Manual.”

ARM Software Development Support Toolkit User Guide

This is your guide to the ARM SDT. It gives procedures and examples for developing and debugging user application programs. This User’s Guide sometimes abbreviates the title to “ARM SDT User Guide.”

ARM Limited Architectural Reference Manual

This is the reference manual for the ARM architecture.



2.3 Main Components

This Section shows the layout of the Oki ML670100 evaluation board and describes the main components.

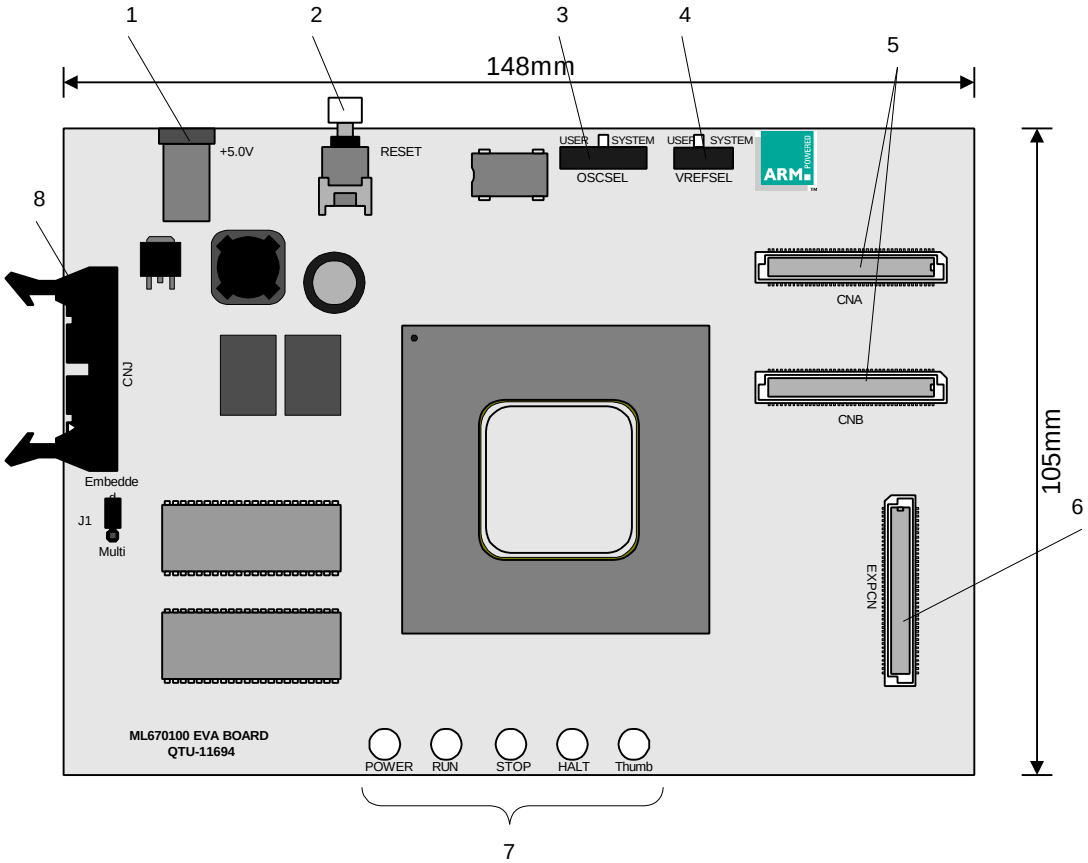


Figure 2-3 Oki ML670100 Eva Board Layout

[1] DC connector

This connector supplies the board with its system power supply. Connect it to the specified power supply (5 V DC +/-5%, 2.5 A) with the supplied power supply cable.

[2] System reset switch (RESET)

Pressing this switch produces a system reset for the board.

[3] Clock selector (OSCSEL) switch

This switches the CPU operating clock between an internal oscillator circuit that quadruples an internal 8-MHz oscillation with a phase-locked loop and an external clock signal from an oscillator circuit in the user application system.

[4] Vref selector (VREFSEL) switch

This switches the reference voltage for the built-in analog-to-digital converter between an internal 3.3 V and one from the user application system.

[5] User interface connectors (CNA and CNB)

These are for connecting the evaluation chip pins to the user application system with the included user interface cable.

[6] Expansion peripheral interface connector (EXPCN)

These are for connecting expansion peripherals to the evaluation chip with the optional expansion peripheral cable.

[7] Indicators

These LEDs give the board's operating status.

[8] ICE interface connector (CNJ)

This is for connecting an EmbeddedICE or Multi-ICE interface unit for communicating with the development host.

2.4 Main Functions

This Section describes the main functions of the Oki ML670100 evaluation board.

2.4.1 Remote Debugging

One function of the Oki ML670100 evaluation board is debugging a user application program by linking the board via an EmbeddedICE or Multi-ICE Interface Unit to a computer running armsd and other components of the ARM Software Development Support Toolkit.

The following Figure shows the cable connections for this configuration.

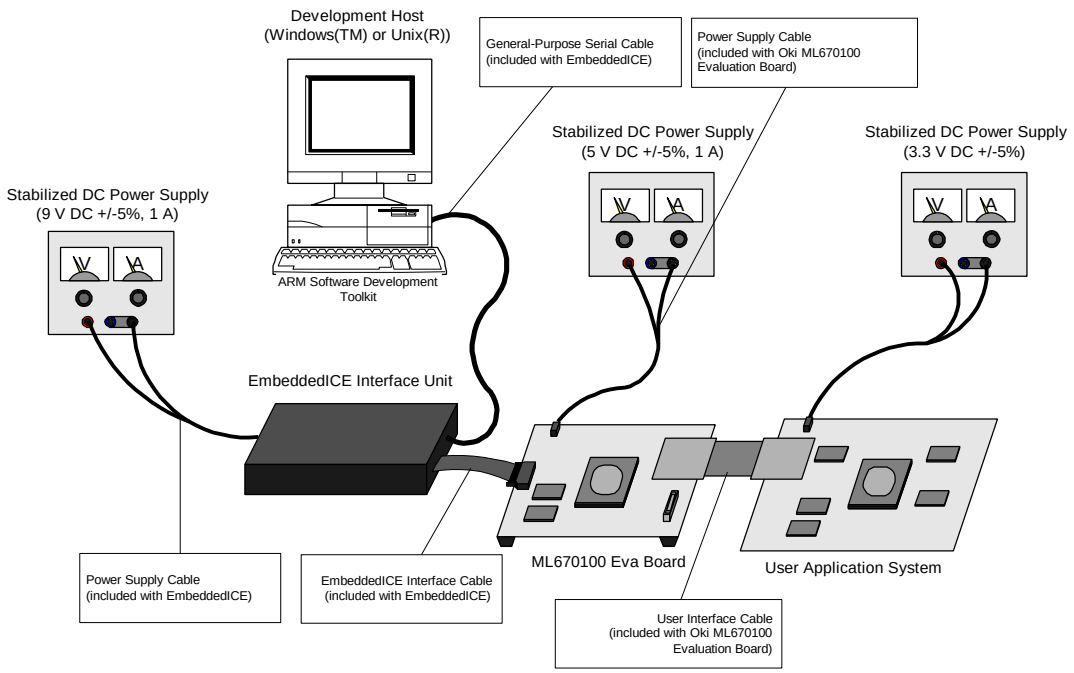


Figure 2-4 Connecting Cables for Remote Debugging

For the related procedures, see Section 3.6 “Setting Up for Remote Debugging.”

2.4.2 Expansion Peripherals

The expansion peripheral interface connector (EXPCN) provides a means for connecting additional peripherals to the evaluation chip on the board. Simply connect it to the expansion peripheral evaluation board with the cable included with the latter. The peripherals on the expansion peripheral evaluation board then appear as onboard peripherals.

2.4.3 Indicators (POWER, ERROR, BUSY, and RUN)

The Oki ML670100 evaluation board has four LEDs that give the operating status. For the locations, see the Figure in Section 2.3 "Main Components."

This Section lists their functions.

POWER (red): This LED indicates the status of the Oki ML670100 evaluation board's power supply. It lights when the board is receiving the proper voltage.

RUN (green): This LED indicates the operating state of the Oki ML670100 evaluation board. It lights during real-time emuation.

STOP (yellow): This LED indicates the status of the evaluation chip on the board. It lights when the CPU is in STOP mode.

HALT (greenish yellow): This LED indicates the status of the evaluation chip on the board. It lights when the CPU is in HALT mode.

Thumb (orange): This LED indicates the status of the evaluation chip

on the board. It lights when the CPU is in Thumb mode.

2.5 Hardware Specifications

The Oki ML670100 evaluation board has the following specifications.

System CPU:	ML670100
Internal program memory:	256 kilobytes
Internal data memory (RAM):	8 kilobytes
Peripherals:	Most ML670100 peripherals (See Note 2.)
Expansion peripheral slot:	One (EXPCN connector)
User interfaces:	One (CNA and CNB connectors)
Other:	Clock selector (OSCSEL) switch, Vref selector (VREFSEL) switch, and five indicator LEDs

[Note 2]

The only onboard ML670100 peripheral that the board cannot emulate is PIO8. For further details, see Chapter 6 "Important Usage Notes."

3 Setup and Operation

This Chapter describes the procedures for setting up and operating the Oki ML670100 evaluation board.

3.1 Operating Conditions

Use the Oki ML670100 evaluation board only in environments satisfying the following conditions.

Oki ML670100 Eva Board Operating Conditions	
Item	**Description**
System input power voltage [rating]	DC +5V +/-5% [DC +5V]
Maximum current drain	1 A
Environmental conditions	Operating temperature: 5 to 35°C Operating humidity: 40 to 60%

Note that the board has the following dimensions and weight.

Oki ML670100 Eva Board Dimensions and Weight	
Item	**Description**
Dimensions	105(W)×148(D) ×30(H) [mm]
Weight	approximately 0.1 kg

3.2 Switches and Settings

The following Figure shows the switches controlling Oki ML670100 evaluation board operation. This Section describes their uses.

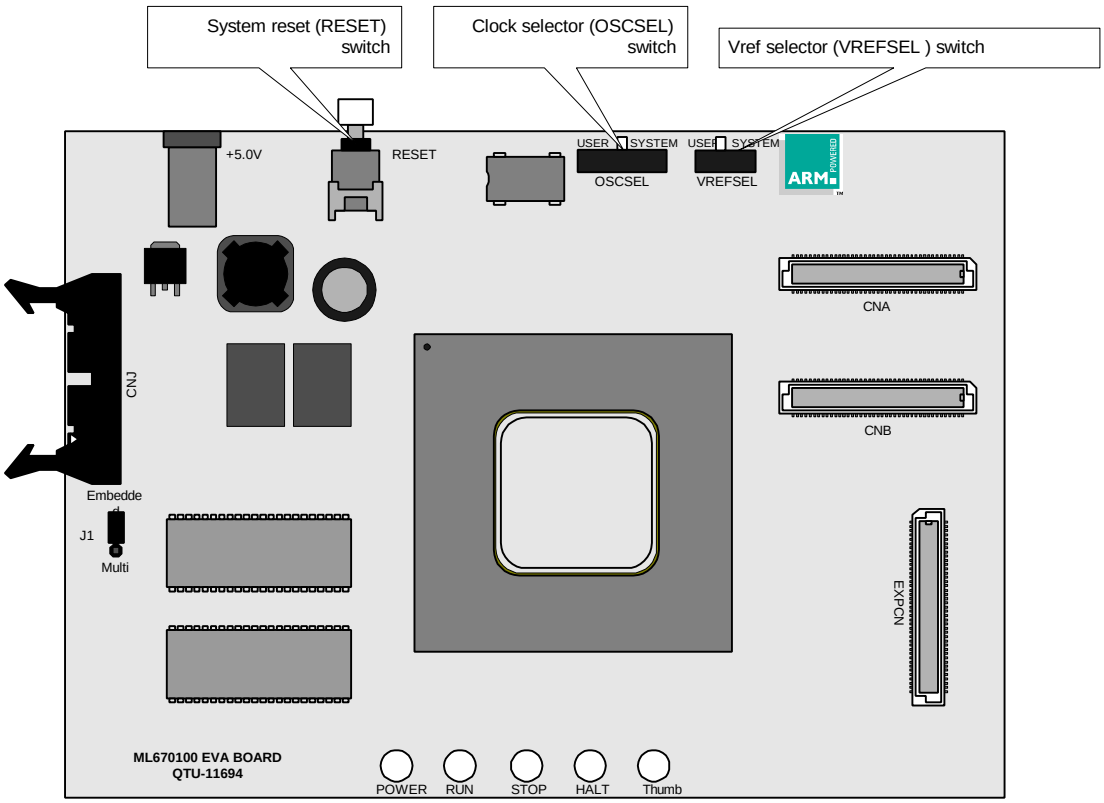


Figure 3-1 Oki ML670100 Eva Board Switches

3.2.1 System Reset (RESET) Switch

Pressing this switch resets the Oki ML670100 evaluation board.

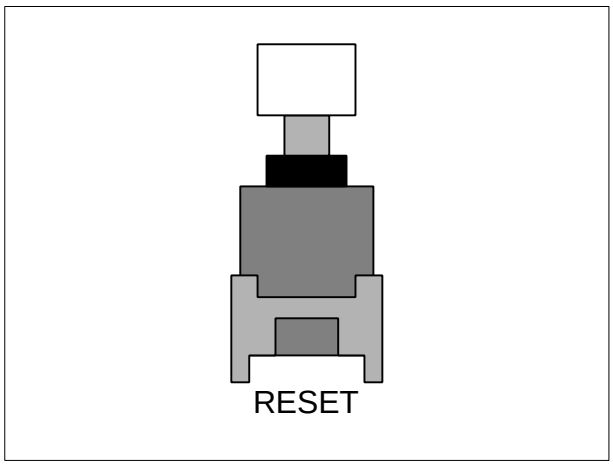


Figure 3-2 System Reset (RESET) Switch

The Oki ML670100 evaluation board has two types of reset:

- A power on reset produced by applying the power for the first time
- A system reset produced by pressing this push-button switch

Both types reset the evaluation chip on the board.

[Caution]

Do not press the system reset (RESET) switch during remote debugging because doing so also resets the in-circuit emulator interface, possibly breaking the link between the board and the ARM Software Development Support Toolkit running on the development host.

3.2.2 Clock Selector (OSCSEL) Switch

This switch offers two choices for the evaluation chip's CPU operating clock: an internal oscillator circuit and an external clock signal from an oscillator circuit in the user application system.

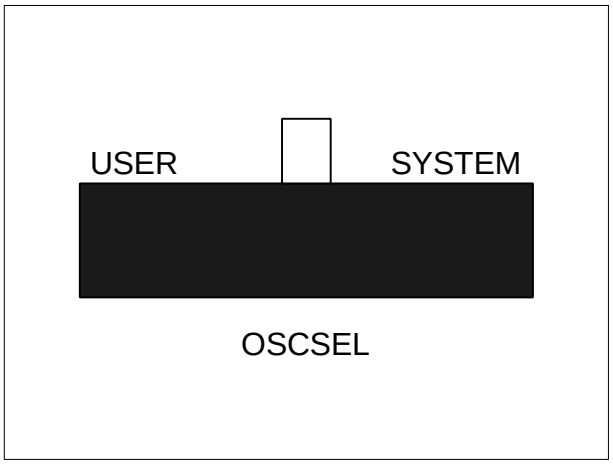


Figure 3-3 Clock Selector (OSCSEL) Switch

The SYSTEM position supplies an 8-MHz oscillation from an internal oscillator circuit to the OSC0 pin on the evaluation chip. The FSEL and PLLEN pins on the evaluation chip go to "High" level.

The USER position provides user access to the OSC0, FSEL, and PLLEN pins on the evaluation chip via the user interface connectors.

The following Figure shows the related circuitry.

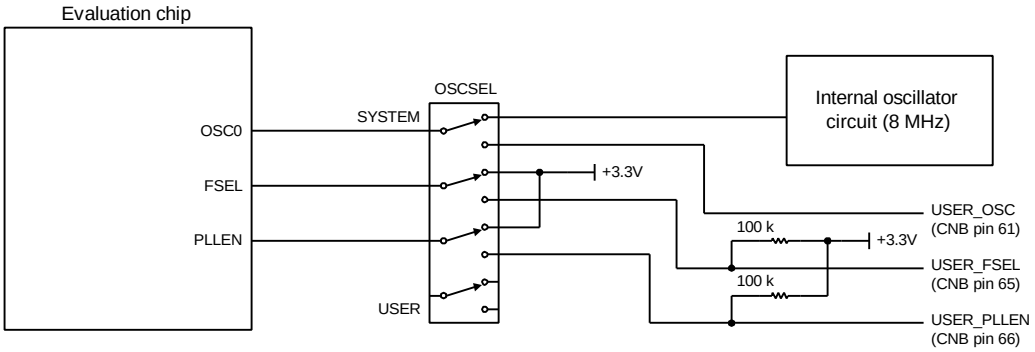


Figure 3-4 Clock Selector (OSCSEL) Switch Circuitry

Note how the USER_FSEL and USER_PLLEN pins (connected to the FSEL and PLLEN pins on the evaluation chip, respectively) include 100-kΩ pull-up resistors.

The USER position prevents access to the internal oscillator circuit. The user application system must therefore provide the USER_OSC pin (and thus the OSC0 pin on the evaluation chip) a clock signal with a guaranteed duty.

3.2.3 Vref Selector (VREFSEL) Switch

This switch offers two choices for the reference voltage (Vref) for the evaluation chip's built-in analog-to-digital converter: an internal 3.3 V and one from the user application system. (Note that the latter must be greater than that at GND and not exceed VDD.)

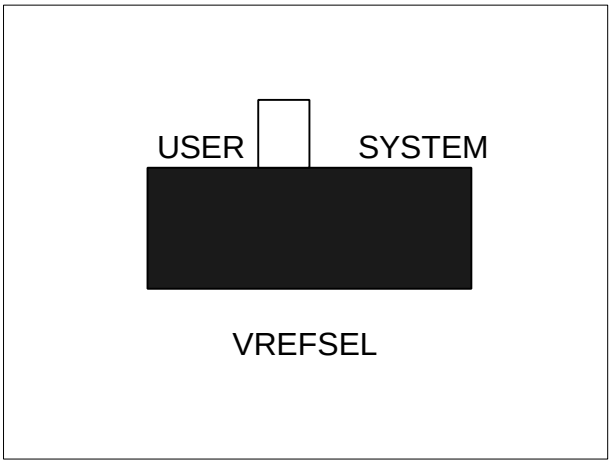


Figure 3-5 Vref Selector (VREFSEL) Switch

The SYSTEM position supplies an internal 3.3-V level to the Vref pin on the evaluation chip (the equivalent of the pin with the same name on the ML670100).

The USER position provides user access to the Vref pin on the evaluation chip via the USER-Vref pin on the user interface connectors.

The following Figure shows the related circuitry.

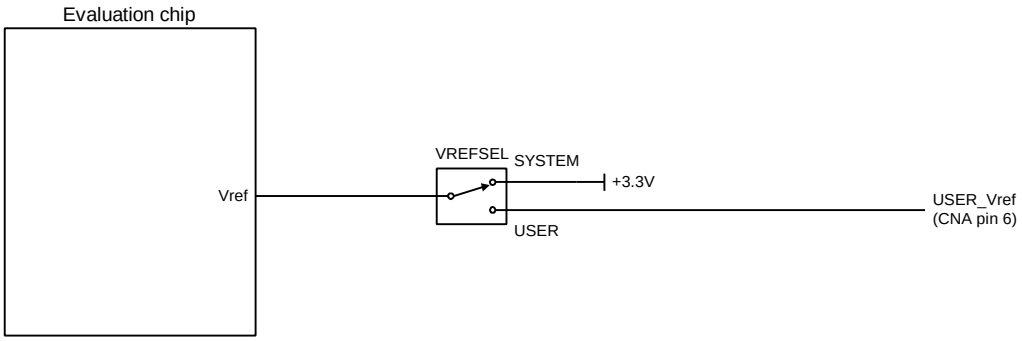


Figure 3-6 Vref Selector (VREFSEL) Switch Circuitry

3.3 Connecting Power Supply Cable

The following Figure shows the power cable shipped with the Oki ML670100 evaluation board.

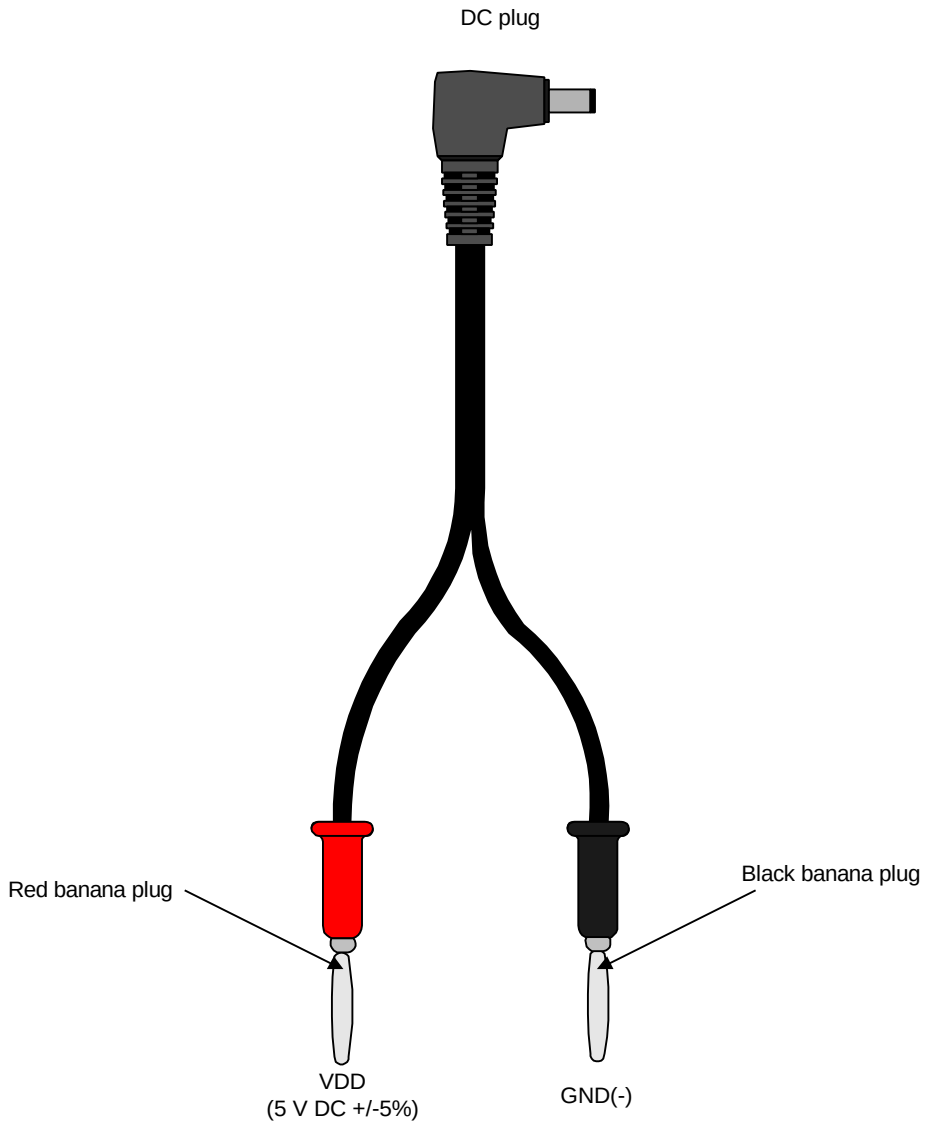


Figure 3-7 Power Supply Cable

Supply power to the board by connecting it with this cable to a stabilized DC power supply (5 V DC ±5%).

Below are the procedures for connecting both ends of this cable.

[1] Connect the cable to the board's DC connector.

Fit the plug end of the power supply cable into the DC connector in the upper left corner of the Oki ML670100 evaluation board.

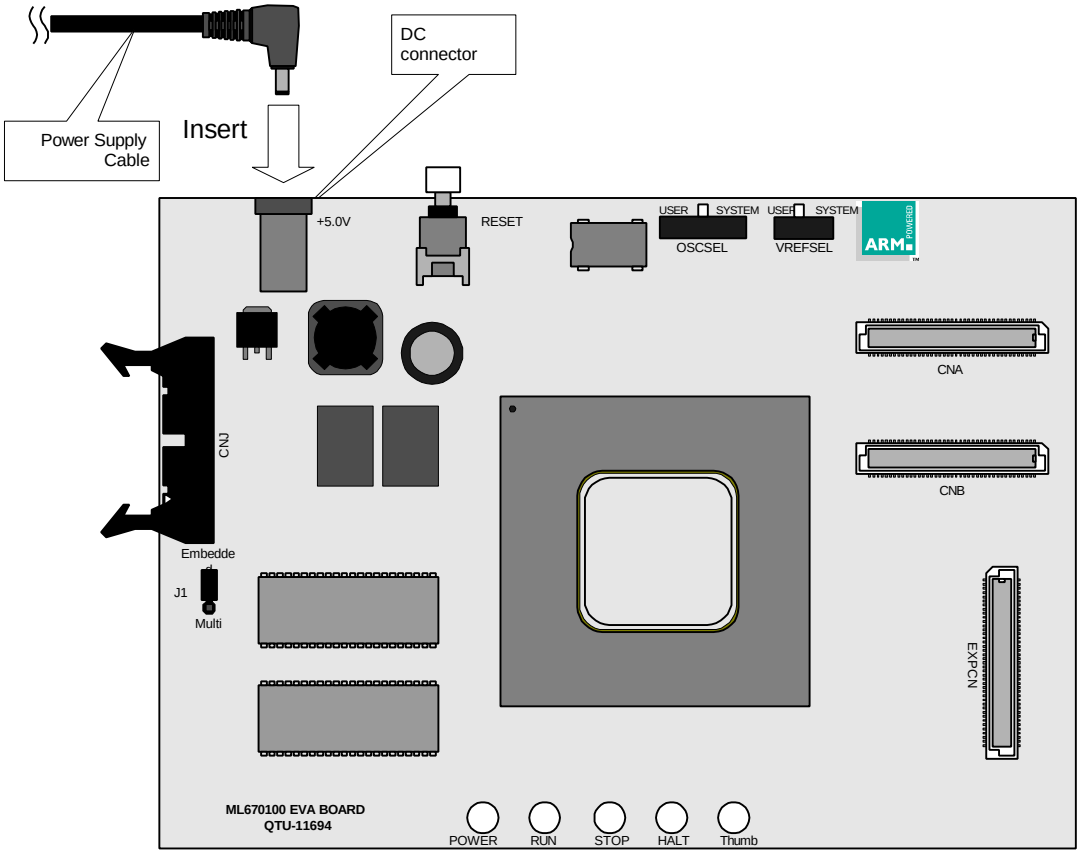


Figure 3-8 Connecting Power Supply Cable 1/2

[2] Connect the banana plugs to a stabilized DC power supply.

Connect the red banana plug to the stabilized DC power supply's plus outlet and the black one to the minus outlet. Double-check to make sure that the connections are not reversed.

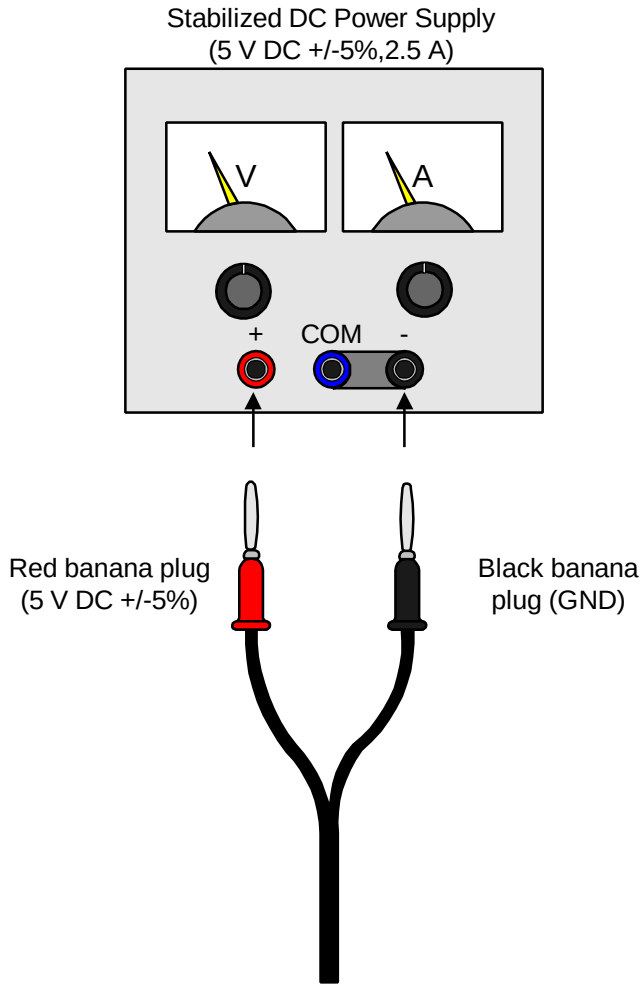


Figure 3-9 Connecting Power Supply Cable 2/2

Warning

Make sure that the banana plugs go into the correct outlets. Reversing the polarity leads to breakdown or fire and risks electrical shock.

3.4 Connecting User Interface Cable

The user interface cable included with the Oki ML670100 evaluation board is for connecting the I/O pins on the evaluation chip to the user application system.
The following Figure shows its external appearance.

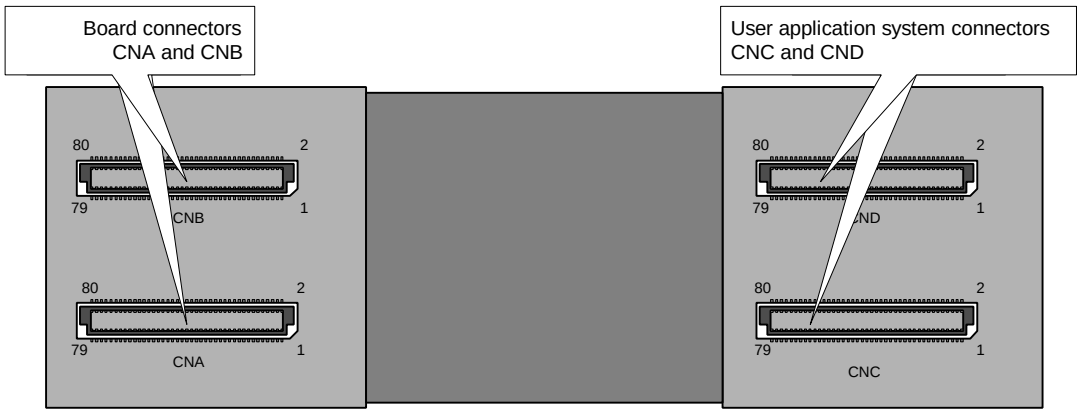


Figure 3-10 User Interface Cable

The cable has a total of four interface connectors: two each for the Oki ML670100 evaluation board and the user application system. The connectors labeled CNA and CNB plug into their counterparts on the Oki ML670100 evaluation board; CNC and CND are for the user application system.

Below are the procedures for connecting both ends of this cable.

[1] Connect CNA and CNB to the board.

Plug the connectors labeled CNA and CNB into their counterparts on the Oki ML670100 evaluation board.

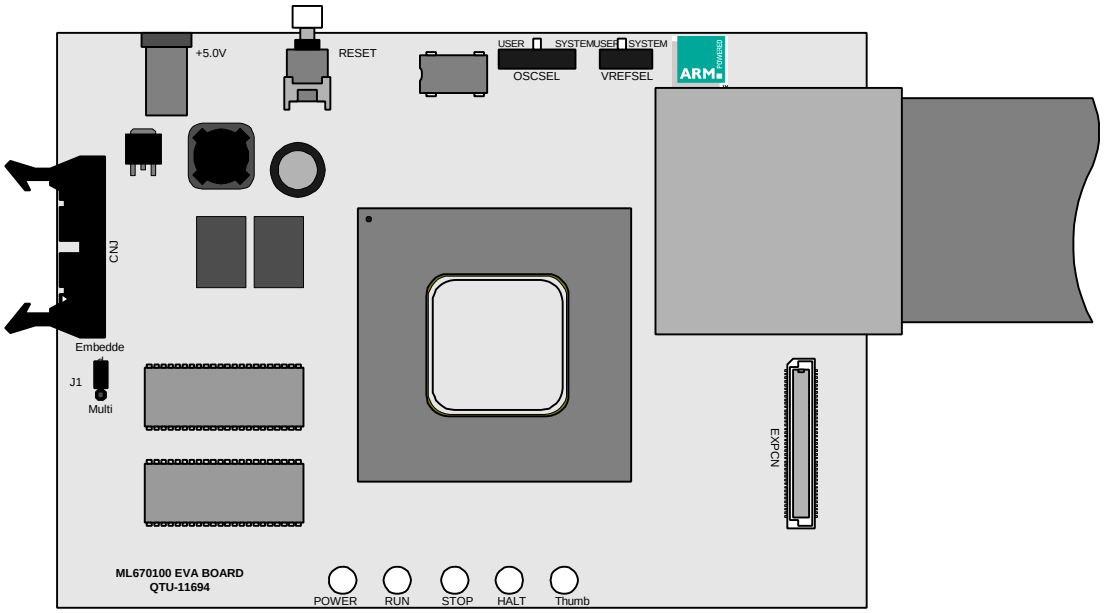


Figure 3-11 Connecting User Interface Cable 1/2

[2] Connect CNC and CND to the board.

Plug the connectors labeled CNC and CND into their counterparts on the user application system.

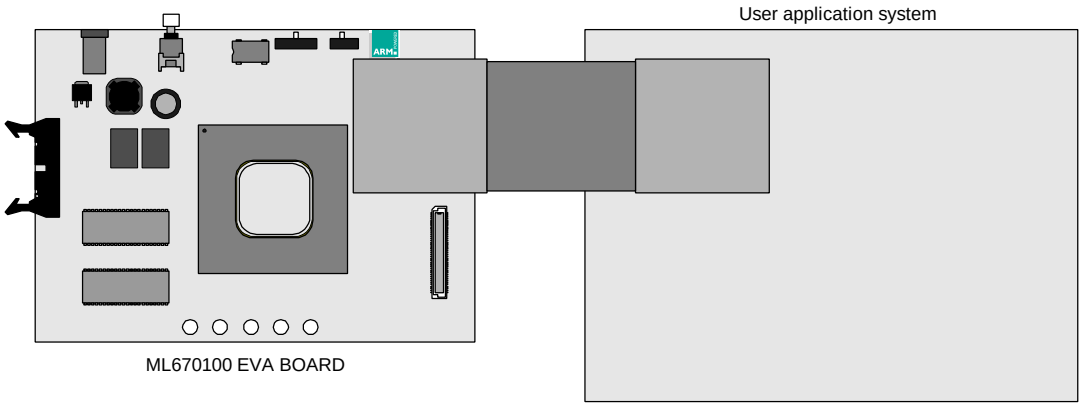


Figure 3-12 Connecting User Interface Cable 2/2

For further information on user interface cable pin assignments and circuitry, see the corresponding sections in Chapters 4 "User System Interface" and 7 "Appendices."

3.5 Connecting to In-Circuit Emulator

Connecting the Oki ML670100 evaluation board to an EmbeddedICE or Multi-ICE Interface Unit from ARM Limited permits communications with the development host.

The connection point is the ICE interface connector (CNJ) on the left side of the board.

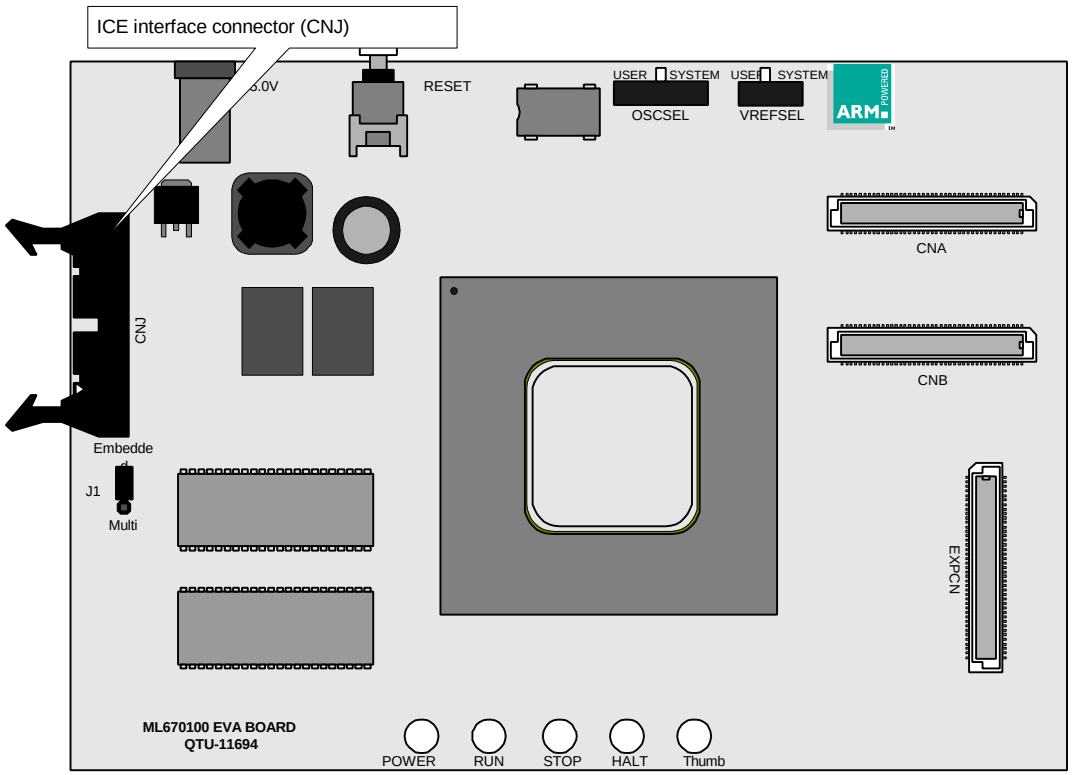


Figure 3-13 ICE Interface Connector (CNJ)

Below are the procedures for connecting these interface units.

[1] Connect interface cable to CNJ.

Plug one end of the 14-pin interface cable supplied with the in-circuit emulator into the ICE interface connector (CNJ) on the board.

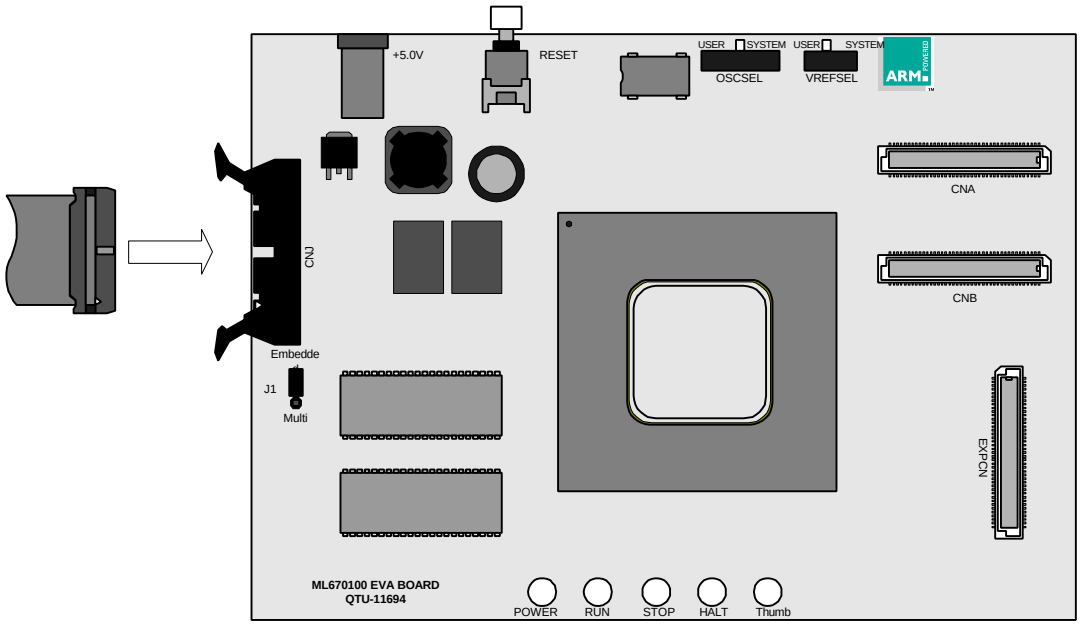


Figure 3-14 Connecting In-Circuit Emulator 1/2

After plugging in the connector, securing it firmly with the clamps. Failure to close the clamps can lead to a loose or broken connection.

[2] Connect interface cable to in-circuit emulator.

Connect the other end of the interface cable to the EmbeddedICE or Multi-ICE Interface Unit. The Figure below shows the connector on the former.

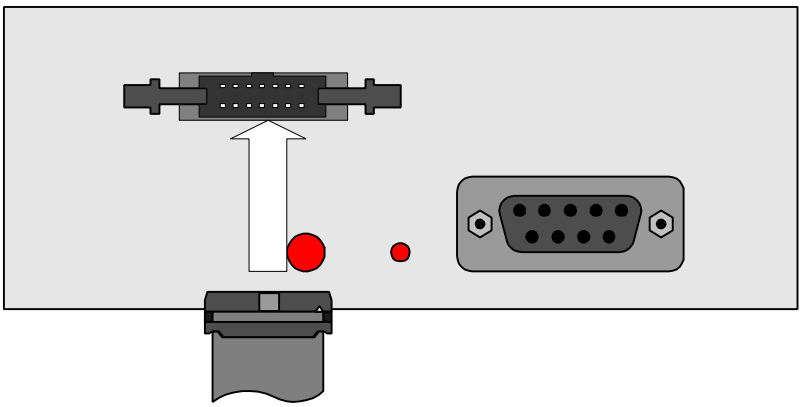


Figure 3-15 Connecting In-Circuit Emulator 2/2

For further details on the EmbeddedICE and Multi-ICE interface cables, refer to the User's Manual for the in-circuit emulator.

3.6 Setting Up for Remote Debugging

This Section describes the procedures for setting up for remote debugging. It assumes that the ARM Software Development Support Toolkit has already been installed. The examples use ARM Debugger for Windows, the Windows® version of this software, and the ARM EmbeddedICE Interface Unit as the interface to the Oki ML670100 evaluation board.

3.6.1 Necessary Items

Remote debugging with the Oki ML670100 evaluation board requires the following components.

- Oki ML670100 evaluation board
- ARM Software Development Support Toolkit running on the development host
- ARM EmbeddedICE Interface Unit
- Stabilized DC power supply (5 V DC ±5%, 1 A)
- Stabilized DC power supply (9 V DC ±5%, 1.0 A)
- Development host (Windows® or UNIX®)
- User application system
- User interface cable

Note: The last two items on the above list, the user application system and the user interface cable, are optional.

3.6.2 Connecting Cables

The following Figure shows all connections for the entire debugging system. For further details on a particular connection, see the corresponding Section earlier in this Chapter.

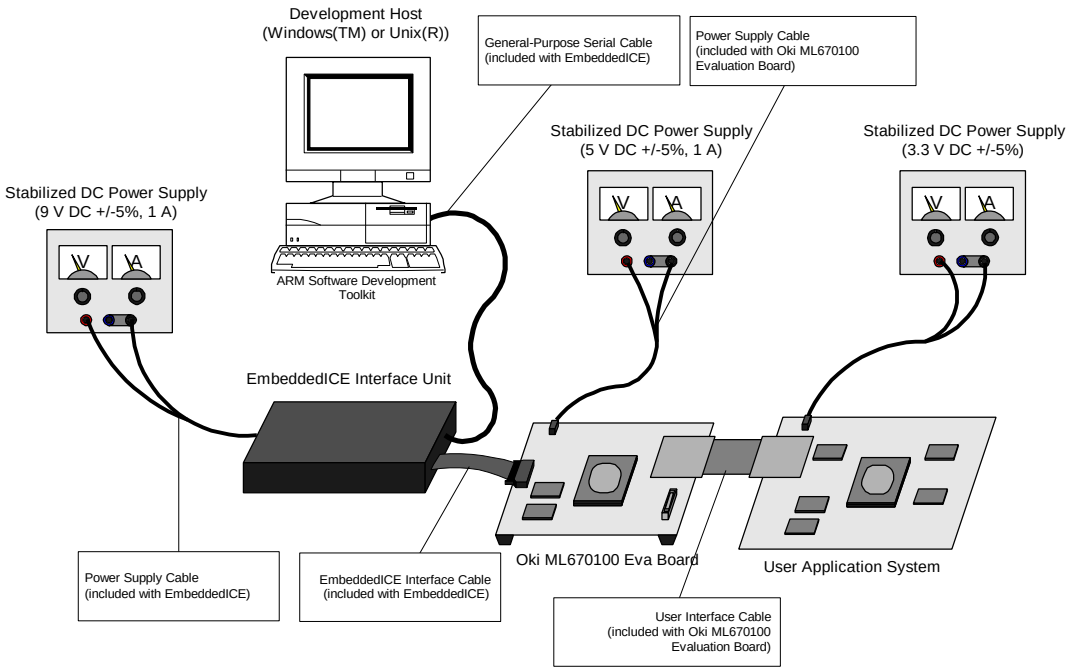


Figure 3-16 Connecting Cables for Remote Debugging

3.6.3 Checking Switch Settings

Make sure that the following selection switches are in the proper positions for remote debugging. Starting up the board with incorrect settings can lead to faulty operation or breakdown.

- Clock selector (OSCSEL) switch
- Vref selector (VREFSEL) switch

3.6.4 Applying Power

Apply the power to the EmbeddedICE or Multi-ICE Interface Unit, Oki ML670100 evaluation board, and, if present, the user application system.

Always apply the power in the order given.

3.6.5 Loading Debugger

On the development host, load the debugger.

The ARM Debugger for Windows defaults to ARMulator operation, so use the Options | Configure debugger... command to switch to remote debugging operation.

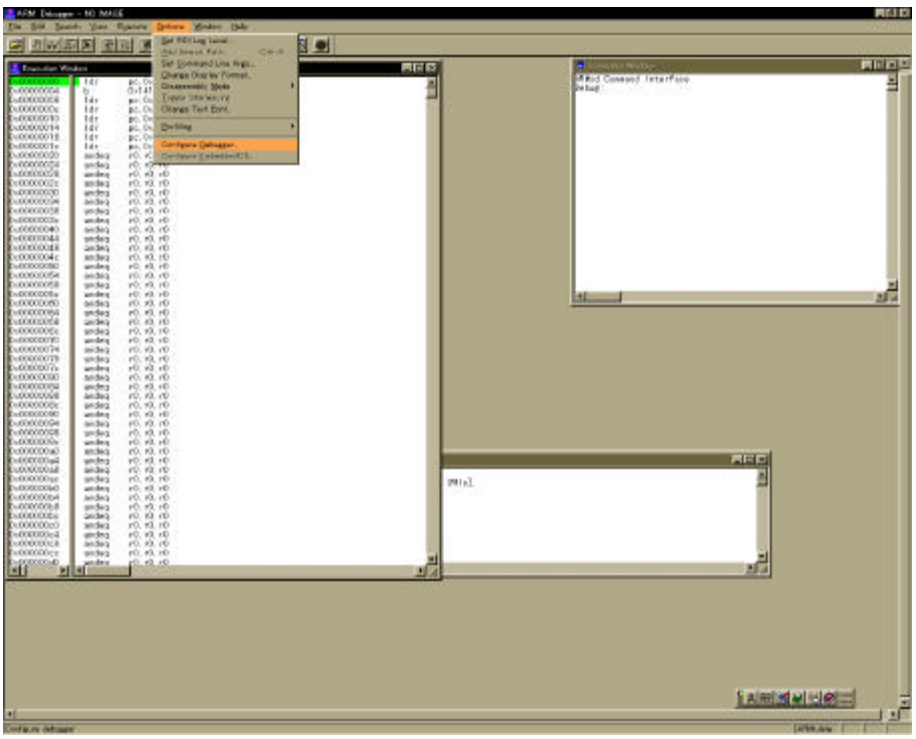


Figure 3-17 ARM Debugger for Windows Starting Screen

Select Remote_A from the list in the dialog box that appears.

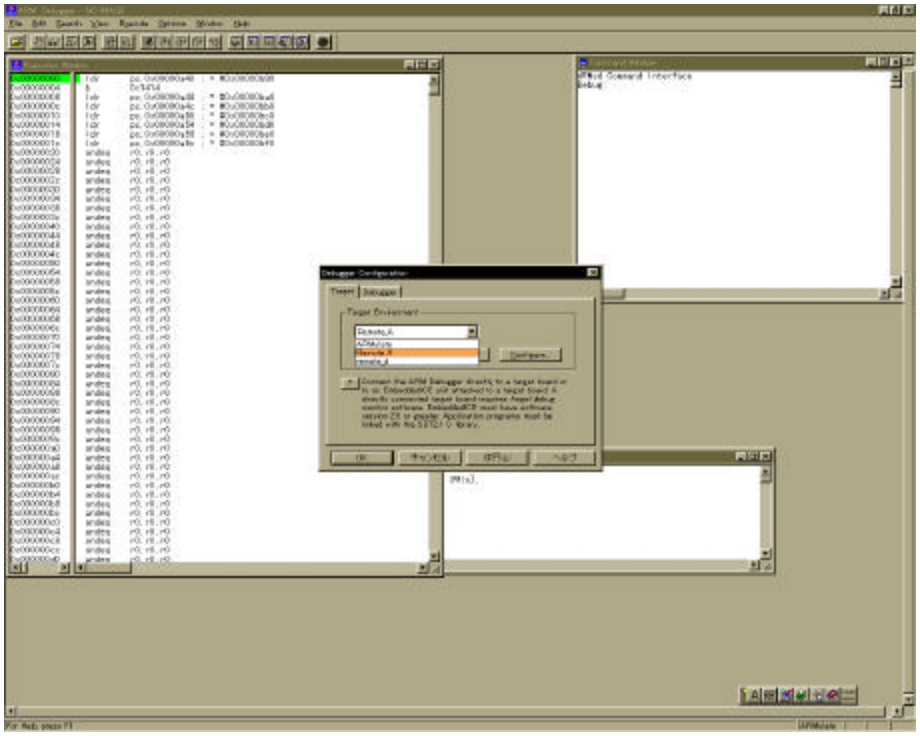


Figure 3-18 Debugger Configuration Dialog Box

Press the Configure button and set the serial port parameters in the dialog box that appears.

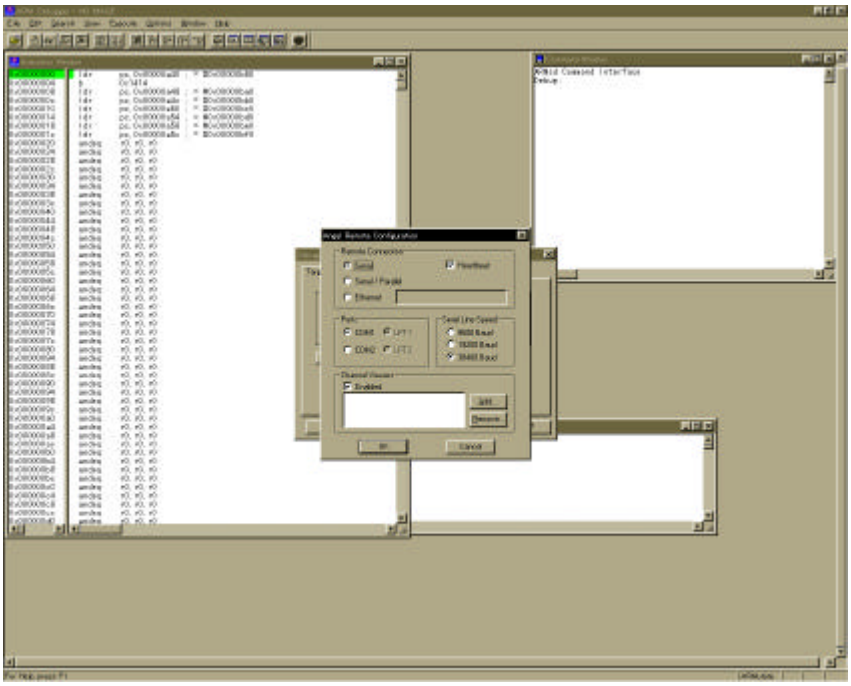


Figure 3-19 Serial Port Parameters Dialog Box

Once the debugger has established a link with the in-circuit emulator interface unit, the following screen appears.

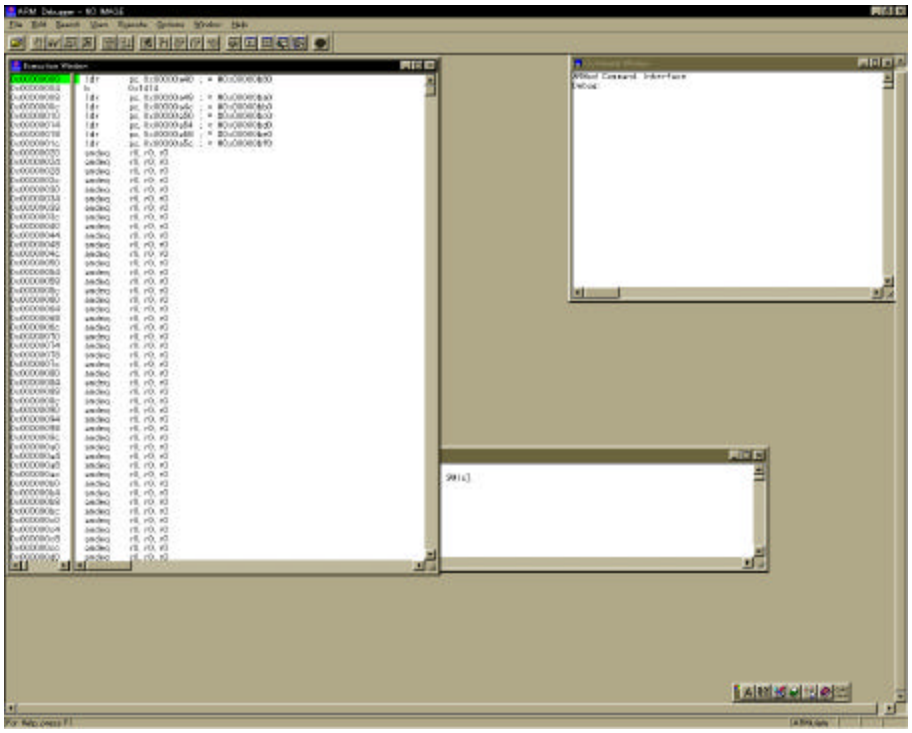


Figure 3-20 ARM Debugger for Windows

When linkage is complete, all LEDs but the POWER indicator go out.
The Oki ML670100 evaluation board is now ready for remote debugging.

For further details on remote debugging with the ARM Software Development Support Toolkit, see the ARM Software Development Support Toolkit User Guide.

4 User System Interface

This Chapter provides further particulars on the connection between the Oki ML670100 evaluation board and the user application system for debugging a user application program.

4.1 Overview

The evaluation chip on the Oki ML670100 evaluation board features the same CPU core, memory spaces, onboard peripherals, and I/O pins (See Note 1.) as the ML670100.

The board provides access to the evaluation chip's I/O pins via the user interface connectors. Connect these to the user application program with the user interface cable supplied for debugging while connected to the embedded system.

The following Figure gives a block diagram for this board.

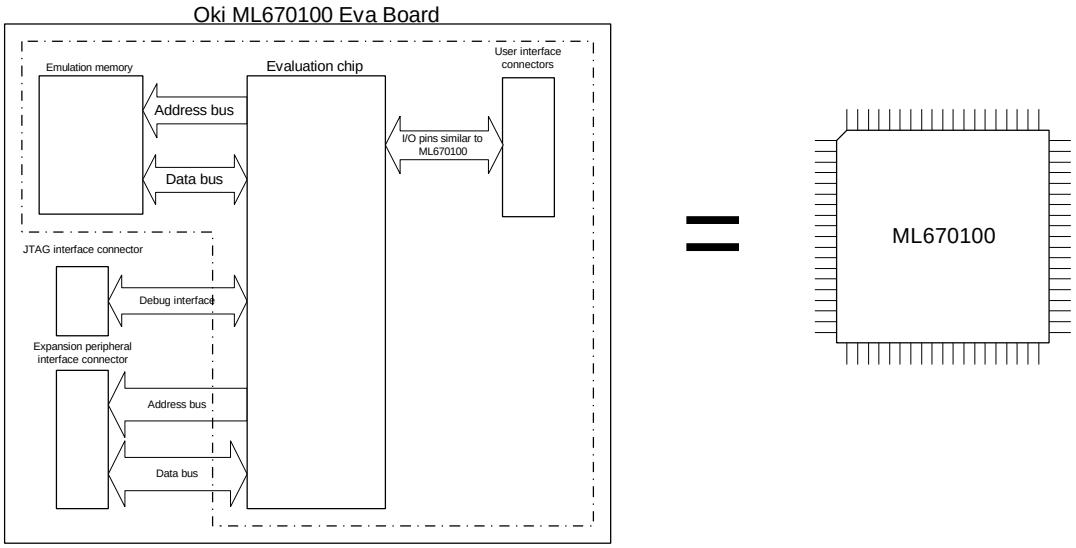


Figure 4-1 Oki ML670100 Eva Board Block Diagram

[Note 1]

The only onboard ML670100 peripheral that the board cannot emulate is PIO8. For further details, see Chapter 6 "Important Usage Notes."

4.2 User Interface Connectors

The user interface connectors (CNA and CNB) on the right side of the board are for connecting the evaluation chip pins to the user application system with the included user interface cable for overall system emulation.

The following Figure gives the connector location.

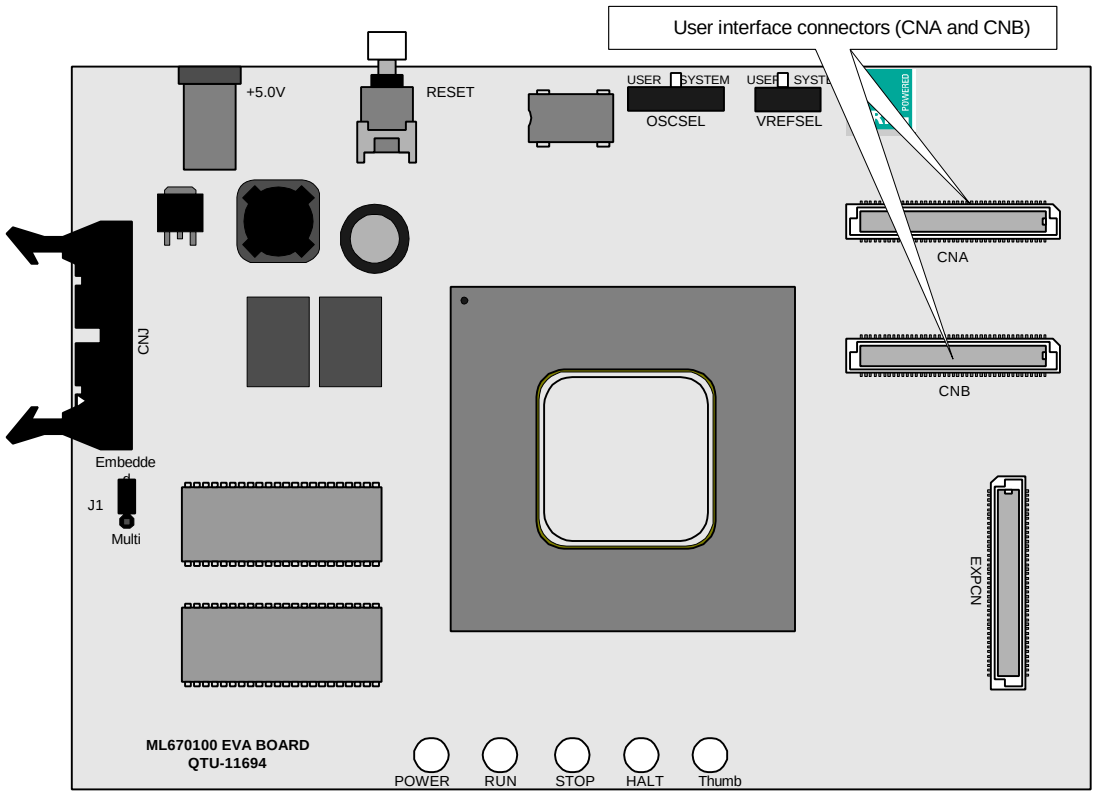


Figure 4-2 User Interface Connectors

The following two Tables give the pin assignments for the user interface connectors (CNA and CNB).

Table 4-1 Pin Assignments for User Interface Connector CNA

Pin Assignments for User Interface Connector CNA					
Pin	**Signal Name**	**I/O**	**Pin**	**Signal Name**	**I/O**
1	AI4	I	41	XA2	O
2	AI3	I	42	XA3	O
3	AI2	I	43	XA4	O
4	AI1	I	44	XA5	O
5	AI0	I	45	XA6	O
6	VREF	I	46	XA7	O
7	N.C.	-	47	GND	O
8	N.C.	-	48	N.C.	-
9	N.C.	-	49	XA8	O
10	DBSEL	I	50	XA9	O
11	PIO6.0	I/O	51	XA10	O
12	PIO6.1	I/O	52	XA11	O
13	PIO6.2	I/O	53	XA12	O
14	PIO6.3	I/O	54	XA13	O
15	PIO6.4	I/O	55	XA14	O
16	PIO6.5	I/O	56	XA15	O
17	PIO6.6	I/O	57	GND	O
18	PIO6.7	I/O	58	N.C.	-
19	PIO7.0	I/O	59	PIO0.0	I/O
20	PIO7.1	I/O	60	PIO0.1	I/O
21	PIO7.2	I/O	61	PIO0.2	I/O
22	GND	O	62	PIO0.3	I/O
23	N.C.	-	63	PIO0.4	I/O
24	PIO7.3	I/O	64	PIO0.5	I/O
25	PIO7.4	I/O	65	PIO0.6	I/O
26	PIO7.5	I/O	66	PIO0.7	I/O
27	PIO7.6	I/O	67	EFIQ/	I
28	PIO7.7	I/O	68	EA/	I
29	RESERVE0	-	69	GND	O
30	RESERVE1	-	70	N.C.	-
31	RESERVE2	-	71	XD0	I/O
32	RESERVE3	-	72	XD1	I/O
33	RESERVE4	-	73	N.C.	-
34	RESERVE5	-	74	N.C.	-
35	RESERVE6	-	75	N.C.	-
36	RESERVE7	-	76	N.C.	-
37	GND	O	77	GND	O
38	N.C.	-	78	GND	O
39	XA0	O	79	GND	O
40	XA1	O	80	GND	O

Table 4-2 Pin Assignments for User Interface Connector CNB

Pin Assignments for User Interface Connector CNB					
Pin	**Signal Name**	**I/O**	**Pin**	**Signal Name**	**I/O**
1	XD2	I/O	41	PIO4.0	I/O
2	XD3	I/O	42	PIO4.1	I/O
3	XD4	I/O	43	PIO4.2	I/O
4	XD5	I/O	44	PIO4.3	I/O
5	XD6	I/O	45	PIO4.4	I/O
6	XD7	I/O	46	PIO4.5	I/O
7	GND	O	47	PIO4.6	I/O
8	N.C.	-	48	PIO4.7	I/O
9	PIO1.0	I/O	49	GND	O
10	PIO1.1	I/O	50	N.C.	-
11	PIO1.2	I/O	51	PIO5.0	I/O
12	PIO1.3	I/O	52	PIO5.1	I/O
13	PIO1.4	I/O	53	PIO5.2	I/O
14	PIO1.5	I/O	54	PIO5.3	I/O
15	PIO1.6	I/O	55	PIO5.4	I/O
16	PIO1.7	I/O	56	PIO5.5	I/O
17	CS0/	O	57	PIO5.6	I/O
18	RD/	O	58	PIO5.7	I/O
19	WRE_WRL/	O	59	CLKOUT	O
20	GND	O	60	GND	I/O
21	N.C.	-	61	OSC0	I
22	PIO2.0	I/O	62	N.C.	-
23	PIO2.1	I/O	63	N.C.	-
24	PIO2.2	I/O	64	N.C.	-
25	PIO2.3	I/O	65	FSEL	I
26	PIO2.4	I/O	66	PLLEN	I
27	PIO2.5	I/O	67	RESET/	I
28	PIO2.6	I/O	68	GND	O
29	PIO2.7	I/O	69	GND	O
30	GND	O	70	AI7	I
31	N.C.	-	71	AI6	I
32	PIO3.0	I/O	72	AI5	I
33	PIO3.1	I/O	73	N.C.	-
34	PIO3.2	I/O	74	N.C.	-
35	PIO3.3	I/O	75	N.C.	-
36	PIO3.4	I/O	76	N.C.	-
37	PIO3.5	I/O	77	GND	O
38	PIO3.6	I/O	78	GND	O
39	PIO3.7	I/O	79	GND	O
40	GND	O	80	GND	O

The Oki ML670100 evaluation board provides the additional control circuitry shown in the following Figure between the user interface connectors (CNA and CNB) and the following evaluation chip pins: RESET/, PLLEN, FSEL, OSC0, VREF, DBSEL, EA/, and EFIQ/.

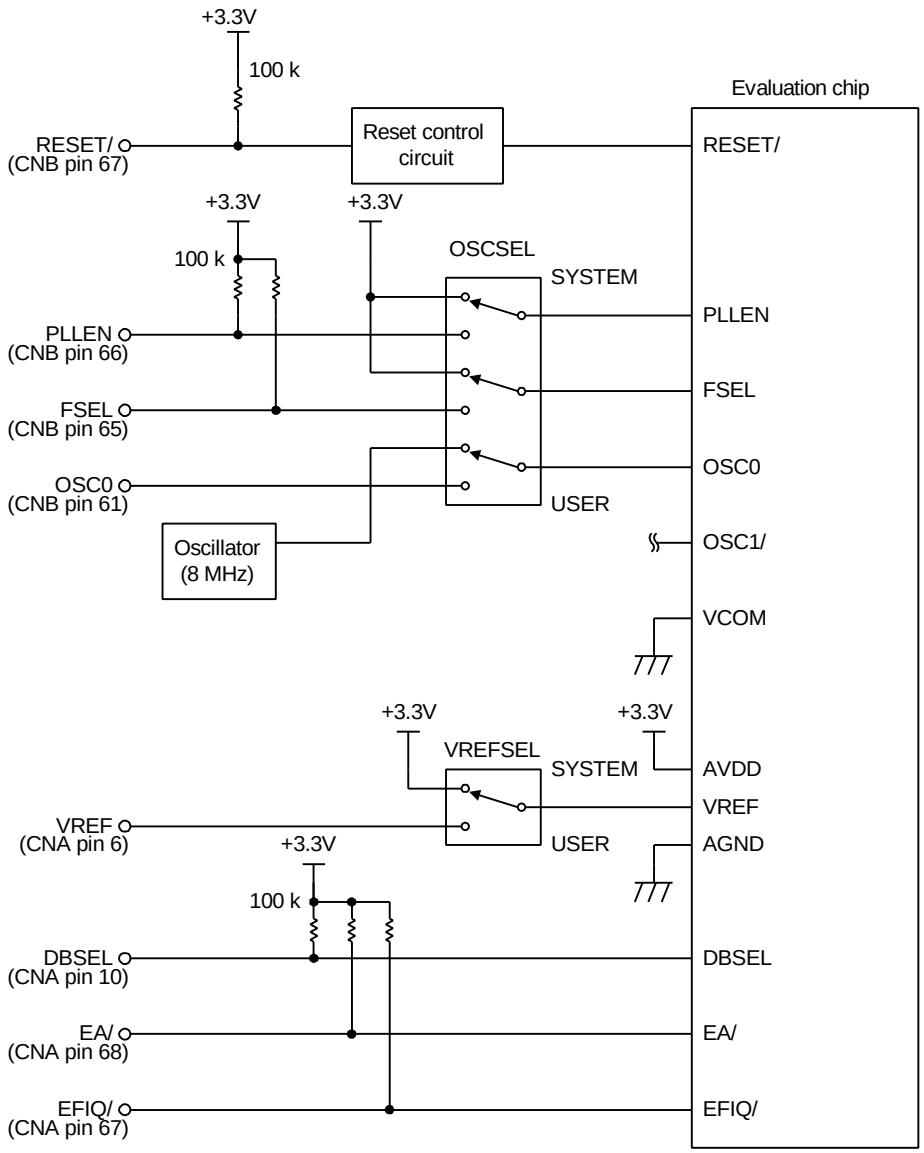


Figure 4-3 User Interface Connector Control Circuitry

Most of the pins shown (RESET/, PLLEN, FSEL, DBSEL, EA/, and EFIQ/) have 100-kΩ resistors that pull their levels up to +3.3 V. When the OSCSEL and VREFSEL switches are in their USER positions, however, it is up to the user application system to provide inputs at the proper levels.

The reset control circuit accepts input from the user application system only in emulation mode.

Not shown are the PIO8[7:0] pins, the only onboard ML670100 peripheral that the Oki ML670100 evaluation board does not emulate.

The user interface connectors do not provide access to the following evaluation chip pins: AVDD, AGND, VCOM, OSC1, and TEST. The power supply pins AVDD and AGND use the board's power supply– VDD (+3.3 V) and GND. The board also connects VCOM to GND.

CNA pins 29 to 36 (RESERVE[7:0]) provide the user application program with access to expansion peripherals connected to the expansion peripheral interface connector. For further details, see Chapter 5 "Expansion Peripheral Interface."

4.3 User Interface Cable

Plugging into the above-mentioned user interface connectors on the board is the user interface cable included with the Oki ML670100 evaluation board.

The following Figure shows its external appearance.

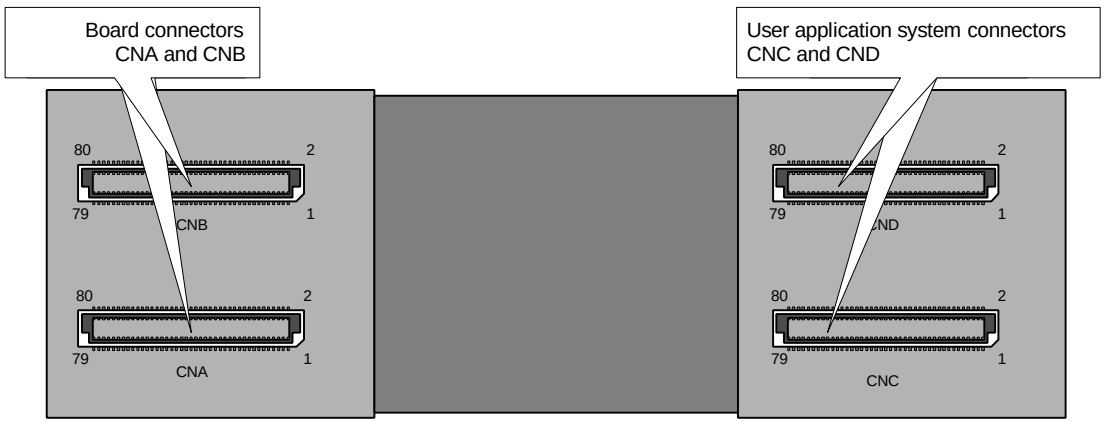


Figure 4-4 User Interface Cable

The Figure on the next page gives the user interface cable pin connections.

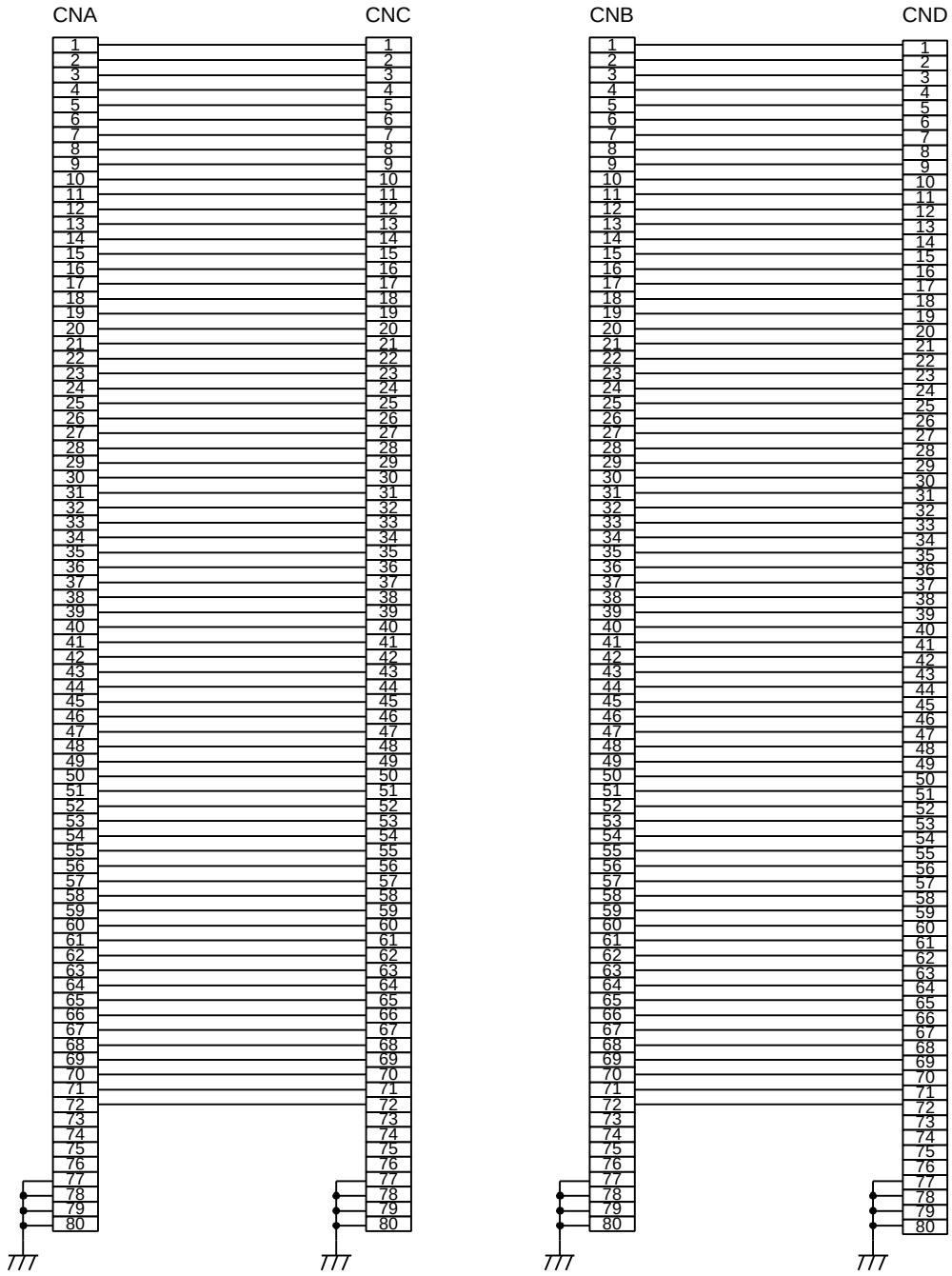


Figure 4-5 User Interface Cable Pin Connections

4.4 User Application System Connector Layout

The following Figure gives the standard layout dimensions for the connectors that the user application program uses to connect to the Oki ML670100 evaluation board via the user interface cable.

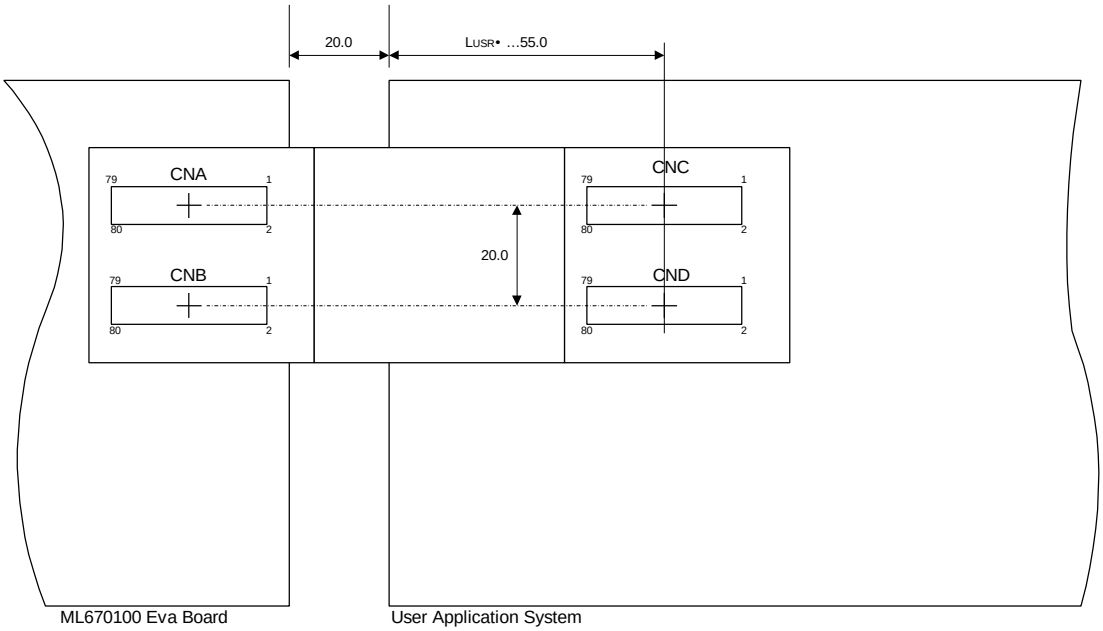


Figure 4-6 User Application System Connector Layout

The following connector matches these specifications.

Manufacturer:	Hirose Denki
Model number:	FX8C-80P-SV6
Number required:	2

5 Expansion Peripheral Interface

This Chapter describes the procedures for debugging expansion peripherals with the Oki ML670100 evaluation board.

5.1 Overview

The Oki ML670100 evaluation board allows the user to freely add go beyond the standard peripherals built into the evaluation chip by adding expansion peripherals using memory addresses reserved for the purpose. User application system access to these additional peripherals is via an external dedicated bus linked to the internal bus joining the onboard peripherals. This link makes expansion peripherals appear exactly the same as onboard peripherals.

To make up for access speed differences, the interface includes wait state support.

The following Figure gives a block diagram for expansion peripherals.

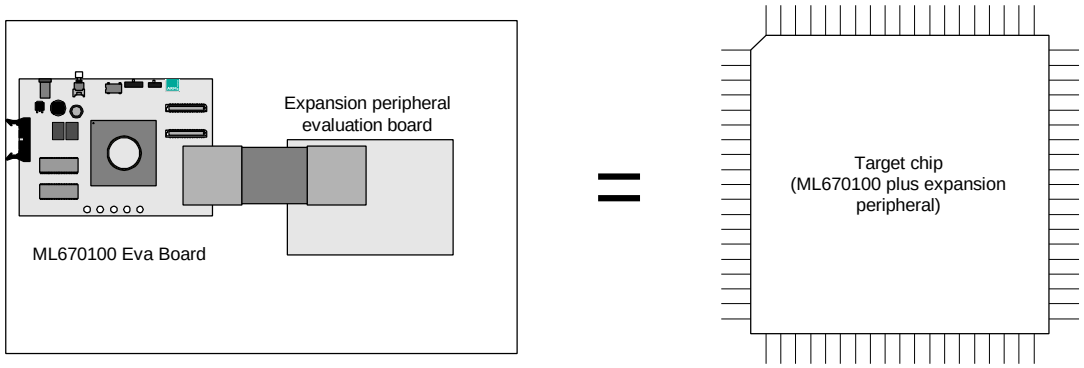


Figure 5-1 Expansion Peripheral Block Diagram

5.2 Address Space

The following Figure shows the addresses reserved for expansion peripherals.

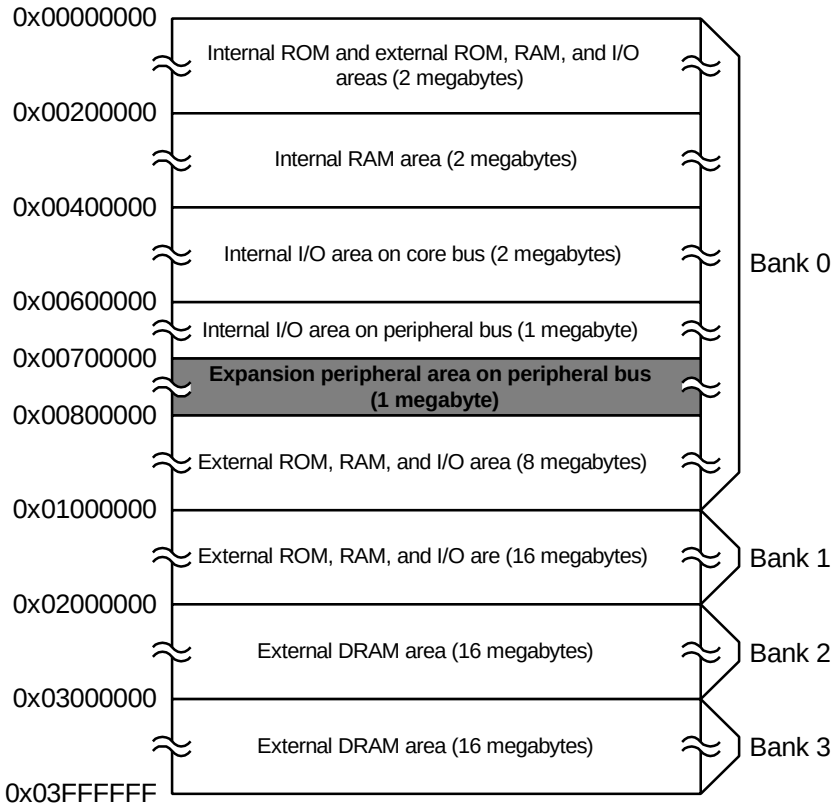


Figure 5-2 Oki ML670100 Eva Board Address Space

As the Figure shows, the expansion peripheral area consists of the addresses 0x70000 through 0x7ffff. Accessing an address in this range asserts the chip select signal (AP_nSELX). (See below.)

The ML670100 normally marks these addresses as reserved, blocking access. The Oki ML670100 evaluation board, however, allows access as long as there are expansion peripherals connected to the external bus.

5.3 Expansion Peripheral Interface Connector (EXPCN)

The connection point for these external expansion peripherals is the expansion peripheral interface connector (EXPCN). Simply connect the expansion peripheral evaluation board to it with the expansion peripheral cable.

The following Figure gives the connector location.

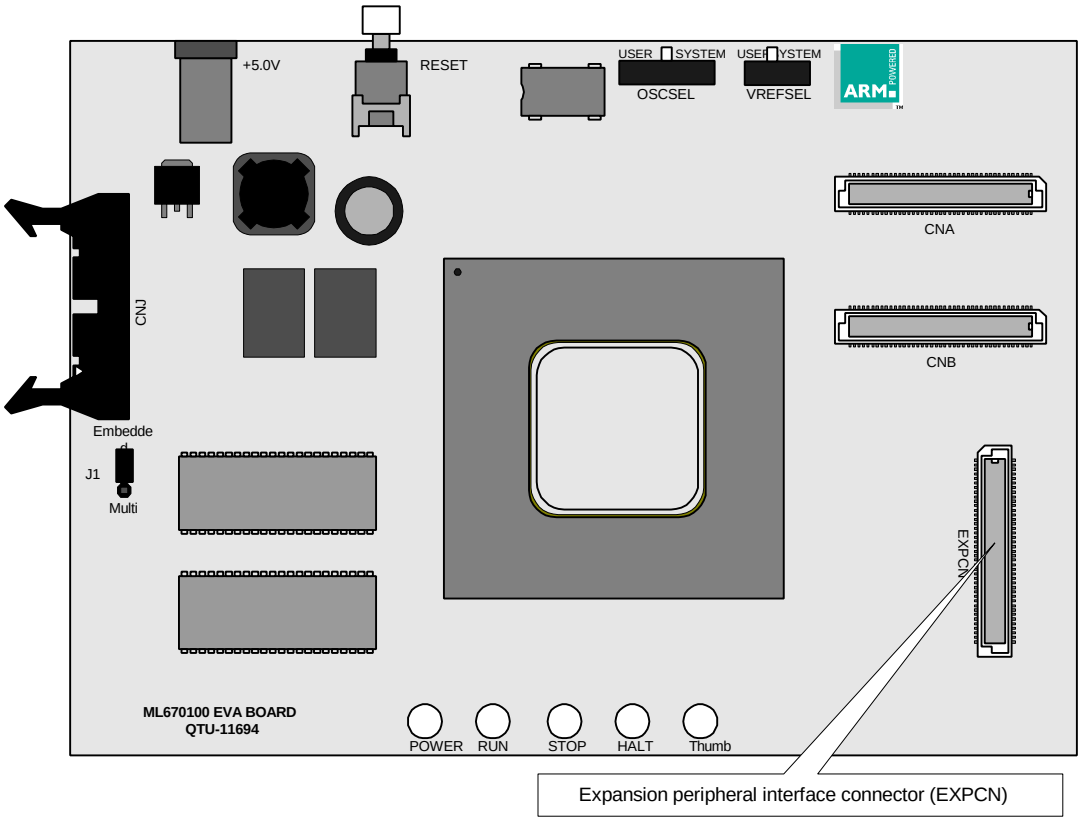


Figure 5-3 Expansion Peripheral Interface Connector (EXPCN)

The following Table gives the expansion peripheral cable pin assignments and signal names.

Table 5-1 Expansion Peripheral Interface Connector (EXPCN) Pin Assignments

Expansion Peripheral Interface Connector (EXPCN) Pin Assignments					
Pin	**Signal Name**	**I/O**	**Pin**	**Signal Name**	**I/O**
1	AP_A19	O	41	GND	O
2	AP_A18	O	42	GND	O
3	AP_A17	O	43	AP_nR/W	O
4	AP_A16	O	44	GND	O
5	AP_A15	O	45	STOPM	O
6	AP_A14	O	46	TBIT	O
7	AP_A13	O	47	HALTM	O
8	AP_A12	O	48	LOCK	O
9	AP_A11	O	49	nTRANS	O
10	AP_A10	O	50	GND	O
11	AP_A9	O	51	ECLK	O
12	AP_A8	O	52	GND	O
13	AP_A7	O	53	CLKOUT	O
14	AP_A6	O	54	GND	O
15	AP_A5	O	55	nERST	O
16	AP_A4	O	56	GND	O
17	AP_A3	O	57	DBGACK	O
18	AP_A2	O	58	GND	O
19	AP_A1	O	59	GND	O
20	AP_A0	O	60	RESERVE0	-
21	AP_nSELX	O	61	RESERVE1	-
22	AP_MAS	O	62	RESERVE2	-
23	GND	O	63	RESERVE3	-
24	GND	O	64	RESERVE4	-
25	AP_D15	I/O	65	RESERVE5	-
26	AP_D14	I/O	66	RESERVE6	-
27	AP_D13	I/O	67	RESERVE7	-
28	AP_D12	I/O	68	GND	O
29	AP_D11	I/O	69	+5.0V	O
30	AP_D10	I/O	70	+5.0V	O
31	AP_D9	I/O	71	+5.0V	O
32	AP_D8	I/O	72	+5.0V	O
33	AP_D7	I/O	73	+3.3V	O
34	AP_D6	I/O	74	+3.3V	O
35	AP_D5	I/O	75	+3.3V	O
36	AP_D4	I/O	76	+3.3V	O
37	AP_D3	I/O	77	GND	O
38	AP_D2	I/O	78	GND	O
39	AP_D1	I/O	79	GND	O
40	AP_D0	I/O	80	GND	O

The following pages describe the signal lines for this connector.

AP_A[19:0]	These outputs form the evaluation chip's address bus to the expansion peripherals.
AP_nSELX	This output is the evaluation chip's chip select signal for the expansion peripherals. It uses negative logic.
AP_MAS	This output indicates the data width for accessing the expansion peripherals from the evaluation chip: "High" level for half-word (16-bit) access; "Low" level for byte (8-bit) access. Applications include selecting the effective byte lane in conjunction with bit 0 of the above address bus.
AP_D[15:0]	These signal lines form the evaluation chip's data bus to the expansion peripherals.
AP_nR/W	This output specifies the I/O direction for accessing the expansion peripherals from the evaluation chip: "High" level for a write; "Low" level for a read.
STOPM	This output indicates the status of the evaluation chip. It goes to "High" level when the CPU is in STOP mode.
TBIT	This output indicates the status of the evaluation chip. It goes to "High" level when the CPU is in Thumb mode.

HALTM	This output indicates the status of the evaluation chip. It goes to “High” level when the CPU is in HALT mode.
LOCK	This output indicates the lock status of the evaluation chip. It goes to “High” level when the CPU activates locking for such operations as accessing memory, expansion peripherals, etc. with the SWAP instruction.
nTRANS	This output indicates the status of the evaluation chip. It uses negative logic. It goes to “Low” level when the CPU is in USER mode.
ECLK	This output provides the internal clock signal used by the evaluation chip’s core (ARM7TDMI).
CLKOUT	This output inverts the clock supplied to the evaluation chip’s core. It functions the same as the CLKOUT pin on the ML670100.
nERST	This output is the evaluation chip’s internal reset signal. It uses negative logic. Use it to reset expansion peripherals.
DBGACK	This output indicates the status of the evaluation chip. It goes to “High” level when the CPU is in DEBUG mode. “Low” level indicates emulation mode.

RESERVE[7:0]	These extra signal lines go to both the expansion peripheral interface and user interface connectors, providing the user application system access to the expansion peripherals.
+5.0V	These outputs provide access to the Oki ML670100 evaluation board's system power supply (5 V DC +/-5%).
+3.3V	These outputs provide access to the Oki ML670100 evaluation board's internally generated operating voltage (3.3 V DC +/-5%).
GND	These outputs provide the reference voltage (GND: 0 V) for the signal lines.

[Reference]

Please refer to the ARM7TDMI data sheet for further particulars on the following signal lines: TBIT, LOCK, nTRANS, ECLK, nERST, and DBGACK.

5.4 Interface Timing

The expansion peripheral interface uses clock synchronous buses, synchronizing the data bus (AP_D[15:0]), address bus (AP_A[19:0]), and other signals with the CLKOUT signal.

The following Figure shows the signal timing.

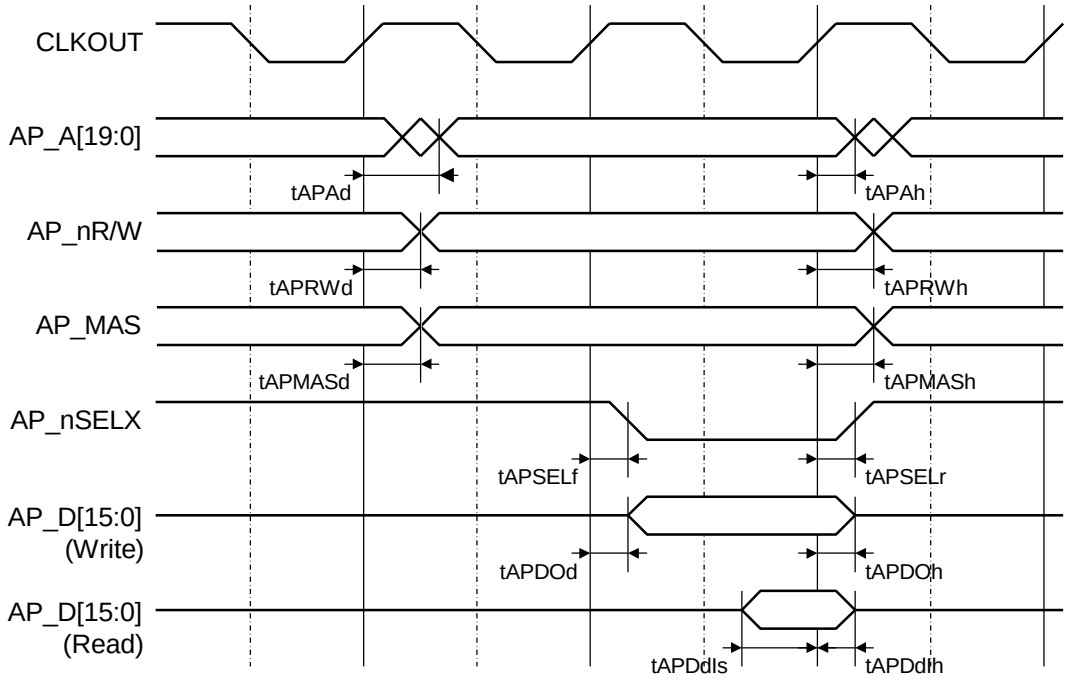


Figure 5-4 Expansion Peripheral Interface Timing 1/3

Table 5-2 Expansion Peripheral Interface Timing 1/3 (Preliminary)

Expansion Peripheral Interface Timing 1/3 (Preliminary)			
Symbol	**Description**	**Min (ns)**	**Max (ns)**
tAPAd	AP_A[19:0] delay	-	16
tAPAh	AP_A[19:0] hold time	7	-
tAPRWd	AP_nR/W delay	-	13
tAPRWh	AP_nR/W hold time	7	-
tAPMASd	AP_MAS delay	-	14
tAPMASh	AP_MAS hold time	6	-
tAPSELf	AP_nSELX assert delay	-	13
tAPSELr	AP_nSELX negate delay	5	-
tAPDOd	AP_D[15:0] output delay	-	23
tAPDOh	AP_D[15:0] output hold time	6	-
tAPDdIs	AP_D[15:0] input setup time	-	17
tAPDdIh	AP_D[15:0] input hold time	0	-

The other signals use the following timing.

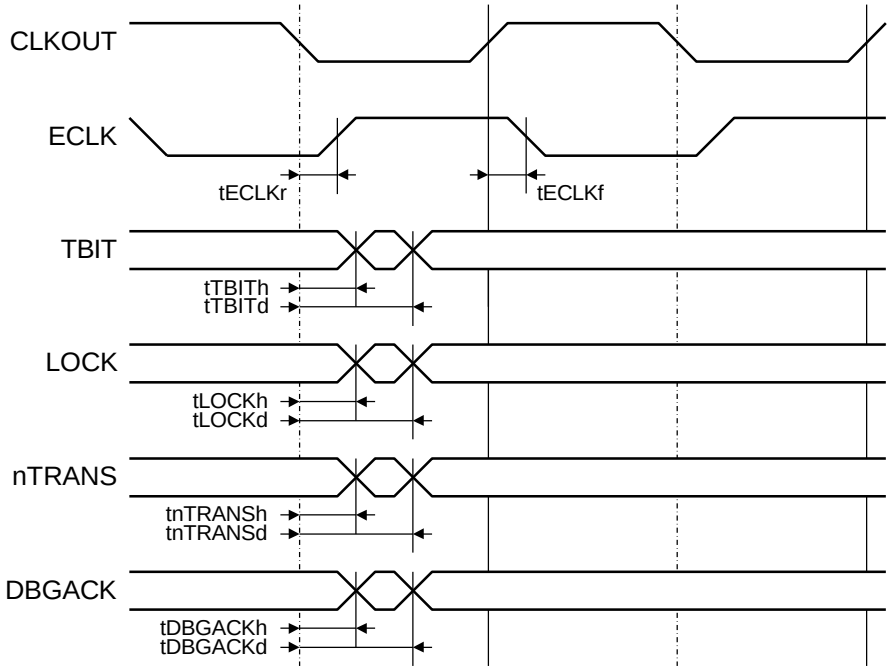


Figure 5-5 Expansion Peripheral Interface Timing 2/3

Table 5-3 Expansion Peripheral Interface Timing 2/3 (Preliminary)

Expansion Peripheral Interface Timing 2/3 (Preliminary)			
Symbol	**Description**	**Min (ns)**	**Max (ns)**
tECLKr	ECLK rising delay	6	11
tECLKf	ECLK falling delay	6	14
tTBITd	TBIT delay	-	28
tTBITh	TBIT hold time	8	-
tLOCKd	LOCK delay	-	26
tLOCKh	LOCK hold time	8	-
tnTRANSd	nTRANS delay	-	28
tnTRANSh	nTRANS hold time	8	-
tDBGACKd	DBGACK delay	-	
tDBGACKh	DBGACK hold time		-

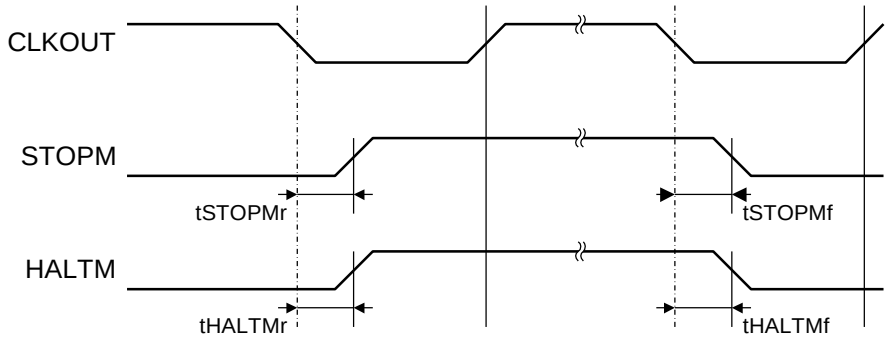


Figure 5-6 Expansion Peripheral Interface Timing 3/3

Table 5-4 Expansion Peripheral Interface Timing 3/3 (Preliminary)

Expansion Peripheral Interface Timing 3/3 (Preliminary)			
Symbol	**Description**	**Min (ns)**	**Max (ns)**
tSTOPMr	STOPM rising delay	-	14
tSTOPMf	STOPM falling delay	7	-
tHALTMr	HALTM rising delay	-	14
tHALTMf	HALTM falling delay	8	-

5.5 Inserting Wait Cycles

The evaluation chip on the Oki ML670100 evaluation board gives the program control over the wait cycles introduced into the access timing for expansion peripherals. Controlling this function is the Expansion Peripheral Programmable Wait Control Register (XPWCON, Address: 0x600710).

The following Figure shows the bits in this register.

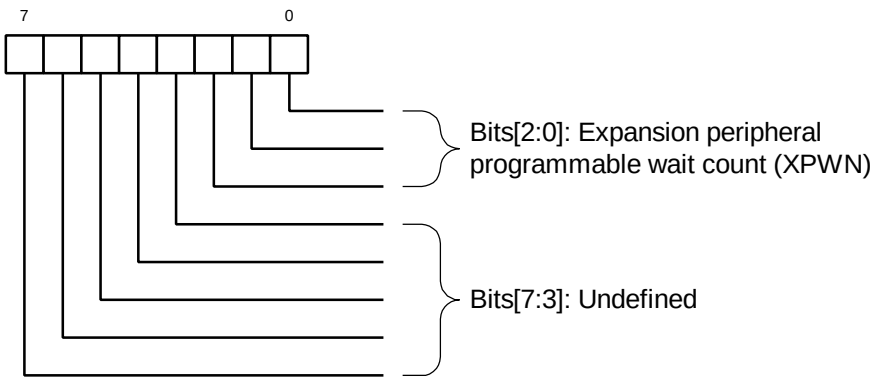


Figure 5-7 Expansion Peripheral Programmable Wait Control Register Bit Field

The above Figure shows the bit field (XPWN, bits[2:0]) for specifying the number of wait cycles (XPWN) inserted when accessing the expansion peripheral.
The following Table shows the relationship between the number written to XPWN and the number of wait cycles inserted.

Table 5-5 Expansion Peripheral Programmable Wait Count (XPWN) Settings

Expansion Peripheral Programmable Wait Count (XPWN) Settings	
XPWN[2:0]	**Wait cycles**
[000]	0 cycles
[001]	1 wait cycle
[010]	2 wait cycles
[011]	3 wait cycles
[100]	4 wait cycles
[101]	5 wait cycles
[110]	6 wait cycles
[111]	7 wait cycles

This register provides both read and write access, but completely ignores the undefined bits[7:3]. The initial setting for this register is XPWN[2:0]=3'b111.

The following Figure shows the expansion peripheral access timing for one wait cycle.

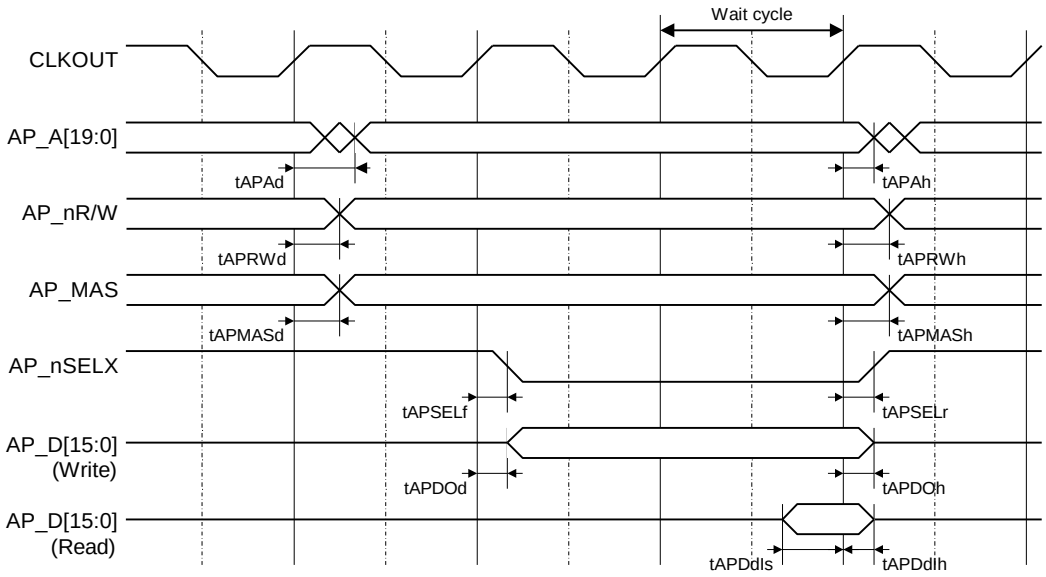


Figure 5-8 Expansion Peripheral Access Timing

The timing parameters here are the same as the ones given in Section 5.4 above.

5.6 Expansion Peripheral Interface Cable

An option available for the Oki ML670100 evaluation board is the expansion peripheral interface cable for joining the above-mentioned expansion peripheral interface connector to the expansion peripheral evaluation board.

The following Figure shows the cable's external appearance and the major connections.

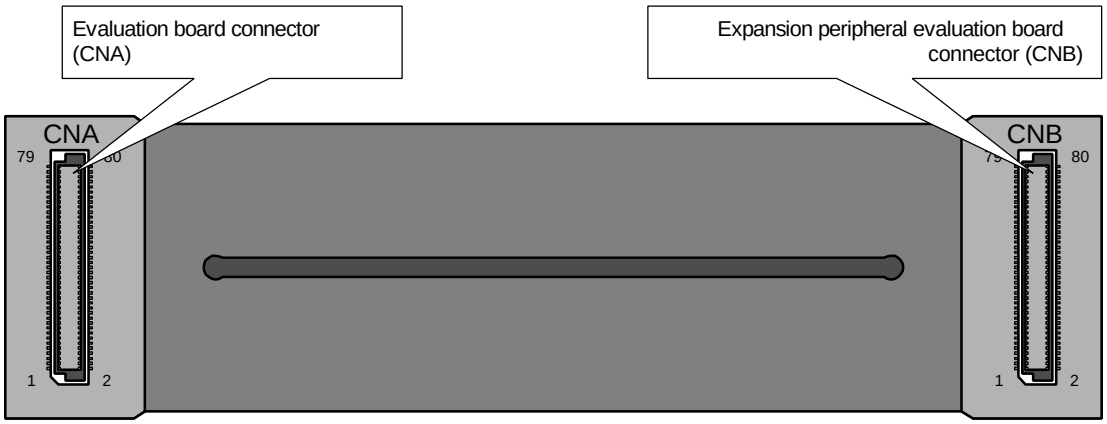


Figure 5-9 Expansion Peripheral Interface Cable

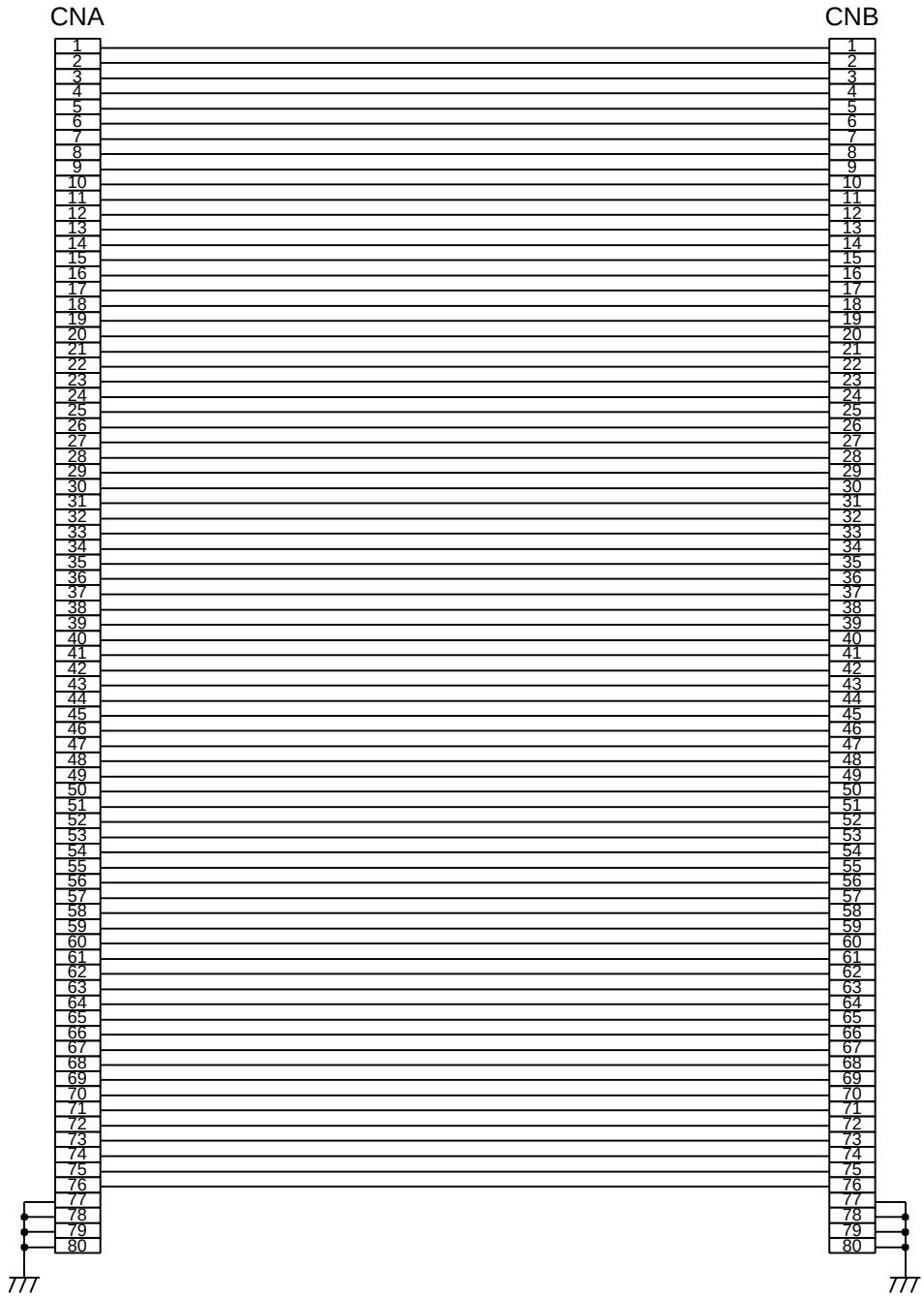


Figure 5-10 Expansion Peripheral Interface Connections

5.7 Expansion Peripheral Evaluation Board Connector Layout

The following Figure gives the standard layout dimensions for the connector that the expansion peripheral evaluation board uses to connect to the Oki ML670100 evaluation board via the expansion peripheral interface cable.

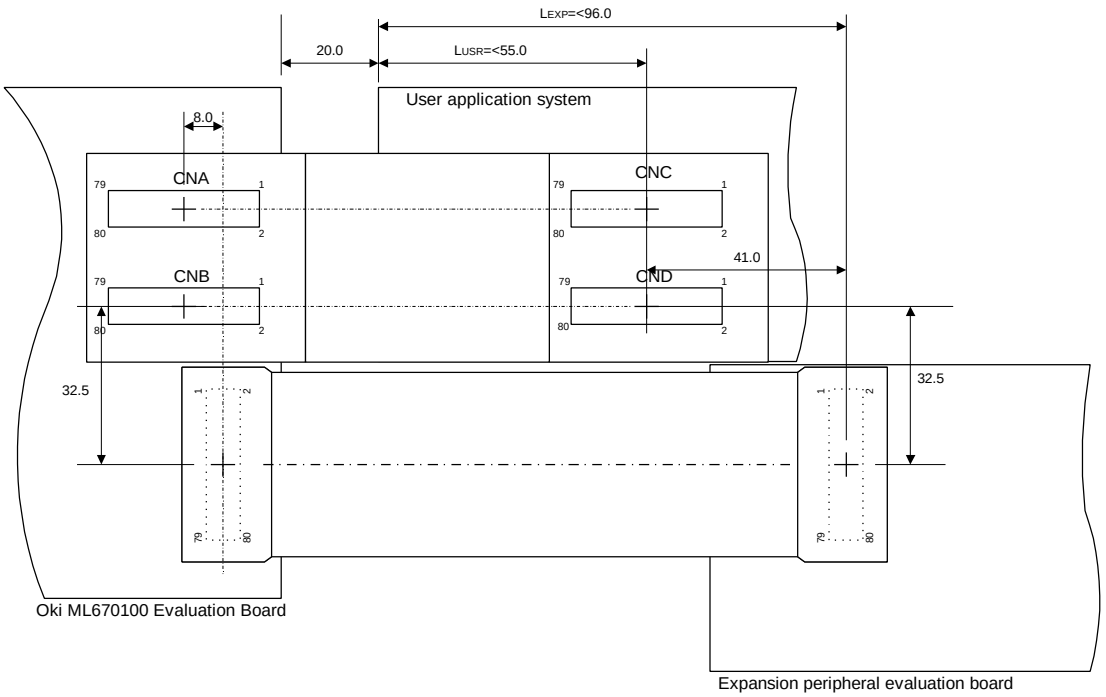


Figure 5-11 Expansion Peripheral Evaluation Board Connector Layout

The figure shows the user application system and expansion peripheral evaluation board connected independently.

The following connector matches these specifications.

Manufacturer:	Hirose Denki
Model number:	FX8C-80P-SV6
Number required:	1

6 Important Usage Notes

This Chapter lists certain items to keep in mind when debugging user application program with the Oki ML670100 evaluation board.

6.1 Differences from Target Chip

This Section describes the points where the Oki ML670100 evaluation board differs from the target device, the Oki ML670100 microcontroller.

6.1.1 User Interface Differences

The Oki ML670100 evaluation board provides the additional control circuitry shown in the following Figure between the user interface connectors (CNA and CNB) and the following evaluation chip pins: RESET/, PLLEN, FSEL, OSC0, VREF, DBSEL, EA/, and EFIQ/.

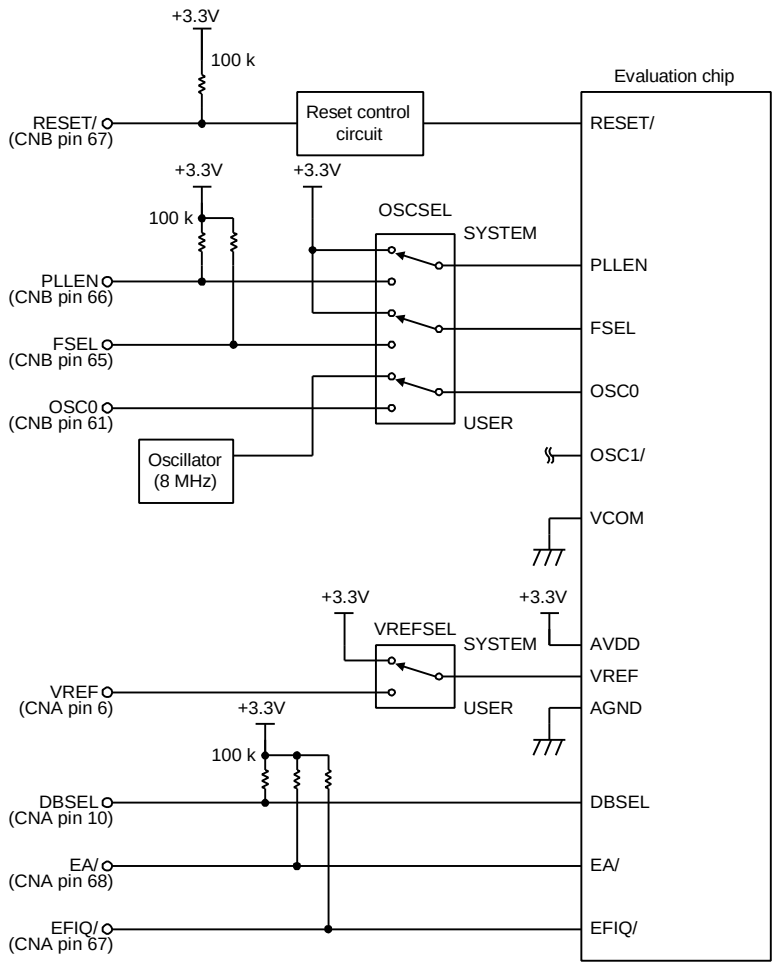


Figure 6-1 User Interface Connector Control Circuitry

Most of the pins shown (RESET/, PLLEN, FSEL, DBSEL, EA/, and EFIQ/) have 100-kΩ resistors that pull their levels up to +3.3 V. When the OSCSEL and VREFSEL switches are in their USER positions, however, it is up to the user application system to provide inputs at the proper levels.

The reset control circuit accepts input from the user application system only in emulation mode.

Not shown are the PIO8[7:0] pins, the only onboard ML670100 peripheral that the Oki ML670100 evaluation board does not emulate.

6.1.2 Memory Map Differences

The Oki ML670100 evaluation board differs from the ML670100 in the amounts of internal ROM and RAM present.

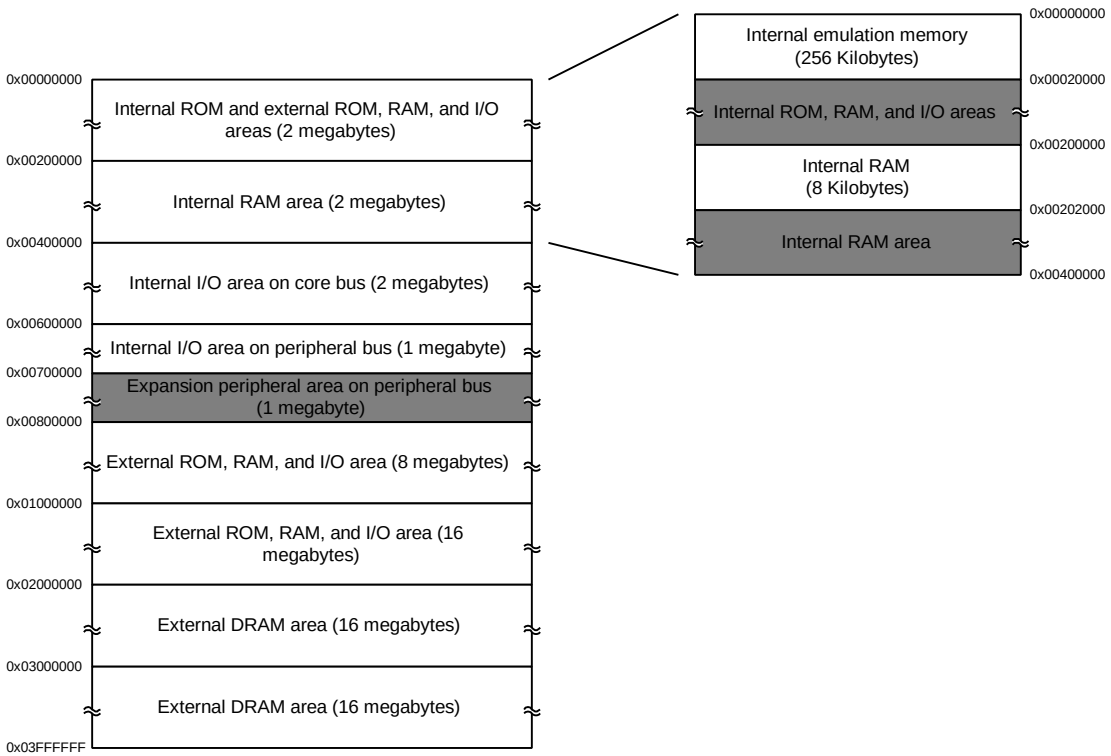


Figure 6-2 Oki ML670100 Eva Board Address Space

As the Figure shows, the Oki ML670100 evaluation board features the same memory areas as the ML670100 except for three areas: the expansion peripheral area, the onboard RAM, and the emulation memory.

For extra room during development, the the onboard RAM and emulation memory have double the capacity of their counterparts in the ML670100: 256 kilobytes (0x000000 to 0x02ffff) instead of 128 kilobytes (0x000000 to 0x01ffff) for the former and 8 kilobytes (0x200000 to 0x201ffff) instead of 4 kilobytes (0x200000 to 0x200fff) for the latter.

The emulation memory consists of SRAM, which can be modified, instead of the ROM in the target device. At the same time, however, it is also thus open to overwriting should the user application program run out of control.

6.2 Other Notes

This Section lists other items to keep in mind when debugging user application program with the Oki ML670100 evaluation board.

6.2.1 System Reset (RESET) Switch

Do not press the system reset (RESET) switch during remote debugging because doing so also resets the in-circuit emulator interface, possibly breaking the link between the board and the ARM Software Development Support Toolkit running on the development host.

6.2.2 User Interface Cable

Do not bend the user interface cable included with the Oki ML670100 evaluation board. Rough treatments risks damaging not only the cable, but also the user application system.

6.2.3 External Clock Input

When the OSCSEL switch is in its USER position, the user application system must provide an external clock signal satisfying the following specifications.

Frequency: See Table below for range configuration.
Duty: 50%
Level: 3.3 V DC ±5% (±3%)

Table 6-1 Configuring Oki ML670100 Eva Board for External Clock Signal Frequency

Configuring Oki ML670100 Eva Board for External Clock Signal Frequency		
FSEL	**PLLEN**	**OSC0 Pin Input Frequency Range**
"H"	"H"	DC to 8 MHz
"L"	"H"	DC to 16 MHz
X	"L"	DC to 32 MHz

X:Don't Care

[Caution]

Make sure that the FSEL and PLLEN levels indicate the correct range for the input frequency. A mismatch risks erratic CPU operation and hardware breakdown.

7 Appendices

7.1 User Interface Connector Pin Assignments

The following two Tables give the pin assignments for the user interface connectors (CNA and CNB).

Table 7-1 Pin Assignments for User Interface Connector CNA

Pin Assignments for User Interface Connector CNA					
Pin	**Signal Name**	**I/O**	**Pin**	**Signal Name**	**I/O**
1	AI4	I	41	XA2	O
2	AI3	I	42	XA3	O
3	AI2	I	43	XA4	O
4	AI1	I	44	XA5	O
5	AI0	I	45	XA6	O
6	VREF	I	46	XA7	O
7	N.C.	-	47	GND	O
8	N.C.	-	48	N.C.	-
9	N.C.	-	49	XA8	O
10	DBSEL	I	50	XA9	O
11	PIO6.0	I/O	51	XA10	O
12	PIO6.1	I/O	52	XA11	O
13	PIO6.2	I/O	53	XA12	O
14	PIO6.3	I/O	54	XA13	O
15	PIO6.4	I/O	55	XA14	O
16	PIO6.5	I/O	56	XA15	O
17	PIO6.6	I/O	57	GND	O
18	PIO6.7	I/O	58	N.C.	-
19	PIO7.0	I/O	59	PIO0.0	I/O
20	PIO7.1	I/O	60	PIO0.1	I/O
21	PIO7.2	I/O	61	PIO0.2	I/O
22	GND	O	62	PIO0.3	I/O
23	N.C.	-	63	PIO0.4	I/O
24	PIO7.3	I/O	64	PIO0.5	I/O
25	PIO7.4	I/O	65	PIO0.6	I/O
26	PIO7.5	I/O	66	PIO0.7	I/O
27	PIO7.6	I/O	67	EFIQ/	I
28	PIO7.7	I/O	68	EA/	I
29	RESERVE0	-	69	GND	O
30	RESERVE1	-	70	N.C.	-
31	RESERVE2	-	71	XD0	I/O
32	RESERVE3	-	72	XD1	I/O
33	RESERVE4	-	73	N.C.	-
34	RESERVE5	-	74	N.C.	-
35	RESERVE6	-	75	N.C.	-
36	RESERVE7	-	76	N.C.	-
37	GND	O	77	GND	O
38	N.C.	-	78	GND	O
39	XA0	O	79	GND	O
40	XA1	O	80	GND	O

Table 7-2 Pin Assignments for User Interface Connector CNB

Pin Assignments for User Interface Connector CNB					
Pin	**Signal Name**	**I/O**	**Pin**	**Signal Name**	**I/O**
1	XD2	I/O	41	PIO4.0	I/O
2	XD3	I/O	42	PIO4.1	I/O
3	XD4	I/O	43	PIO4.2	I/O
4	XD5	I/O	44	PIO4.3	I/O
5	XD6	I/O	45	PIO4.4	I/O
6	XD7	I/O	46	PIO4.5	I/O
7	GND	O	47	PIO4.6	I/O
8	N.C.	-	48	PIO4.7	I/O
9	PIO1.0	I/O	49	GND	O
10	PIO1.1	I/O	50	N.C.	-
11	PIO1.2	I/O	51	PIO5.0	I/O
12	PIO1.3	I/O	52	PIO5.1	I/O
13	PIO1.4	I/O	53	PIO5.2	I/O
14	PIO1.5	I/O	54	PIO5.3	I/O
15	PIO1.6	I/O	55	PIO5.4	I/O
16	PIO1.7	I/O	56	PIO5.5	I/O
17	CS0/	O	57	PIO5.6	I/O
18	RD/	O	58	PIO5.7	I/O
19	WRE_WRL/	O	59	CLKOUT	O
20	GND	O	60	GND	I/O
21	N.C.	-	61	OSC0	I
22	PIO2.0	I/O	62	N.C.	-
23	PIO2.1	I/O	63	N.C.	-
24	PIO2.2	I/O	64	N.C.	-
25	PIO2.3	I/O	65	FSEL	I
26	PIO2.4	I/O	66	PLLEN	I
27	PIO2.5	I/O	67	RESET/	I
28	PIO2.6	I/O	68	GND	O
29	PIO2.7	I/O	69	GND	O
30	GND	O	70	AI7	I
31	N.C.	-	71	AI6	I
32	PIO3.0	I/O	72	AI5	I
33	PIO3.1	I/O	73	N.C.	-
34	PIO3.2	I/O	74	N.C.	-
35	PIO3.3	I/O	75	N.C.	-
36	PIO3.4	I/O	76	N.C.	-
37	PIO3.5	I/O	77	GND	O
38	PIO3.6	I/O	78	GND	O
39	PIO3.7	I/O	79	GND	O
40	GND	O	80	GND	O

7.2 User Interface Connector Control Circuitry

The Oki ML670100 evaluation board provides the additional control circuitry shown in the following Figure between the user interface connectors (CNA and CNB) and the evaluation chip pins.

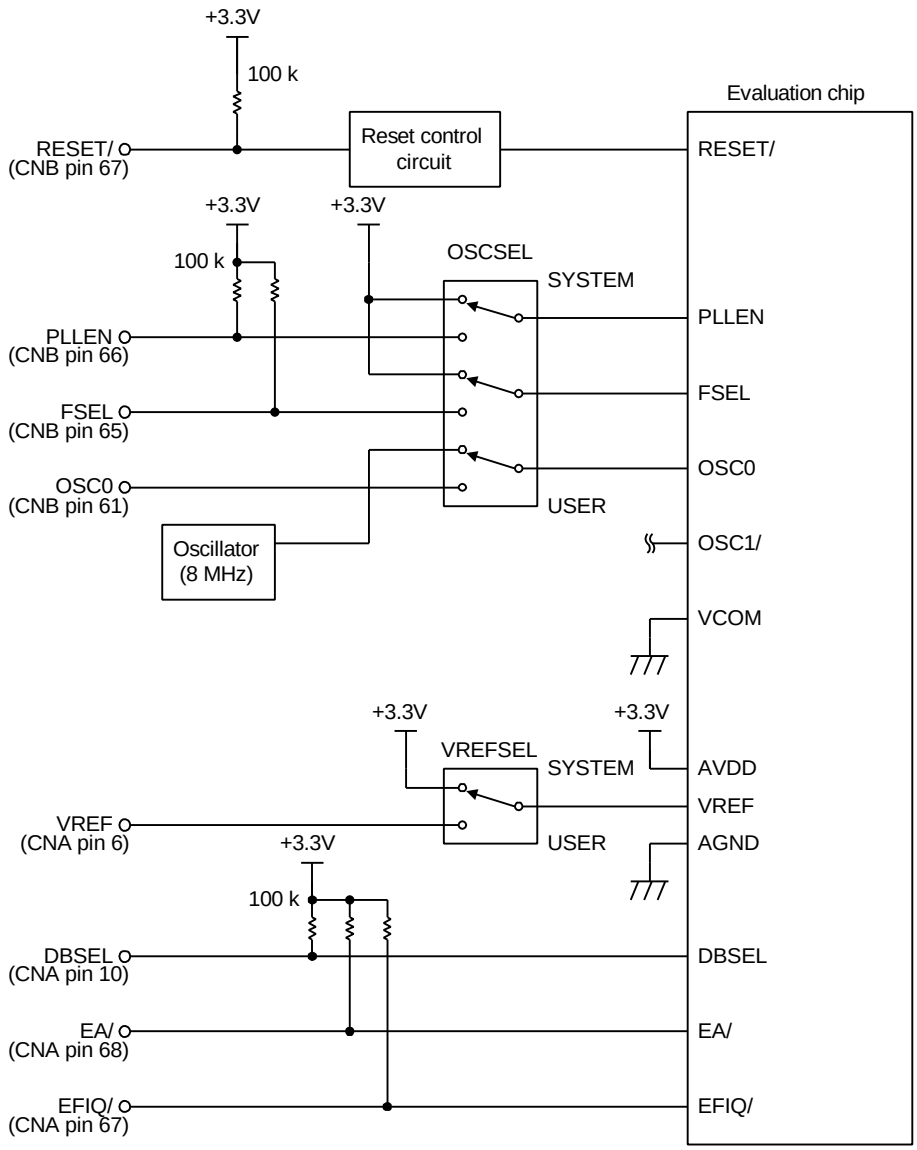


Figure 7-1 User Interface Connector Control Circuitry

7.3 Expansion Peripheral Interface Connector (EXPCN) Pin Assignments

The following Table gives the expansion peripheral cable pin assignments and signal names.

Table 7-3 Expansion Peripheral Interface Connector (EXPCN) Pin Assignments

Expansion Peripheral Interface Connector (EXPCN) Pin Assignments					
Pin	**Signal Name**	**I/O**	**Pin**	**Signal Name**	**I/O**
1	AP_A19	O	41	GND	O
2	AP_A18	O	42	GND	O
3	AP_A17	O	43	AP_nR/W	O
4	AP_A16	O	44	GND	O
5	AP_A15	O	45	STOPM	O
6	AP_A14	O	46	TBIT	O
7	AP_A13	O	47	HALTM	O
8	AP_A12	O	48	LOCK	O
9	AP_A11	O	49	nTRANS	O
10	AP_A10	O	50	GND	O
11	AP_A9	O	51	ECLK	O
12	AP_A8	O	52	GND	O
13	AP_A7	O	53	CLKOUT	O
14	AP_A6	O	54	GND	O
15	AP_A5	O	55	nERST	O
16	AP_A4	O	56	GND	O
17	AP_A3	O	57	DBGACK	O
18	AP_A2	O	58	GND	O
19	AP_A1	O	59	GND	O
20	AP_A0	O	60	RESERVE0	-
21	AP_nSELX	O	61	RESERVE1	-
22	AP_MAS	O	62	RESERVE2	-
23	GND	O	63	RESERVE3	-
24	GND	O	64	RESERVE4	-
25	AP_D15	I/O	65	RESERVE5	-
26	AP_D14	I/O	66	RESERVE6	-
27	AP_D13	I/O	67	RESERVE7	-
28	AP_D12	I/O	68	GND	O
29	AP_D11	I/O	69	+5.0V	O
30	AP_D10	I/O	70	+5.0V	O
31	AP_D9	I/O	71	+5.0V	O
32	AP_D8	I/O	72	+5.0V	O
33	AP_D7	I/O	73	+3.3V	O
34	AP_D6	I/O	74	+3.3V	O
35	AP_D5	I/O	75	+3.3V	O
36	AP_D4	I/O	76	+3.3V	O
37	AP_D3	I/O	77	GND	O
38	AP_D2	I/O	78	GND	O
39	AP_D1	I/O	79	GND	O
40	AP_D0	I/O	80	GND	O