OKI Semiconductor

This version: Nov. 1997
Previous version: Jul. 1996

MSC1218

63-Bit Triplex Controller/Driver with Digital Dimming Function

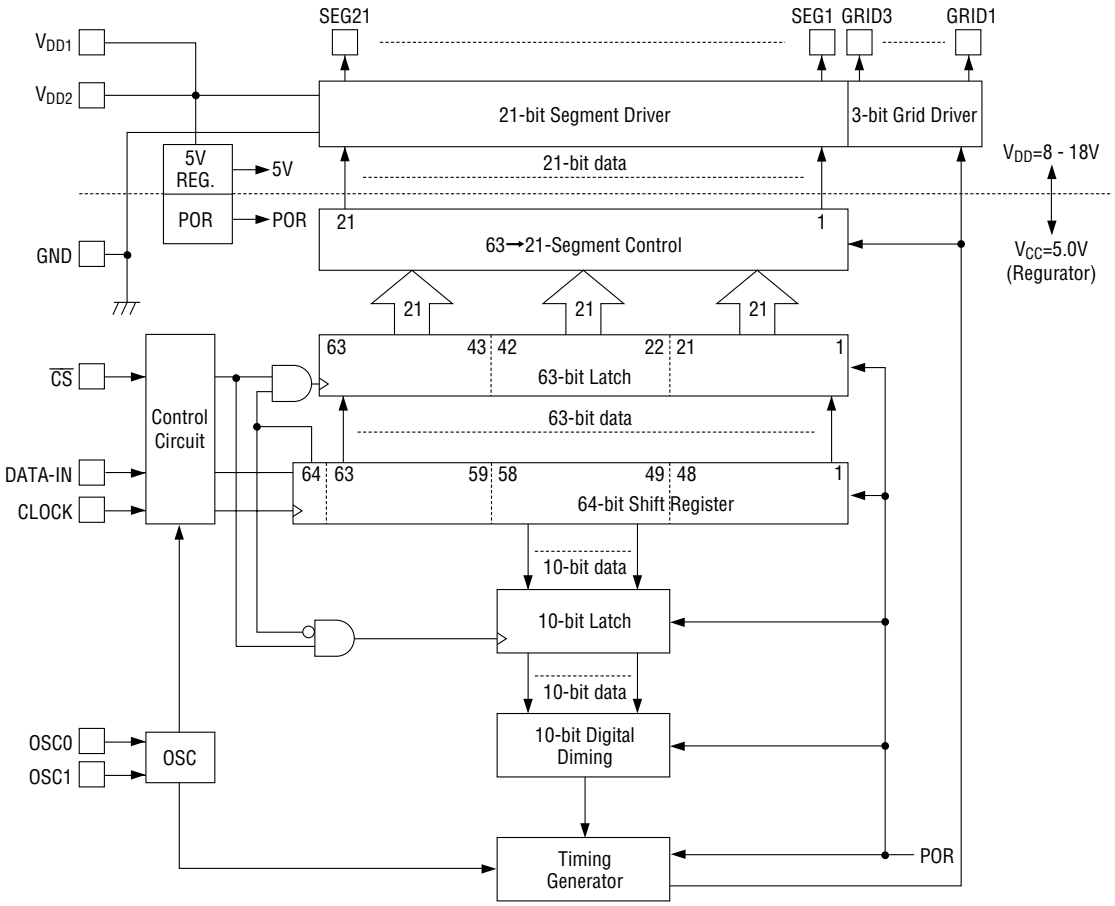
GENERAL DESCRIPTION

The MSC1218 is a Bi-CMOS driver for 1/3 duty vacuum fluorescent display tube.
It contains a 64-bit shift register, a 63-bit latch, a 10-bit digital dimming circuit, and three grids.
The MSC1218 has only three microcontroller interface signal lines: $\overline{CS}$, D-IN, and CLOCK.
The chip select function enables the D-IN and CLOCK lines to be shared with other peripheral circuits.

FEATURES

- Power supply Voltage : 8 to 18V (built-in 5V regulator for logic circuit)
- Operating temperature : -40 to +85°C
- 21-segment driver outputs : I_{OH}=–6mA at V_{OH}=V_{DD}–0.8V
- 3-grid driver outputs : I_{OH}=–16mA at V_{OH}=V_{DD}–0.8V
- Built-in digital dimming circuit : 10-bit resolution
- Built-in RC oscillation circuit : External R and C
- Built-in Power-On-Reset circuit
- Package:
  32-pin plastic SSOP(SSOP32-P-430-1.00-K) (Product name: MSC1218GS-K)

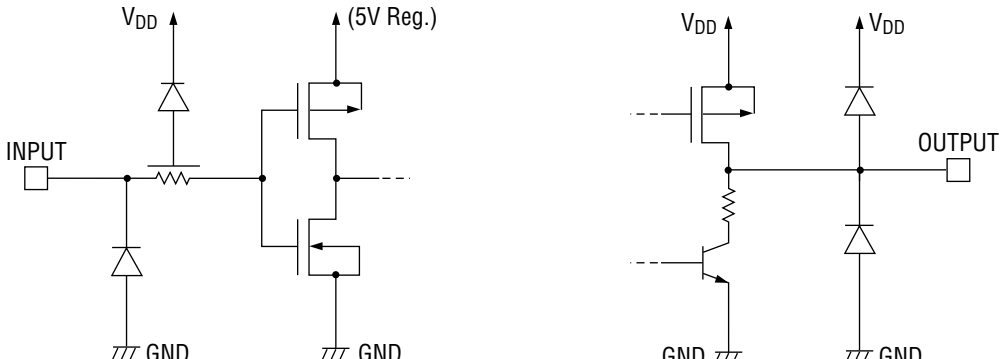
BLOCK DIAGRAM



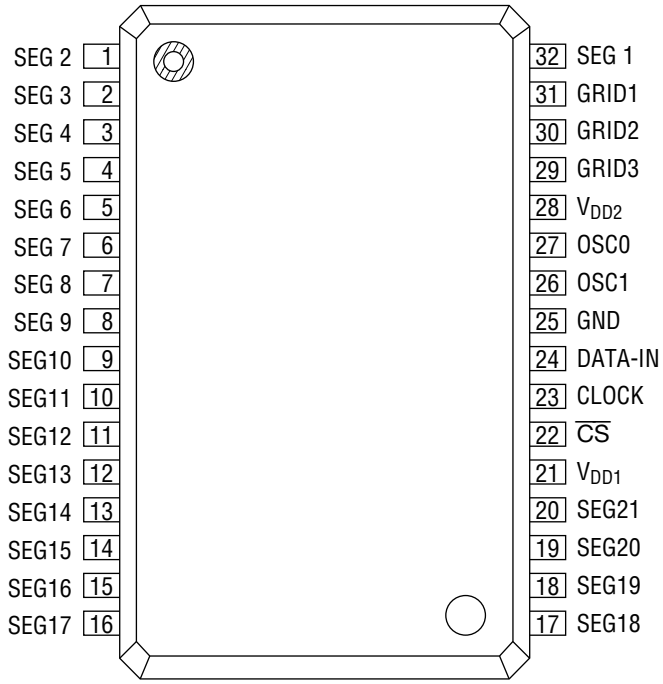
64 bits=0: Digital Dimming Mode
64 bits=1: VF Data Input Mode

INPUT AND OUTPUT CONFIGURATION

- Schematic Diagrams of Logic Portion Input Circuit
- Schematic Diagrams of Driver Output Circuit



PIN CONFIGURATION (TOP VIEW)



32-Pin Plastic SSOP

PIN DESCRIPTIONS

Pin	Symbol	Type	Decription
32, 1 - 20	SEG1 - 21	O	Output pins for segment signals for driving VF display tube (anode).
29 - 31	GRID1 - 3	O	Output pins for grid signals for driving VF display tube (grid).
24	D-IN	I	Serial data input pin (positive logic).
23	CLOCK	I	Shift clock input pin. Serial data shifts at the rising edge of CLOCK.
27	OSC0	I	RC oscillator connecting pins. Oscillation frequency is 3.2MHz. Connect a resistor between the OSC1 and OSC0 pins and a capacitor between the OSC0 pin and the ground.
26	OSC1	O	
22	$\overline{CS}$	I	Chip select input pin. Data transfer is inhibited when this pin is "H".
21 28	V_{DD1} V_{DD2}	—	Power supply pins. When using these pins, connect each of them to the power supply.
25	GND	—	Ground pin.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	—	–0.3 to +20	V
Input Voltage	V_{IN}	All input pins	–0.3 to +6.0	V
Storage Temperature	T_{STG}	—	–65 to +150	°C
Power Dissipation	P_D	Ta = +85°C	400	mW

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	—	8	—	18	V
High Level Input Voltage (1)	V_{IH1}	All inputs except OSC0	3.8	—	5.5	V
High Level Input Voltage (2)	V_{IH2}	OSC0	4.5	—	5.5	V
Low Level Input Voltage (1)	V_{IL1}	All inputs except OSC0	0	—	0.8	V
Low Level Input Voltage (2)	V_{IL2}	OSC0	0	—	0.5	V
Clock Frequency	f_C	—	—	—	250	kHz
Oscillation Frequency	f_{OSC}	R = 4.7kΩ, C = 10pF	—	3.2	—	MHz
Frame Frequency	f_{FR}	f_{osc} = 3.2MHz	—	260	—	Hz
Operating Temperature	T_{op}	—	–40	—	85	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics

(Ta = –40 to +85°C, V_{DD} = 8 to 18V (Unless otherwise noted))

Parameter	Symbol	Condition	Min.	Max.	Unit
High Level Input Voltage (1) (All inputs except OSC0)	V_{IH1}	—	3.8	5.5	V
High Level Input Voltage (2) (All inputs except OSC0)	V_{IH2}	External input only	4.5	5.5	V
Low Level Input Voltage (1) (OSC0)	V_{IL1}	—	0.0	0.8	V
Low Level Input Voltage (2) (OSC0)	V_{IL2}	External input only	0.0	0.8	V
High Level Input Current (All inputs)	I_{IH}	V_{IH1} = 5.0V	–5	5	µA
Low Level Input Current (All inputs)	I_{IL}	V_{IL} = 0.0V	–5	5	µA
High Level Output Voltage (SEG1-20)	V_{OH1}	V_{DD}= 9.5V I_{OH1} = –6mA	V_{DD}–0.8	—	V
High Level Output Voltage (GRID1-3)	V_{OH2}	V_{DD}= 9.5V I_{OH2} = –16mA	V_{DD}–0.8	—	V
Low Level Output Voltage (1) (SEG1-20, GRID1-3)	V_{OL1}	V_{DD}= 9.5V I_{OL1} = 500µA	—	2	V
Low Level Output Voltage (2) (SEG1-20, GRID1-3)	V_{OL2}	V_{DD}= 9.5V I_{OL2} = 200µA	—	1	V
Low Level Output Voltage (3) (SEG1-20, GRID1-3)	V_{OL3}	V_{DD}= 9.5V I_{OL3} = 2µA	—	0.3	V
Current Consumption	V_{DD}	f_{OSC}= 3.2MHz No load	—	10	V

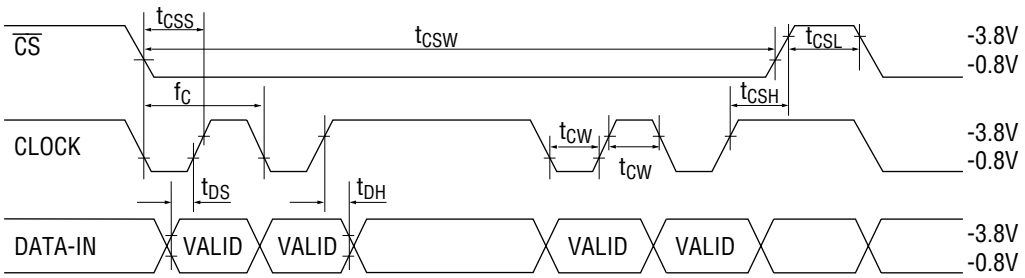
AC Characteristics

(Ta = –40 to +85°C, V_{DD} = 8 to 18V (Unless otherwise noted))

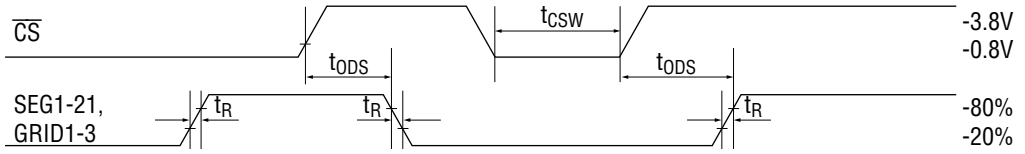
Parameter	Symbol	Condition	Min.	Max.	Unit
Oscillation Frequency	f_{OSC}	R=4.7kΩ, C=10pF	2	4.4	MHz
External Input Frequency to OSC0	f_{OSCI}	External input only	2.7	3.7	MHz
Clock Frequency	f_C	—	—	250	kHz
Clock Pulse Width	t_{CW}	—	1.3	—	µs
Data Setup Time	t_{DS}	—	1	—	µs
Data Hold Time	t_{DH}	—	200	—	ns
$\overline{CS}$ Pulse Width	t_{CSW}	—	8	—	µs
$\overline{CS}$ Off Time	t_{CSL}	—	32	—	µs
$\overline{CS}$ Setup Time ($\overline{CS}$ – Clock)	t_{CSS}	—	2	—	µs
$\overline{CS}$ Hold Time (Clock – $\overline{CS}$)	t_{CSH}	—	2	—	µs
$\overline{CS}$–All Output Delay Time	t_{ODS}	C_I=100pF	—	8	µs
Slew Rate (All Drivers)	t_R	C_I=100pF t=20% to 80% or 80% to 20%	—	5	µs
Power – $\overline{CS}$ Time at Power-on	t_{PCS}	—	300	—	µs
Hold Time at Power-off	t_{POF}	When mounted on the unit V_{DD} = 0.0V	5	—	ms
Rise Time at Power-on	t_{PRZ}	When mounted on the unit	—	100	µs

TIMING DIAGRAM

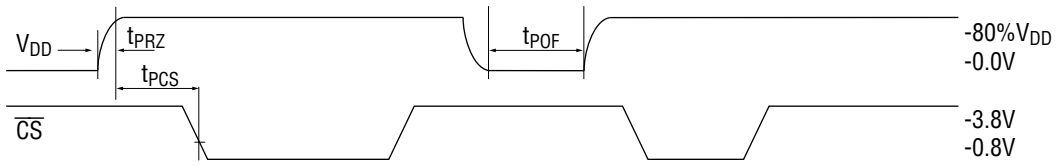
1) Data Input Timing



2) Data Output Timing



3) Power-on Timing



FUNCTIONAL DESCRIPTION

● Power-on Reset

The built-in Power-on-Reset (POR) circuit initializes the internal circuits when power is applied. The following condition is established after POR.

1) Contents of the shift register and latches are "0".
2) Duty cycle of digital dimming is set to "0".
3) All the outputs are OFF.

● Function Mode

The function mode is selected according to the output of the last bit of the shift register. The function modes are as follows.

M0 (Last bit)	Function
0	Digital dimming data input mode
1	Display data input mode

● Digital Dimming Data Input

When M0="0", the digital dimming data input mode is selected and the input data length is 16 bits.

The digital dimming data input is valid only when the low level is applied to the $\overline{CS}$ pin.

The digital dimming data that was input to DATA-IN is input into the shift register at the rising edge of the CLOCK.

Data is automatically loaded to the latches from the shift register at the rising edge of $\overline{CS}$.

The digital dimming data consists of 10 bits.

The output duty varies from 0/1024 (0%) to 1016/1624 (99%) for each grid.

The 10-bit digital dimming data should be input starting with the LSB.

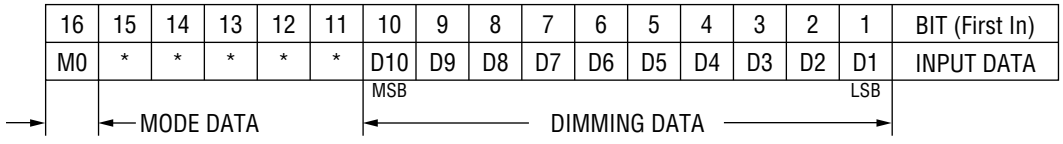
[Data Configuration]

Digital dimming data input mode

Input data: 16bits

Digital dimming data: 10 bits

Mode selector: 1 bit



(MSB)				INPUT DATA					(LSB)	DUTY CYCLE
0	0	0	0	0	0	0	0	0	0	0/1024
0	0	0	0	0	0	0	0	0	1	1/1024
				⋮						⋮
1	1	1	1	1	1	1	0	0	0	1016/1024
				⋮						⋮
1	1	1	1	1	1	1	1	1	1	1016/1024

[Input Configuration]

● **Dimming data**

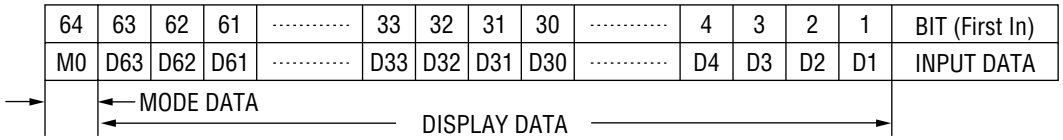
BYTE	B7	B6	B5	B4	B3	B2	B1	B0
1	D8	D7	D6	D5	D7	D3	D2	D1
2	M0	*	*	*	*	*	D10	D9

● **Display Data Input**

When M0="1", the display data input mode is selected and the input data length is 16 bits.
The display data input is valid only when the low level is applied to the $\overline{CS}$ pin.
The display data that was input to DATA-IN is input into the shift register at the rising edge of CLOCK.
The data is automatically loaded to the latched from the shift register at the rising edge of CS.

[Data Configuration]

Display data input mode
Input data: 64bits
Display data: 63 bits
Mode selector: 1 bit



[Input Configuration]

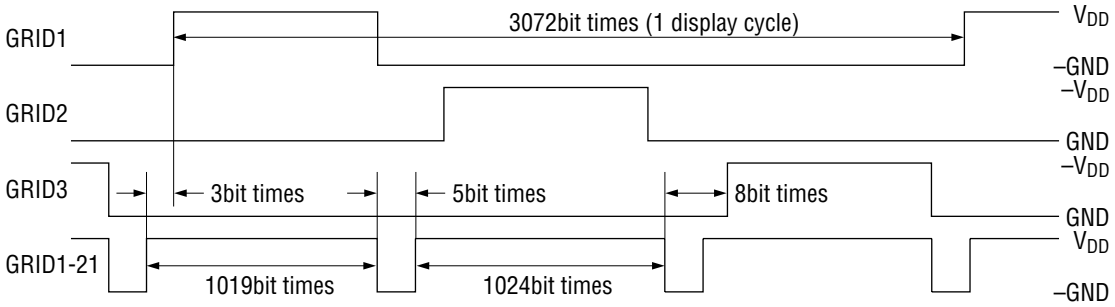
Display data

BYTE	B7	B6	B5	B4	B3	B2	B1	B0
1	D8	D7	D6	D5	D7	D3	D2	D1
2	D16	D15	D14	D13	D12	D11	D10	D9
3	D24	D23	D22	D21	D20	D19	D18	D17
4	D32	D31	D30	D29	D28	D27	D26	D25
5	D40	D39	D38	D37	D36	D35	D34	D33
6	D48	D47	D46	D45	D44	D43	D42	D41
7	D56	D55	D54	D53	D52	D51	D50	D49
8	D64	D63	D62	D61	D60	D59	D58	D57

[Configuration of Segment output and Shift Register]

Segment	GRID 1	GRID 2	GRID 3	Segment	GRID 1	GRID 2	GRID 3	Segment	GRID 1	GRID 2	GRID 3
SEG1	D1	D22	D43	SEG8	D8	D29	D50	SEG15	D15	D36	D57
SEG2	D2	D23	D44	SEG9	D9	D30	D51	SEG16	D16	D37	D58
SEG3	D3	D24	D45	SEG10	D10	D31	D52	SEG17	D17	D38	D59
SEG4	D4	D25	D46	SEG11	D11	D32	D53	SEG18	D18	D39	D60
SEG5	D5	D26	D47	SEG12	D12	D33	D54	SEG19	D19	D40	D61
SEG6	D6	D27	D48	SEG13	D13	D34	D55	SEG20	D20	D41	D62
SEG7	D7	D28	D49	SEG14	D14	D35	D56	SEG21	D21	D42	D63

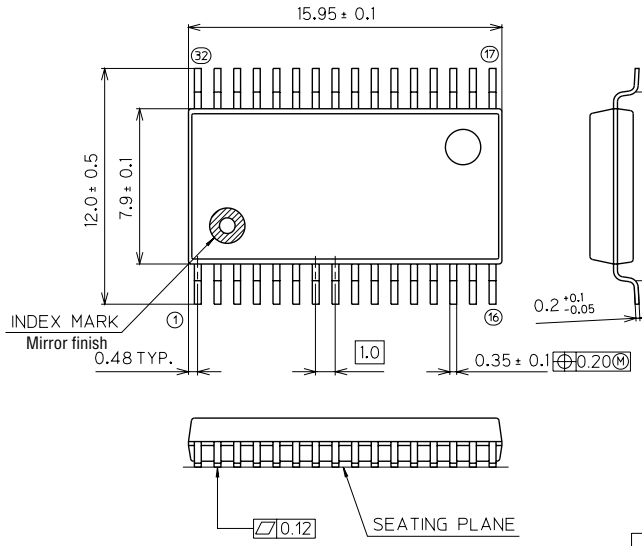
Output Timing *1bit time=4f_{OSC}



PACKAGE DIMENSIONS

(Unit : mm)

SSOP32-P-430-1.00-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.60 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).