This version: Mar. 6. 2000
Previous version: Mar. 8. 1999

OKI Semiconductor

MSC23440D-xxBS10/DS10

4,194,304-word x 40-bit DYNAMIC RAM MODULE : FAST PAGE MODE TYPE

DESCRIPTION

The MSC23440D-xxBS10/DS10 is a 4,194,304-word x 40-bit CMOS dynamic random access memory module which is composed of ten 16Mb DRAMs (4Mx4) in SOJ packages mounted with ten decoupling capacitors. This is a 72-pin single in-line memory module. This module supports any application where high density and large capacity of storage memory are required.

FEATURES

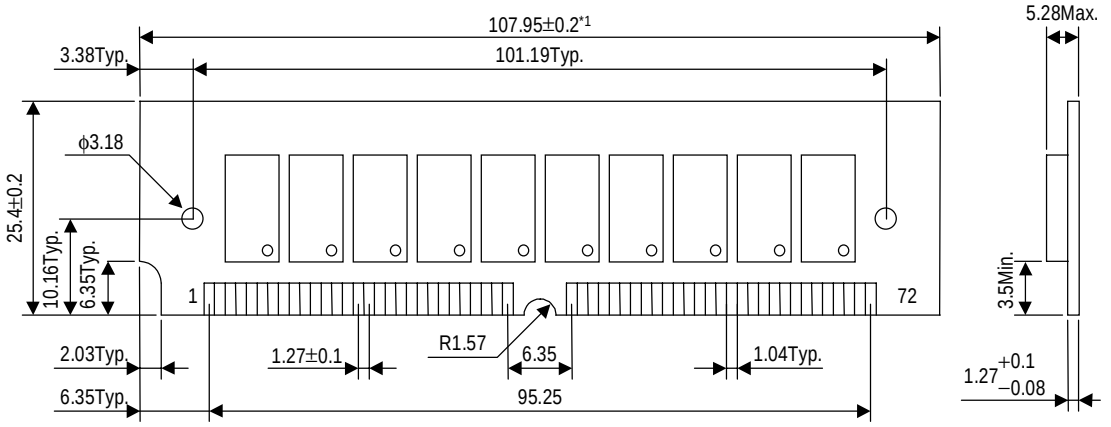
- 4,194,304-word x 40-bit organization
- 72-pin Single In-Line Memory Module
  MSC23440D-xxBS10 : Gold tab
  MSC23440D-xxDS10 : Solder tab
- Single 5V power supply, ±10% tolerance
- Input : TTL compatible
- Output : TTL compatible, 3-state
- Refresh : 2048cycles/32ms
- Fast page mode, read modify write capability
- /CAS before /RAS refresh, hidden refresh, /RAS only refresh capability
- Multi-bit test mode capability

PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation (Max.)	
	t_{RAC}	t_{AA}	t_{CAC}	t_{OEA}		Operating	Standby
MSC23440D-60BS10/DS10	60ns	30ns	15ns	15ns	110ns	4950mW	55mW
MSC23440D-70BS10/DS10	70ns	35ns	20ns	20ns	130ns	4675mW	

MODULE OUTLINE

MSC23440D-xxBS10/DS10 (Unit : mm)



Note:
1. Tolerance over 12.5mm from board edge is ±0.5.

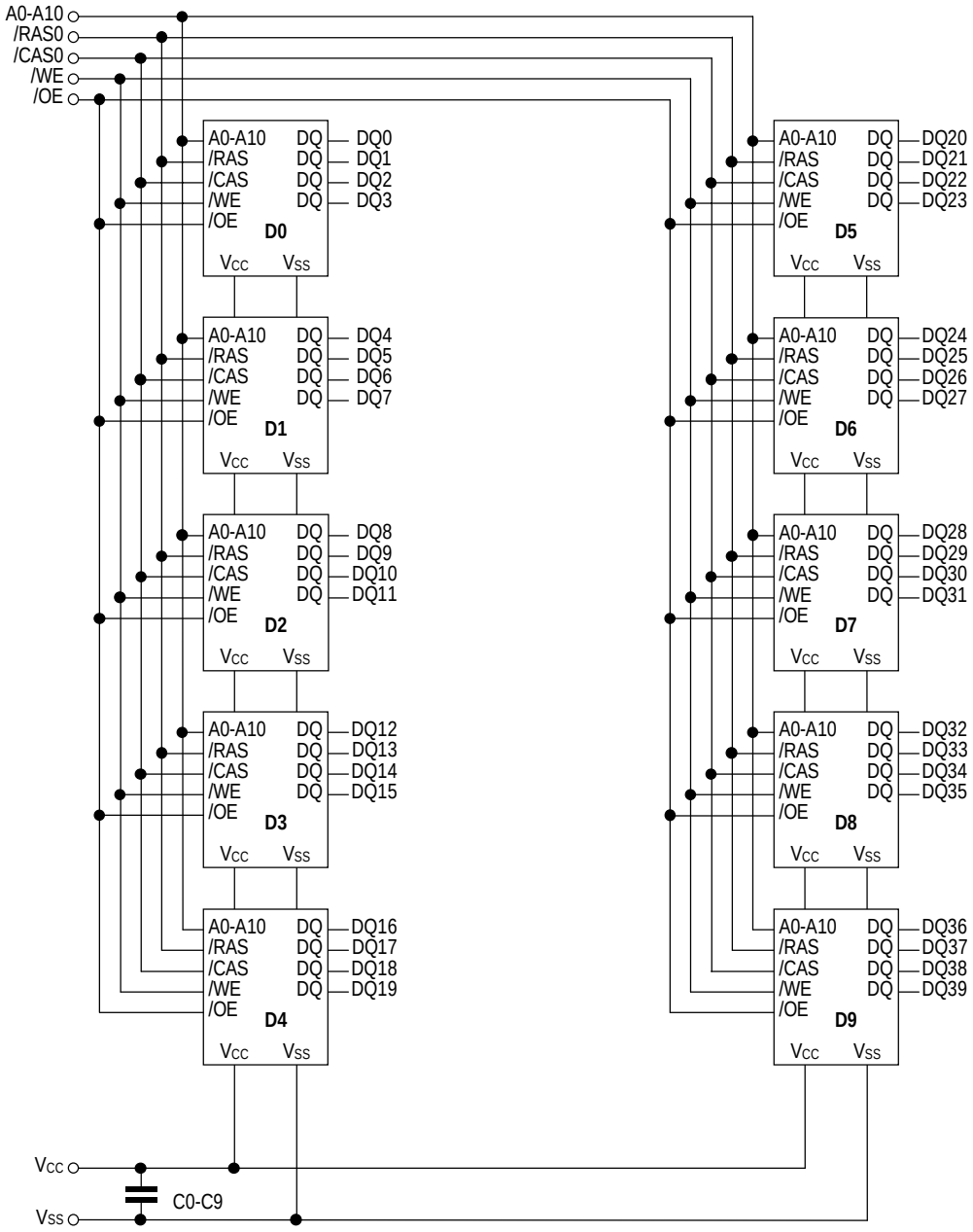
PIN CONFIGURATION

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	19	/OE	37	DQ19	55	DQ28
2	DQ0	20	DQ8	38	DQ20	56	DQ29
3	DQ1	21	DQ9	39	V_{SS}	57	DQ30
4	DQ2	22	DQ10	40	/CAS0	58	DQ31
5	DQ3	23	DQ11	41	A10	59	V_{CC}
6	DQ4	24	DQ12	42	NC	60	DQ32
7	DQ5	25	DQ13	43	NC	61	DQ33
8	DQ6	26	DQ14	44	/RAS0	62	DQ34
9	DQ7	27	DQ15	45	NC	63	DQ35
10	V_{CC}	28	A7	46	DQ21	64	DQ36
11	PD5	29	DQ16	47	/WE	65	DQ37
12	A0	30	V_{CC}	48	V_{SS}	66	DQ38
13	A1	31	A8	49	DQ22	67	PD1
14	A2	32	A9	50	DQ23	68	PD2
15	A3	33	NC	51	DQ24	69	PD3
16	A4	34	NC	52	DQ25	70	PD4
17	A5	35	DQ17	53	DQ26	71	DQ39
18	A6	36	DQ18	54	DQ27	72	V_{SS}

Presence Detect Pins

Pin No.	Pin Name	-60	-70
67	PD1	V_{SS}	V_{SS}
68	PD2	NC	NC
69	PD3	NC	V_{SS}
70	PD4	NC	NC
11	PD5	V_{SS}	V_{SS}

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	–0.5 to 7.0	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D *	10	W
Operating Temperature	T_{OPR}	0 to 70	°C
Storage Temperature	T_{STG}	–40 to 125	°C

*: Ta = 25°C

Recommended Operating Conditions

(Ta = 0°C to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	–0.5	—	0.8	V

Capacitance

(V_{CC} = 5V ±10%, Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A10)	C_{IN1}	—	70	pF
Input Capacitance (/RAS0, /CAS0, /WE, /OE)	C_{IN2}	—	80	pF
I/O Capacitance (DQ0 - DQ39)	$C_{I/O}$	—	16	pF

DC Characteristics

(V_{CC} = 5V ±10%, Ta = 0°C to 70°C)

Parameter	Symbol	Condition	-60		-70		Unit	Note
			Min.	Max.	Min.	Max.		
Output High Voltage	V_{OH}	I_{OH} = –5.0mA	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	I_{OL} = 4.2mA	0	0.4	0	0.4	V	
Input Leakage Current	I_{LI}	0V ≤ V_{IN} ≤ 6.5V; All other pins not under test = 0V	–100	100	–100	100	µA	
Output Leakage Current	I_{LO}	DQ disable 0V ≤ V_{OUT} ≤ V_{CC}	–10	10	–10	10	µA	
Average Power Supply Current (Operating)	I_{CC1}	/RAS, /CAS cycling, t_{RC} = Min.	—	900	—	850	mA	1, 2
Power supply current (Standby)	I_{CC2}	/RAS, /CAS = V_{IH}	—	20	—	20	mA	1
		/RAS, /CAS ≥ V_{CC} – 0.2V	—	10	—	10		
Average Power Supply Current (/RAS only refresh)	I_{CC3}	/RAS cycling, /CAS = V_{IH}, t_{RC} = Min.	—	900	—	850	mA	1, 2
Average Power Supply Current (/CAS before /RAS refresh)	I_{CC6}	/RAS cycling, /CAS before /RAS	—	900	—	850	mA	1, 2
Average Power Supply Current (Fast Page Mode)	I_{CC7}	/RAS = V_{IL}, /CAS cycling, t_{PC} = Min.	—	700	—	650	mA	1, 3

Notes: 1. I_{CC} Max. is specified as I_{CC} for output open condition.
2. The address can be changed once or less while /RAS = V_{IL}.
3. The address can be changed once or less while /CAS = V_{IH}.

AC Characteristics (1/2)

(V_{CC} = 5V ±10%, Ta = 0°C to 70°C) Note: 1, 2, 3, 11, 12

Parameter	Symbol	-60		-70		Unit	Note
		Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	110	—	130	—	ns	
Read Modify Write Cycle Time	t_{RWC}	155	—	180	—	ns	
Fast Page Mode Cycle Time	t_{PC}	40	—	45	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t_{PRWC}	85	—	95	—	ns	
Access Time from /RAS	t_{RAC}	—	60	—	70	ns	4, 5, 6
Access Time from /CAS	t_{CAC}	—	15	—	20	ns	4, 5
Access Time from Column Address	t_{AA}	—	30	—	35	ns	4, 6
Access Time from /CAS Precharge	t_{CPA}	—	35	—	40	ns	4
Access Time from /OE	t_{OEA}	—	15	—	20	ns	4
Output Low Impedance Time from /CAS	t_{CLZ}	0	—	0	—	ns	4
/CAS to Data Output Buffer Turn-off Delay Time	t_{OFF}	0	15	0	20	ns	7
/OE to Data Output Buffer Turn-off Delay Time	t_{OEZ}	0	15	0	20	ns	7
Transition Time	t_T	3	50	3	50	ns	3
Refresh Period	t_{REF}	—	32	—	32	ms	
/RAS Precharge Time	t_{RP}	40	—	50	—	ns	
/RAS Pulse Width	t_{RAS}	60	10K	70	10K	ns	
/RAS Pulse Width (Fast Page Mode)	t_{RASP}	60	100K	70	100K	ns	
/RAS Hold Time	t_{RSH}	15	—	20	—	ns	
/RAS Hold Time referenced to /OE	t_{ROH}	15	—	20	—	ns	
/CAS Precharge Time (Fast Page Mode)	t_{CP}	10	—	10	—	ns	
/CAS Pulse Width	t_{CAS}	15	10K	20	10K	ns	
/CAS Hold Time	t_{CSH}	60	—	70	—	ns	
/CAS to /RAS Precharge Time	t_{CRP}	5	—	5	—	ns	
/RAS Hold Time from /CAS Precharge	t_{RHCP}	35	—	40	—	ns	
/RAS to /CAS Delay Time	t_{RCD}	20	45	20	50	ns	5
/RAS to Column Address Delay Time	t_{RAD}	15	30	15	35	ns	6
Row Address Set-up Time	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	10	—	15	—	ns	
Column Address to /RAS Lead Time	t_{RAL}	30	—	35	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	ns	8
Read Command Hold Time referenced to /RAS	t_{RRH}	0	—	0	—	ns	8

AC Characteristics (2/2)

(V_{CC} = 5V ±10%, Ta = 0°C to 70°C) Note: 1, 2, 3, 11, 12

Parameter	Symbol	-60		-70		Unit	Note
		Min.	Max.	Min.	Max.		
Write Command Set-up Time	t_{WCS}	0	—	0	—	ns	9
Write Command Hold Time	t_{WCH}	10	—	10	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	ns	
/OE Command Hold Time	t_{OEH}	15	—	20	—	ns	
Write Command to /RAS Lead Time	t_{RWL}	15	—	20	—	ns	
Write Command to /CAS Lead Time	t_{CWL}	15	—	20	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	ns	10
Data-in Hold Time	t_{DH}	10	—	15	—	ns	10
/OE to Data-in Delay Time	t_{OED}	15	—	20	—	ns	
/CAS to /WE Delay Time	t_{CWD}	40	—	45	—	ns	9
Column Address to /WE Delay Time	t_{AWD}	55	—	60	—	ns	9
/RAS to /WE Delay Time	t_{RWD}	85	—	95	—	ns	9
/CAS Precharge /WE Delay Time	t_{CPWD}	60	—	70	—	ns	9
/CAS Active Delay Time from /RAS Precharge	t_{RPC}	5	—	5	—	ns	
/RAS to /CAS Set-up Time (/CAS before /RAS)	t_{CSR}	10	—	10	—	ns	
/RAS to /CAS Hold Time (/CAS before /RAS)	t_{CHR}	10	—	10	—	ns	
/WE to /RAS Precharge Time (/CAS before /RAS)	t_{WRP}	10	—	10	—	ns	
/WE Hold Time from /RAS (/CAS before /RAS)	t_{WRH}	10	—	10	—	ns	
/RAS to /WE Set-up Time (Test Mode)	t_{WTS}	10	—	10	—	ns	
/RAS to /WE Hold Time (Test Mode)	t_{WTH}	10	—	10	—	ns	

Notes: 1. A start-up delay of 200µs is required after power-up, followed by a minimum of eight initialization cycles (/RAS only refresh or /CAS before /RAS refresh) before proper device operation is achieved.

2. The AC characteristics assumes t_T = 5ns.

3. V_{IH}(Min.) and V_{IL}(Max.) are reference levels for measuring input timing signals. Transition times (t_T) are measured between V_{IH} and V_{IL}.

4. This parameter is measured with a load circuit equivalent to 2 TTL loads and 100pF.

5. Operation within the t_{RCD}(Max.) limit ensures that t_{RAC}(Max.) can be met.
t_{RCD}(Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(Max.) limit, then the access time is controlled by t_{CAC}.

6. Operation within the t_{RAD}(Max.) limit ensures that t_{RAC}(Max.) can be met.
t_{RAD}(Max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(Max.) limit, then the access time is controlled by t_{AA}.

7. t_{OFF}(Max.) and t_{OEZ}(Max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.

8. t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. t_{WCS}, t_{CWD}, t_{RWD}, t_{AWD} and t_{CPWD} are not restrictve operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(Min.), then the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$(Min.), $t_{RWD} \geq t_{RWD}$(Min.), $t_{AWD} \geq t_{AWD}$(Min.) and $t_{CPWD} \geq t_{CPWD}$(Min.), then the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, then the condition of the data out (at access time) is indeterminate.

10. These parameters are referenced to the /CAS leading edge in an early write cycle, and to the /WE leading edge in an /OE control write cycle, or a read modify write cycle.

11. The test mode is initiated by performing a /WE and /CAS before /RAS refresh cycle. This mode is latched and remains in effect until the exit cycle is generated. The test mode specified in this data sheet is a 4-bit parallel test function. CA0 and CA1 are not used. In a read cycle, if all internal bits are equal, the DQ pin will indicate a high level. If any internal bits are not equal, the DQ pin will indicate a low level. The test mode is cleared and the memory device returned to its normal operating state by a /RAS only refresh or /CAS before /RAS refresh cycle.

12. In a test mode read cycle, the value of access time parameters is delayed for 5ns for the specified value. These parameters should be specified in test mode cycle by adding the above value to the specified value in this data sheet.