

OKI Semiconductor

1A

MSM27V1655CZ

524,288-Double Word x 32-Bit or 1,048,576-Word x 16-Bit

4-Double Word x 32-Bit or 8-Word x 16-Bit Page Mode One Time PROM

DESCRIPTION

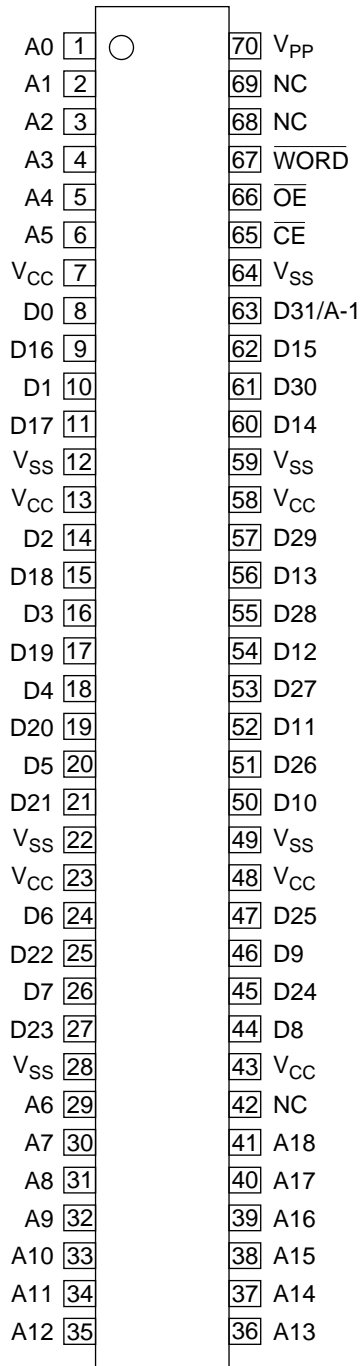
The MSM27V1655CZ is a 16Mbit electrically Programmable Read-Only Memory with page mode. Its configuration can be electrically switched between 524,288 double word x 32bit and 1,048,576word x 16bit. The MSM27V1655CZ operates on a single +3.3V power supply and is TTL compatible. The MSM27V1655CZ provides Page mode which can greatly reduce the read access time. Since the MSM27V1655CZ operates asynchronously, external clocks are not required, making this device easy-to-use. The MSM27V1655CZ is suitable as large-capacity fixed memory for microcomputers and data terminals. It is manufactured using a CMOS double silicon gate technology and is offered in 70-pin SSOP, 70-pin TSOP packages.

FEATURES

- 524,288 double word x 32bit / 1,048,576 word x 16bit electrically switchable configuration
- Single +3.3V power supply
- Access time 100ns
 - Page mode access time 30ns
- Input / Output TTL compatible
- Three-state output
- Packages

70-pin plastic SSOP (SSOP70-P-500-0.80-K)
70-pin plastic TSOP (TSOP1170-P-400-0.65-K)

PIN CONFIGURATION (TOP VIEW)

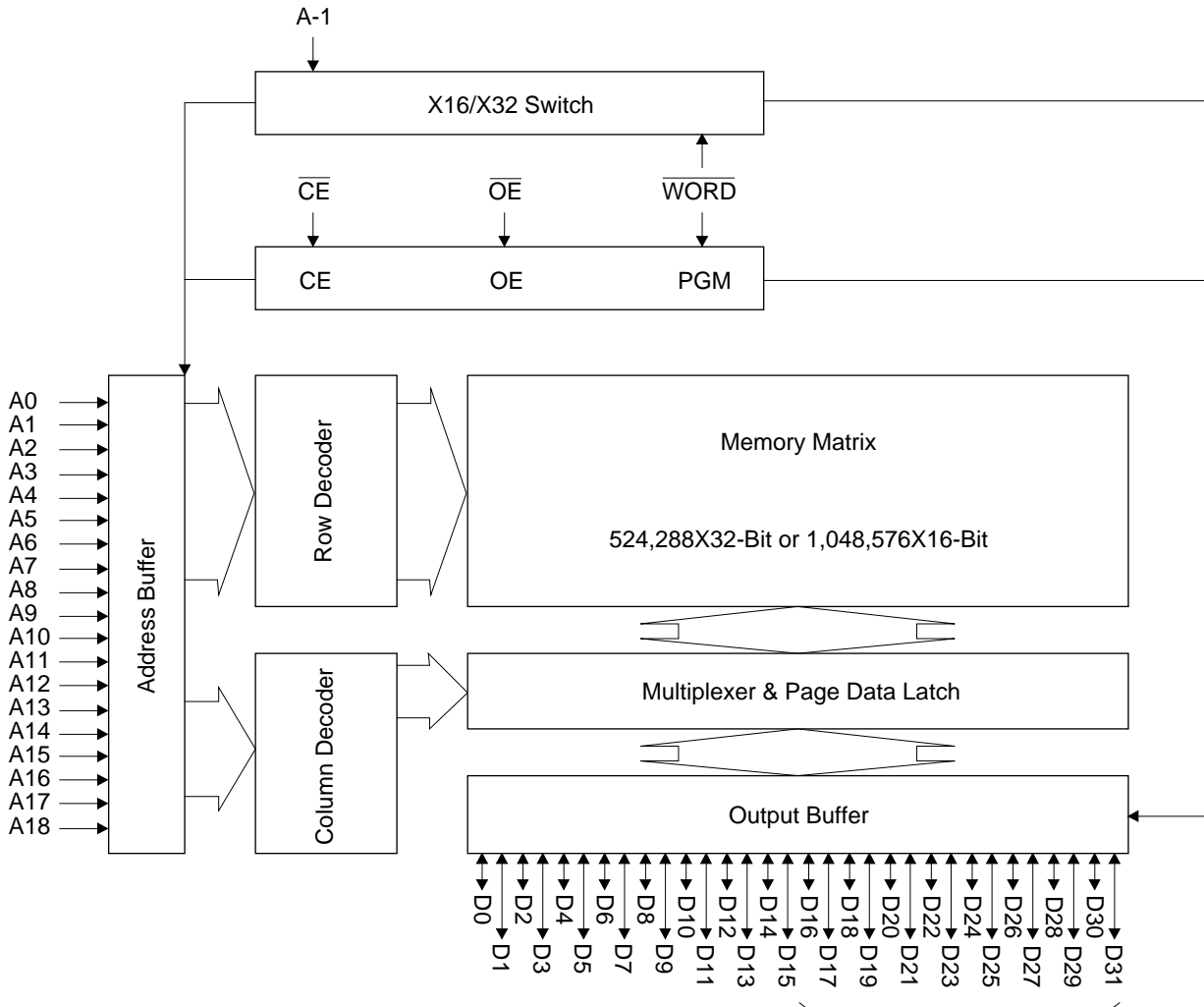


PIN NAMES	FUNCTIONS
D31/A-1	Data output / Address input
A0 - A18	Address input
D0 - D30	Data output
CE	Chip enable
OE	Output enable
V _{CC}	Power supply voltage
V _{SS}	GND
WORD	Mode switch
V _{PP}	Program power supply voltage
NC	Non connection

70-pin SSOP , TSOP

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BLOCK DIAGRAM



In 16-bit output mode, these pins are three-stated and pin D31 functions as the A-1 address pin.

FUNCTION TABLE

MODE	CE	OE	WORD	V _{PP}	V _{CC}	D0 - D15	D16 - D30	D31/A-1
READ (32-Bit)	L	L	H	*	3.0V to 3.6V	D _{OUT}		
READ (16-Bit)	L	L	L			D _{OUT}	Hi-Z	L/H
OUTPUT DISABLE	L	H	H			Hi-Z		*
			L			Hi-Z		*
STAND-BY	H	*	H	Hi-Z		*		
			L	Hi-Z		*		
PROGRAM	L	H	L	11.0V	5.0V	D _{IN}	Hi-Z	L/H
PROGRAM INHIBIT	H	H				Hi-Z		
PROGRAM VERIFY	H	L				D _{OUT}	Hi-Z	L/H

*: Don't Care

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Value	Unit
Operating temperature under bias	T_{opr}	-	0 to 70	°C
Storage temperature	T_{stg}	-	-55 to 125	°C
Input voltage	V_I	relative to V_{SS}	-0.5 to $V_{CC} + 0.5$	V
Output voltage	V_O		-0.5 to $V_{CC} + 0.5$	V
Power supply voltage	V_{CC}		-0.5 to 7	V
Program power supply voltage	V_{PP}		-0.5 to 12.5	V
Power dissipation per package	P_D	-	1.0	W

RECOMMENDED OPERATING CONDITIONS FOR READ

(Ta=0 to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
V_{CC} power supply voltage	V_{CC}	$V_{CC}=3.0V-3.6V$	3.0	-	3.6	V
V_{PP} power supply voltage	V_{PP}		-0.5	-	$V_{CC}+0.5$	V
Input "H" level	V_{IH}		2.2	-	$V_{CC}+0.5$	V
Input "L" level	V_{IL}		-0.5	-	0.6	V

Voltage is relative to V_{SS}

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ELECTRICAL CHARACTERISTICS (Read operation)

DC Characteristics

($V_{CC}=3.3V\pm 0.3V$, $T_a=0$ to $70^\circ C$)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input leakage current	I_{LI}	$V_I=0$ to V_{CC}	-	-	10	μA
Output leakage current	I_{LO}	$V_O=0$ to V_{CC}	-	-	10	μA
V_{CC} power supply current (Standby)	I_{CS1}	$\overline{CE}=V_{CC}$	-	-	50	μA
	I_{CS2}	$\overline{CE}=V_{IH}$	-	-	1	mA
V_{CC} power supply current (Read)	I_{CCA}	$\overline{CE}=V_{IL}$, $\overline{OE}=V_{IH}$ $t_c=100ns$	-	-	80	mA
V_{PP} power supply current	I_{PP}	$V_{PP}=V_{CC}$	-	-	10	μA
Input "H" level	V_{IH}	-	2.2	-	$V_{CC}+0.5$	V
Input "L" level	V_{IL}	-	-0.5	-	0.6	V
Output "H" level	V_{OH}	$I_{OH}=-400\mu A$	2.4	-	-	V
Output "L" level	V_{OL}	$I_{OL}=2.1mA$	-	-	0.45	V

Voltage is relative to V_{SS}

AC Characteristics

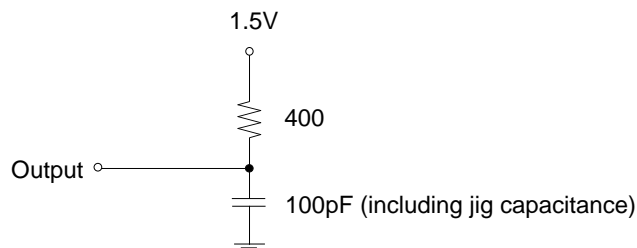
($V_{CC}=3.3V\pm 0.3V$, $T_a=0$ to $70^\circ C$)

Parameter	Symbol	Condition	Min.	Max.	Unit
Address access cycle time	T_C	-	100	-	ns
Address access time	T_{ACC}	$\overline{CE}=\overline{OE}=V_{IL}$	-	100	ns
Page set up time	T_{PSET}	NOTE(1)	120	-	ns
Page access cycle time	T_{PC}	-	30	-	ns
Page access time	T_{PAC}	-	-	30	ns
\overline{CE} access time	T_{CE}	$\overline{OE}=V_{IL}$	-	100	ns
\overline{OE} access time	T_{OE}	$\overline{CE}=V_{IL}$	-	30	ns
Output disable time	T_{CHZ}	$\overline{OE}=V_{IL}$	0	30	ns
	T_{OHZ}	$\overline{CE}=V_{IL}$	0	25	ns
Output hold time	T_{OH}	$\overline{CE}=\overline{OE}=V_{IL}$	0	-	ns

NOTE(1) T_{PSET} is defined as the end of either \overline{CE} trailing edge or address transition in random access term until the first page address transition.

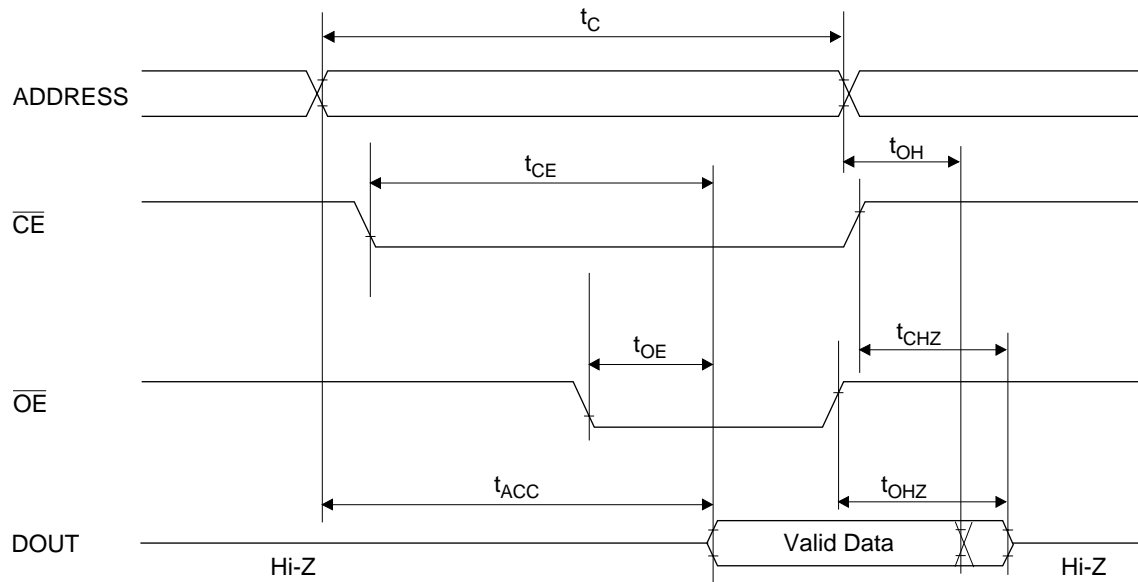
Measurement conditions

- Input signal level ----- 0V/3V
- Input timing reference level ----- 0.8V/2.0V
- Output load ----- 100pF
- Output timing reference level ----- 0.8V/2.0V

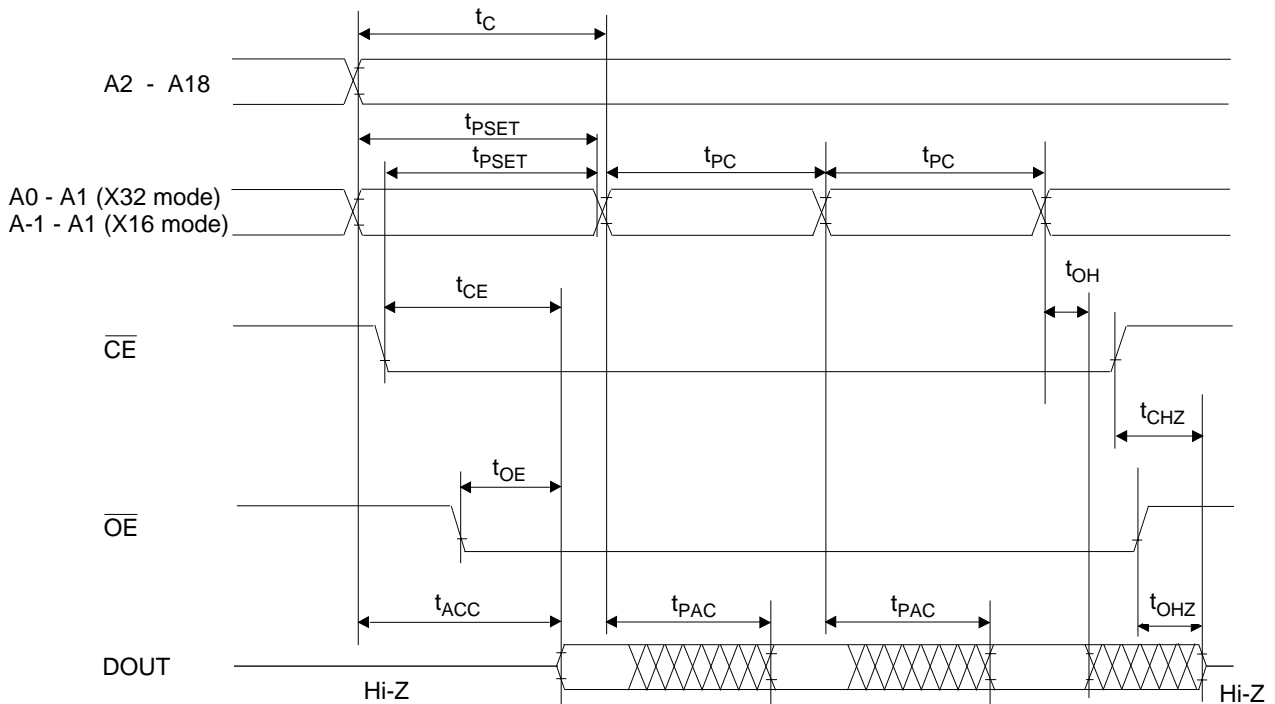


TIMING CHART

NORMAL MODE READ CYCLE



PAGE MODE READ CYCLE



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ELECTRICAL CHARACTERISTICS (Programming operation)**DC Characteristics**

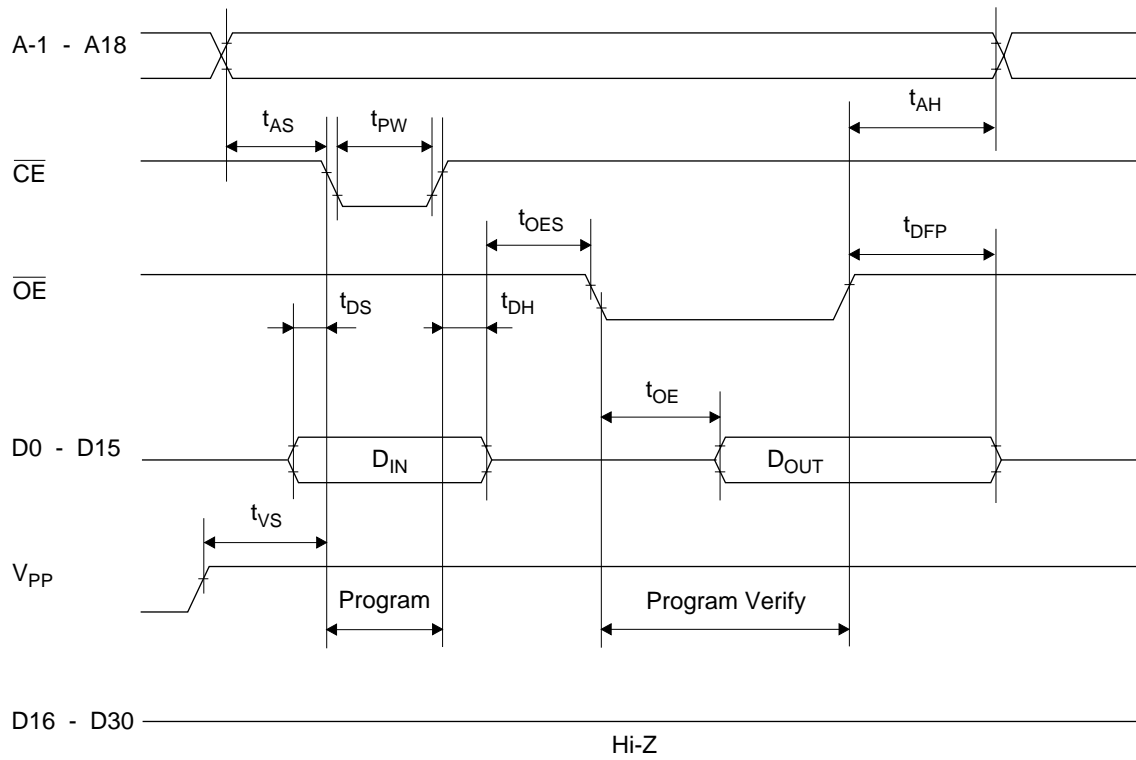
(Ta=25°C±5°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input leakage current	I _{LI}	V _I =V _{CC} +0.5V	-	-	10	μA
V _{PP} power supply current (Program)	I _{PP2}	$\overline{CE}=V_{IL}$	-	-	50	mA
V _{CC} power supply current	I _{CC}	-	-	-	100	mA
Input "H" level	V _{IH}	-	2.2	-	V _{CC} +0.5	V
Input "L" level	V _{IL}	-	-0.5	-	0.8	V
Output "H" level	V _{OH}	I _{OH} =-400μA	2.4	-	-	V
Output "L" level	V _{OL}	I _{OL} =2.1mA	-	-	0.45	V
Program voltage	V _{PP}	-	10.75	11.0	11.25	V
V _{CC} power supply voltage	V _{CC}	-	4.75	5.0	5.25	V

Voltage is relative to V_{SS}**AC Characteristics**(V_{CC}=5.0V±0.25V, V_{pp}=11.0V±0.25V, Ta=25°C±5°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Address set-up time	T _{AS}	-	2	-	-	μs
\overline{OE} set-up time	T _{OES}	-	2	-	-	μs
Data set-up time	T _{DS}	-	2	-	-	μs
Address hold time	T _{AH}	-	0	-	-	μs
Data hold time	T _{DH}	-	2	-	-	μs
Output float delay from \overline{OE}	T _{DFP}	-	0	-	130	ns
V _{PP} voltage set-up time	T _{VS}	-	2	-	-	μs
Program pulse width	T _{PW}	-	23	25	27	μs
Data valid from \overline{OE}	T _{OE}	-	-	-	150	ns

Programming Waveform



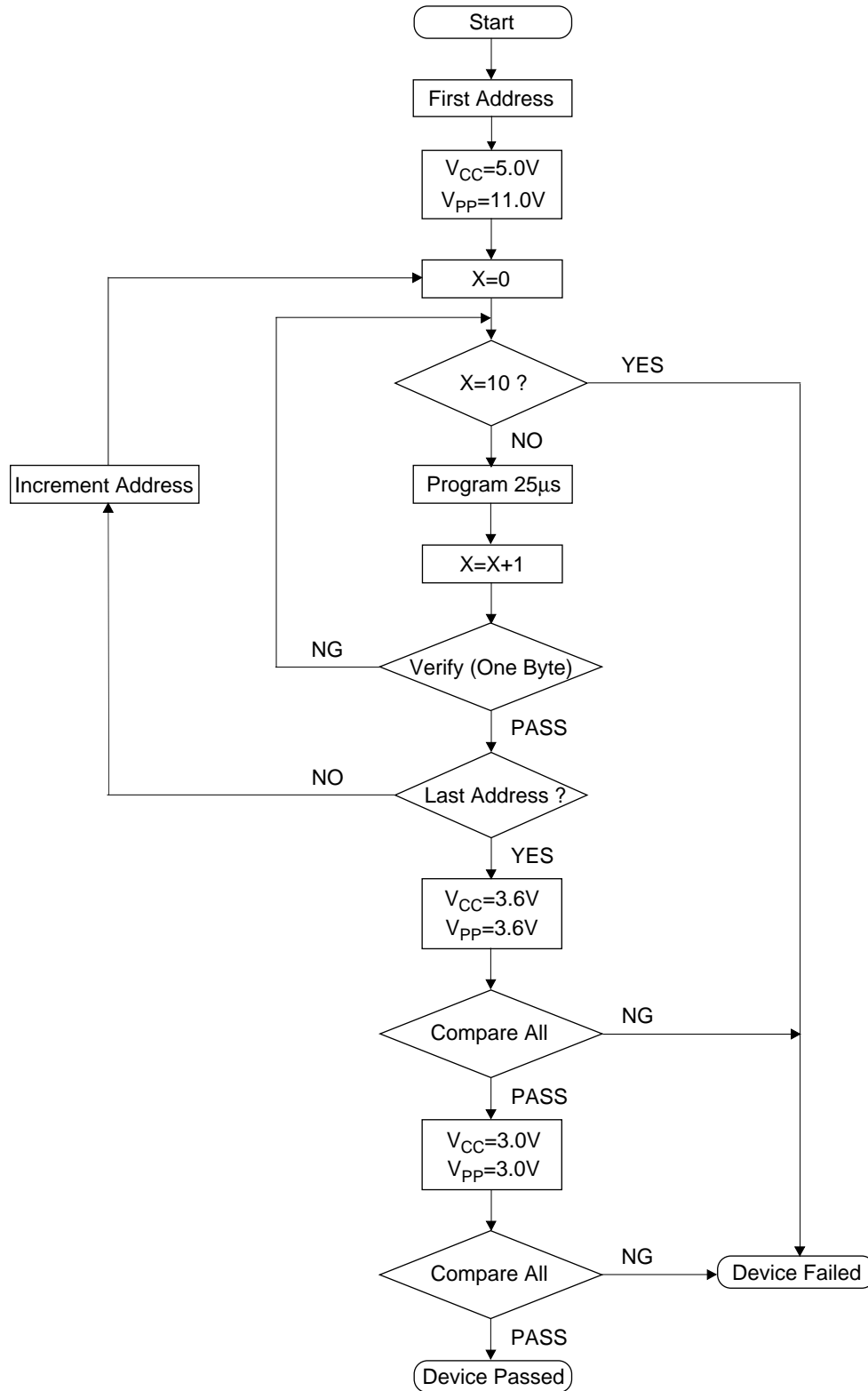
PIN Capacitance

($V_{CC}=3.3V$, $T_a=25^\circ C$, $f=1MHz$)

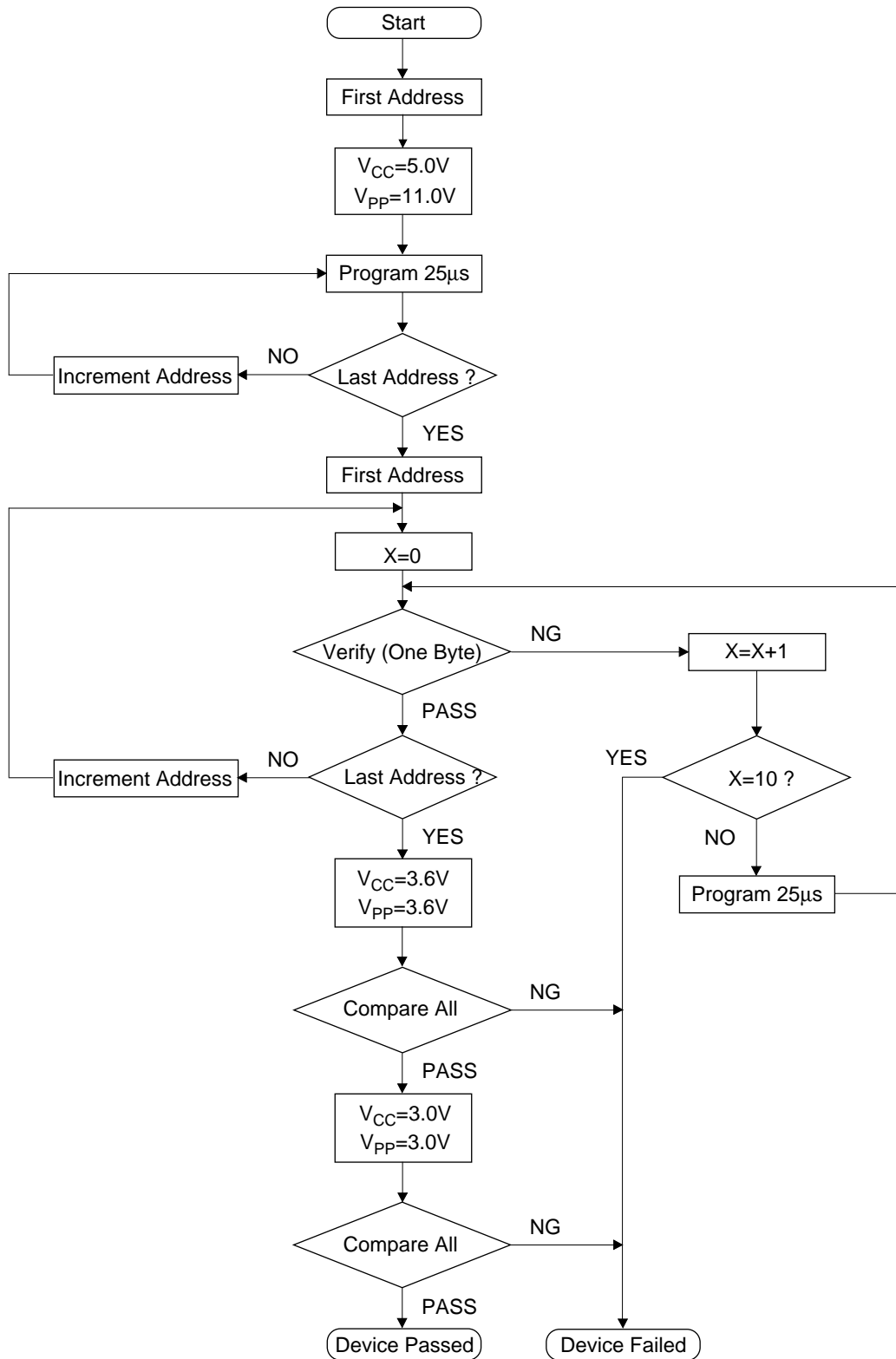
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input	C_{IN1}	$V_I=0V$	-	-	12	pF
V_{PP}	C_{IN2}		-	-	60	
Output	C_{OUT}	$V_O=0V$	-	-	15	

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High Speed Programming Algorithm (I)



High Speed Programming Algorithm (II)



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