OKI Semiconductor

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MSM5416258A

262,144-Word × 16-Bit DYNAMIC RAM : FAST PAGE MODE TYPE WITH EDO

DESCRIPTION

The MSM5416258A is a 262,144-word × 16-bit dynamic RAM fabricated in Oki's CMOS silicon gate technology. The MSM5416258A achieves high integration, high-speed operation, and low-power consumption because Oki manufactures the device in a quadruple-layer polysilicon/double-layer metal CMOS process. The MSM5416258A is available in a 44/40-pin plastic TSOP.

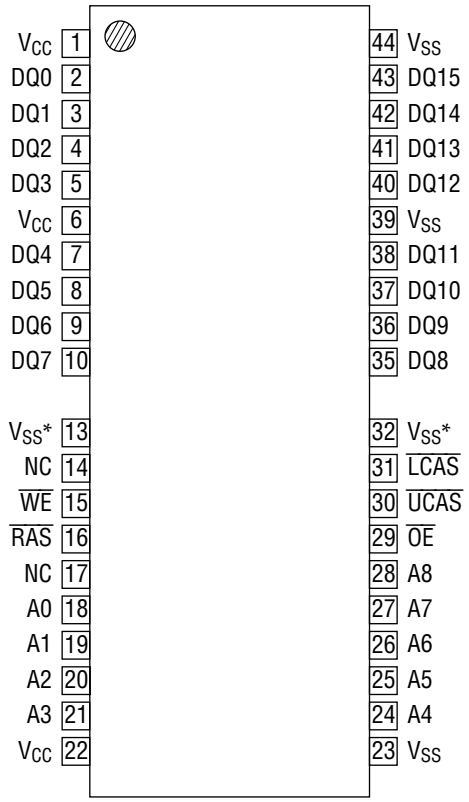
FEATURES

- 262,144-word × 16-bit configuration
- Single 5.0 V power supply, ±0.5 V tolerance
- Input: TTL compatible
- Output: TTL compatible, 3-state
- Refresh: 512 cycles/8 ms
- Fast page mode with EDO, read modify write capability
- Byte wide control: 2 $\overline{CAS}$ control
- $\overline{CAS}$ before $\overline{RAS}$ refresh, hidden refresh, $\overline{RAS}$ only refresh capability
- Package :
  44/40-pin 400 mil plastic TSOP (Type II) (TSOPII44/40-P-400-0.80-K) (Product : MSM5416258A-xxTS-K)
  xx indicates speed rank.

PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)		Power Dissipation (Max.)
	t_{RAC}	t_{AA}	t_{CAC}	t_{OEA}	t_{RC}	t_{HPC}	
MSM5416258A-40	40 ns	22 ns	10 ns	10 ns	80 ns	15 ns	825 mW
MSM5416258A-45	45 ns	24 ns	12 ns	12 ns	90 ns	20 ns	770 mW

PIN CONFIGURATION (TOP VIEW)



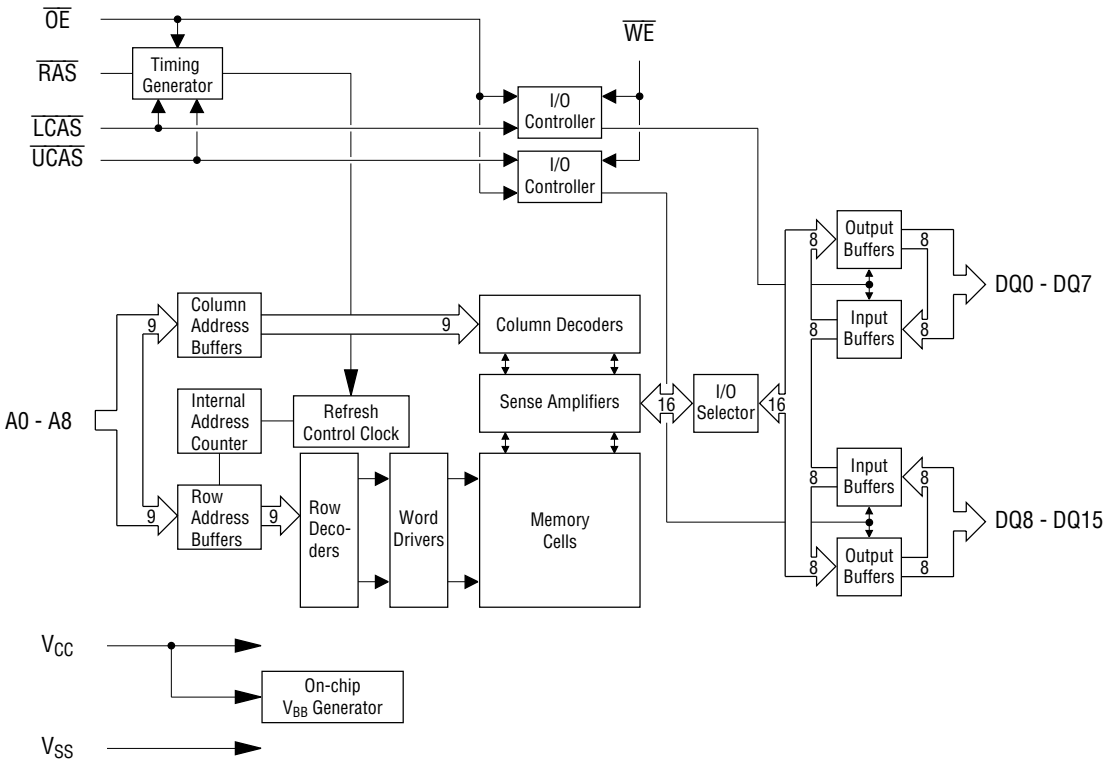
44/40-Pin Plastic TSOP (II)
(K Type)

Pin Name	Function
A0 - A8	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{LCAS}$, $\overline{UCAS}$	Column Address Strobe
DQ0 - DQ15	Data - Input / Data - Output
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply (5.0 V)
V_{SS}	Ground (0 V)
NC	No Connection
V_{SS}*	Ground (0 V)*

Note: The same power supply voltage must be provided to every V_{CC} pin, and the same GND voltage level must be provided to every V_{SS} pin.

: For improved signal integrity, it is recommended to connect the V_{SS} pins, pin 13 and pin 32, to GND: the pins are electrically connected to internal GND.

BLOCK DIAGRAM



FUNCTION TABLE

Input Pin					DQ Pin		Function Mode
$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	DQ0 - DQ7	DQ8 - DQ15	
H	*	*	*	*	High-Z	High-Z	Standby
L	H	H	*	*	High-Z	High-Z	Refresh
L	L	H	H	L	D_{OUT}	High-Z	Lower Byte Read
L	H	L	H	L	High-Z	D_{OUT}	Upper Byte Read
L	L	L	H	L	D_{OUT}	D_{OUT}	Word Read
L	L	H	L	H	D_{IN}	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	D_{IN}	Upper Byte Write
L	L	L	L	H	D_{IN}	D_{IN}	Word Write
L	L	L	H	H	High-Z	High-Z	—

* : "H" or "L"

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	Ta = 25°C	–1.0 to 7.0	V
Short Circuit Output Current	I_{OS}	Ta = 25°C	50	mA
Power Dissipation	P_D	Ta = 25°C	1	W
Operating Temperature	T_{opr}	—	0 to 70	°C
Storage Temperature	T_{stg}	—	–55 to 150	°C

Recommended Operating Conditions

(Ta = 0°C to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	V_{CC} + 1.0	V
Input Low Voltage	V_{IL}	–1.0	—	0.8	V

Capacitance

(V_{CC} = 5.0 V ±0.5 V, Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A8)	C_{IN1}	—	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{WE}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Input / Output Capacitance (DQ0 - DQ15)	$C_{I/O}$	—	7	pF

DC Characteristics

(V_{CC} = 5.0 V ±0.5 V, Ta = 0°C to 70°C)

Parameter	Symbol	Condition	MSM5416258A -40		MSM5416258A -45		Unit	Note
			Min.	Max.	Min.	Max.		
Output High Voltage	V_{OH}	I_{OH} = –2.5 mA	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	I_{OL} = 2.0 mA	0	0.4	0	0.4	V	
Input Leakage Current	I_{LI}	0 V ≤ V_I ≤ V_{CC}	–10	10	–10	10	µA	
Output Leakage Current	I_{LO}	DQi Disable 0 V ≤ V_O ≤ 5.5 V	–10	10	–10	10	µA	
Average Power Supply Current (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = Min.	—	150	—	140	mA	1, 2
Power Supply Current (Standby)	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	—	3	—	3	mA	1
Average Power Supply Current ($\overline{RAS}$ Only Refresh)	I_{CC3}	$\overline{RAS}$ = Cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = Min.	—	150	—	140	mA	1, 2
Average Power Supply Current (Fast Page Mode)	I_{CC4}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling, t_{HPC} = Min.	—	130	—	115	mA	1, 3
Average Power Supply Current ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	I_{CC5}	$\overline{RAS}$ = Cycling, $\overline{CAS}$ before $\overline{RAS}$	—	150	—	140	mA	1, 2

Notes : 1. I_{CC} Max. is specified as I_{CC} for output open condition.
2. The address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. The address can be changed once or less while $\overline{CAS}$ = V_{IH}.

AC Characteristics (1/2)

(V_{CC} = 5.0 V ±0.5 V, Ta = 0°C to 70°C)

Parameter	Symbol	MSM5416258A -40		MSM5416258A -45		Unit	Note
		Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	80	—	90	—	ns	
Read Modify Write Cycle Time	t_{RWC}	115	—	130	—	ns	
Fast Page Mode Cycle Time	t_{HPC}	15	—	20	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t_{PRWC}	55	—	60	—	ns	
Access Time from $\overline{RAS}$	t_{RAC}	—	40	—	45	ns	7, 12, 13
Access Time from $\overline{CAS}$	t_{CAC}	—	10	—	12	ns	7, 12
Access Time from Column Address	t_{AA}	—	22	—	24	ns	7, 13
Access Time from $\overline{OE}$	t_{OEA}	—	10	—	12	ns	
Access Time from $\overline{CAS}$ Precharge	t_{CPA}	—	22	—	24	ns	7, 12
Output Low Impedance Time from $\overline{CAS}$	t_{CLZ}	0	—	0	—	ns	
Data Hold After $\overline{CAS}$ Low	t_{COH}	3	—	3	—	ns	17
Output Buffer Turn-off Delay Time	t_{OFF}	3	8	3	8	ns	8
Output Buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	3	8	3	8	ns	8
Output Buffer Turn-off Delay Time from $\overline{RAS}$	t_{REZ}	1.5	8	1.5	8	ns	8
Output Buffer Turn-off Delay Time from $\overline{WE}$	t_{WEZ}	3	8	3	8	ns	8
Transition Time	t_T	2	35	2	35	ns	
Refresh Period	t_{REF}	—	8	—	8	ms	
$\overline{RAS}$ Precharge Time	t_{RP}	30	—	35	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	40	10,000	45	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	40	100,000	45	100,000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	8	—	10	—	ns	
$\overline{RAS}$ Hold Time Reference to $\overline{OE}$	t_{ROH}	8	—	8	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	5	—	6	—	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	6	10,000	7	10,000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	35	—	35	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	—	5	—	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	22	—	24	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	18	30	18	30	ns	12
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	13	18	13	18	ns	13
Row Address Set-up Time	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	8	—	8	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	6	—	6	—	ns	
Column Address Hold Time from $\overline{RAS}$	t_{AR}	30	—	30	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	22	—	24	—	ns	

AC Characteristics (2/2)

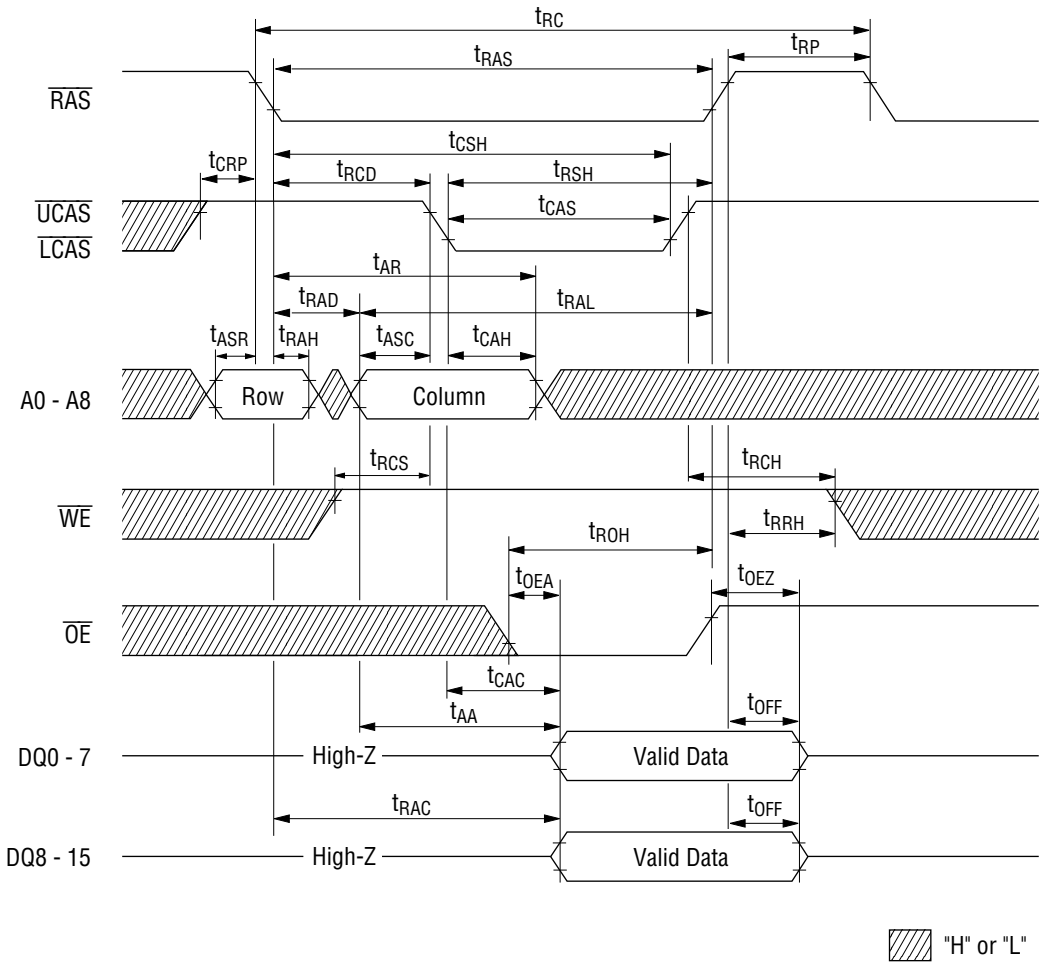
(V_{CC} = 5.0 V ±0.5 V, Ta = 0°C to 70°C)

Parameter	Symbol	MSM5416258A -40		MSM5416258A -45		Unit	Note
		Min.	Max.	Min.	Max.		
Read Command Set-up Time	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	ns	9
Read Command Hold Time Reference to $\overline{RAS}$	t_{RRH}	0	—	0	—	ns	9
$\overline{WE}$ Pulse Width (DQ Disable)	t_{WEP}	10	—	10	—	ns	
Write Command Set-up Time	t_{WCS}	0	—	0	—	ns	11
Write Command Hold Time	t_{WCH}	6	—	6	—	ns	
Write Command Pulse Width	t_{WP}	6	—	6	—	ns	
Write Command Hold Time from $\overline{RAS}$	t_{WCR}	30	—	30	—	ns	
$\overline{OE}$ Command Hold Time	t_{OEH}	6	—	7	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	6	—	7	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	8	—	9	—	ns	
Data to $\overline{CAS}$ Delay Time	t_{DZC}	0	—	0	—	ns	
Data to $\overline{OE}$ Delay Time	t_{DZO}	0	—	0	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	ns	10
Data-in Hold Time	t_{DH}	6	—	7	—	ns	10
Data-in Hold Time referenced to $\overline{RAS}$	t_{DHR}	30	—	30	—	ns	
$\overline{OE}$ to Data-in Delay Time	t_{OED}	8	—	8	—	ns	
$\overline{OE}$ "L" to $\overline{CAS}$ "H" Lead Time	t_{OCH}	10	—	10	—	ns	
$\overline{CAS}$ "H" to $\overline{OE}$ "L" Lead Time	t_{CHO}	10	—	10	—	ns	
Hi-Z Command Pulse Width	t_{OEP}	10	—	10	—	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	22	—	22	—	ns	11
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	32	—	32	—	ns	11
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	50	—	55	—	ns	11
$\overline{CAS}$ Active Delay Time from $\overline{RAS}$ Precharge	t_{RPC}	0	—	0	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	—	10	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	10	—	10	—	ns	

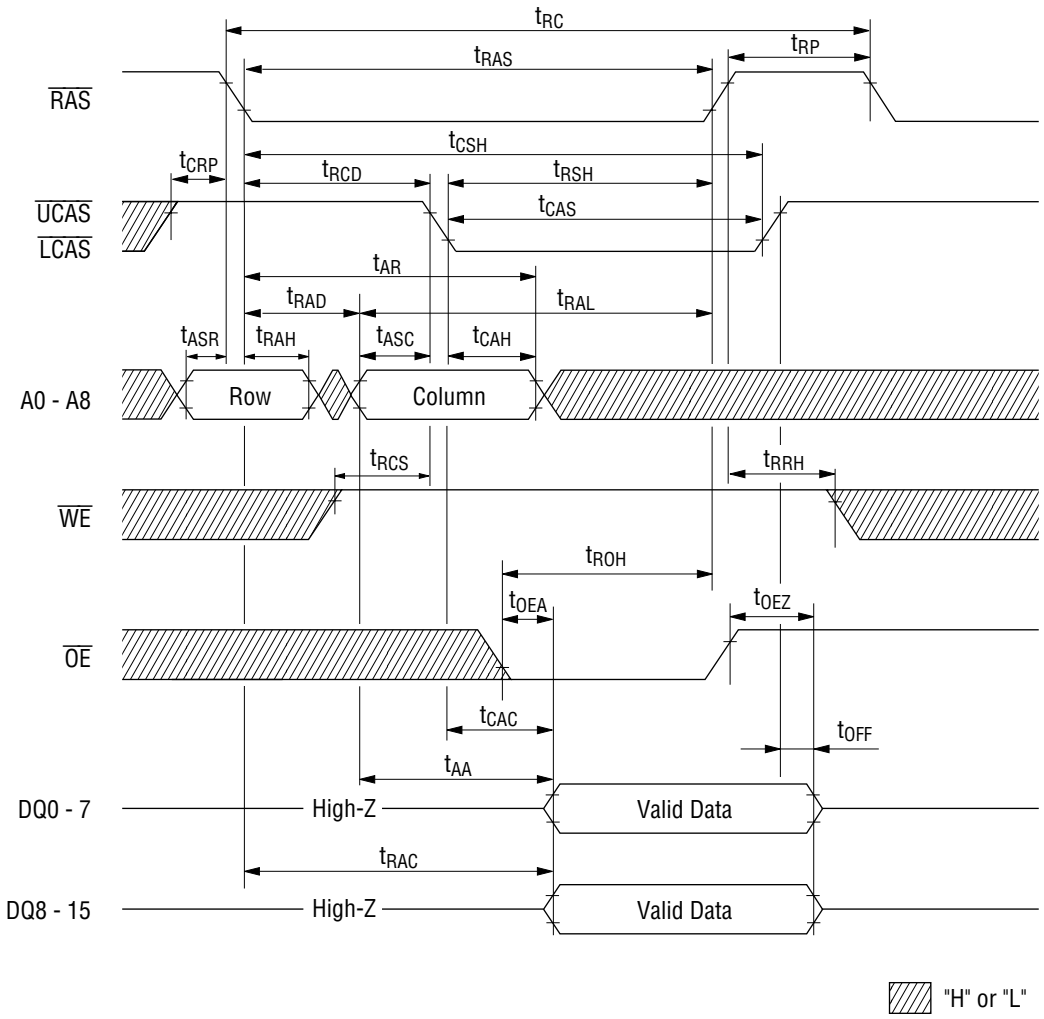
Notes:
1. All voltages are referenced to V_{SS}.
2. This parameter is dependent upon the cycle rate.
3. This parameter is dependent upon the output loading. Specified values are obtained with the output open.
4. An initial pause of 200 µs is required after power-up, followed by any 8 $\overline{RAS}$ cycles. (Example : $\overline{RAS}$-only-refresh) before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ cycles instead of 8 $\overline{RAS}$ cycles are required.
5. The AC characteristics assume t_T = 5 ns.
6. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Data outputs are measured with a load of 50 pF. DOUT reference levels: V_{OH}/V_{OL} = 2.0 V/1.4 V. Note that V_{OL} is defined as 1.4 V when V_{SS}* pins, pin 13 and pin 32, were open. The data output measurements under V_{OH}/V_{OL} = 2.0 V/0.8 V are guaranteed when V_{SS}* pins, pin 13 and pin 32, were connected to GND.
8. t_{REZ} (Max.), t_{OFF} (Max.), t_{WEZ} (Max.) and t_{OEZ} (Max.) define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels. This parameter is sampled and not 100% tested.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to $\overline{CAS}$ leading edge of early write cycles and to $\overline{WE}$ leading edge in $\overline{OE}$-controlled write cycles and read-modify-write cycles.
11. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (Min.), the cycle is an early write cycle and the data out pins will remain open circuit throughout the entire cycle. If $t_{RWD} \geq t_{RWD}$ (Min.), $t_{CWD} \geq t_{CWD}$ (Min.) and $t_{AWD} \geq t_{AWD}$ (Min.), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out is indeterminate.
12. Operation within the t_{RCD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled by t_{CAC}.
13. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, then access time is controlled by t_{AA}.
14. Input levels at the AC testing are 3.0 V/0 V.
15. Addresses (A0 - A8) may be changed two times or less while $\overline{RAS}$ = V_{IL}.
16. Addresses (A0 - A8) may be changed once or less while $\overline{CAS}$ = V_{IH} and $\overline{RAS}$ = V_{IL}.
17. This is guaranteed by design. (t_{COH} = t_{CAC} - output transition time). This parameter is not 100% tested.
18. This parameter is dependent upon the number of address transitions. Specified values are measured with a maximum of two transitions per address cycle in Fast Page Mode.

TIMING WAVEFORM

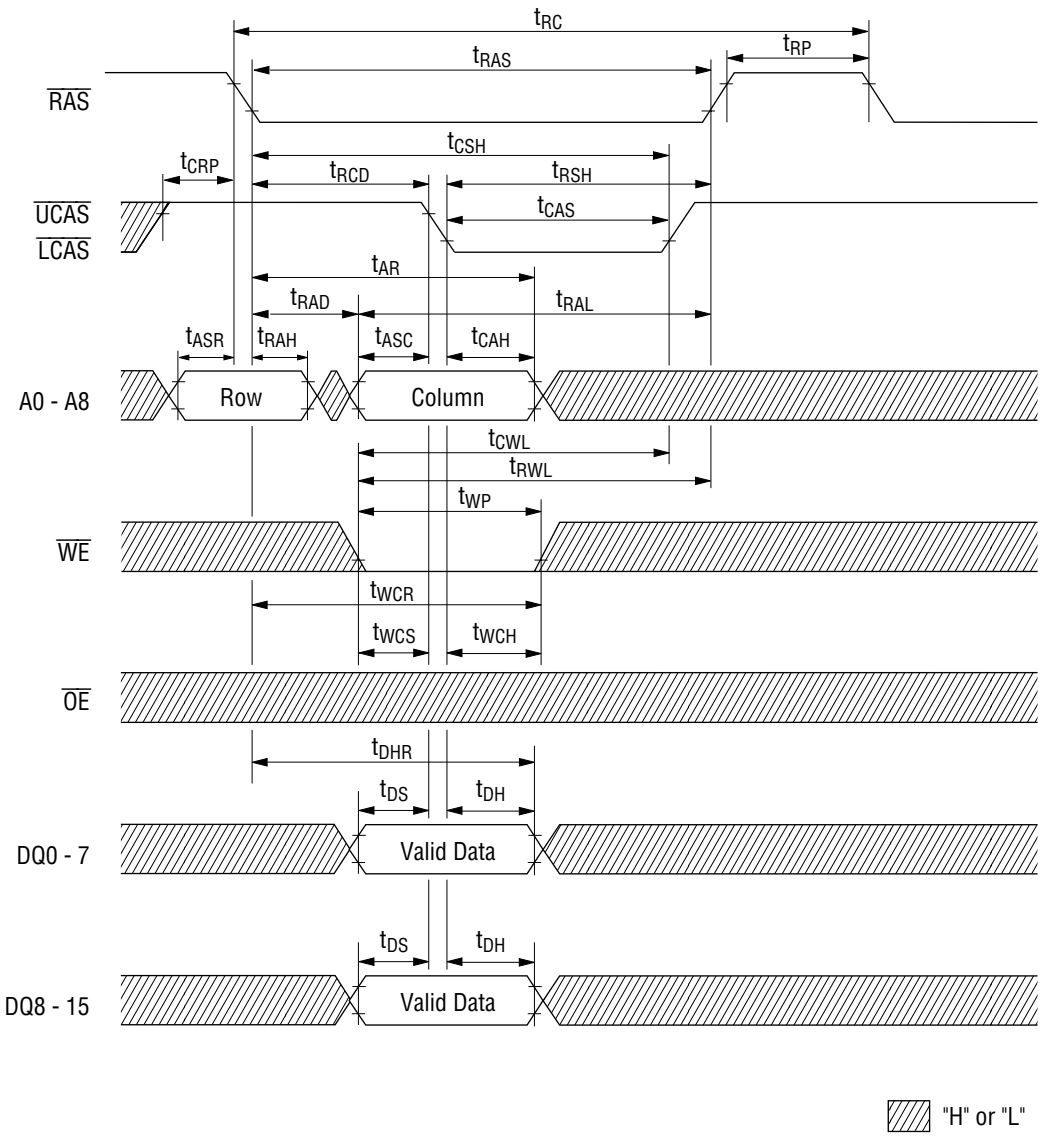
Read Cycle ($\overline{RAS}$ Output Control)



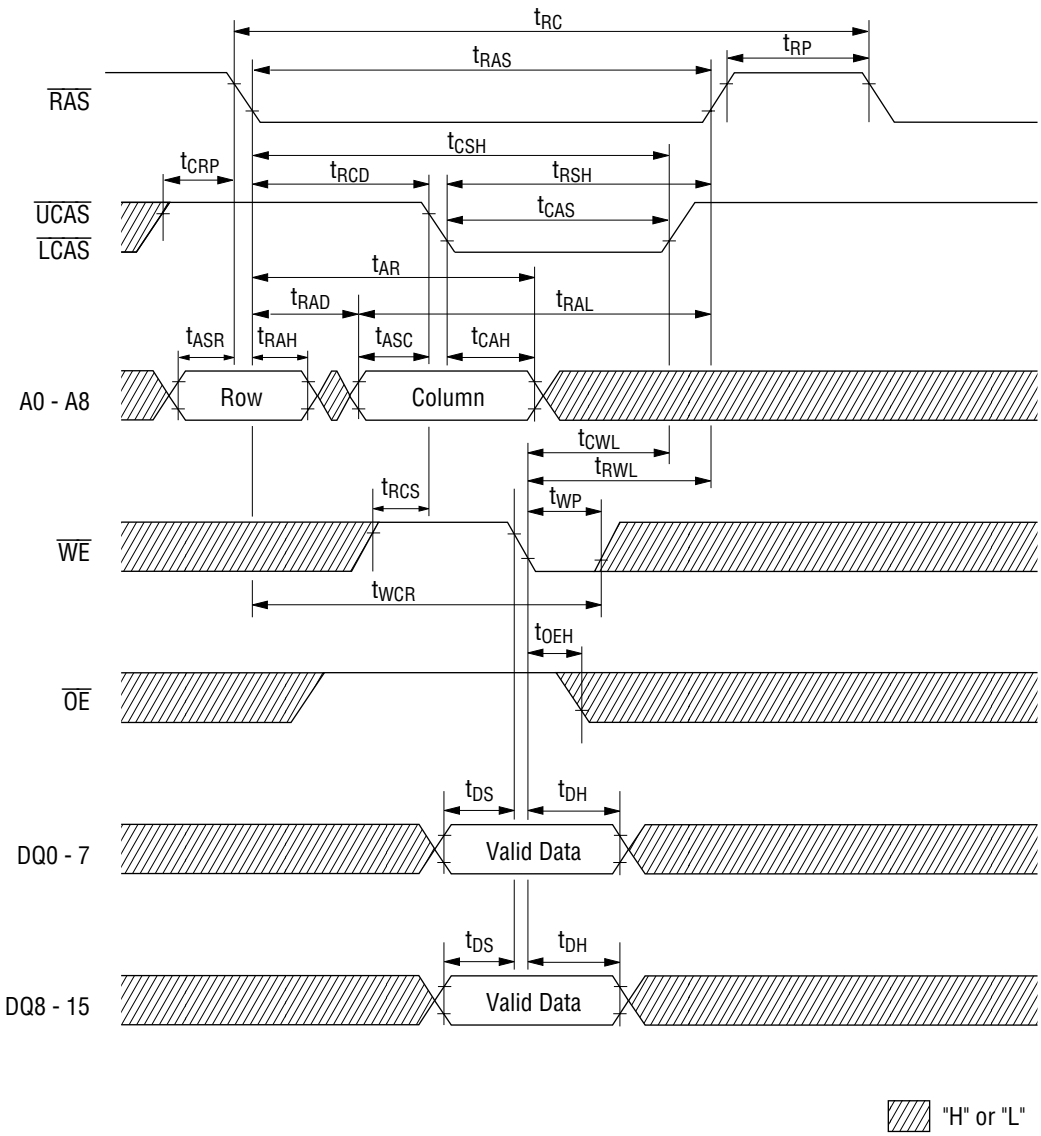
Read Cycle ($\overline{CAS}$ Output Control)



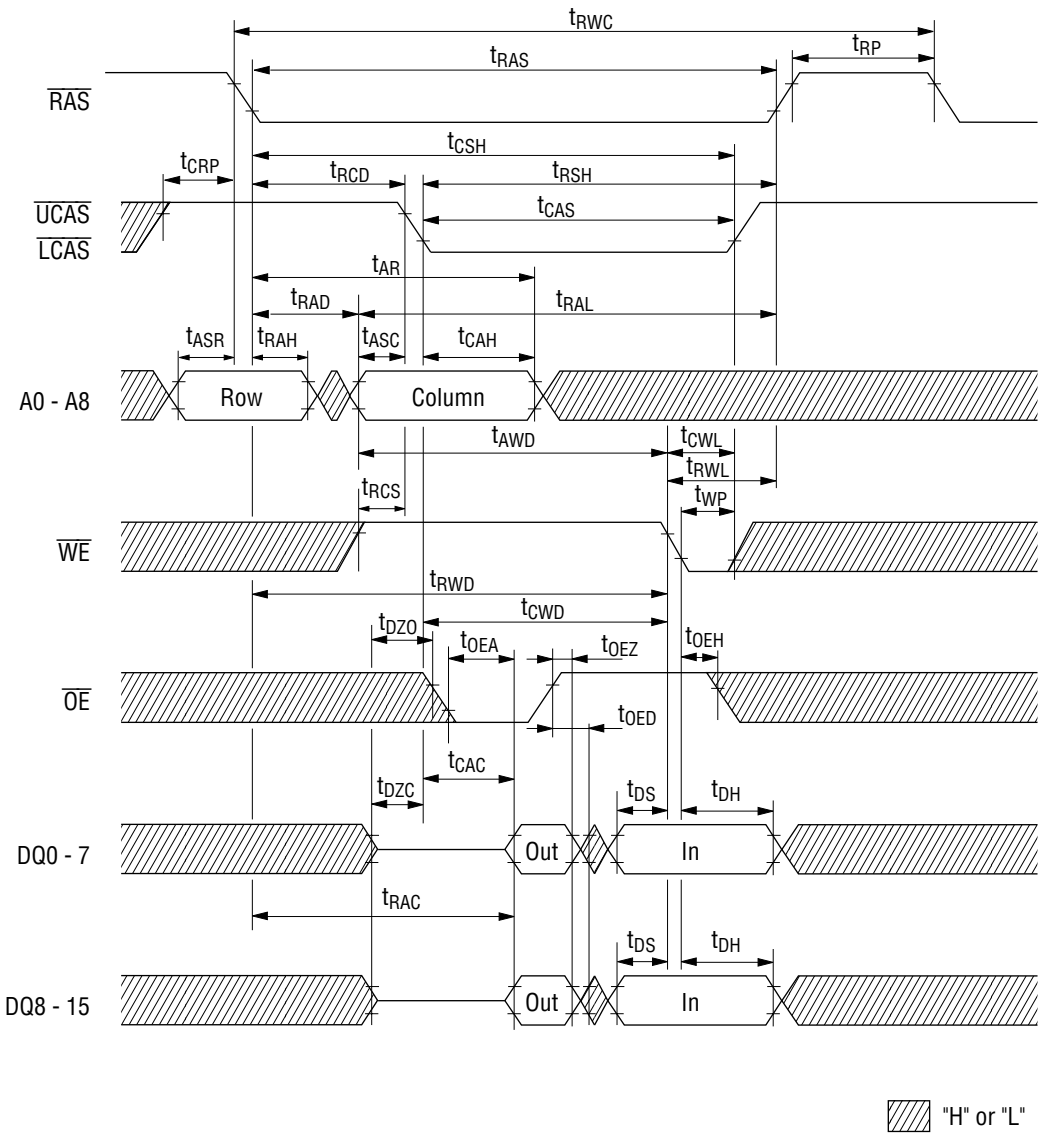
Early Write Cycle ($\overline{LCAS}$ and $\overline{UCAS}$ Active)



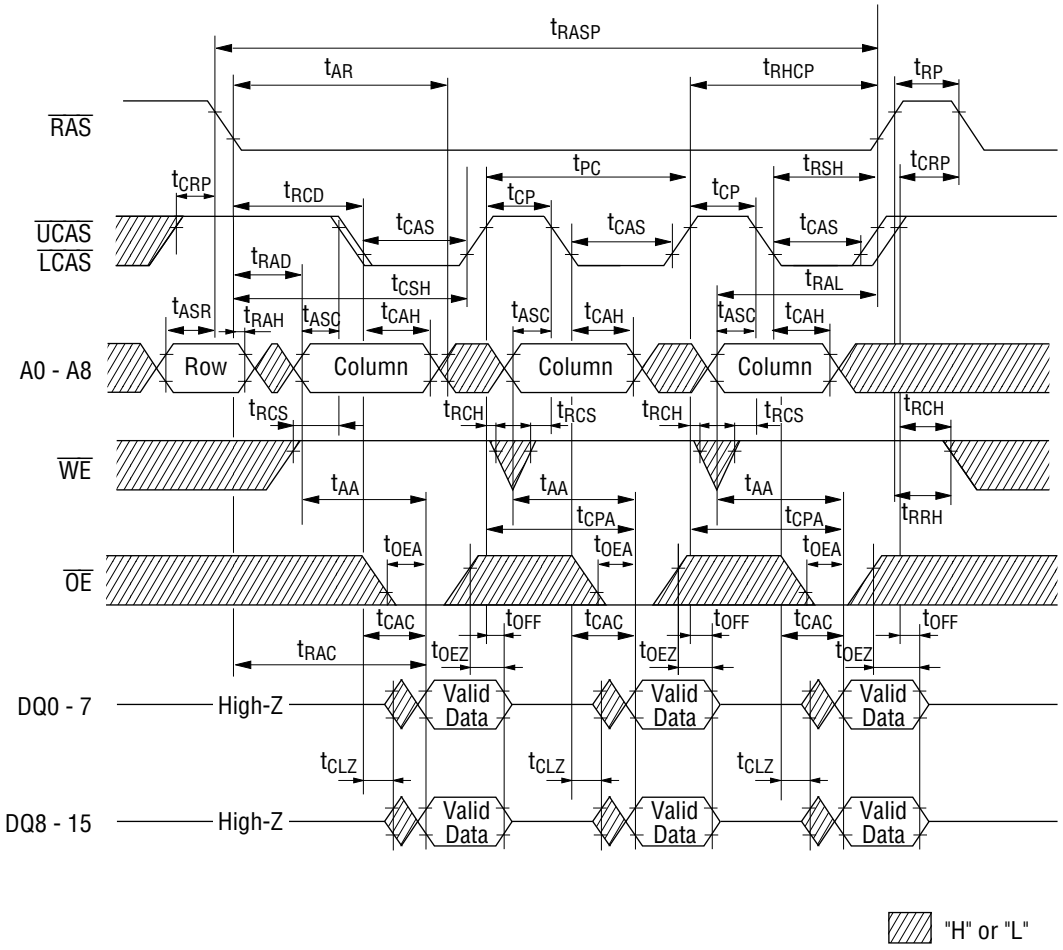
Late Write Cycle ($\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ Active)



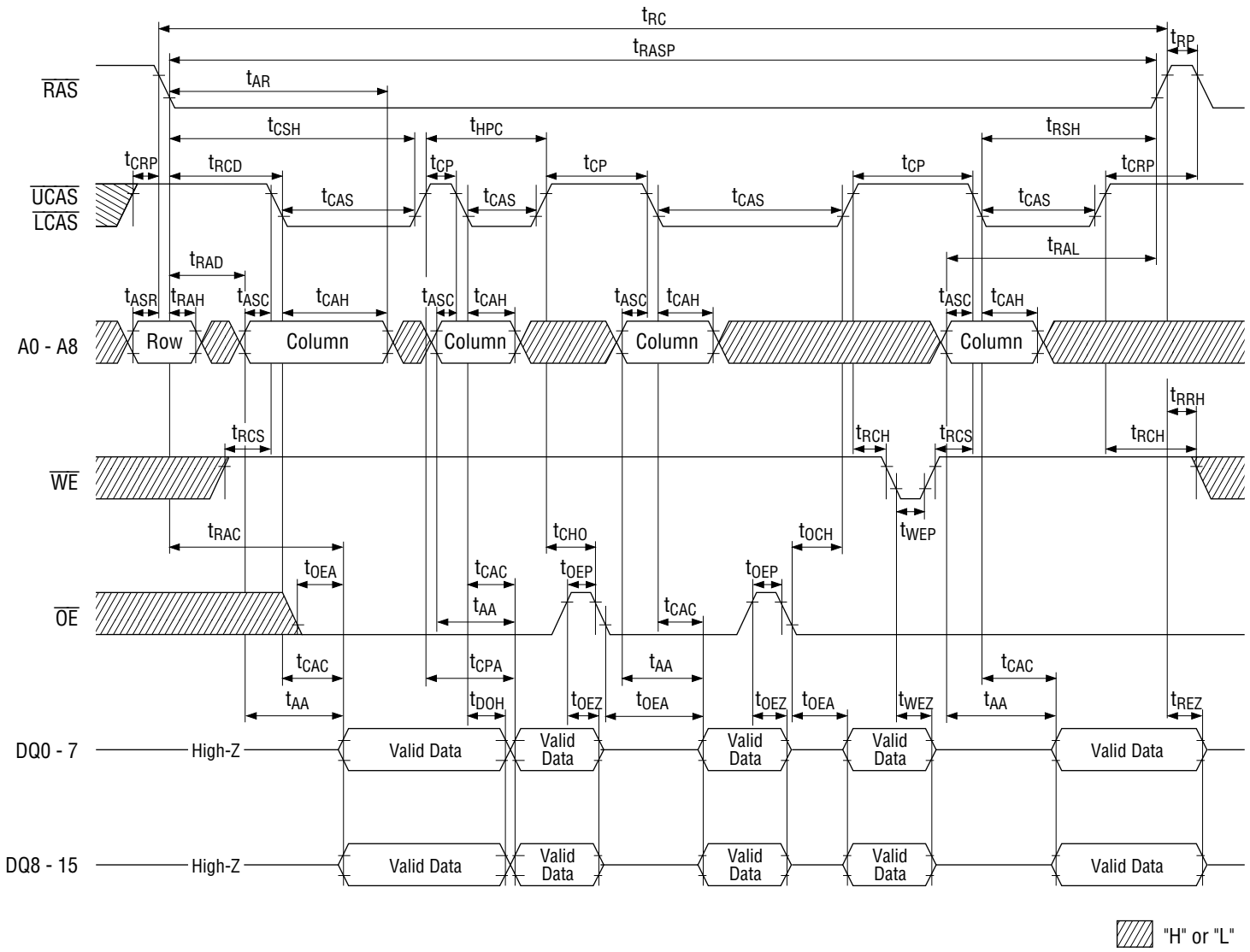
Read Modify Write Cycle ($\overline{LCAS}$ and $\overline{UCAS}$ Active)



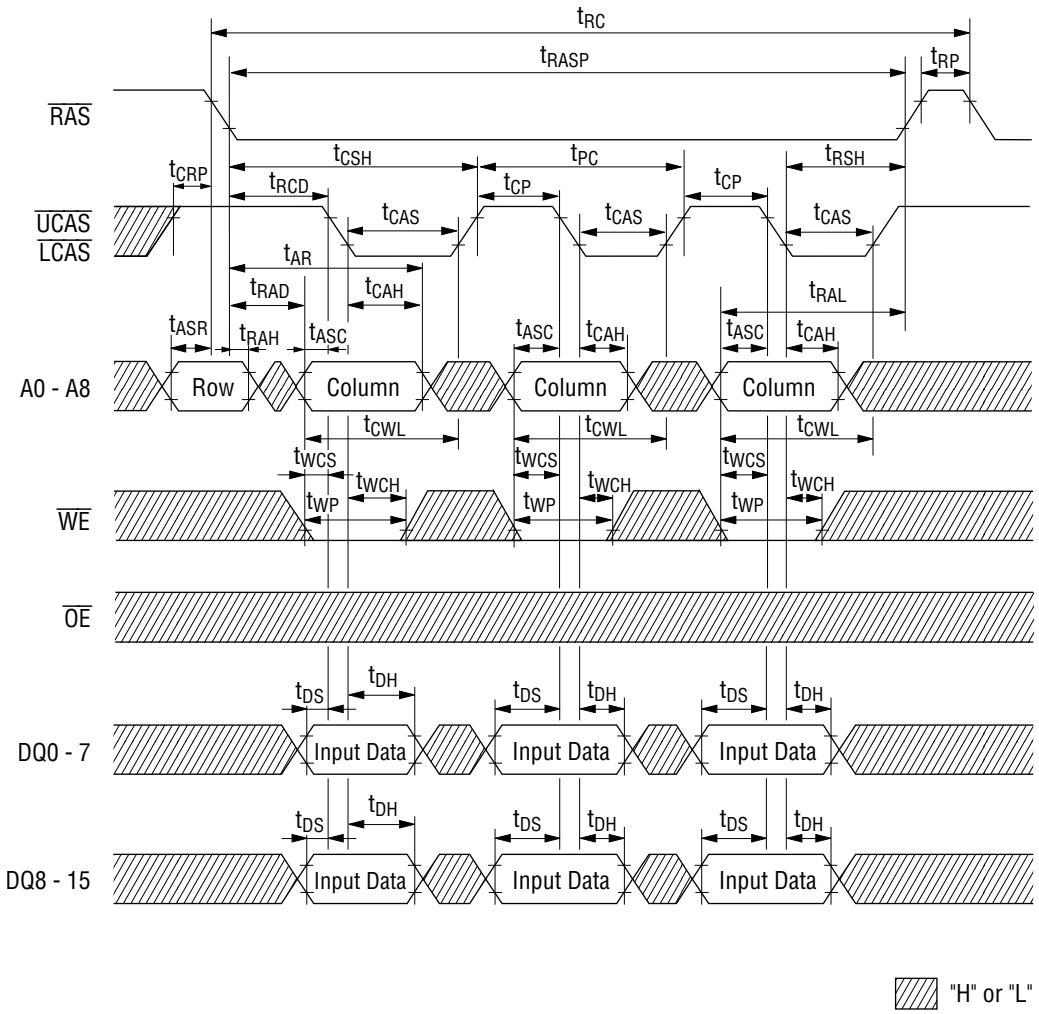
Fast Page Mode Read Cycle



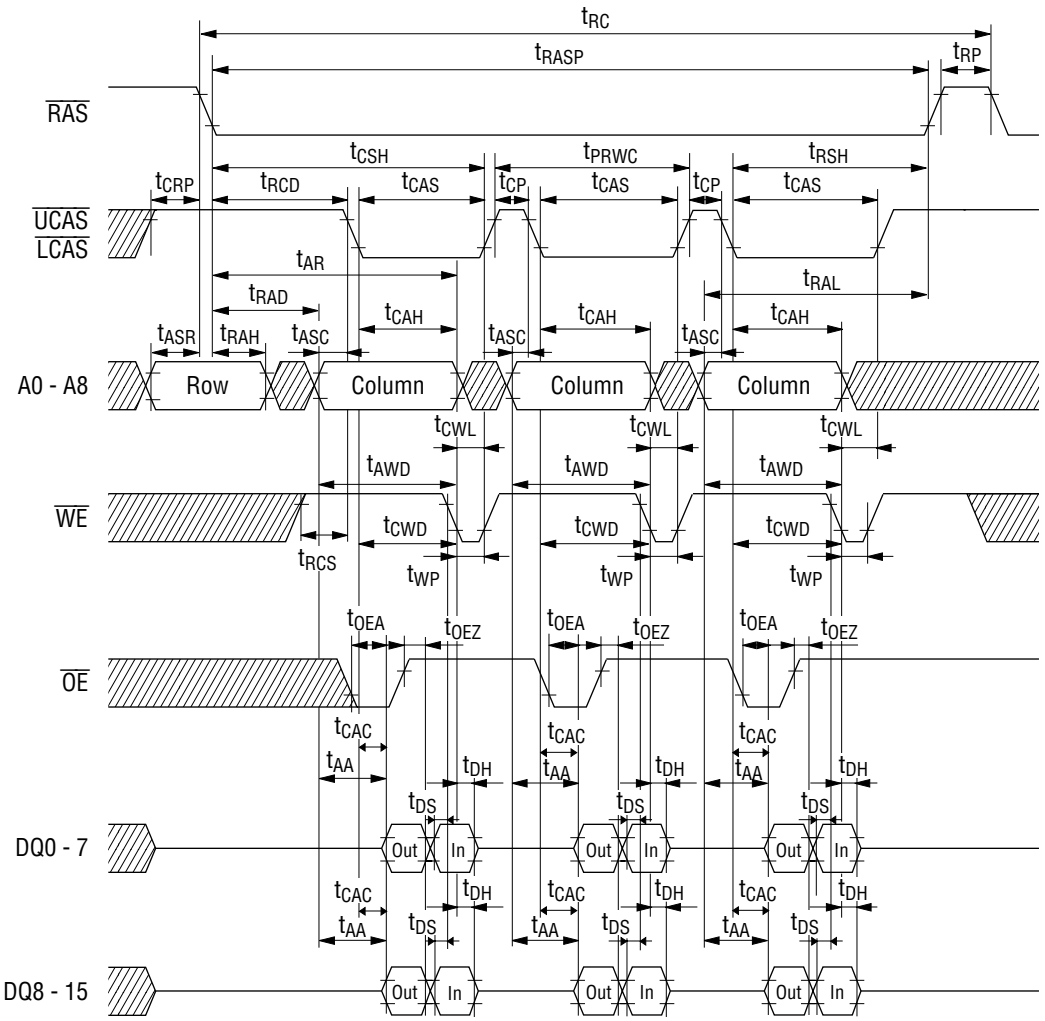
Fast Page Mode Read High-Z Operation



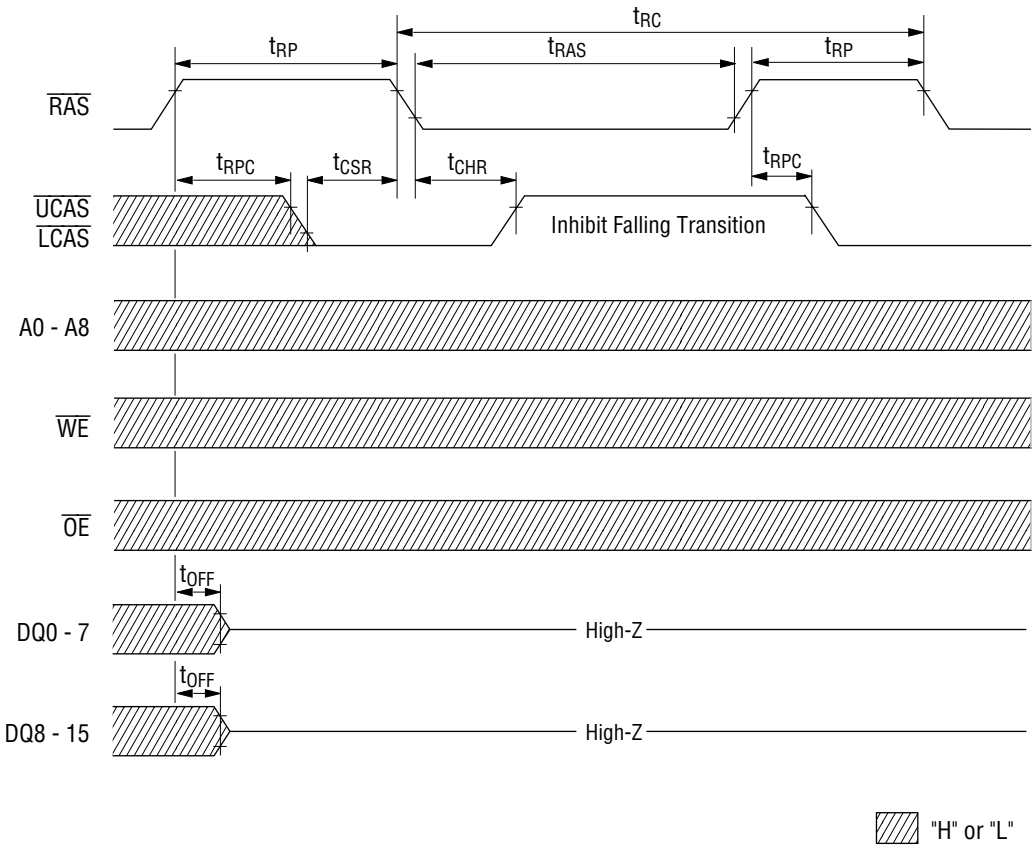
Fast Page Mode Early Write Cycle



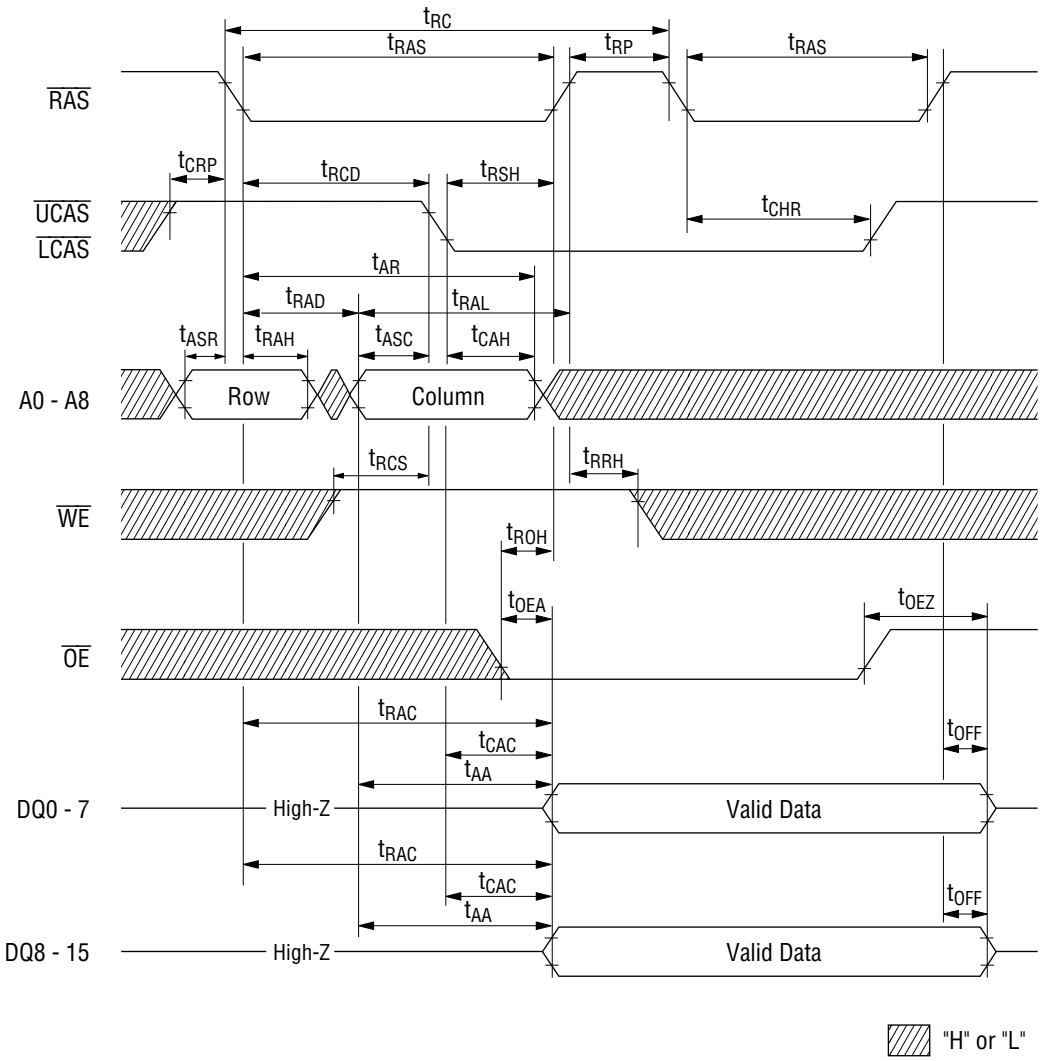
Fast Page Mode Read Modify Write Cycle



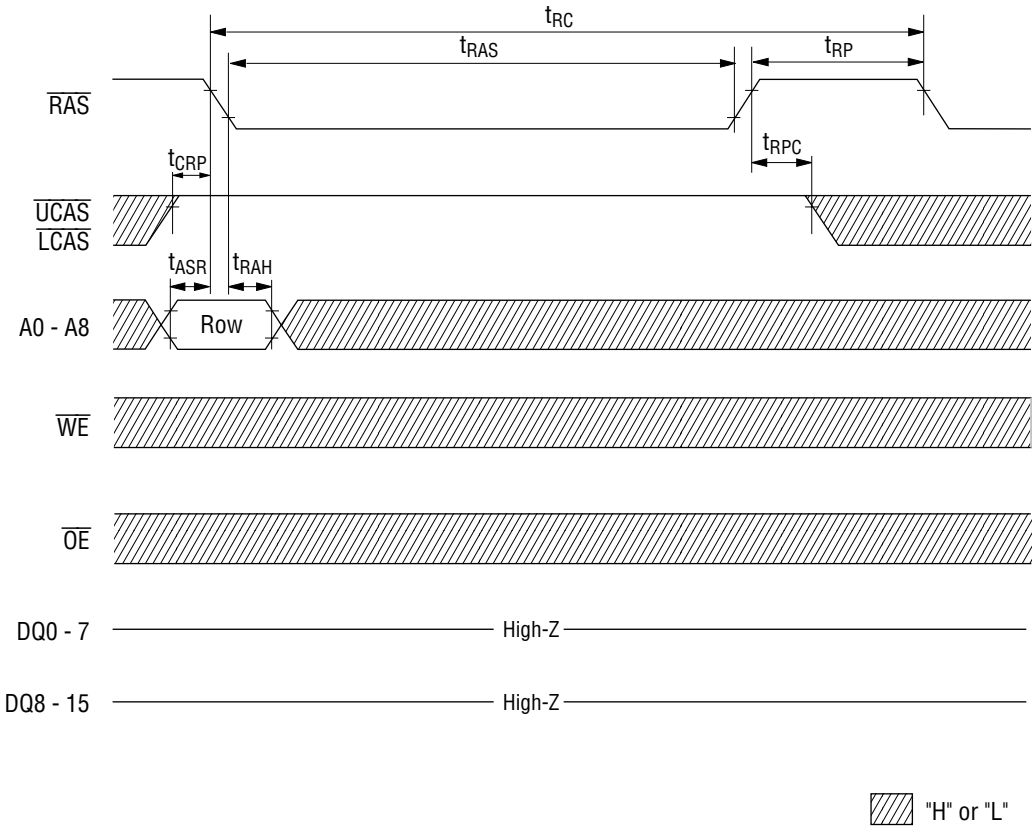
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle



Hidden Refresh Cycle



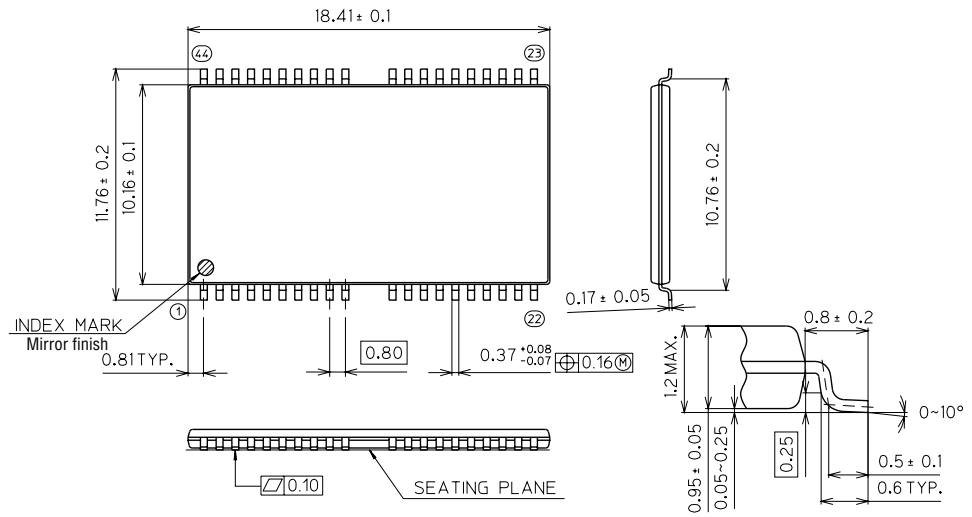
$\overline{\text{RAS}}$ Only Refresh Cycle



PACKAGE DIMENSIONS

(Unit : mm)

TSOPII44/40-P-400-0.80-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 µm or more
Package weight (g)	0.49 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, TQFP, LQFP, SOJ, QFJ (PLCC), SHP, and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

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