

MSM5432126A**131,072-Word × 32-Bit DYNAMIC RAM : FAST PAGE MODE TYPE WITH EDO****DESCRIPTION**

The MSM5432126A is a Graphics DRAM organized in a 131,072-word × 32-bit configuration. The technology used to fabricate the MSM5432126A is OKI's CMOS silicon gate process technology. The device operates with a single 5 V power supply.

FEATURES

- 131,072-word × 32-bit organization
- Single 5 V power supply, ±10% tolerance
- Refresh: 512 cycles/8 ms
- Fast Page Mode with Extended Data Out (EDO)
- Byte write, Byte read
- $\overline{\text{RAS}}$ only refresh
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
- Hidden refresh
- Package options:

64-pin 525 mil plastic SSOP

(SSOP64-P-525-0.80-K)

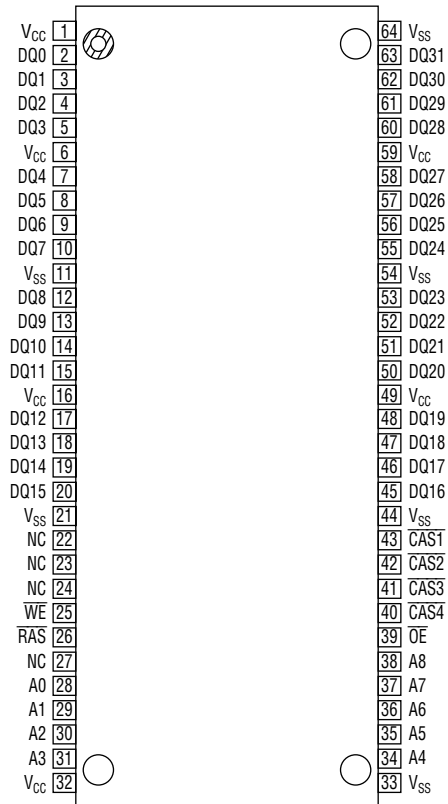
(Product : MSM5432126A-xxGS-K)

xx indicates speed rank.

PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t _{RAC}	t _{AA}	t _{CAC}	t _{OEA}		Operating (Max.)	Standby (Max.)
MSM5432126A-40	40 ns	20 ns	11 ns	11 ns	80 ns	1100 mW	11 mW
MSM5432126A-45	45 ns	23 ns	13 ns	13 ns	90 ns	1045 mW	
MSM5432126A-50	50 ns	25 ns	15 ns	15 ns	100 ns	990 mW	

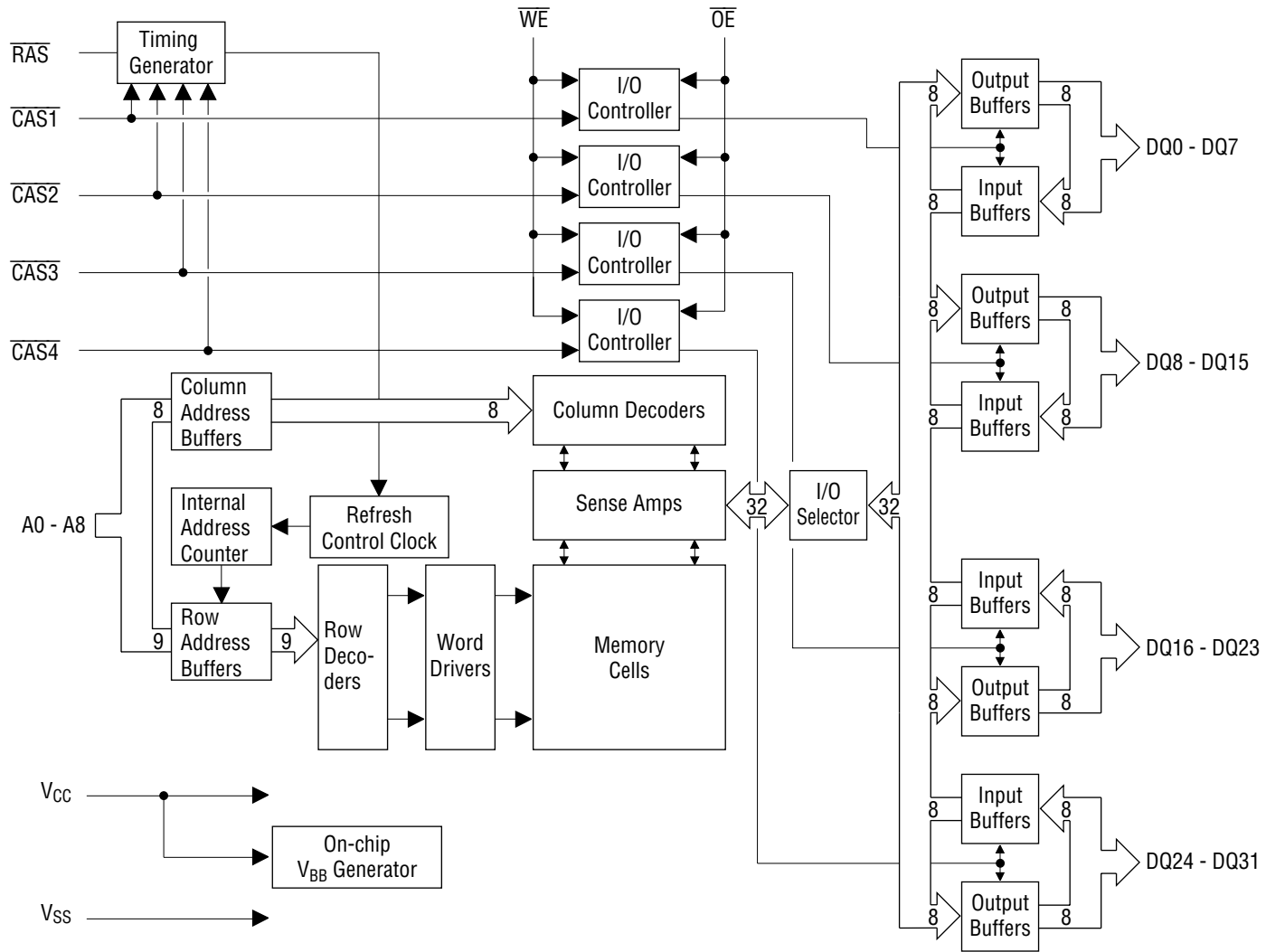
PIN CONFIGURATION (TOP VIEW)



64-Pin Plastic SSOP

Pin Name	Function
A0 - A8	Address Input
DQ0 - DQ31	Data Input / Data Output
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS1}} - \overline{\text{CAS4}}$	Column Address Strobe
$\overline{\text{WE}}$	Write Enable
$\overline{\text{OE}}$	Output Enable
V _{CC}	Power Supply (5 V)
V _{SS}	Ground (0 V)
NC	No Connection

Note: The same power supply voltage must be provided to every V_{CC} pin, and the same GND voltage level must be provided to every V_{SS} pin.



BLOCK DIAGRAM

ELECTRICAL CHARACTERISTICS**Absolute Maximum Ratings**

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	-0.5 to 7.0	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D	1	W
Operating Temperature	T_{opr}	0 to 70	°C
Storage Temperature	T_{stg}	-55 to 150	°C

Recommended Operating Conditions

(Ta = 0°C to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	3.0	—	$V_{CC} + 1.0$	V
Input Low Voltage	V_{IL}	-0.3	—	0.3	V

Capacitance(V_{CC} = 5 V ±10%, Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance	C_{IN}	—	8	pF
Input / Output Capacitance	C_{IO}	—	9	pF

DC Characteristics

 $(V_{CC} = 5V \pm 10\%, T_a = 0^\circ\text{C to } 70^\circ\text{C})$

Parameter	Symbol	Condition	MSM5432126A -40		MSM5432126A -45		MSM5432126A -50		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	V_{OH}	$I_{OH} = -0.1 \text{ mA}$	2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V	
Output Low Voltage	V_{OL}	$I_{OL} = 0.1 \text{ mA}$	0	0.8	0	0.8	0	0.8	V	
Input Leakage Current	I_{LI}	$0 \text{ V} < V_{IN} < V_{CC}$; All other pins not under test = 0 V	-10	10	-10	10	-10	10	μA	
Output Leakage Current	I_{LO}	$0 \text{ V} < V_{OUT} < 5.5 \text{ V}$ Output Disable	-10	10	-10	10	-10	10	μA	
Average Power Supply Current (Operating)	I_{CC1}	$\overline{\text{RAS}}, \overline{\text{CAS}}$ cycling, $t_{RC} = \text{Min.}$	—	190	—	180	—	170	mA	1, 2, 3
Power Supply Current (Standby)	I_{CC2}	$\overline{\text{RAS}} \geq V_{CC} - 0.2 \text{ V}$, $\overline{\text{CAS}} \geq V_{CC} - 0.2 \text{ V}$	—	2	—	2	—	2	mA	
Average Power Supply Current ($\overline{\text{RAS}}$ Only Refresh)	I_{CC3}	$\overline{\text{RAS}} = \text{cycling}$, $\overline{\text{CAS}} = V_{IH}$, $t_{RC} = \text{Min.}$	—	190	—	180	—	170	mA	1, 2, 3
Average Power Supply Current (Fast Page Mode)	I_{CC4}	$\overline{\text{RAS}} = V_{IL}$, $\overline{\text{CAS}}$ cycling, $t_{HPC} = \text{Min.}$	—	200	—	190	—	180	mA	1, 2, 4
Average Power Supply Current ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	I_{CC5}	$\overline{\text{RAS}} = \text{cycling}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$	—	190	—	180	—	170	mA	1, 2, 4

- Notes:
1. Specified values are obtained with minimum cycle time.
 2. I_{CC} is dependent on output loading. Specified values are obtained with the output open.
 3. Address can be changed once or less while $\overline{\text{RAS}} = V_{IL}$.
 4. Address can be changed once or less while $\overline{\text{CAS}} = V_{IH}$.

AC Characteristics (1/2)

(V_{CC} = 5 V ±10%, T_a = 0°C to 70°C) Note 1, 2, 3

Parameter	Symbol	MSM5432126A -40		MSM5432126A -45		MSM5432126A -50		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t _{RC}	80	—	90	—	100	—	ns	
Read Modify Write Cycle	t _{RWC}	125	—	135	—	145	—	ns	
Fast Page Mode Cycle Time	t _{HPC}	15	—	18	—	20	—	ns	
Fast Page Mode Read-Modify-Write Cycle Time	t _{PRWC}	60	—	65	—	70	—	ns	
Access Time from $\overline{\text{RAS}}$	t _{RAC}	—	40	—	45	—	50	ns	4, 9, 10
Access Time from Column Address	t _{AA}	—	20	—	23	—	25	ns	4, 10
Access Time from $\overline{\text{CAS}}$	t _{CAC}	—	11	—	13	—	15	ns	4, 9
Access Time from $\overline{\text{CAS}}$ Precharge	t _{CPA}	—	26	—	28	—	30	ns	4, 13
Output Buffer Turn-off Delay Time from $\overline{\text{RAS}}$	t _{REZ}	3	20	3	20	3	20	ns	5
Output Buffer Turn-off Delay Time from $\overline{\text{CAS}}$	t _{CEZ}	3	20	3	20	3	20	ns	5
Transition Time (Rise and Fall)	t _T	3	35	3	35	3	35	ns	3
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	34	—	39	—	44	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RAS}	40	10k	45	10k	50	10k	ns	
$\overline{\text{RAS}}$ Pulse Width (Hyper Page Mode Only)	t _{RASP}	40	100k	45	100k	50	100k	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	10	—	12	—	14	—	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	40	—	45	—	50	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	5	10k	6	10k	7	10k	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	18	28	20	32	20	35	ns	9
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	13	20	15	22	15	25	ns	10
Column Address to $\overline{\text{RAS}}$ Lead Time	t _{RAL}	20	—	22	—	24	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	5	—	6	—	7	—	ns	13
$\overline{\text{CAS}}$ Precharge Time (Hyper Page Mode)	t _{CP}	4	—	6	—	7	—	ns	15
Row Address Set-up Time	t _{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t _{RAH}	5	—	6	—	7	—	ns	
Column Address Set-up Time	t _{ASC}	0	—	0	—	0	—	ns	12
Column Address Hold Time	t _{CAH}	6	—	7	—	8	—	ns	12
Column Address Hold Time referenced to $\overline{\text{RAS}}$	t _{AR}	25	—	30	—	35	—	ns	
Read Command Set-up Time	t _{RCS}	0	—	0	—	0	—	ns	12
Read Command Hold Time	t _{RCH}	0	—	0	—	0	—	ns	6, 12
Read Command Hold Time referenced to $\overline{\text{RAS}}$	t _{RRH}	0	—	0	—	0	—	ns	6
$\overline{\text{CAS}}$ "H" to $\overline{\text{RAS}}$ "H" Lead Time	t _{CRL}	0	—	0	—	0	—	ns	
$\overline{\text{RAS}}$ "H" to $\overline{\text{CAS}}$ "H" Lead Time	t _{RCL}	0	—	0	—	0	—	ns	
Data Output Hold after $\overline{\text{CAS}}$ Low	t _{DOH}	3	—	3	—	3	—	ns	11
Write Command Set-up Time	t _{WCS}	0	—	0	—	0	—	ns	8, 12
Write Command Hold Time	t _{WCH}	6	—	7	—	8	—	ns	12

AC Characteristics (2/2)

(V_{CC} = 5 V ±10%, T_a = 0°C to 70°C) Note 1, 2, 3

Parameter	Symbol	MSM5432126A -40		MSM5432126A -45		MSM5432126A -50		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Command Hold Time referenced to $\overline{\text{RAS}}$	t _{WCR}	25	—	30	—	35	—	ns	
Write Command Pulse Width	t _{WP}	7	—	8	—	9	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t _{RWL}	7	—	8	—	9	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t _{CWL}	7	—	8	—	9	—	ns	14
Output Buffer Turn-off Delay Time from $\overline{\text{WE}}$	t _{WEZ}	3	20	3	20	3	20	ns	5
Data Set-up Time	t _{DS}	0	—	0	—	0	—	ns	7, 12
Data Hold Time	t _{DH}	6	—	7	—	8	—	ns	7, 12
Data Hold Time referenced to $\overline{\text{RAS}}$	t _{DHR}	25	—	30	—	35	—	ns	
$\overline{\text{OE}}$ to Data-in Delay Time	t _{OE D}	12	—	12	—	12	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{RWD}	60	—	65	—	70	—	ns	8
Column Address to $\overline{\text{WE}}$ Delay Time	t _{AWD}	38	—	42	—	45	—	ns	8
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{CWD}	28	—	32	—	35	—	ns	8
Data to $\overline{\text{CAS}}$ Delay Time	t _{DZC}	0	—	0	—	0	—	ns	
Data to $\overline{\text{OE}}$ Delay Time	t _{DZO}	0	—	0	—	0	—	ns	
Access Time from $\overline{\text{OE}}$	t _{OE A}	—	11	—	13	—	15	ns	
Output Buffer Turn-off Delay Time from $\overline{\text{OE}}$	t _{OE Z}	3	20	3	20	3	20	ns	5
$\overline{\text{OE}}$ Command Hold Time	t _{OE H}	7	—	8	—	9	—	ns	
$\overline{\text{RAS}}$ Hold Time referenced to $\overline{\text{OE}}$	t _{ROH}	10	—	10	—	10	—	ns	
$\overline{\text{OE}}$ "L" to $\overline{\text{CAS}}$ "H" Lead Time	t _{OCH}	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ "H" to $\overline{\text{OE}}$ "L" Lead Time	t _{CHO}	10	—	10	—	10	—	ns	
$\overline{\text{OE}}$ Precharge Time	t _{OE P}	10	—	10	—	10	—	ns	
$\overline{\text{WE}}$ Pulse Width (Output Disable)	t _{WPE}	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Set-up Time for $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Cycle	t _{CSR}	5	—	6	—	8	—	ns	12
$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Cycle	t _{CHR}	5	—	6	—	8	—	ns	13
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time	t _{RPC}	10	—	10	—	10	—	ns	12
$\overline{\text{CAS}}$ Precharge Time (Refresh Counter Test)	t _{CPT}	15	—	20	—	25	—	ns	15
Refresh Period	t _{REF}	—	8	—	8	—	8	ms	

- Notes:
1. An initial pause of 200 μ s is required after power-up followed by any 8 $\overline{\text{RAS}}$ cycles (Example : $\overline{\text{RAS}}$ only refresh) before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycles instead of 8 $\overline{\text{RAS}}$ cycles are required.
 2. The AC characteristics assume at $t_T = 3$ ns.
 3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} . Input levels at the AC testing are 3.0 V/0 V.
 4. Data outputs are measured with a load of 30 pF.
DOUT reference levels : $V_{OH}/V_{OL} = 2.0$ V/0.8 V.
 5. t_{REZ} (Max.), t_{CEZ} (Max.), t_{WEZ} (Max.) and t_{OEZ} (Max.) define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels. This parameter is sampled and not 100% tested.
 6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
 7. These parameters are referenced to $\overline{\text{CAS}}$ leading edge of early write cycles and to $\overline{\text{WE}}$ leading edge in $\overline{\text{OE}}$ controlled write cycles and read modify write cycles.
 8. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (Min.), the cycle is an early write cycle and the data out pin will remain open circuit throughout the entire cycle; If $t_{RWD} \geq t_{RWD}$ (Min.), $t_{CWD} \geq t_{CWD}$ (Min.) and $t_{AWD} \geq t_{AWD}$ (Min.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell; If neither of the above sets of conditions is satisfied, the condition of the data out is indeterminate.
 9. Operation within the t_{RCD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled by t_{CAC} .
 10. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, then access time is controlled by t_{AA} .
 11. This is guaranteed by design. ($t_{DOH} = t_{CAC}$ - output transition time) This parameter is not 100% tested.
 12. These parameters are determined by the earliest falling edge of $\overline{\text{CAS1}}$, $\overline{\text{CAS2}}$, $\overline{\text{CAS3}}$, or $\overline{\text{CAS4}}$.
 13. These parameters are determined by the latest rising edge of $\overline{\text{CAS1}}$, $\overline{\text{CAS2}}$, $\overline{\text{CAS3}}$, or $\overline{\text{CAS4}}$.
 14. t_{CWL} should be satisfied by all $\overline{\text{CAS}}$ es.
 15. t_{CP} and t_{CPT} are determined by the time that all $\overline{\text{CAS}}$ es are high.

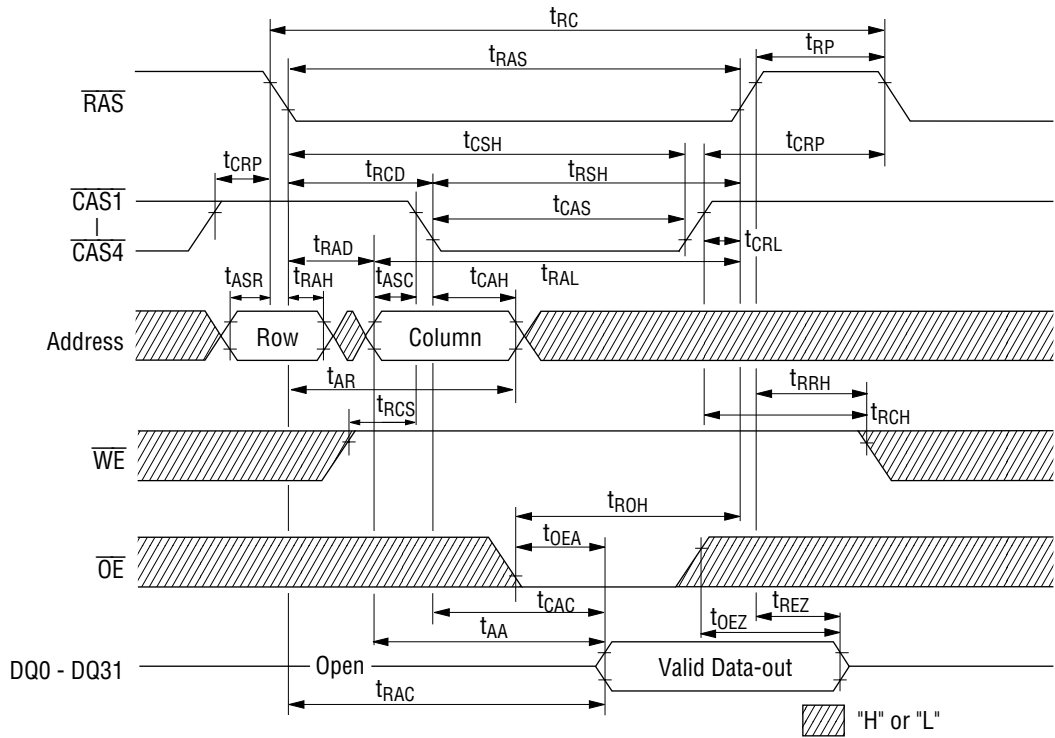
CASn-DQ FUNCTION TABLE

CAS1	CAS2	CAS3	CAS4	DQ0-7	DQ8-15	DQ16-23	DQ24-31
H	H	H	H	*	*	*	*
H	H	H	L	*	*	*	Enable
H	H	L	H	*	*	Enable	*
H	H	L	L	*	*	Enable	Enable
H	L	H	H	*	Enable	*	*
H	L	H	L	*	Enable	*	Enable
H	L	L	H	*	Enable	Enable	*
H	L	L	L	*	Enable	Enable	Enable
L	H	H	H	Enable	*	*	*
L	H	H	L	Enable	*	*	Enable
L	H	L	H	Enable	*	Enable	*
L	H	L	L	Enable	*	Enable	Enable
L	L	H	H	Enable	Enable	*	*
L	L	H	L	Enable	Enable	*	Enable
L	L	L	H	Enable	Enable	Enable	*
L	L	L	L	Enable	Enable	Enable	Enable

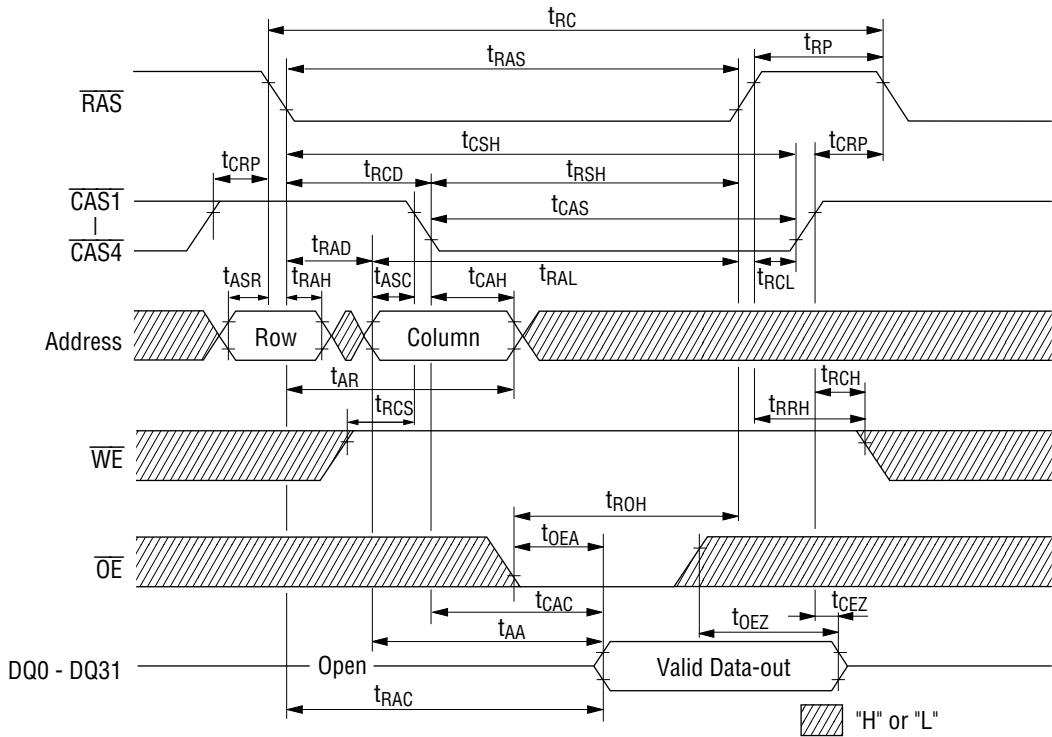
	Enable	*
Read cycle	Valid Data-out	High-Z
Write cycle	Write Data	Don't Care

TIMING WAVEFORM

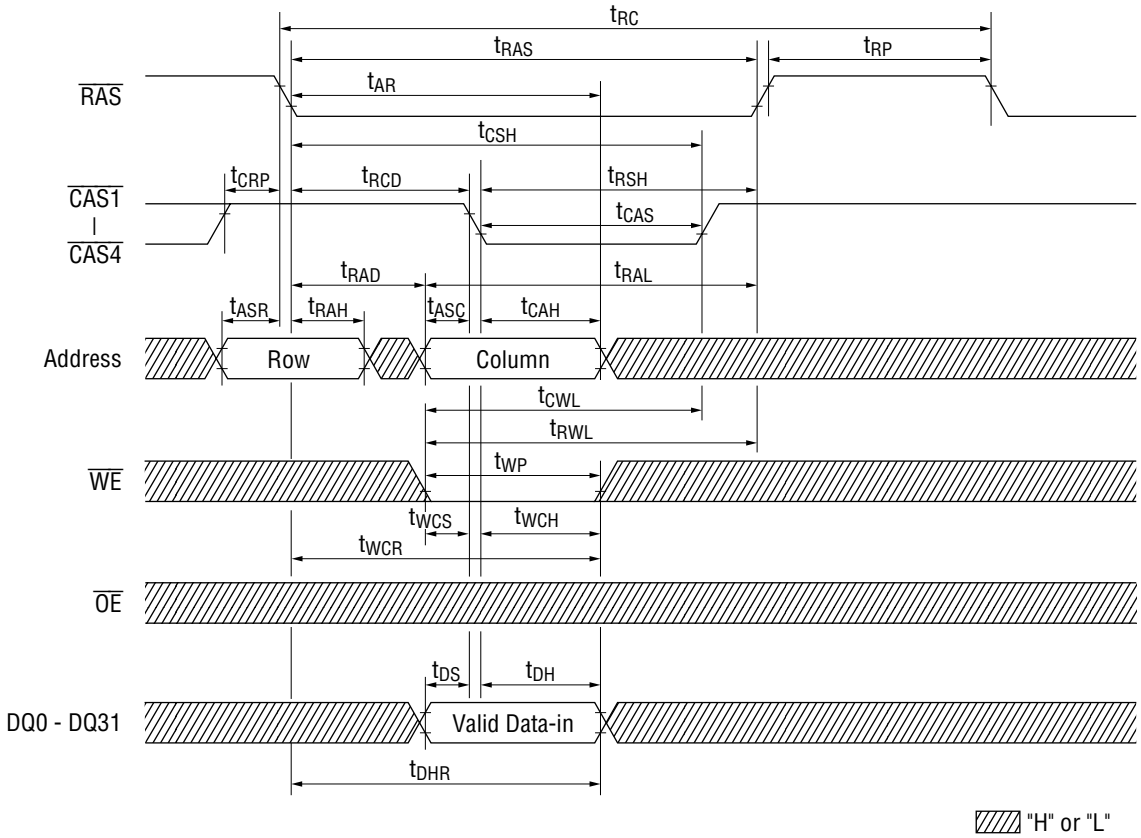
Read Cycle (Outputs Controlled by $\overline{\text{RAS}}$)



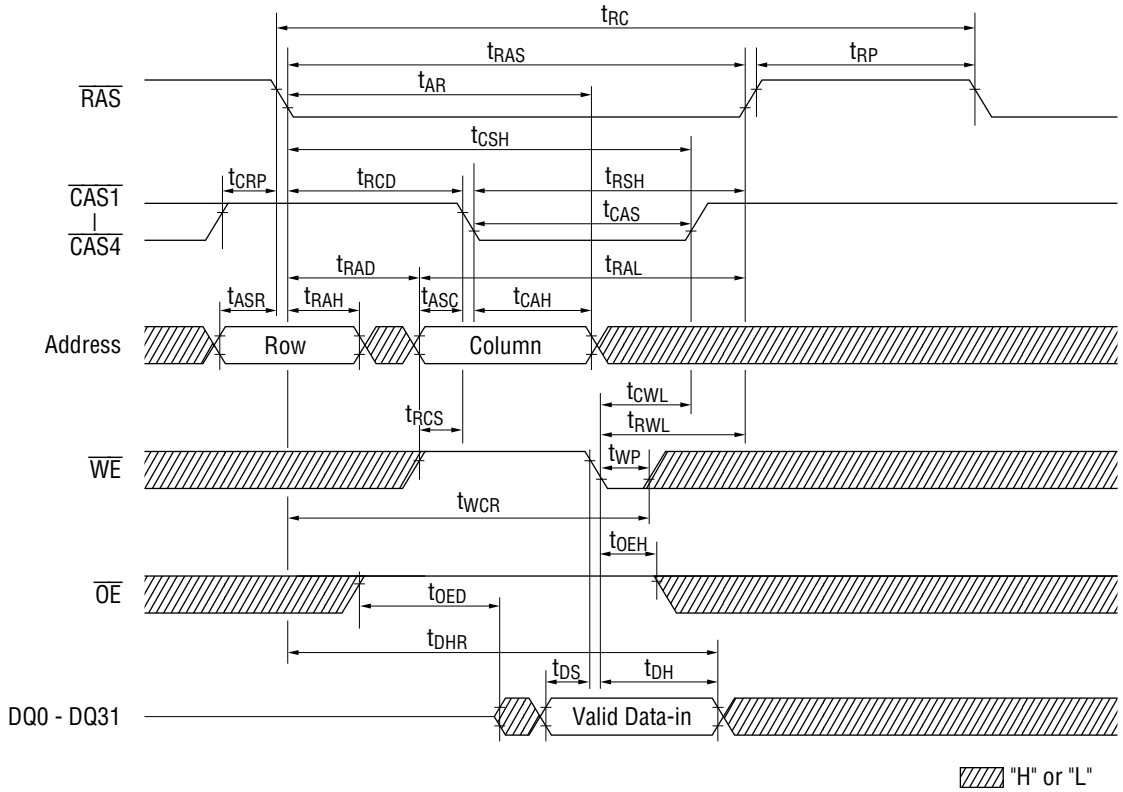
Read Cycle (Outputs Controlled by $\overline{\text{CAS}}$)



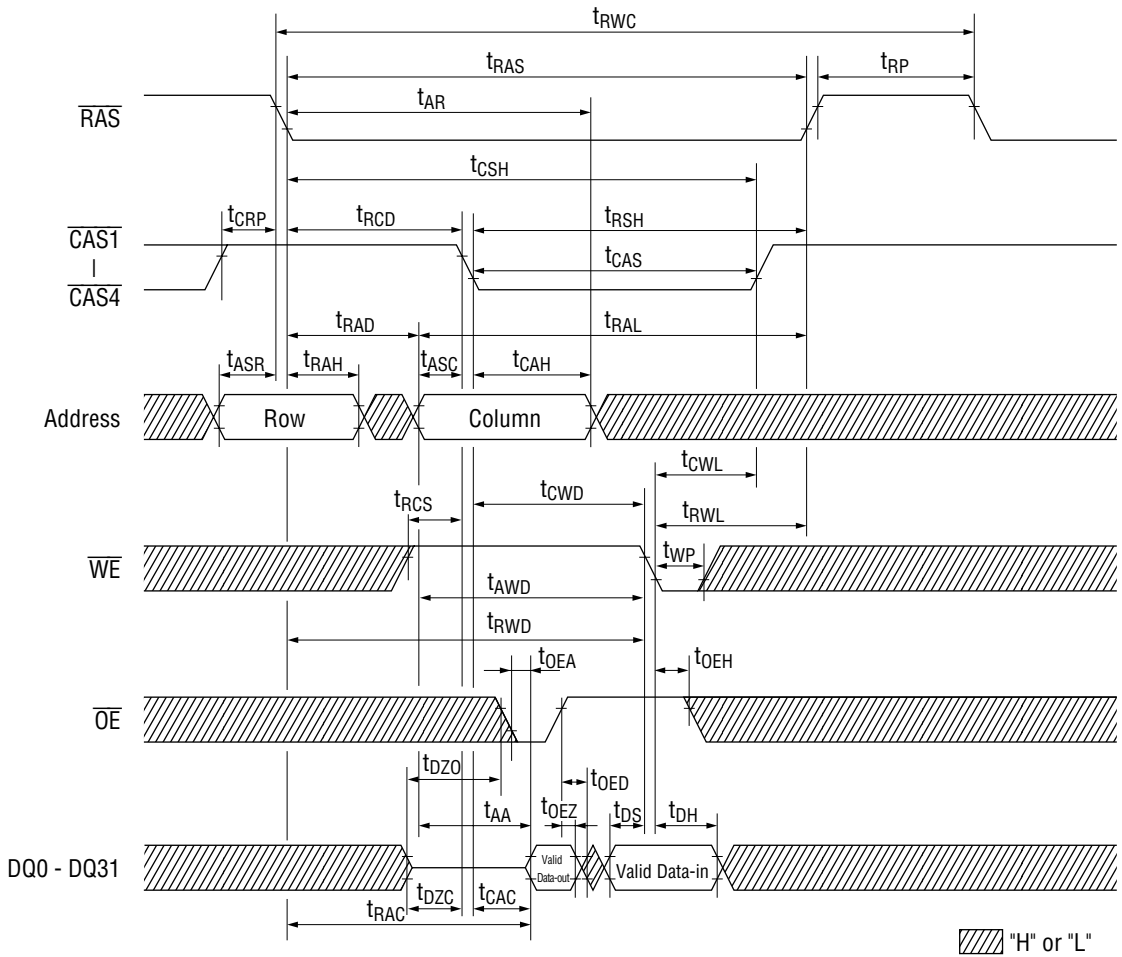
Write Cycle (Early Write)



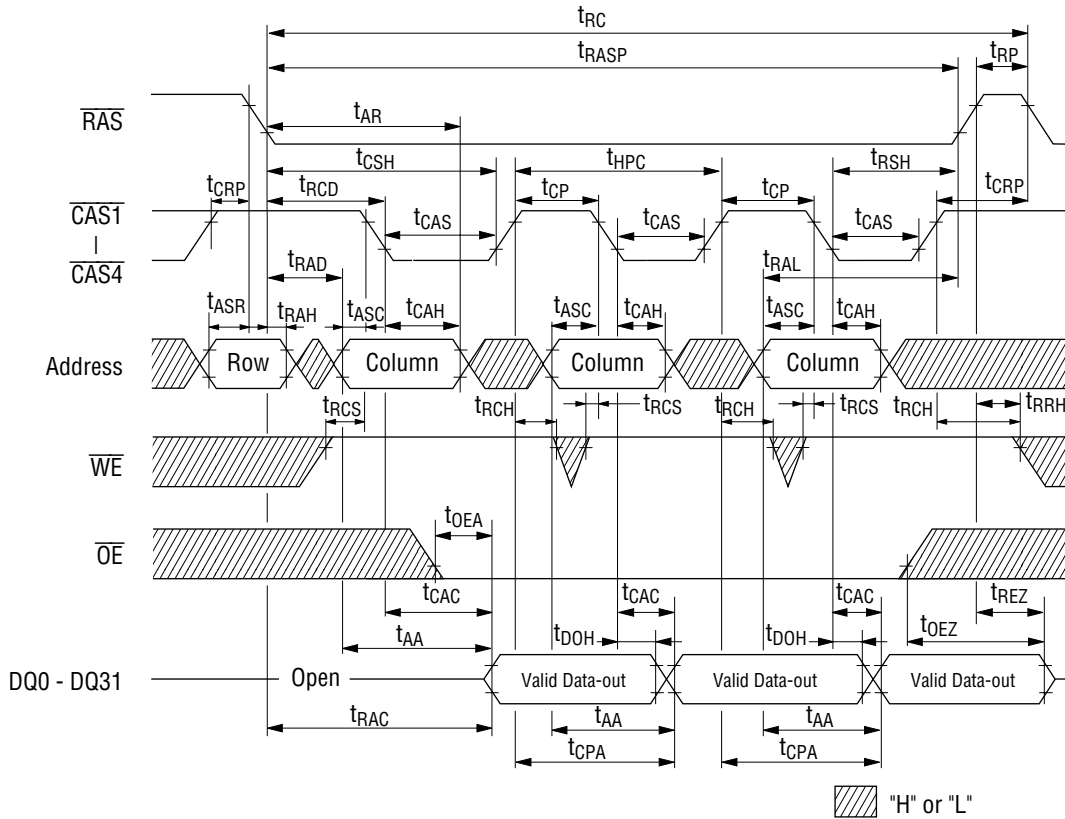
Write Cycle (\overline{OE} Control Write)



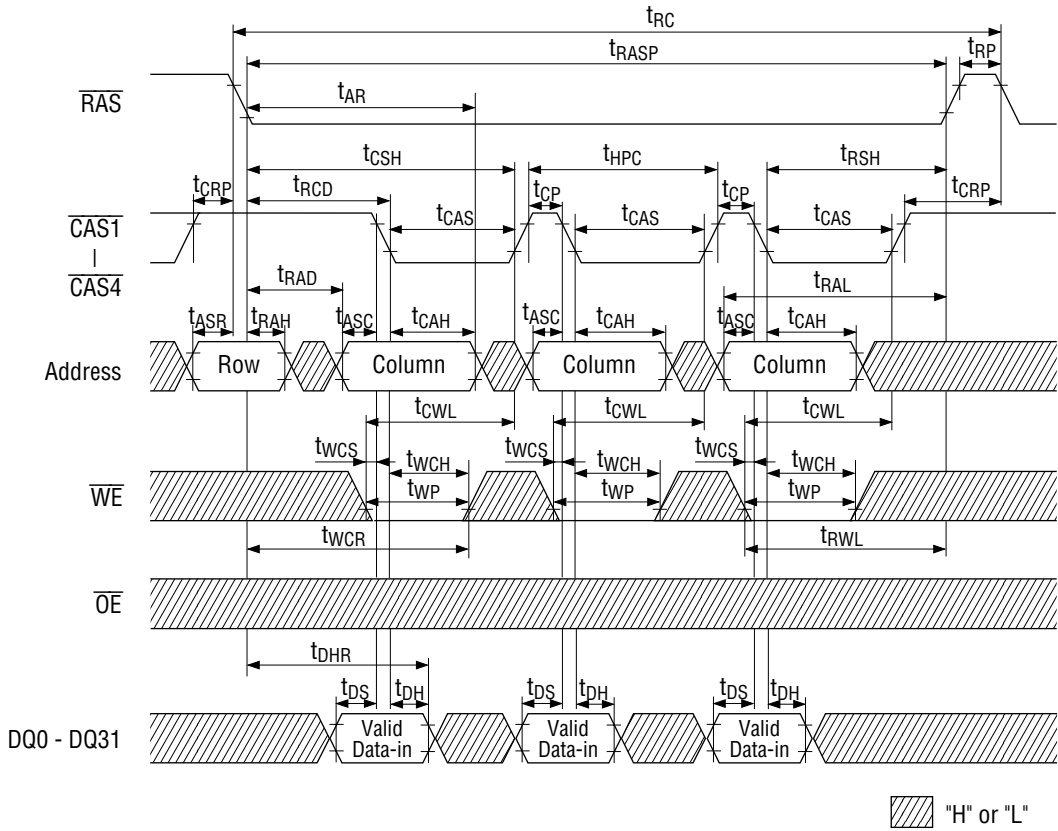
Read Modify Write Cycle



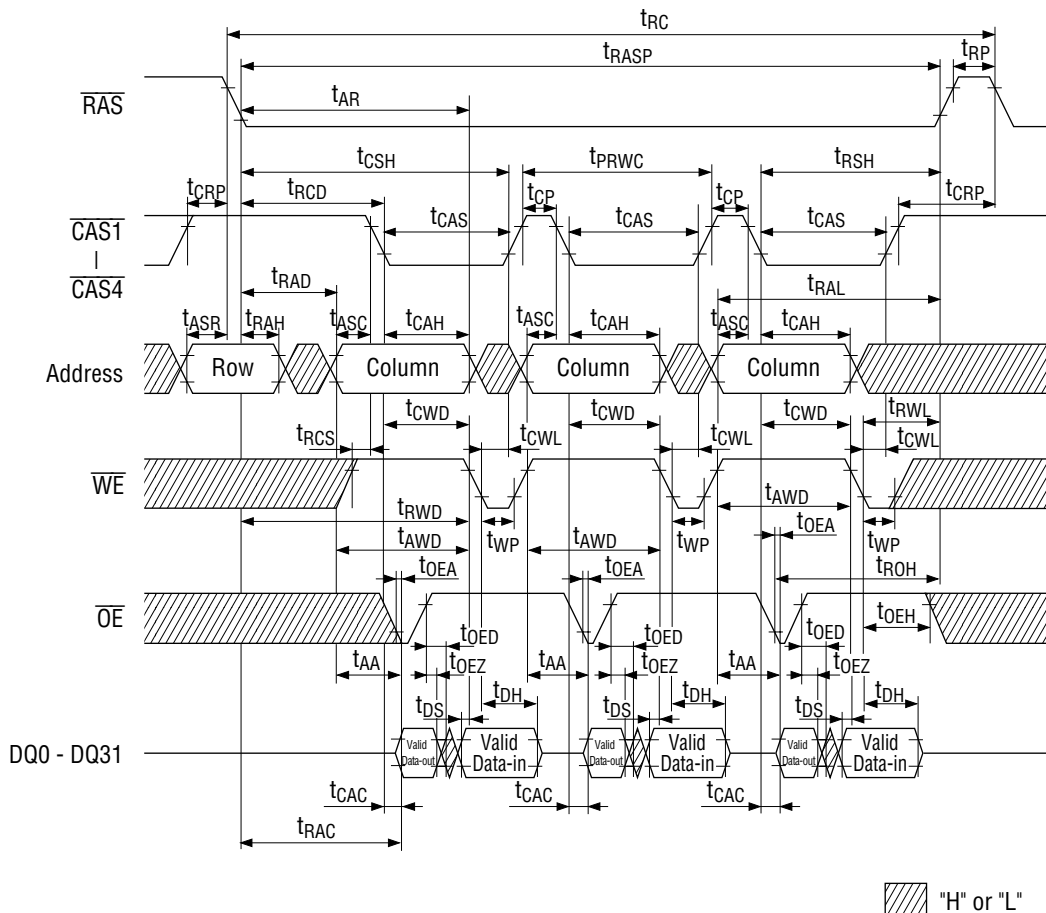
Fast Page Mode Read Cycle with EDO



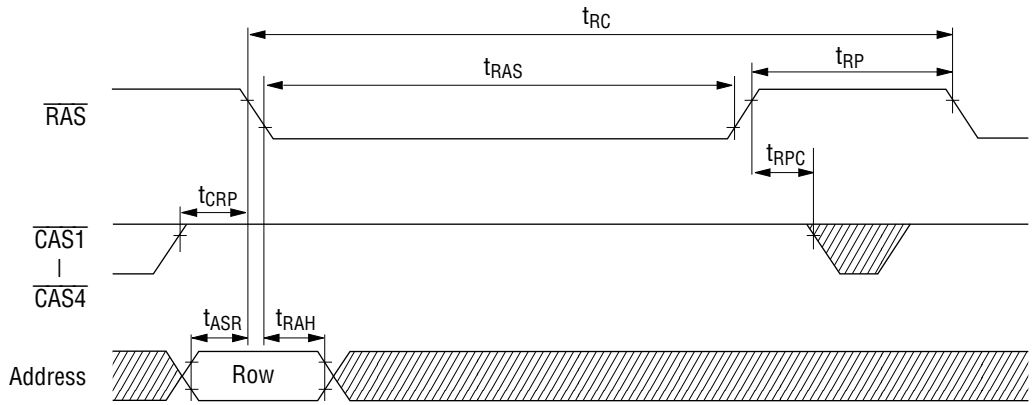
Fast Page Mode Write Cycle (Early Write)




Fast Page Mode Read Modify Write Cycle



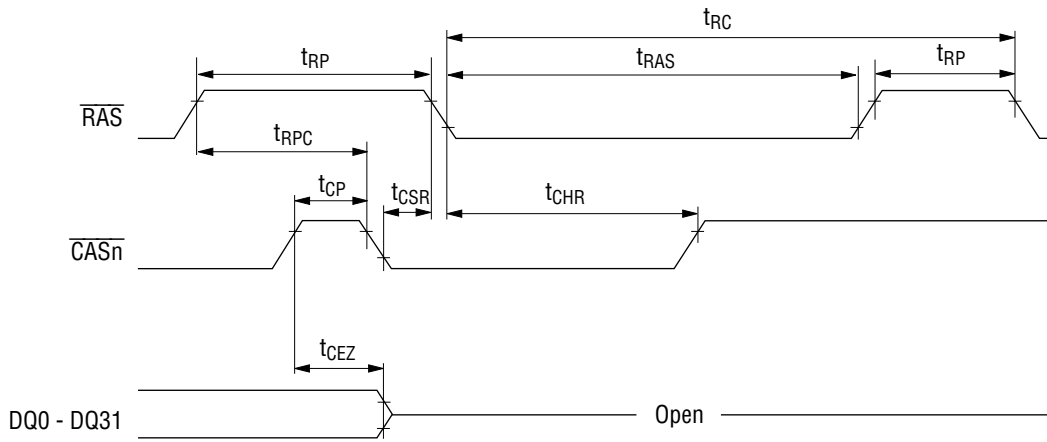
RAS Only Refresh Cycle



Note: DQs are open, $\overline{\text{WE}}$, $\overline{\text{OE}}$ = "H" or "L"

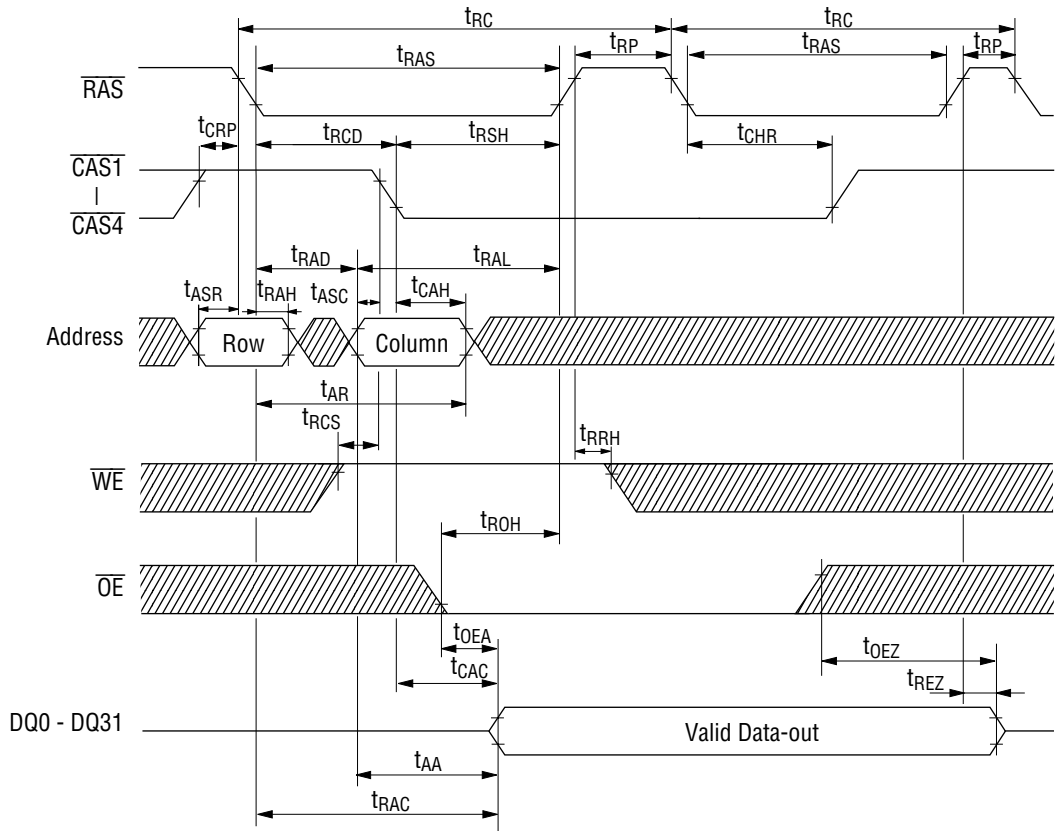
 "H" or "L"

CAS before RAS Refresh Cycle

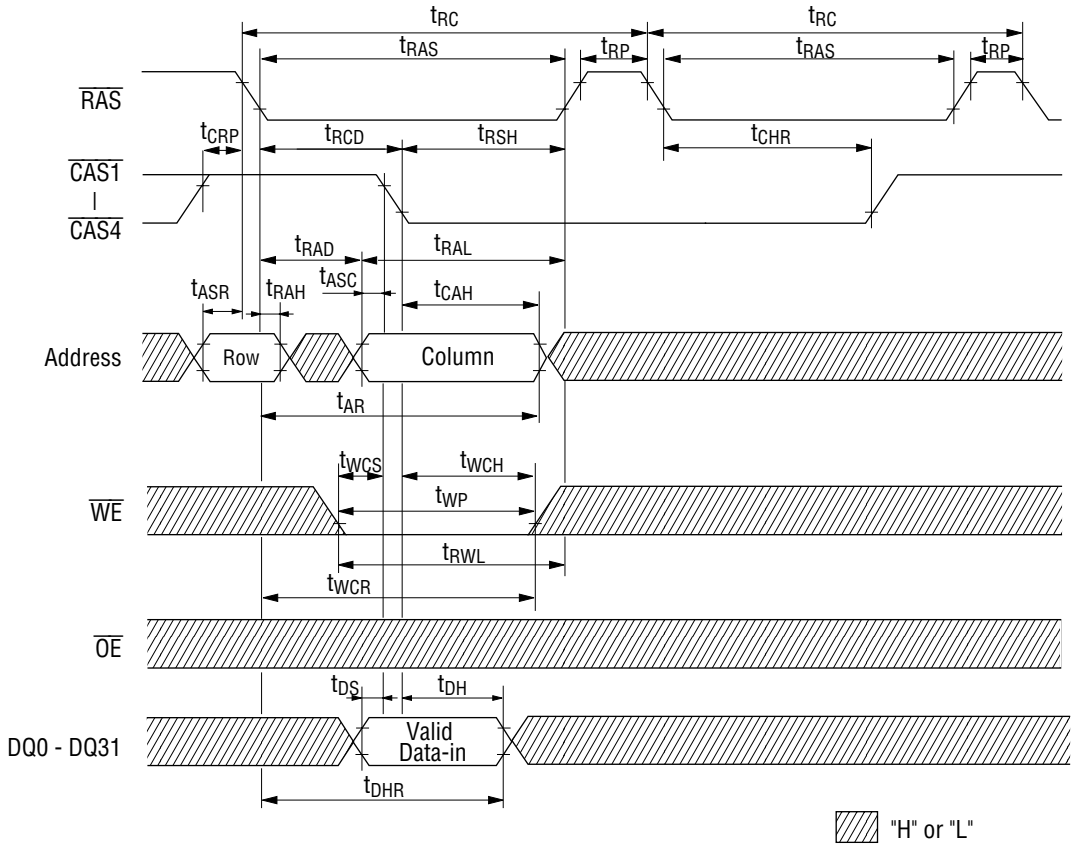


Note: $\overline{\text{WE}}$, $\overline{\text{OE}}$, A0 - A8 = "H" or "L"

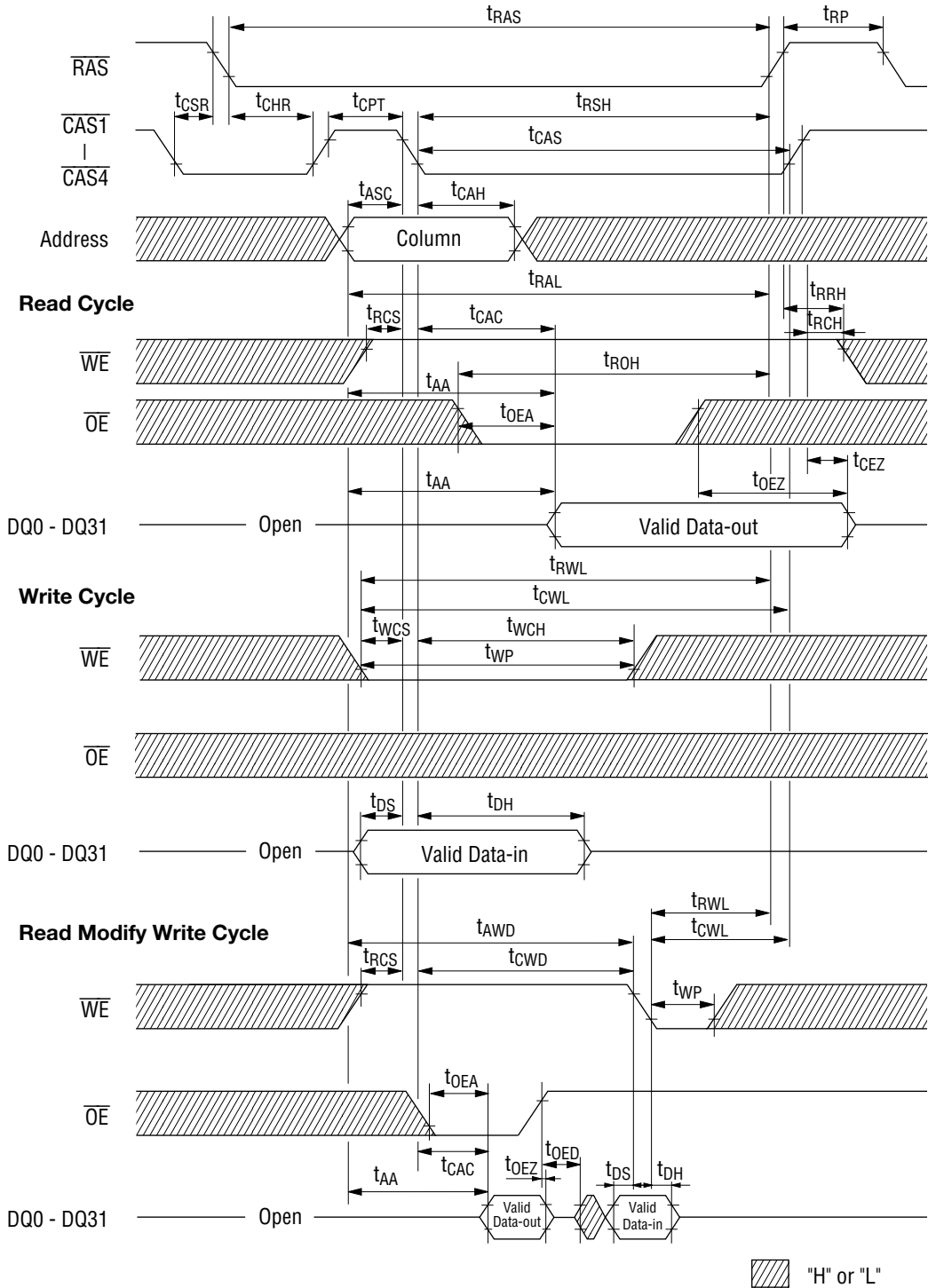
Hidden Refresh Read Cycle

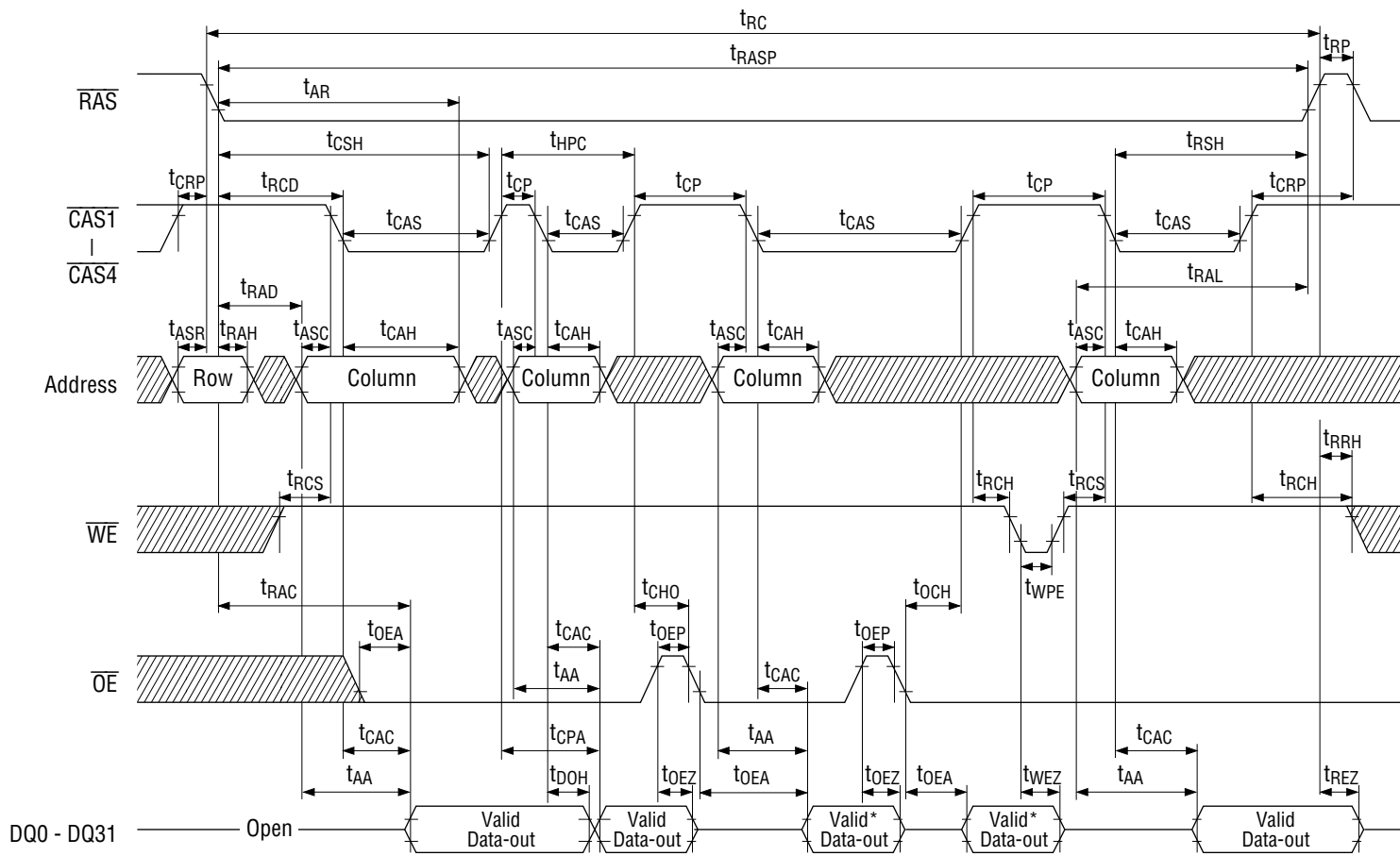


Hidden Refresh Write Cycle



CAS before RAS Refresh Counter Test Cycle

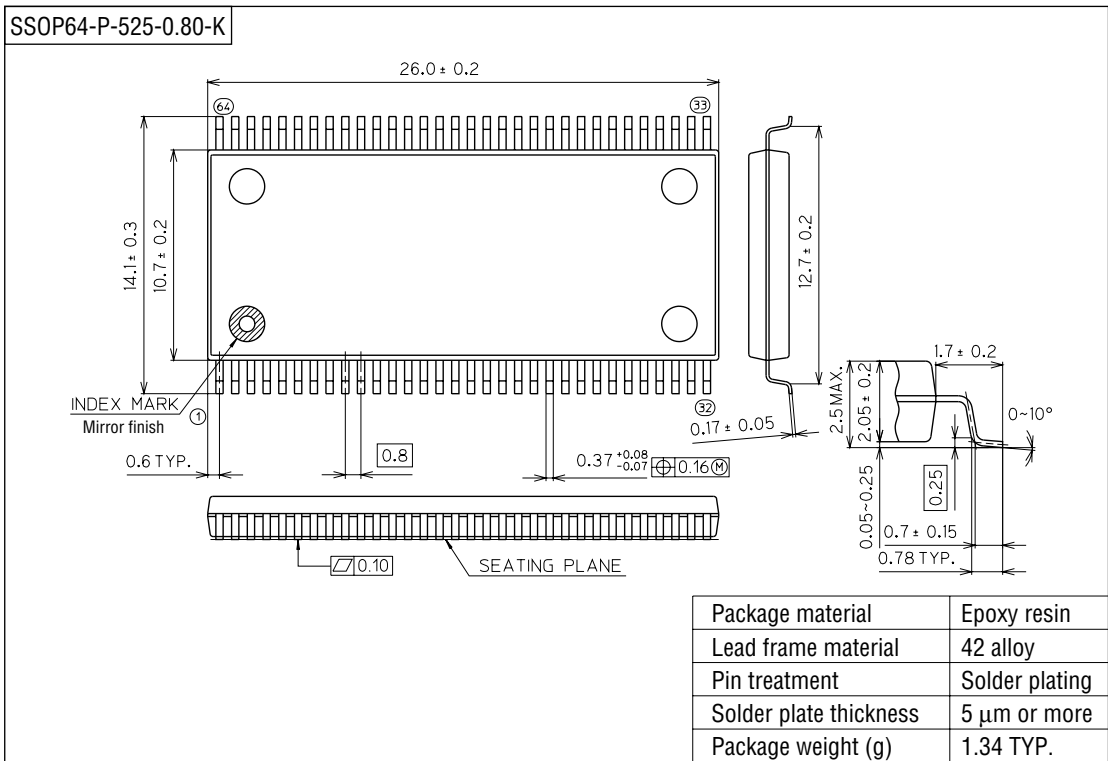




* : Same Data ▨ "H" or "L"

PACKAGE DIMENSIONS

(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).