OKI Semiconductor

This version: Jan. 1998

MSM54V32126A

131,072-Word × 32-Bit DYNAMIC RAM : FAST PAGE MODE TYPE WITH EDO

DESCRIPTION

The MSM54V32126A is a Graphics DRAM organized in a 131,072-word × 32-bit configuration. The technology used to fabricate the MSM54V32126A is OKI's CMOS silicon gate process technology. The device operates with a single 3.3 V power supply.

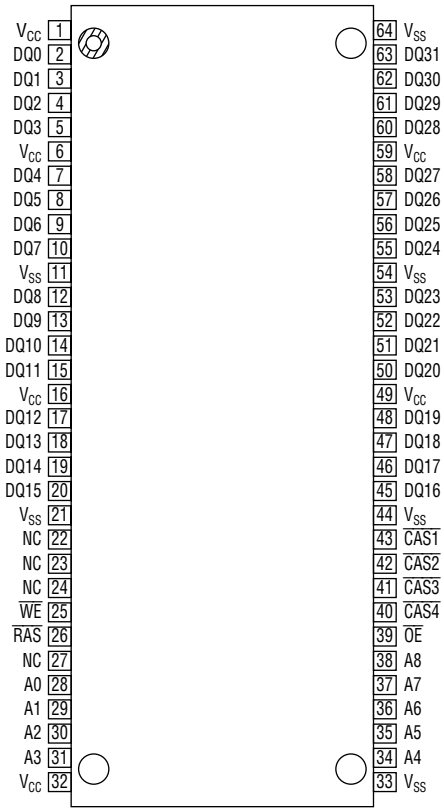
FEATURES

- 131,072-word × 32-bit organization
- Single 3.3 V power supply, ±0.3 V tolerance
- Refresh: 512 cycles/8 ms
- Fast Page Mode with Extended Data Out (EDO)
- Byte write, Byte read
- $\overline{RAS}$ only refresh
- $\overline{CAS}$ before $\overline{RAS}$ refresh
- $\overline{CAS}$ before $\overline{RAS}$ self-refresh
- Hidden refresh
- Package options:
  64-pin 525 mil plastic SSOP (SSOP64-P-525-0.80-K) (Product : MSM54V32126A-xxGS-K)
  70/64-pin 400 mil plastic TSOP (Type II) (TSOPII70/64-P-400-0.65-K) (Product : MSM54V32126A-xxTS-K)
  xx indicates speed rank.

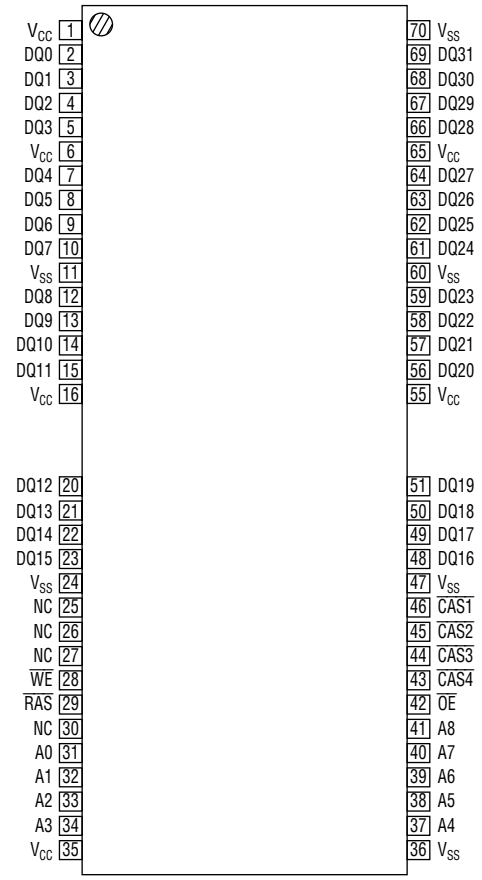
PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}	t_{OEA}		Operating (Max.)	Standby (Max.)
MSM54V32126A-45	45 ns	23 ns	13 ns	13 ns	90 ns	540 mW	3.1 mW
MSM54V32126A-50	50 ns	25 ns	15 ns	15 ns	100 ns	504 mW	
MSM54V32126A-60	60 ns	30 ns	18 ns	18 ns	120 ns	486 mW	

PIN CONFIGURATION (TOP VIEW)



64-Pin Plastic SSOP

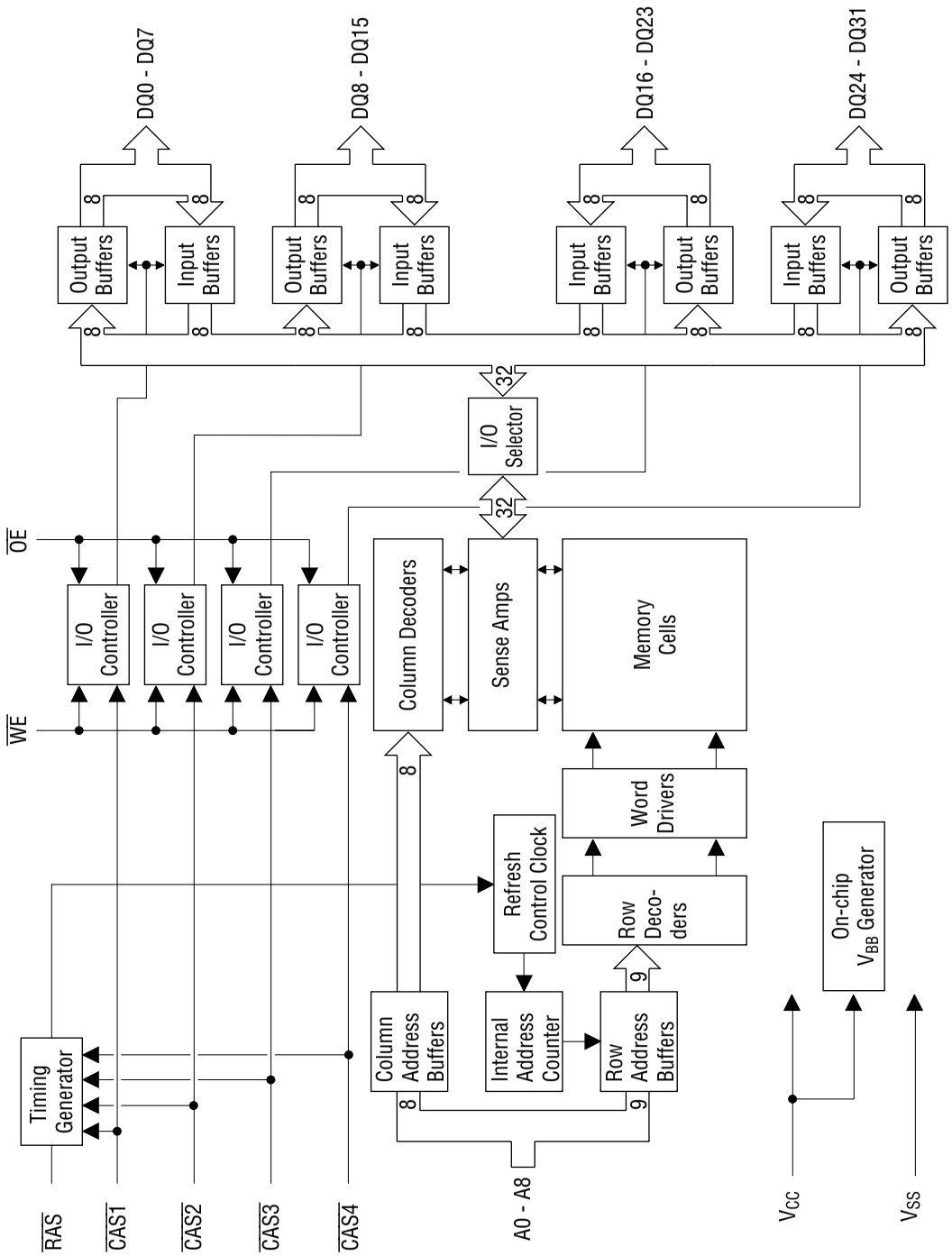


70/64-Pin Plastic TSOP (II)
(K Type)

Pin Name	Function
A0 - A8	Address Input
DQ0 - DQ31	Data Input / Data Output
$\overline{RAS}$	Row Address Strobe
$\overline{CAS1}$ - $\overline{CAS4}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply (3.3 V)
V_{SS}	Ground (0 V)
NC	No Connection

Note: The same power supply voltage must be provided to every V_{CC} pin, and the same GND voltage level must be provided to every V_{SS} pin.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	–0.5 to 4.5	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D	1	W
Operating Temperature	T_{opr}	0 to 70	°C
Storage Temperature	T_{stg}	–55 to 150	°C

Recommended Operating Conditions

(Ta = 0°C to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	3.0	3.3	3.6	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	3.0	—	3.6	V
Input Low Voltage	V_{IL}	–0.3	—	0.3	V

Capacitance

(V_{CC} = 3.3 V ±0.3 V, Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance	C_{IN}	—	7	pF
Input / Output Capacitance	C_{IO}	—	7	pF

DC Characteristics

(V_{CC} = 3.3 V ±0.3 V, Ta = 0°C to 70°C)

Parameter	Symbol	Condition	MSM54V32126A -45		MSM54V32126A -50		MSM54V32126A -60		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	V_{OH}	I_{OH} = –0.1 mA	2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V	
Output Low Voltage	V_{OL}	I_{OL} = 0.1 mA	0	0.8	0	0.8	0	0.8	V	
Input Leakage Current	I_{LI}	0 V < V_{IN} < V_{CC}; All other pins not under test = 0 V	–10	10	–10	10	–10	10	µA	
Output Leakage Current	I_{LO}	0 V < V_{OUT} < 3.6 V Output Disable	–10	10	–10	10	–10	10	µA	
Average Power Supply Current (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = Min.	—	140	—	130	—	110	mA	1, 2, 3
Power Supply Current (Standby)	I_{CC2}	$\overline{RAS}$ ≥ V_{CC} – 0.2 V, $\overline{CAS}$ ≥ V_{CC} – 0.2 V	—	850	—	850	—	850	µA	
Average Power Supply Current ($\overline{RAS}$ Only Refresh)	I_{CC3}	$\overline{RAS}$ = cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = Min.	—	140	—	130	—	110	mA	1, 2, 3
Average Power Supply Current (Fast Page Mode)	I_{CC4}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{HPC} = Min.	—	150	—	140	—	135	mA	1, 2, 4
Average Power Supply Current ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	I_{CC5}	$\overline{RAS}$ = cycling, $\overline{CAS}$ before $\overline{RAS}$	—	140	—	130	—	110	mA	1, 2, 4
Average Power Supply Current ($\overline{CAS}$ before $\overline{RAS}$ Self-Refresh)	I_{CCS}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = V_{IL}	—	950	—	950	—	950	µA	1, 2

Notes:
1. Specified values are obtained with minimum cycle time.
2. I_{CC} is dependent on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
4. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

AC Characteristics (1/2)

(V_{CC} = 3.3 V ±0.3 V, Ta = 0°C to 70°C) Note 1, 2, 3

Parameter	Symbol	MSM54V32126A -45		MSM54V32126A -50		MSM54V32126A -60		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	90	—	100	—	120	—	ns	
Read Modify Write Cycle	t_{RWC}	135	—	145	—	170	—	ns	
Fast Page Mode Cycle Time	t_{HPC}	18	—	20	—	24	—	ns	
Fast Page Mode Read-Modify-Write Cycle Time	t_{PRWC}	65	—	70	—	80	—	ns	
Access Time from $\overline{RAS}$	t_{RAC}	—	45	—	50	—	60	ns	4, 9,10
Access Time from Column Address	t_{AA}	—	23	—	25	—	30	ns	4, 10
Access Time from $\overline{CAS}$	t_{CAC}	—	13	—	15	—	18	ns	4, 9
Access Time from $\overline{CAS}$ Precharge	t_{CPA}	—	28	—	30	—	35	ns	4, 13
Output Buffer Turn-off Delay Time from $\overline{RAS}$	t_{REZ}	3	20	3	20	3	20	ns	5
Output Buffer Turn-off Delay Time from $\overline{CAS}$	t_{CEZ}	3	20	3	20	3	20	ns	5
Transition Time (Rise and Fall)	t_T	3	35	3	35	3	35	ns	3
$\overline{RAS}$ Precharge Time	t_{RP}	39	—	44	—	54	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	45	10k	50	10k	60	10k	ns	
$\overline{RAS}$ Pulse Width (Hyper Page Mode Only)	t_{RASP}	45	100k	50	100k	60	100k	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	12	—	14	—	14	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	45	—	50	—	60	—	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	6	10k	7	10k	9	10k	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	32	20	35	20	42	ns	9
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	22	15	25	15	30	ns	10
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	22	—	24	—	28	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	6	—	6	—	8	—	ns	13
$\overline{CAS}$ Precharge Time (Hyper Page Mode)	t_{CP}	6	—	7	—	9	—	ns	15
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	6	—	7	—	9	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	12
Column Address Hold Time	t_{CAH}	7	—	8	—	10	—	ns	12
Column Address Hold Time referenced to $\overline{RAS}$	t_{AR}	30	—	35	—	40	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	12
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	ns	6, 12
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	ns	6
$\overline{CAS}$ "H" to $\overline{RAS}$ "H" Lead Time	t_{CRL}	0	—	0	—	0	—	ns	
$\overline{RAS}$ "H" to $\overline{CAS}$ "H" Lead Time	t_{RCL}	0	—	0	—	0	—	ns	
Data Output Hold after $\overline{CAS}$ Low	t_{DOH}	3	—	3	—	3	—	ns	11
Write Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	8, 12
Write Command Hold Time	t_{WCH}	7	—	8	—	10	—	ns	12

AC Characteristics (2/2)

(V_{CC} = 3.3 V ±0.3 V, Ta = 0°C to 70°C) Note 1, 2, 3

Parameter	Symbol	MSM54V32126A -45		MSM54V32126A -50		MSM54V32126A -60		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Command Hold Time referenced to $\overline{RAS}$	t_{WCR}	30	—	35	—	40	—	ns	
Write Command Pulse Width	t_{WP}	8	—	9	—	10	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	8	—	9	—	10	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	8	—	9	—	10	—	ns	14
Output Buffer Turn-off Delay Time from $\overline{WE}$	t_{WEZ}	3	20	3	20	3	20	ns	5
Data Set-up Time	t_{DS}	0	—	0	—	0	—	ns	7, 12
Data Hold Time	t_{DH}	7	—	8	—	10	—	ns	7, 12
Data Hold Time referenced to $\overline{RAS}$	t_{DHR}	30	—	35	—	40	—	ns	
$\overline{OE}$ to Data-in Delay Time	t_{OED}	12	—	12	—	12	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	65	—	70	—	80	—	ns	8
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	42	—	45	—	50	—	ns	8
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	32	—	35	—	40	—	ns	8
Data to $\overline{CAS}$ Delay Time	t_{DZC}	0	—	0	—	0	—	ns	
Data to $\overline{OE}$ Delay Time	t_{DZO}	0	—	0	—	0	—	ns	
Access Time from $\overline{OE}$	t_{OEA}	—	13	—	15	—	18	ns	
Output Buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	3	20	3	20	3	20	ns	5
$\overline{OE}$ Command Hold Time	t_{OEH}	8	—	9	—	10	—	ns	
$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	t_{ROH}	10	—	10	—	12	—	ns	
$\overline{OE}$ "L" to $\overline{CAS}$ "H" Lead Time	t_{OCH}	10	—	10	—	10	—	ns	
$\overline{CAS}$ "H" to $\overline{OE}$ "L" Lead Time	t_{CHO}	10	—	10	—	10	—	ns	
$\overline{OE}$ Precharge Time	t_{OEP}	10	—	10	—	12	—	ns	
$\overline{WE}$ Pulse Width (Output Disable)	t_{WPE}	10	—	10	—	12	—	ns	
$\overline{CAS}$ Set-up Time for $\overline{CAS}$ before $\overline{RAS}$ Cycle	t_{CSR}	6	—	8	—	10	—	ns	12
$\overline{CAS}$ Hold Time for $\overline{CAS}$ before $\overline{RAS}$ Cycle	t_{CHR}	6	—	8	—	10	—	ns	13
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	t_{RPC}	10	—	10	—	10	—	ns	12
$\overline{CAS}$ Precharge Time (Refresh Counter Test)	t_{CPT}	20	—	25	—	30	—	ns	15
Refresh Period	t_{REF}	—	8	—	8	—	8	ms	
$\overline{RAS}$ Pulse Width ($\overline{CAS}$ before $\overline{RAS}$ Self-Refresh)	t_{RASS}	100	—	100	—	100	—	µs	
$\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Self-Refresh)	t_{RPS}	100	—	110	—	130	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Self-Refresh)	t_{CHS}	0	—	0	—	0	—	ns	

Notes:
1. An initial pause of 200 µs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example : $\overline{RAS}$ only refresh) before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ cycles instead of 8 $\overline{RAS}$ cycles are required.
2. The AC characteristics assume at t_T = 3 ns.
3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}. Input levels at the AC testing are 3.0 V/0 V.
4. Data outputs are measured with a load of 30 pF.
   DOUT reference levels : V_{OH}/V_{OL} = 2.0 V/0.8 V.
5. t_{REZ} (Max.), t_{CEZ} (Max.), t_{WEZ} (Max.) and t_{OEZ} (Max.) define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels. This parameter is sampled and not 100% tested.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{CAS}$ leading edge of early write cycles and to $\overline{WE}$ leading edge in $\overline{OE}$ controlled write cycles and read modify write cycles.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (Min.), the cycle is an early write cycle and the data out pin will remain open circuit throughout the entire cycle; If $t_{RWD} \geq t_{RWD}$ (Min.), $t_{CWD} \geq t_{CWD}$ (Min.) and $t_{AWD} \geq t_{AWD}$ (Min.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out is indeterminate.
9. Operation within the t_{RCD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled by t_{CAC}.
10. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, then access time is controlled by t_{AA}.
11. This is guaranteed by design. ($t_{DOH} = t_{CAC}$ - output transition time) This parameter is not 100% tested.
12. These parameters are determined by the earliest falling edge of $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$, or $\overline{CAS4}$.
13. These parameters are determined by the latest rising edge of $\overline{CAS1}$, $\overline{CAS2}$, $\overline{CAS3}$, or $\overline{CAS4}$.
14. t_{CWL} should be satisfied by all $\overline{CAS}$es.
15. t_{CP} and t_{CPT} are determined by the time that all $\overline{CAS}$es are high.

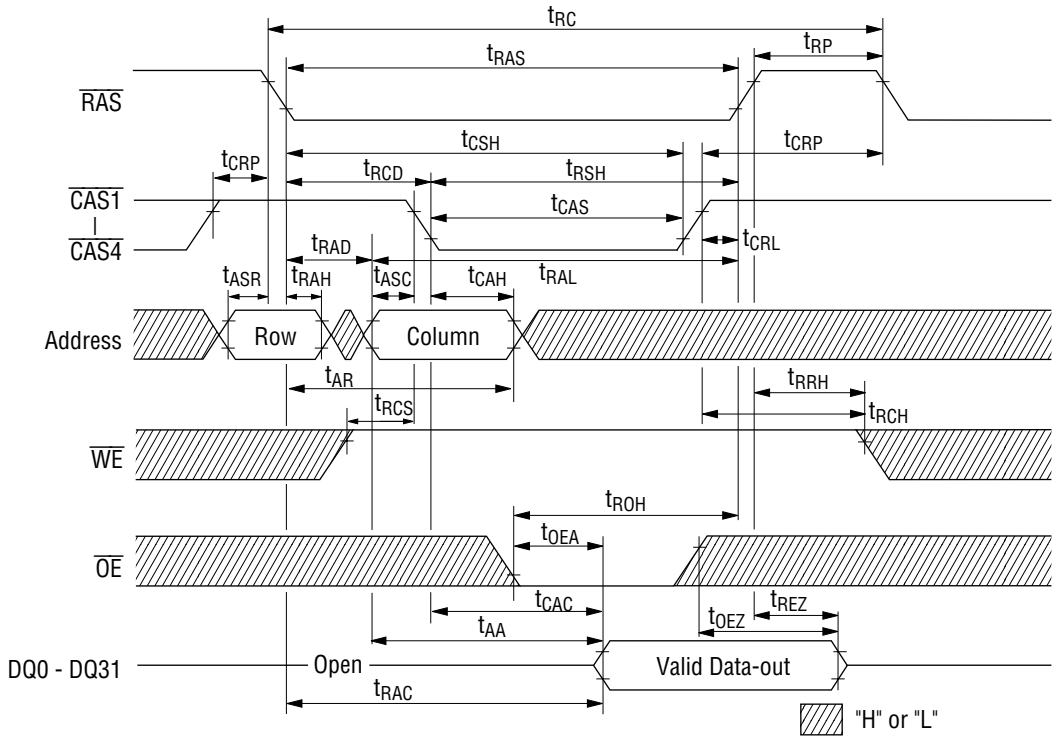
$\overline{\text{CAS}}$n-DQ FUNCTION TABLE

$\overline{\text{CAS1}}$	$\overline{\text{CAS2}}$	$\overline{\text{CAS3}}$	$\overline{\text{CAS4}}$	DQ0-7	DQ8-15	DQ16-23	DQ24-31
H	H	H	H	*	*	*	*
H	H	H	L	*	*	*	Enable
H	H	L	H	*	*	Enable	*
H	H	L	L	*	*	Enable	Enable
H	L	H	H	*	Enable	*	*
H	L	H	L	*	Enable	*	Enable
H	L	L	H	*	Enable	Enable	*
H	L	L	L	*	Enable	Enable	Enable
L	H	H	H	Enable	*	*	*
L	H	H	L	Enable	*	*	Enable
L	H	L	H	Enable	*	Enable	*
L	H	L	L	Enable	*	Enable	Enable
L	L	H	H	Enable	Enable	*	*
L	L	H	L	Enable	Enable	*	Enable
L	L	L	H	Enable	Enable	Enable	*
L	L	L	L	Enable	Enable	Enable	Enable

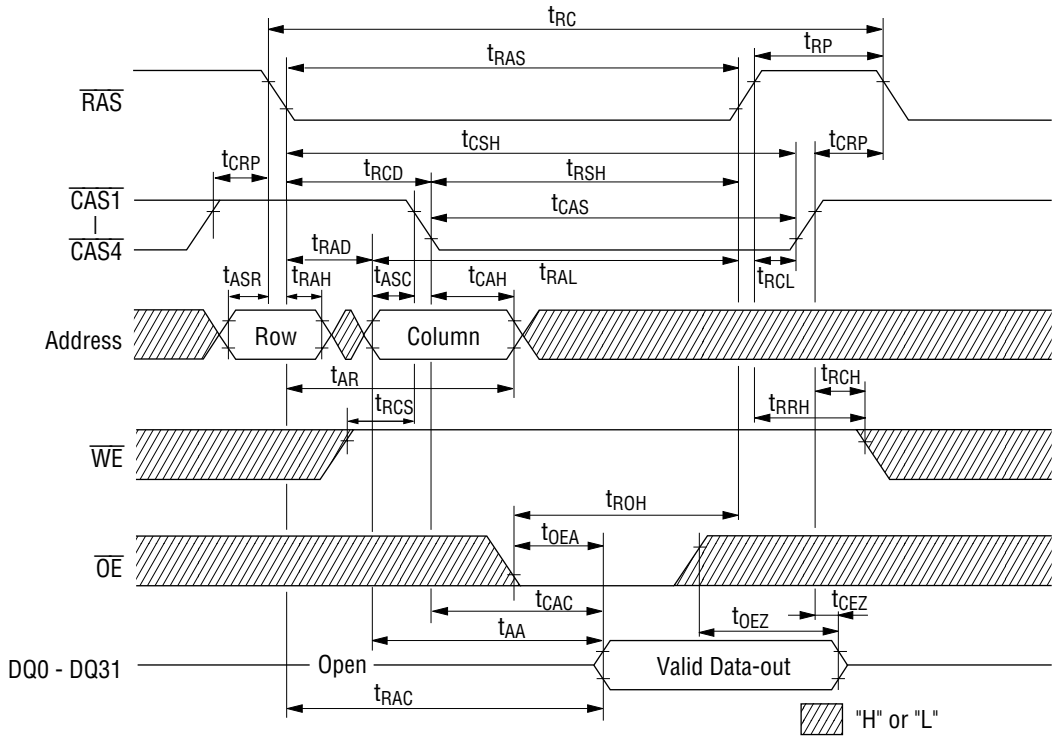
	Enable	*
Read cycle	Valid Data-out	High-Z
Write cycle	Write Data	Don't Care

TIMING WAVEFORM

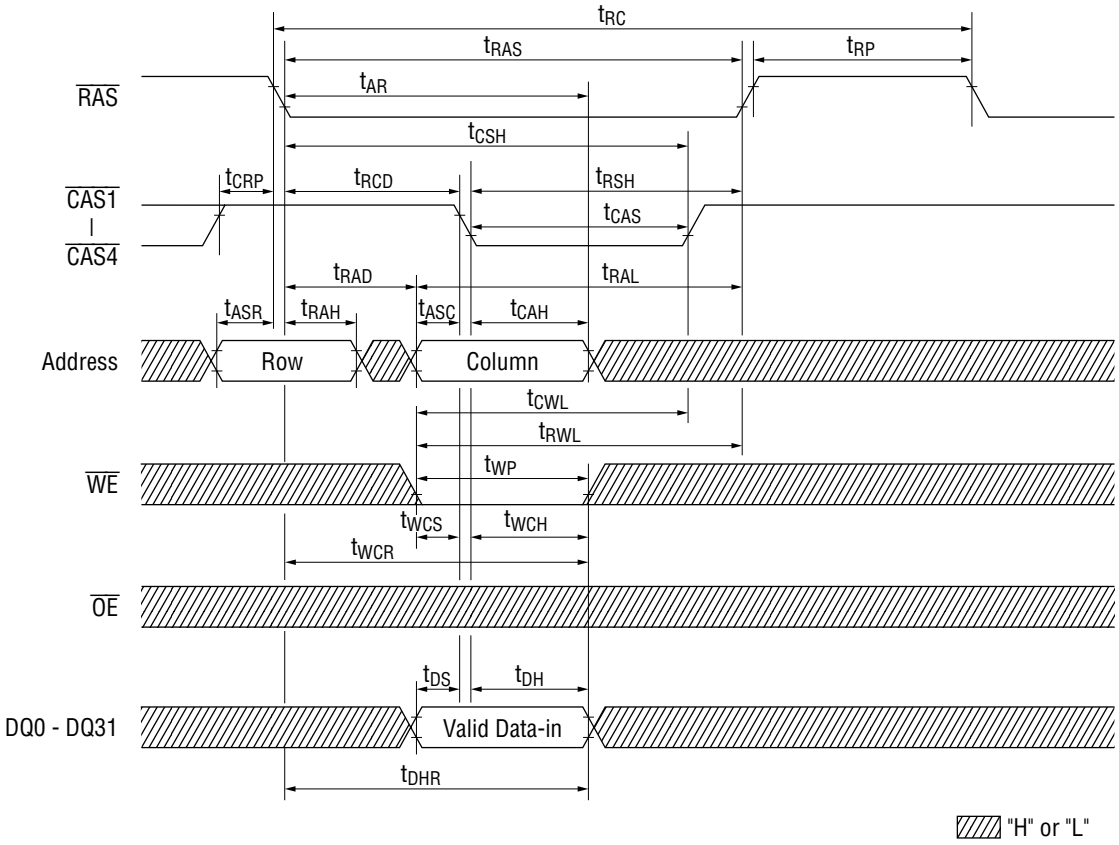
Read Cycle (Outputs Controlled by $\overline{RAS}$)



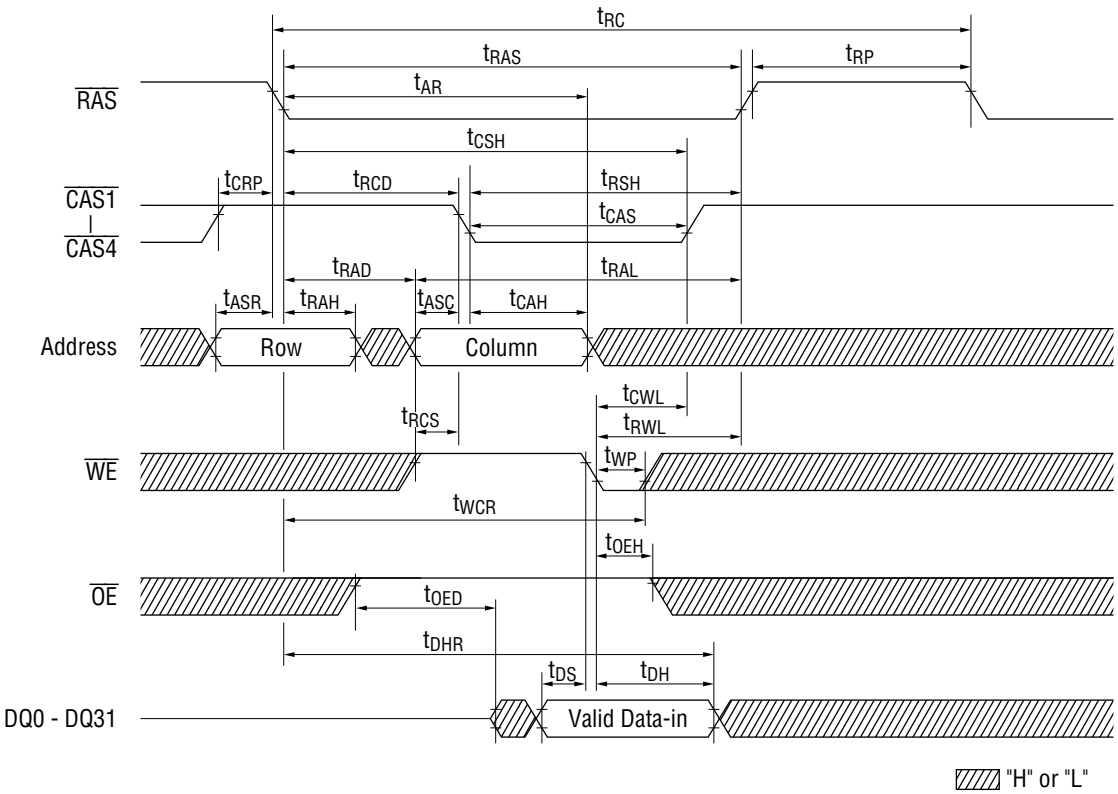
Read Cycle (Outputs Controlled by $\overline{CAS}$)



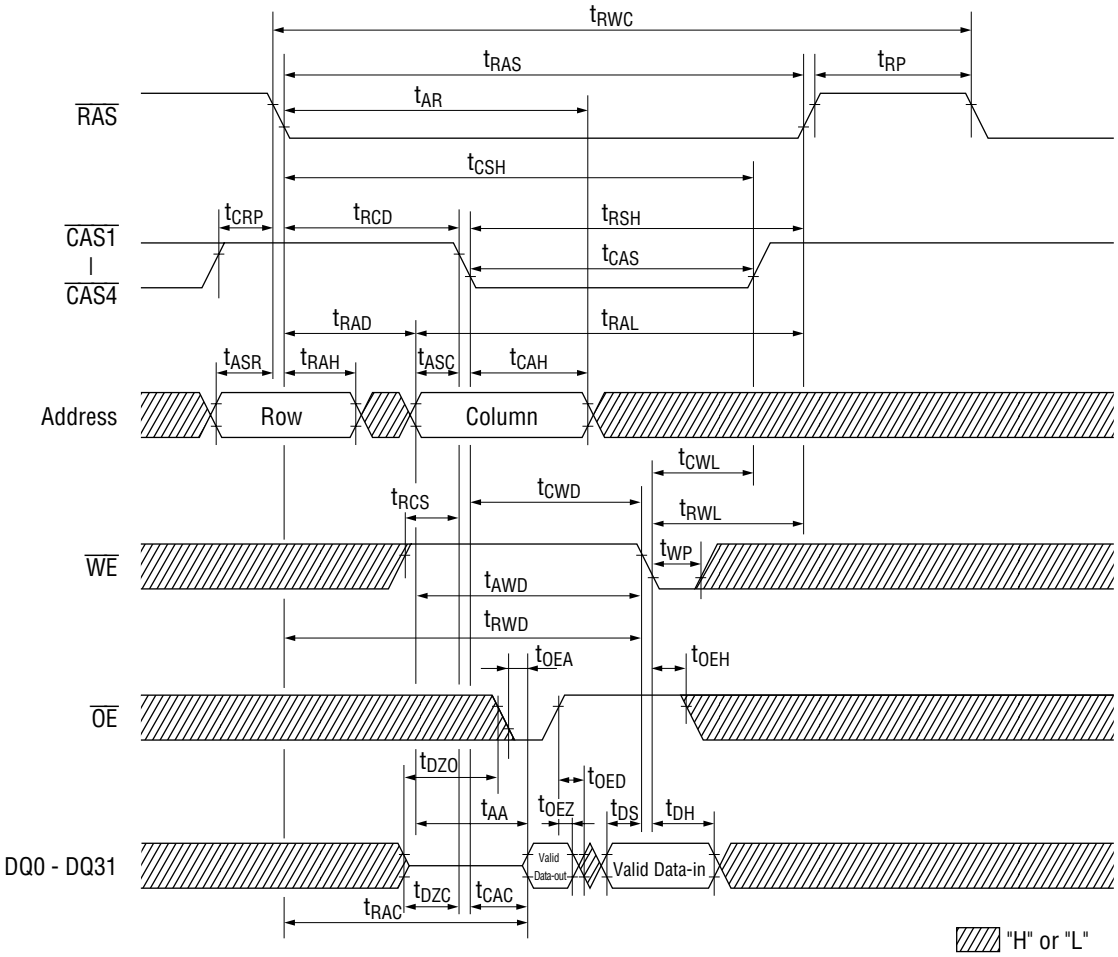
Write Cycle (Early Write)



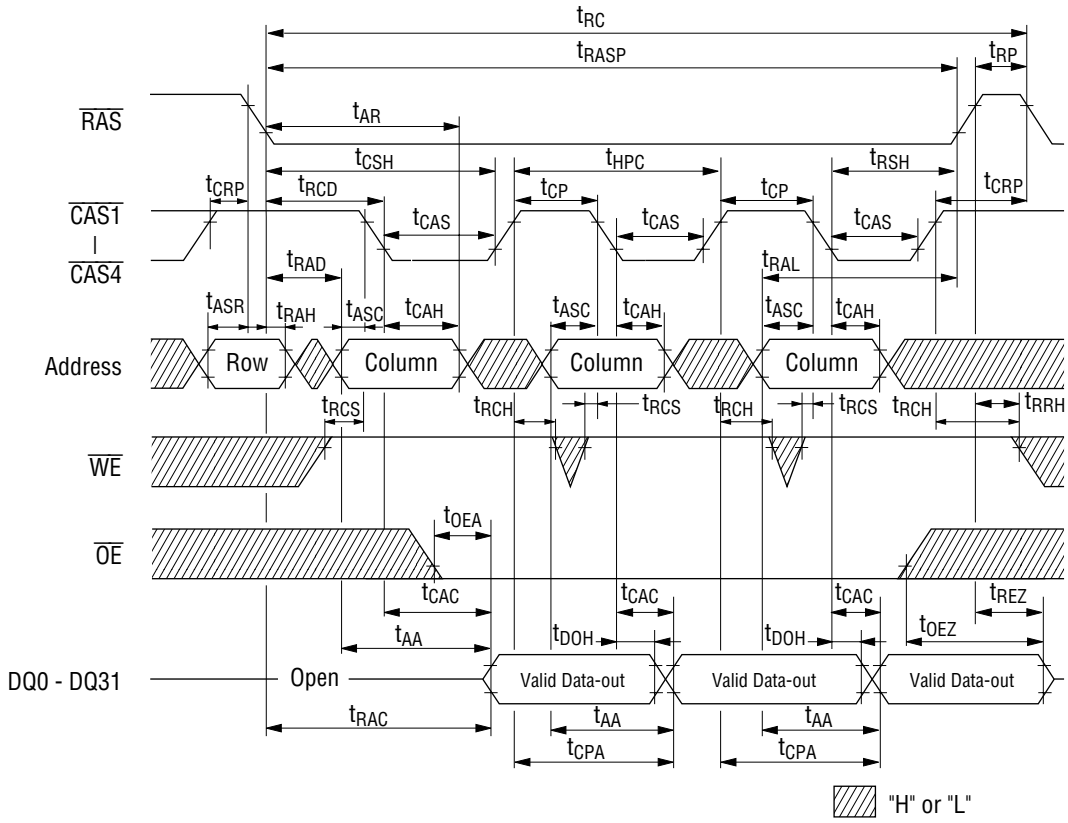
Write Cycle ($\overline{OE}$ Control Write)



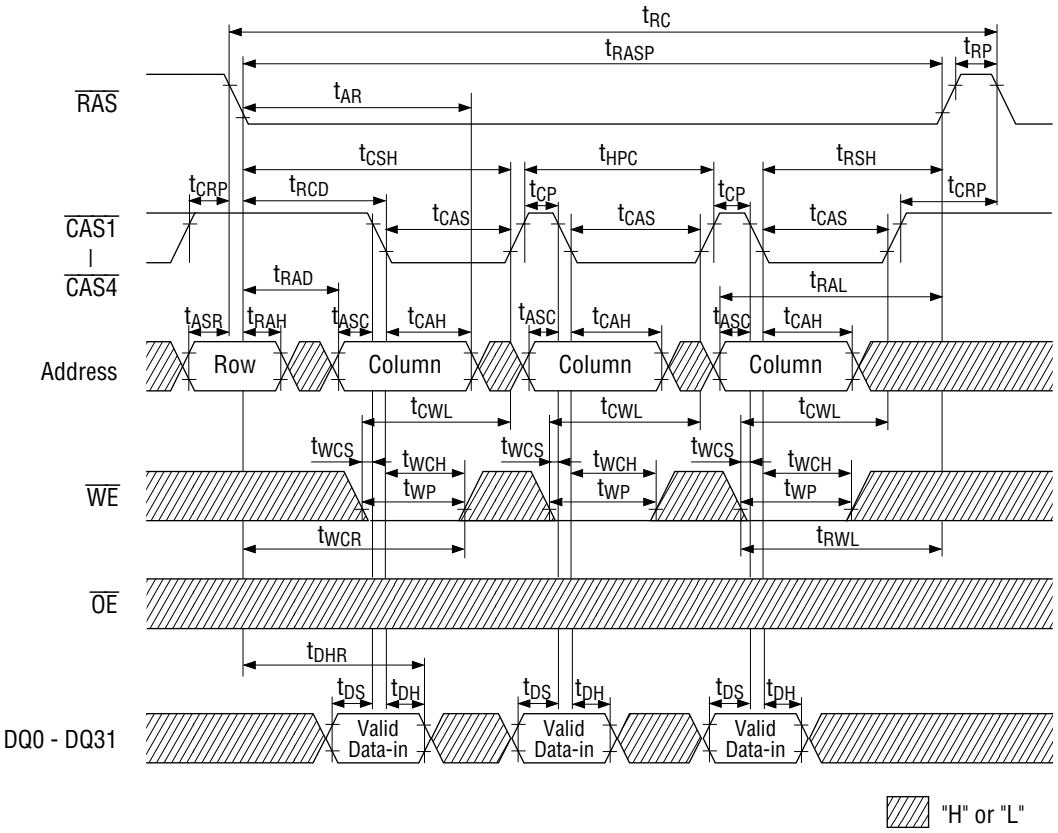
Read Modify Write Cycle



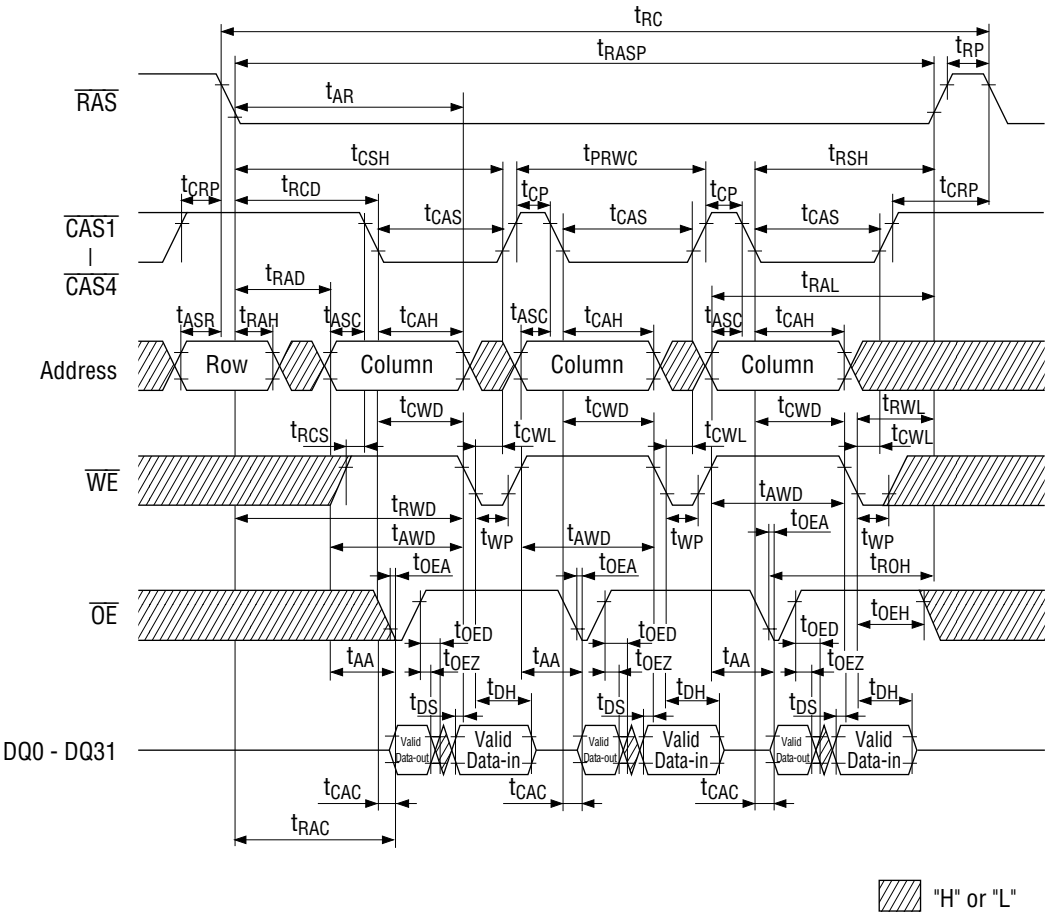
Fast Page Mode Read Cycle with EDO



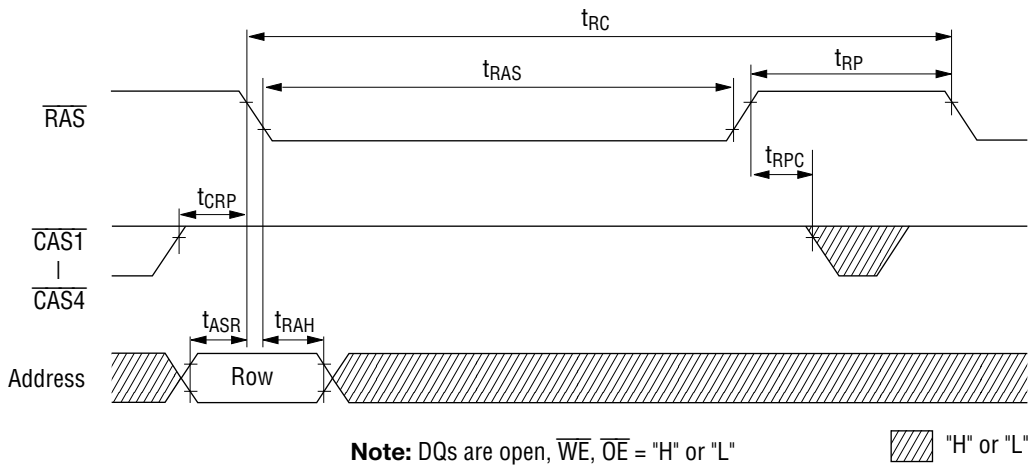
Fast Page Mode Write Cycle (Early Write)



Fast Page Mode Read Modify Write Cycle



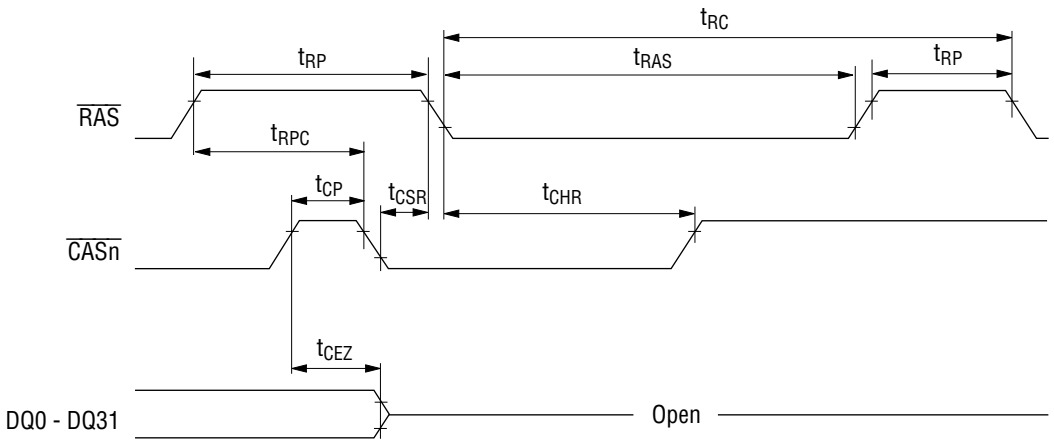
$\overline{RAS}$ Only Refresh Cycle



Note: DQs are open, $\overline{WE}$, $\overline{OE}$ = "H" or "L"

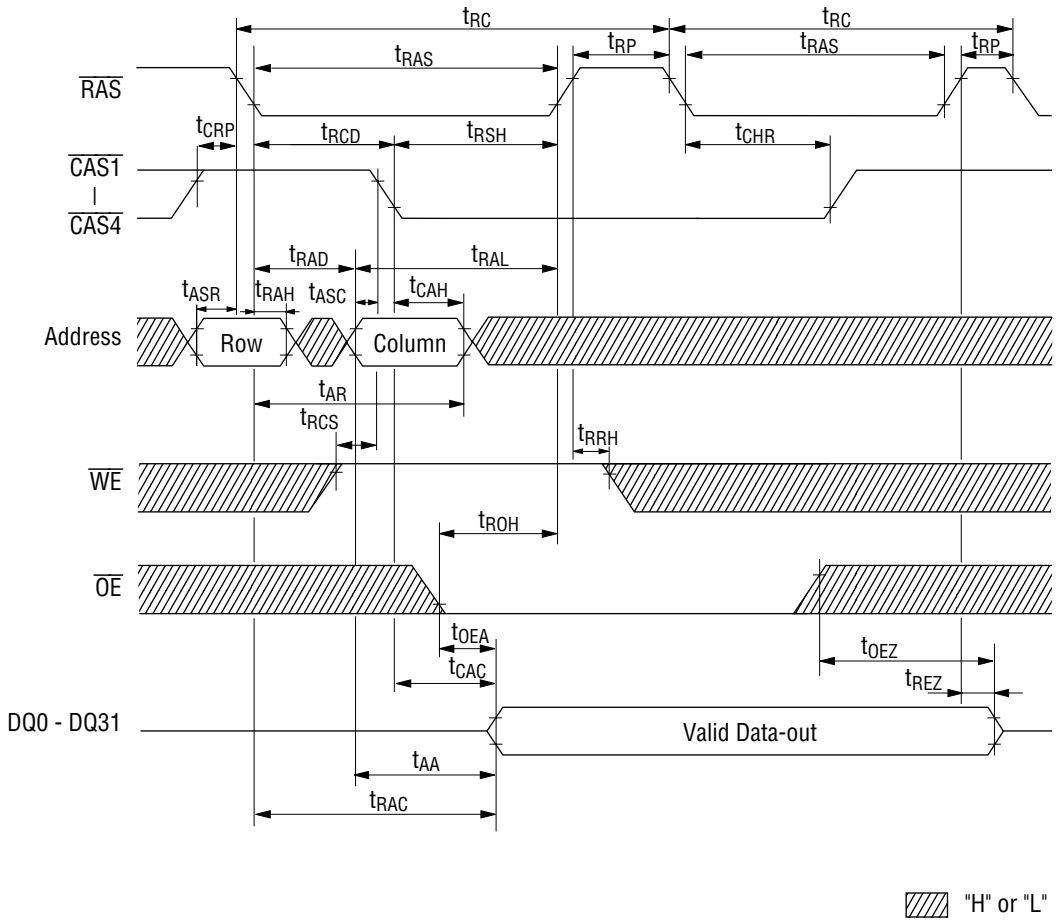
"H" or "L"

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle

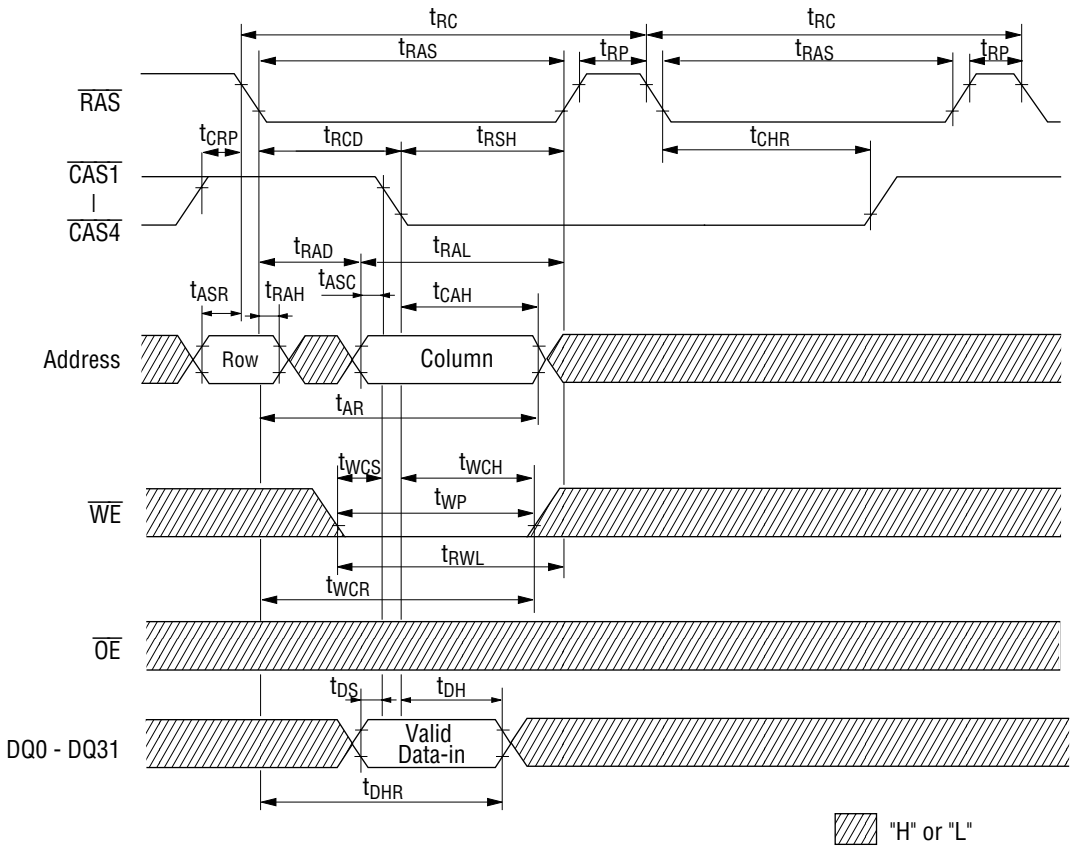


Note: $\overline{\text{WE}}$, $\overline{\text{OE}}$, A0 - A8 = "H" or "L"

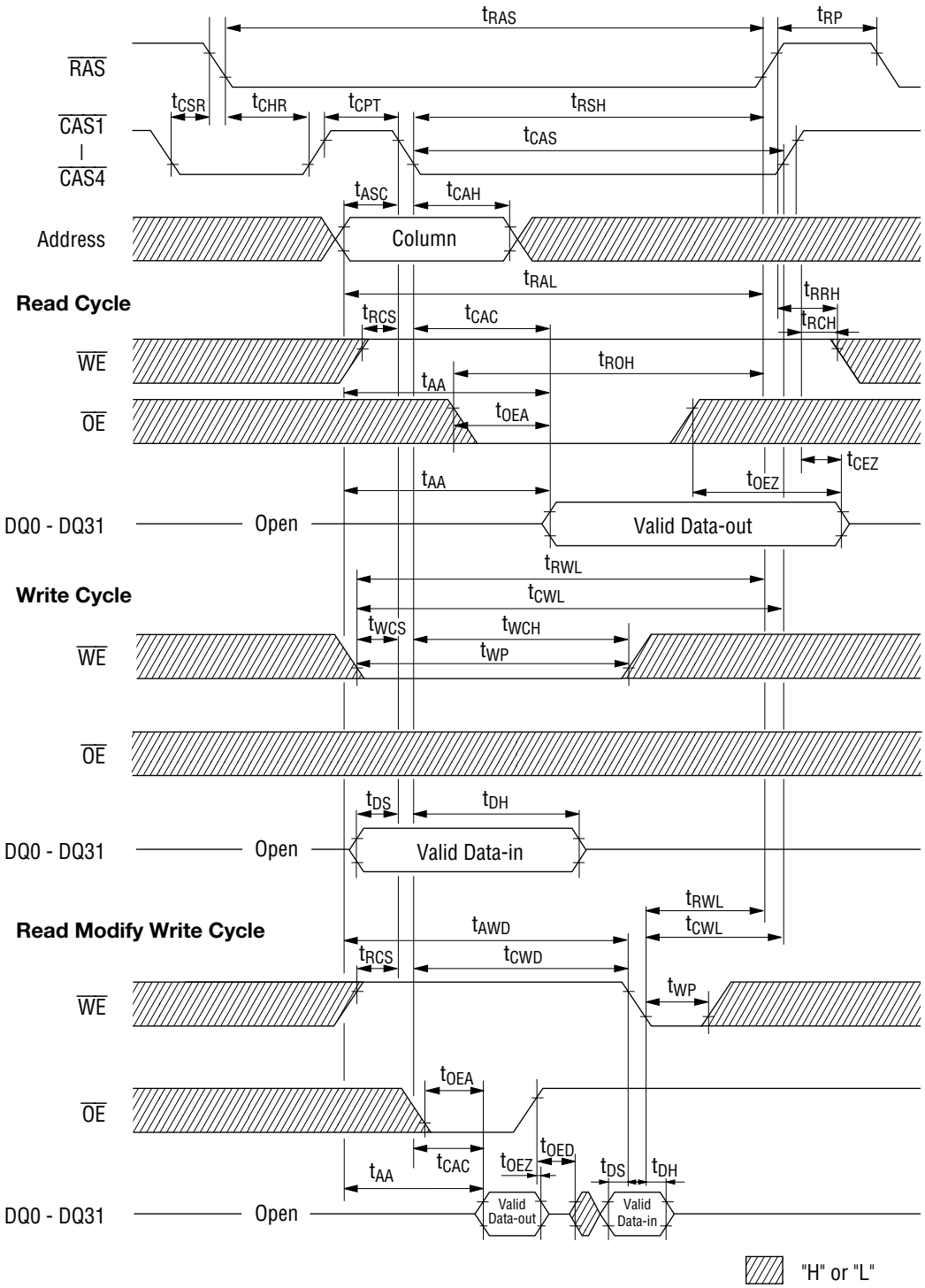
Hidden Refresh Read Cycle



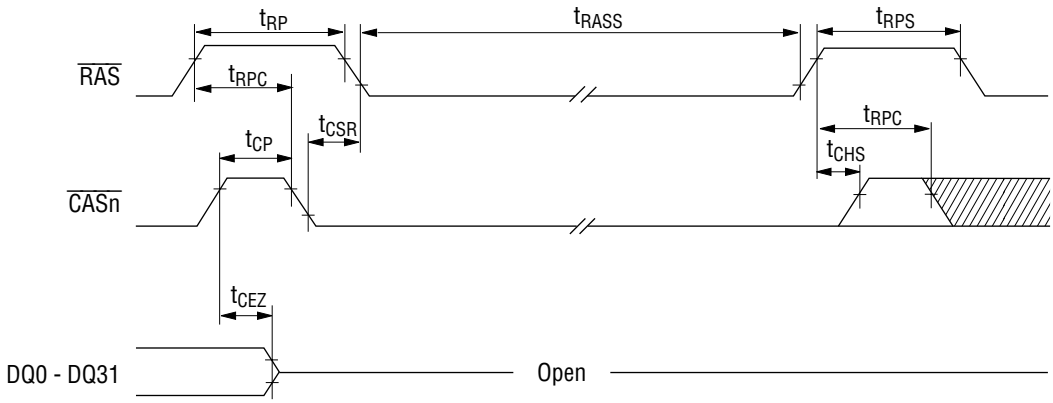
Hidden Refresh Write Cycle



CAS before RAS Refresh Counter Test Cycle

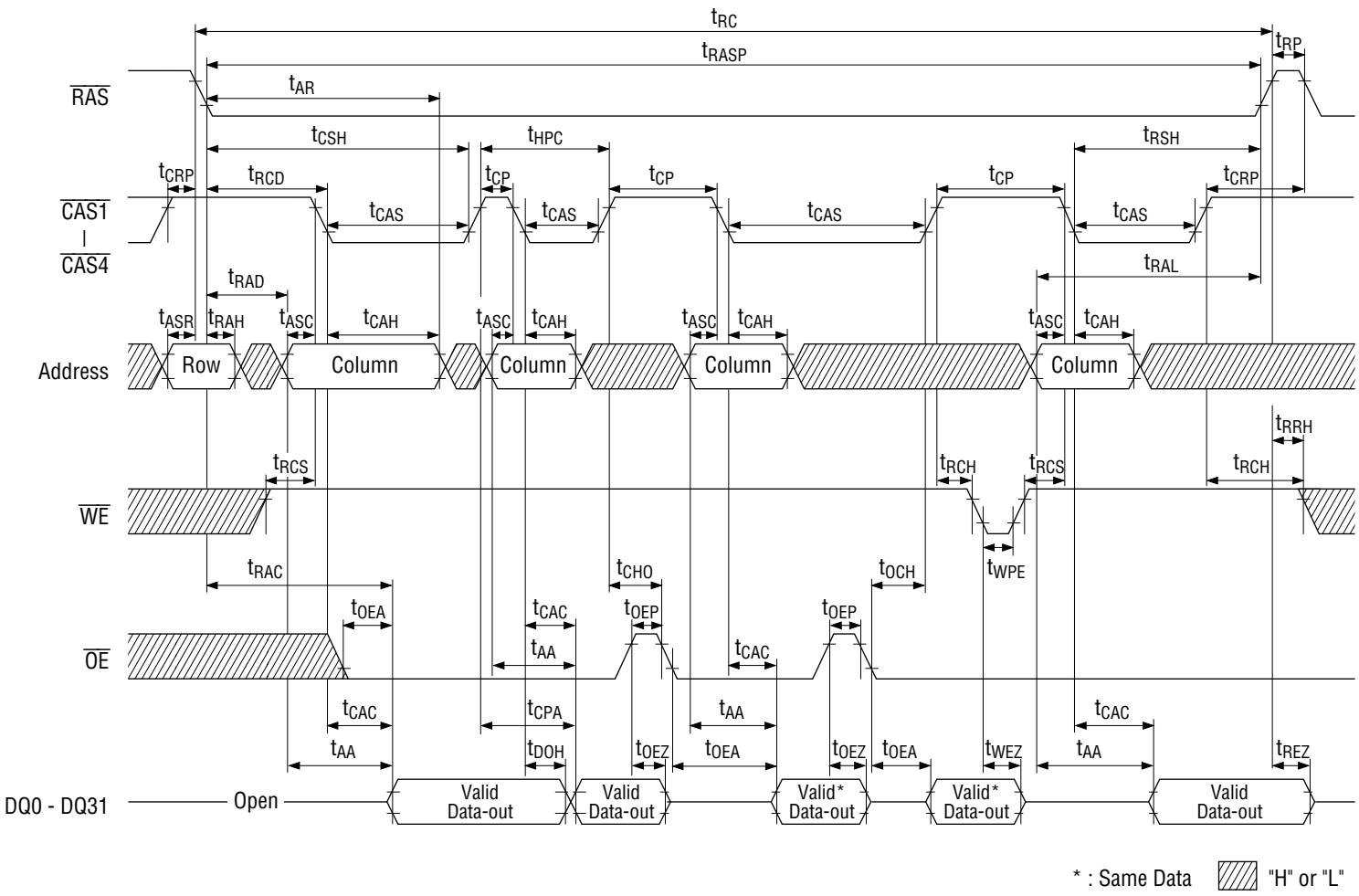


$\overline{CAS}$ before $\overline{RAS}$ Self-Refresh Cycle



Note: $\overline{WE}$, $\overline{OE}$, A0 - A8 = "H" or "L" "H" or "L"

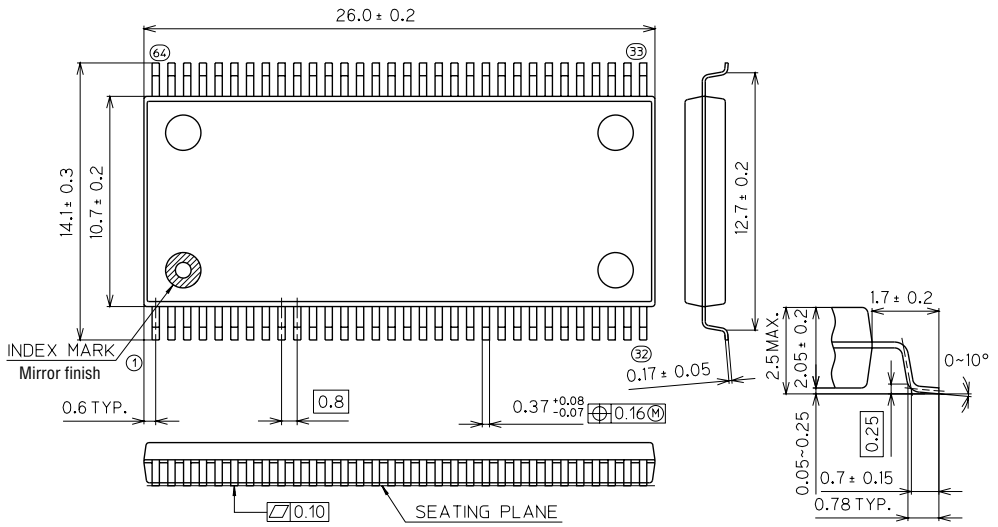
Fast Page Mode Read with EDO High-Z Operation



PACKAGE DIMENSIONS

(Unit : mm)

SSOP64-P-525-0.80-K



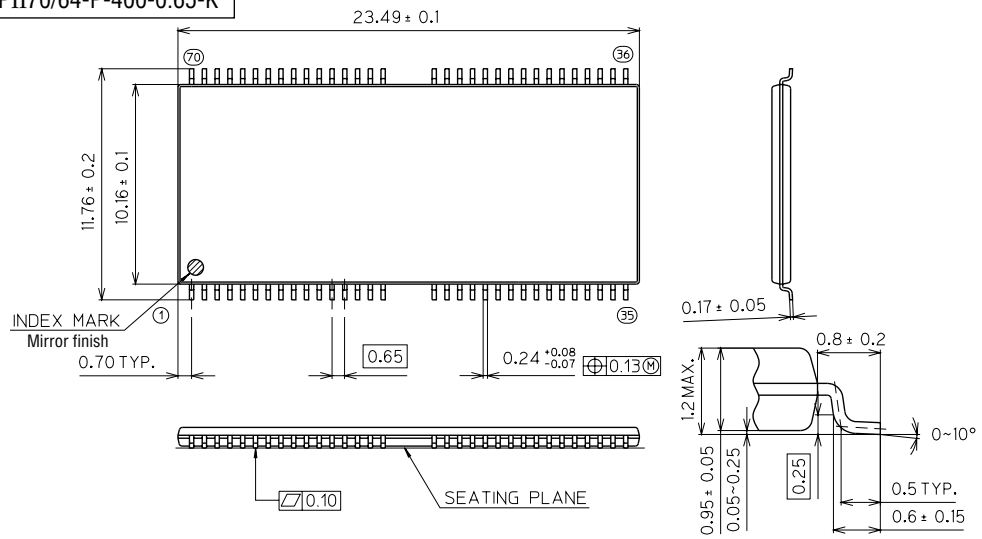
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 µm or more
Package weight (g)	1.34 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

TSOPII70/64-P-400-0.65-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.59 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).