OKI Semiconductor

This version: Nov. 1997
Previous version: Mar. 1996

MSM5839B

40-DOT SEGMENT DRIVER

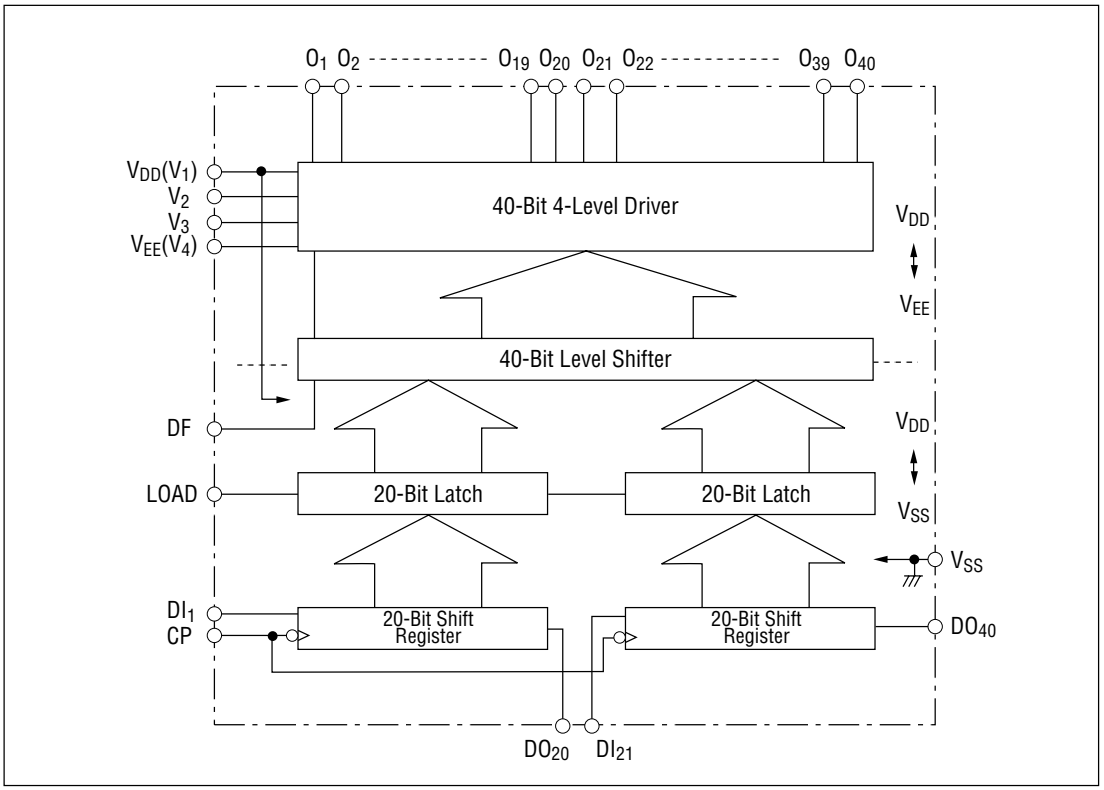
GENERAL DESCRIPTION

The MSM5839B is a dot matrix LCD segment driver LSI which is fabricated using low power CMOS metal gate technology. This LSI consists of two 20-bit shift registers, two 20-bit latches, a 40-bit level shifter and a 40-bit 4-level driver.
It converts serial data, which is received from an LCD controller LSI, to parallel data and outputs LCD driving waveform to the LCD panel.
Expansion of display can easily be made by increasing the number of characters and character patterns.
This LSI can drive a variety of LCD panels because the bias voltage, which determines the LCD driving voltage, can be optionally supplied from the external source.

FEATURES

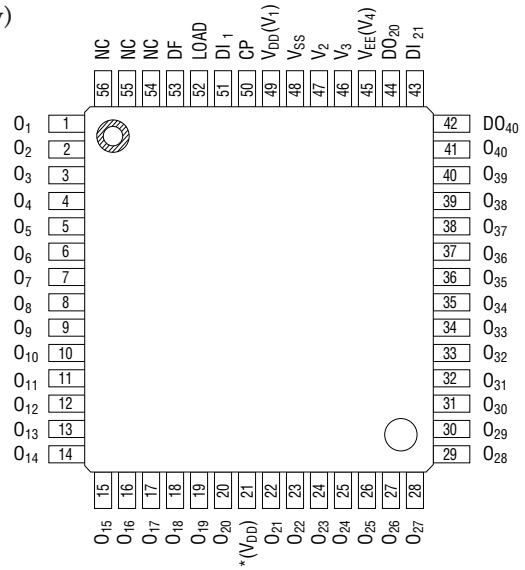
- Supply voltage : 4.5 to 5.5V
- LCD driving voltage : 8 to 18V
- Applicable LCD duty : 1/32 to 1/128
- Bias voltage can be supplied externally
- Applicable common driver : MSM5238 (32 outputs)
- Package options:
  56-pin plastic QFP (QFP56-P-910-0.65-K) (Product name: MSM5839B GS-K)
  56-pin plastic QFP (QFP56-P-910-0.65-L2) (Product name: MSM5839B GS-L2)
  56-pin plastic QFP (QFP56-P-910-0.65-2K) (Product name: MSM5839B GS-2K)

BLOCK DIAGRAM



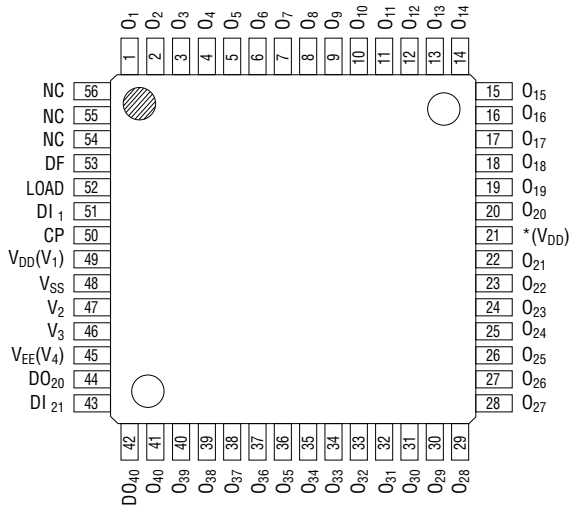
PIN CONFIGURATION

(Top view)



NC: No connection

56-Pin Plastic QFP (Type K)



NC: No connection

56-Pin Plastic QFP (Type L)

* This pin is internally connected to V_{DD}, so connect it to the power supply or leave it open.

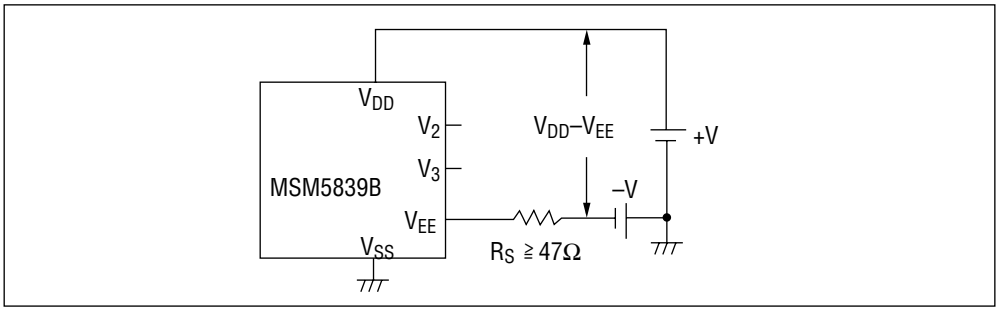
Note : The figure for Type L shows the configuration viewed from the reverse side of the package. Pay attention to the difference in pin arrangement.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage (1)	V_{DD} *1	Ta = 25°C	–0.3 to +6	V
Supply Voltage (2)	V_{DD}–V_{EE} *1 *2	Ta = 25°C	0 to 18	V
	V_{DD}–V_{EE}	Ta = 25°C	0 to 18	V
Input Voltage	V_1	Ta = 25°C	–0.3 to V_{DD} +0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

*1 $V_{DD} > V_2 > V_3 > V_{EE}$

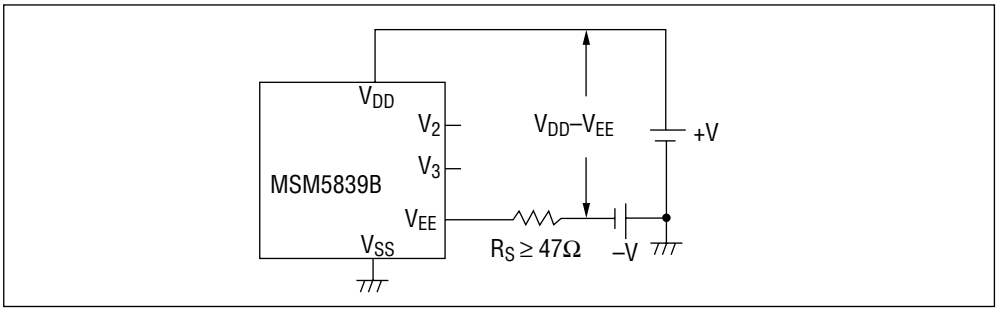
*2 Applies when a series resistor of 47Ω or more is connected as shown below.



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Supply Voltage (1)	V_{DD}	—	4.5 to 5.5	V
Supply Voltage (2)	V_{DD}–V_{EE} *1	—	8 to 16	V
	V_{DD}–V_{EE} *1 *2	—	8 to 18	V
Operating Temperature	T_{op}	—	–20 to +85	°C

*1 $V_{DD}>V_2>V_3>V_{EE}$
*2 Applies when a series resistor of 47Ω or more is connected as shown below.



ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 5V ±10%, Ta = –20 to +85°C)

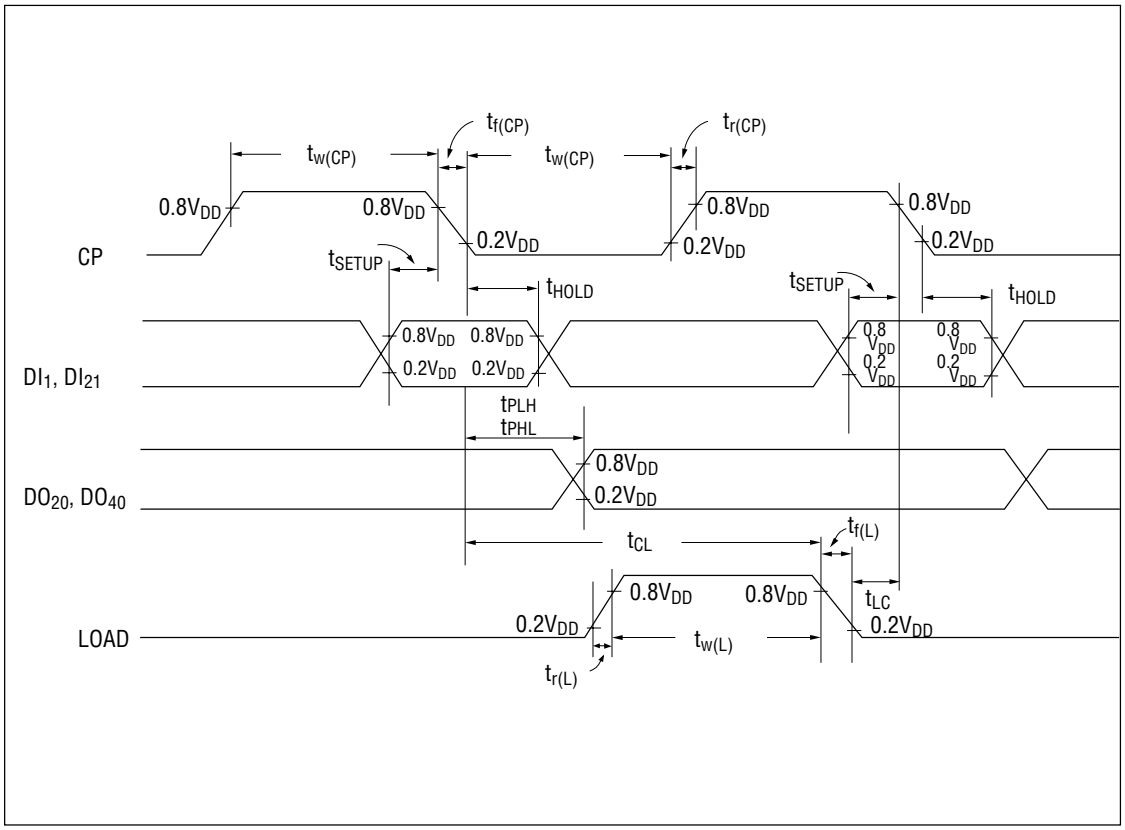
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH} *1	—	0.8V_{DD}	—	V_{DD}	V
"L" Input Voltage	V_{IL} *1	—	V_{SS}	—	0.2V_{DD}	V
"H" Input Current	I_{IH} *1	$V_I = V_{DD}$	—	—	1	µA
"L" Input Current	I_{IL} *1	V_I = 0V	—	—	–1	µA
"H" Output Voltage	V_{OH} *2	I_O =–0.4mA	V_{DD}–0.4	—	—	V
"L" Output Voltage	V_{OL} *2	I_O = 0.4mA	—	—	0.4	V
ON Resistance	R_{ON} *4	V_{DD}–V_{EE}= 10V *3 $\lvert V_N–V_O \rvert$ = 0.25V	—	3.5	7	kΩ
Supply Current	I_{DD}	Connect all inputs to V_{DD} or V_{SS} V_{DD}–V_{EE} = 18V, No load	—	—	100	µA

*1 Applicable to LOAD, CP, DI_1, DI_{21}, DF
*2 Applicable to DO_{20}, DO_{40}
*3 $V_N = V_{DD}$ to V_{EE}, $V_3 = \frac{2}{9}$ (V_{DD}–V_{EE}), $V_2 = \frac{7}{9}$ (V_{DD}–V_{EE})
*4 Applicable to O_1 - O_{40}

Switching Characteristics

(V_{DD} = 5V ±10%, Ta = –20 to +85°C, C_L = 15pF)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H", "L" Propagation Delay Time	tp_{LH} tp_{HL}	—	—	—	250	ns
Clock Frequency	f_{CP}	DUTY = 50%	—	—	3.3	MHz
Clock Pulse Width	$t_{W(CP)}$	—	125	—	—	ns
LOAD Pulse Width	$t_{W(L)}$	—	125	—	—	ns
Data Setup Time DI → CP	t_{SETUP}	—	50	—	—	ns
CP → LOAD Time	t_{CL}	—	250	—	—	ns
LOAD → CP Time	t_{LC}	—	0	—	—	ns
Data Hold Time DI → CP	t_{HOLD}	—	50	—	—	ns
CP Rise/Fall Time	$t_{r(CP)}$ $t_{f(CP)}$	—	—	—	50	ns
LOAD Rise/Fall Time	$t_{r(L)}$ $t_{f(L)}$	—	—	—	1	µs



FUNCTIONAL DESCRIPTION

Pin Functional Description

- **DI_1**
  The data input pin for the 20-bit shift register (from 1st to 20th bit). The display data is input to the data pin in synchronization with a clock pulse.

- **CP**
  Clock pulse input pin for the two 20-bit shift registers. The data is shifted in the two 20-bit shift registers at the falling edge of the clock pulse. Data setup time (t_{SETUP}) and data hold time (t_{HOLD}) are required each between DI_1, DI_{21} and CP. Refer to the Switching Characteristics.

- **DO_{20}**
  The 20th output bit of the shift register.
  The data which is input from DI_1 is clocked out with the delay in the number of bits of the shift register (20). A 40-bit shift register can be configured by connecting the output of this pin to DI_{21} pin.

- **DI_{21}**
  The data input pin for the 20-bit shift register (from 21st to 40th bit).
  Connecting the DO_{20} pin and this pin allows the device to be used as a 40-bit shift register.

- **DO_{40}**
  The 40th output bit of the shift register.
  The data which is input from DI_1 is clocked out with the delay in the number of the bits of the shift register (20).
  When extending the number of characters, this pin is used to cascade connect the next MSM5839B.

- **DF**
  Alternate signal input pin for LCD driving waveform.

- **$V_{DD}(V_1)$, V_{SS}**
  Supply voltage pins. V_{DD} should be 4.5 to 5.5V.
  V_{SS} is the ground pin (V_{SS} = 0V).

- **V_2, V_3, $V_{EE}(V_4)$**
  Bias supply voltage pins to drive the LCD. Bias voltage is supplied from an external source.

- **LOAD**
  The signal for latching the shift register contents is input from this pin.
  When LOAD pin is set at "H", the shift register contents are transferred to the 40-bit 4-level driver. When LOAD pin is set at "L", the last display output data (O_1 to O_{40}), which was transferred when LOAD pin was at "H", is held.

- **O_1 to O_{40}**
  Display data output pins which correspond to each data bit in the latch.
  One of V_{DD}, V_2, V_3 or V_{EE} (V_4) is selected as a display driving voltage source based on the combination of latched data level and DF signal. Refer to the Truth Table below.
  These pins should be connected to the SEGMENT side of the LCD panel.

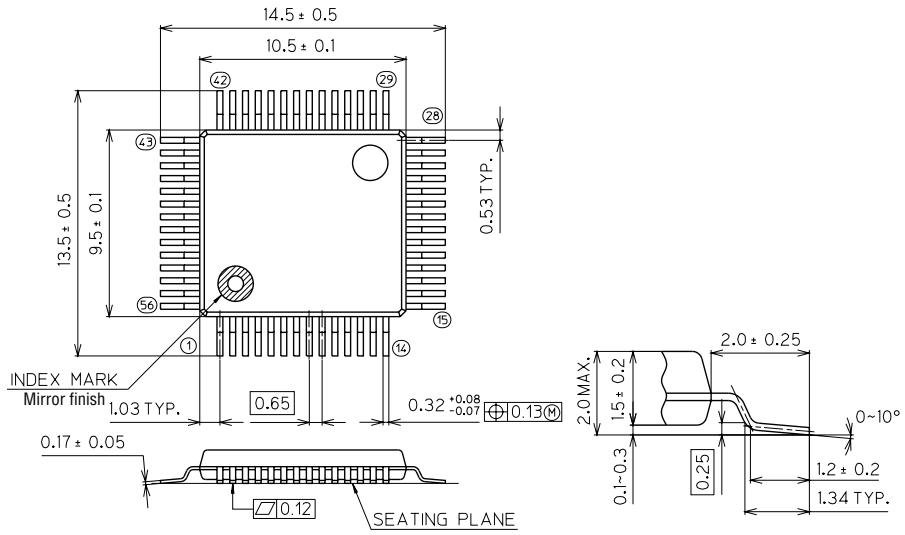
Truth Table

Latched data	DF	LCD driver output
H	H	V_{EE} (V_4)
	L	V_{DD} (V_1)
L	H	V_3
	L	V_2

PACKAGE DIMENSIONS

(Unit : mm)

QFP56-P-910-0.65-K



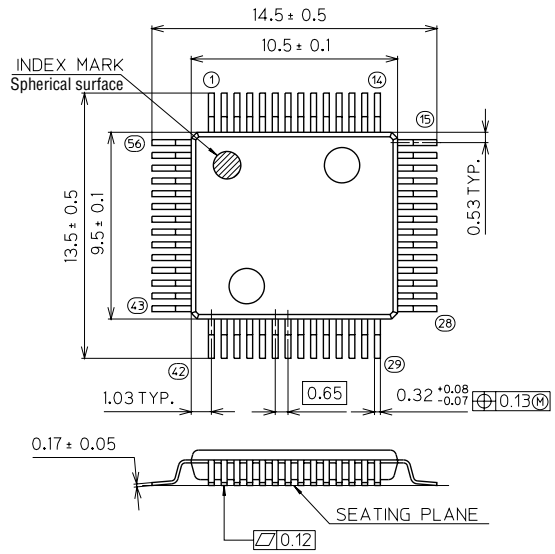
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.36 TYP.

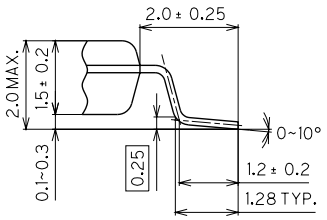
Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

QFP56-P-910-0.65-L2





Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.36 TYP.

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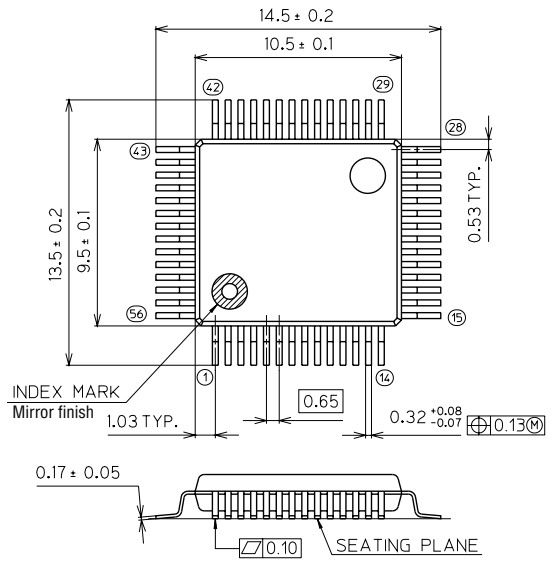
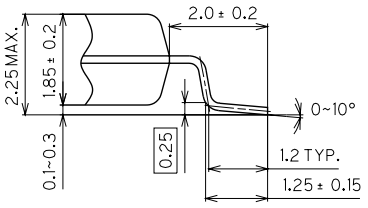
(Unit : mm)

QFP56-P-910-0.65-2K





Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.43 TYP.

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