

MSM64167E

4-Bit Microcontroller with Built-in Dual-Slope Type A/D Converter and LCD Driver

GENERAL DESCRIPTION

The MSM64167E is a low power 4-bit microcontroller that employs Oki's original CPU core nX-4/20.

The MSM64167E contains a dual-slope type A/D converter with a 4-channel input, LCD driver for up to 108 segments, and buzzer output port.

The MSM64167E is best suited for applications such as low power, high precision thermometers, barometers, and hygrometers.

FEATURES

- Operating range
 - Operating frequencies : 32.768 kHz, 700 kHz
 - Operating voltage : 2.6 to 3.6 V
 - Operating temperature : -40 to +85°C
- Memory space
 - Internal program memory : 4064 bytes
 - Internal data memory : 256 nibbles
- Minimum instruction execution time : 4.3 μ s @ 700 kHz
91.6 μ s @ 32.768 kHz
- Dual-slope type A/D converter : 4-channel input
- LCD driver : 31 outputs; duty ratio switchable by software
 - (1) At 1/4 duty and 1/3 bias : 108 segments (max)
 - (2) At 1/3 duty and 1/3 bias : 84 segments (max)
 - (3) At 1/2 duty and 1/2 bias : 58 segments (max)
- Buzzer driver : 1 output (4 output modes selectable)
- Timer : 16-bit \times 1
 - Auto-reload mode
 - Capture mode
 - Clock frequency measuring mode
- Watchdog timer
- Clock : 32.768 kHz crystal oscillator and 700 kHz RC oscillator (with an external resistor)
 - CPU clock : 32.768 kHz/700 kHz (switchable by software)
 - Time base clock : 32.768 kHz
- Power supply voltage : 3 V
- I/O port
 - Input-output port : 3 ports \times 4 bits
 - Output port : 2 ports \times 4 bits
(8 out of the 31 LCD driver outputs can be used as output-only ports by mask option.)
- Serial port : Synchronous/asynchronous mode support
 - Synchronous mode : 32.768 kHz/external clock
 - Asynchronous mode : 9600 bps/4800 bps/2400 bps/1200 bps

- Interrupt sources

- External interrupt : 2 sources

- Internal interrupt : 8 sources

- Package:

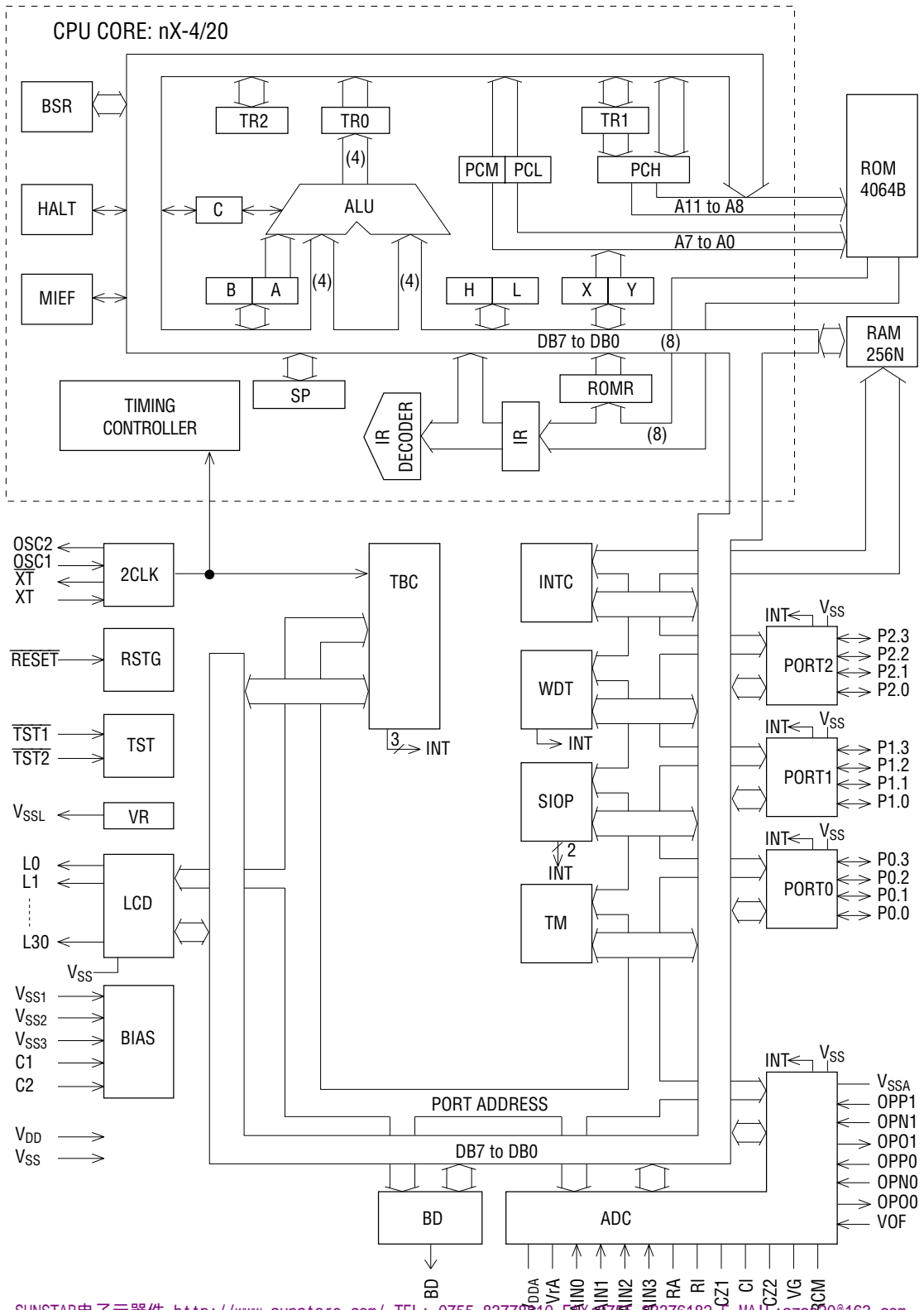
- 80-pin plastic QFP (QFP80-P-1420-0.80-BK) : (Product name : MSM64167E-xxxGA)

- 80-pin plastic TQFP (TQFP80-P-1212-0.50-K) : (Product name : MSM64167E-xxxTB)

- Chip : (Product name : MSM64167E-xxx)

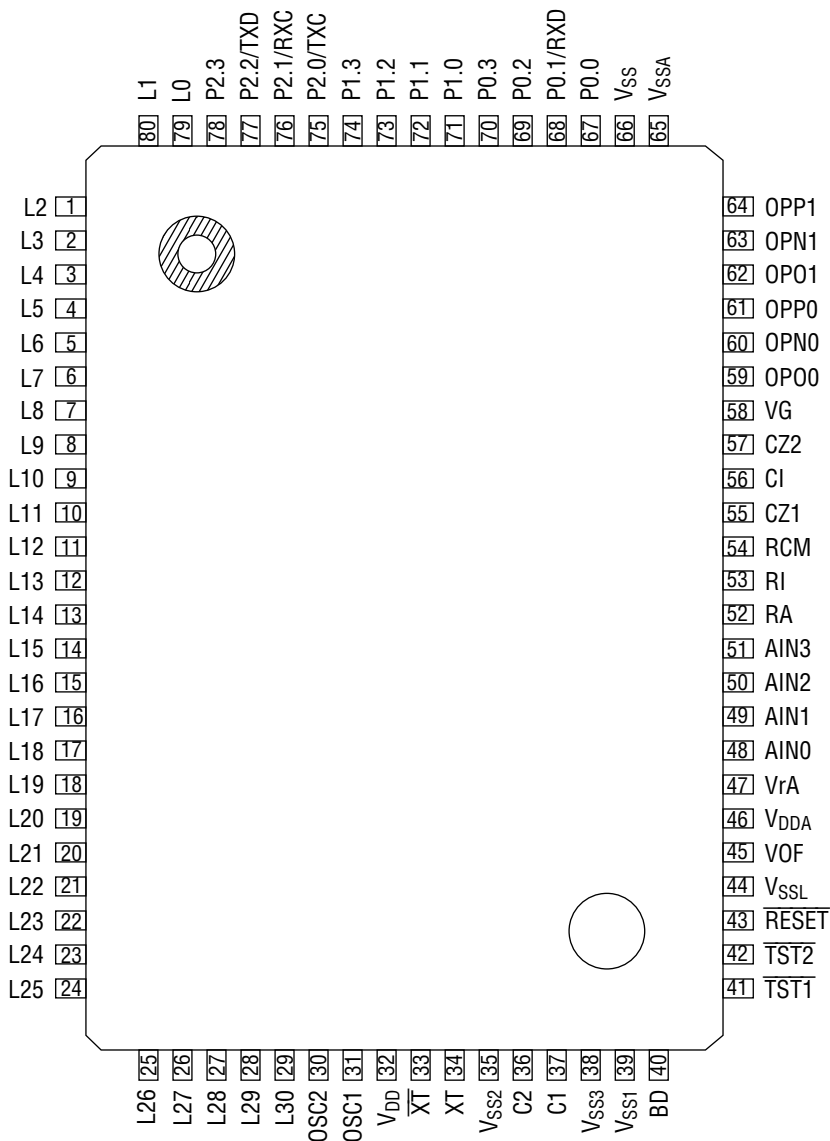
xxx indicates a code number.

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)

MSM64167E-xxxGA

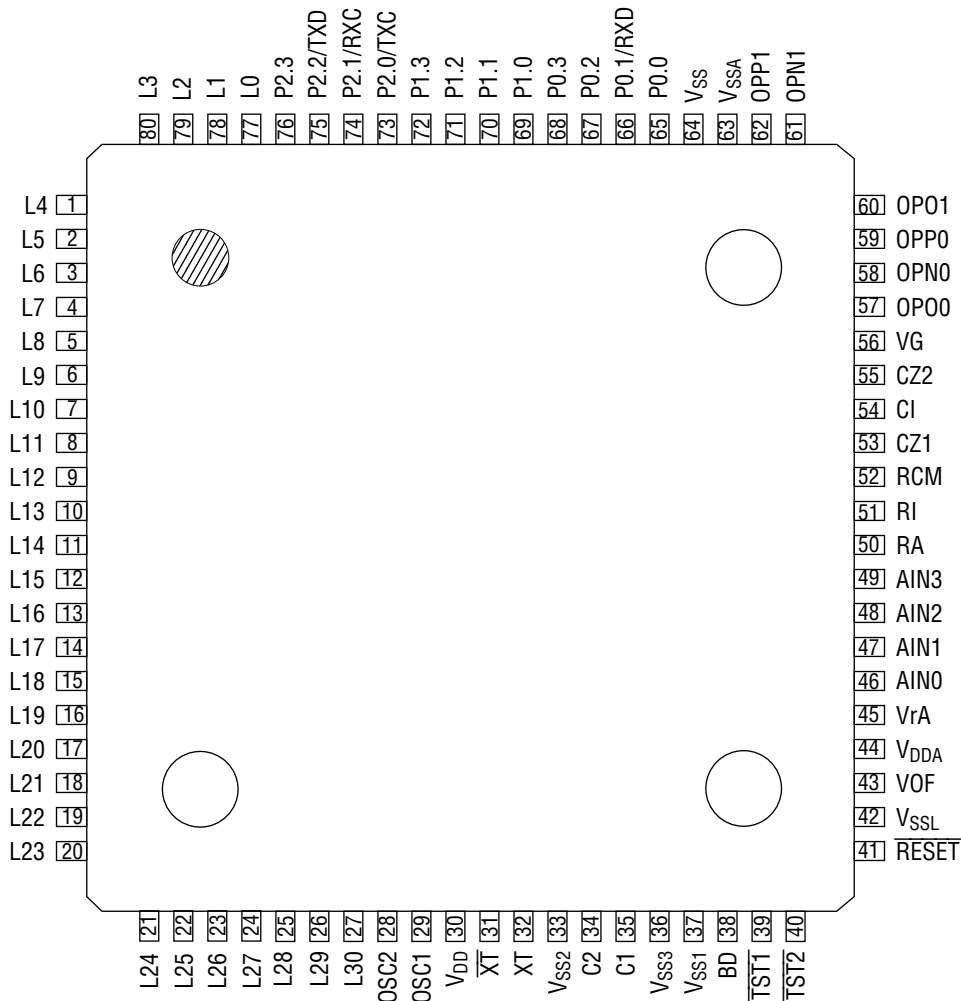


(QFP80-P-1420-0.80-BK)

80-Pin Plastic QFP

PIN CONFIGURATION (TOP VIEW) (continued)

MSM64167E-xxxTB

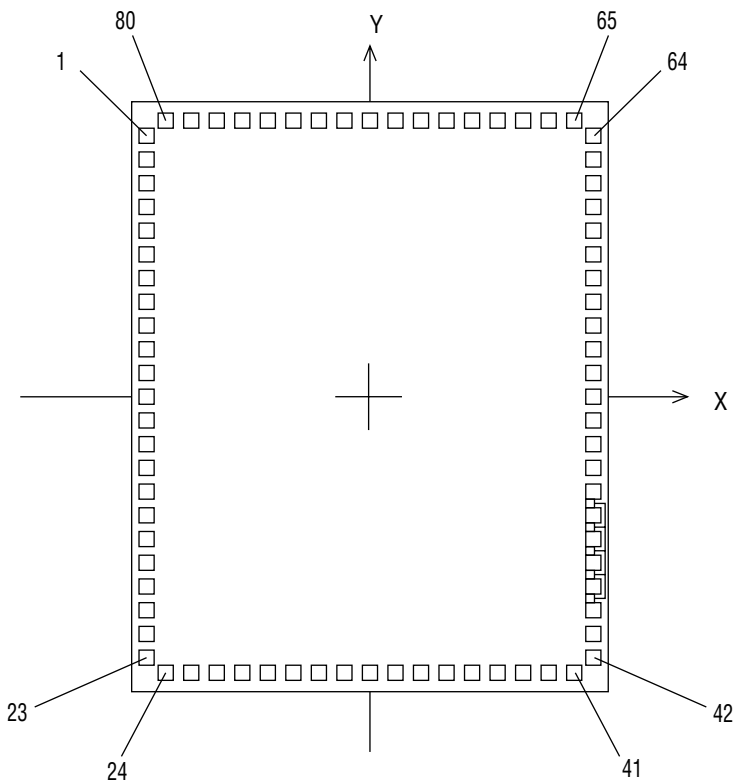


(TQFP80-P-1212-0.50-K)

80-Pin Plastic TQFP

PAD CONFIGURATION

Pad Layout



Chip Size	: 5.95 mm × 4.62 mm
Chip Thickness	: 350 μm (typ.)
Coordinate Origin	: Chip center
Pad Hole Size	: 110 μm × 110 μm
Pad Size	: 130 μm × 130 μm
Minimum Pad Pitch	: 180 μm

Note: The chip substrate voltage is V_{DD} .

Pad Coordinates

Pad No.	Pad Name	X (μm)	Y (μm)	Pad No.	Pad Name	X (μm)	Y (μm)
1	L2/P3.2	-2593	-2155	41	$\overline{\text{TST1}}$	2766	1946
2	L3/P3.3	-2304	-2155	42	$\overline{\text{TST2}}$	2660	2155
3	L4/P4.0	-1842	-2155	43	$\overline{\text{RESET}}$	2394	2155
4	L5/P4.1	-1626	-2155	44	V _{SSL}	2211	2155
5	L6/P4.2	-1430	-2155	45	VOF	1899	2113
6	L7/P4.3	-1234	-2155	46	V _{DDA}	1598	2113
7	L8	-1038	-2155	47	V _{rA}	1294	2113
8	L9	-856	-2155	48	AIN0	991	2113
9	L10	-664	-2155	49	AIN1	688	2155
10	L11	-468	-2155	50	AIN2	506	2155
11	L12	-272	-2155	51	AIN3	324	2155
12	L13	-76	-2155	52	RA	142	2155
13	L14	143	-2155	53	RI	-40	2155
14	L15	367	-2155	54	RCM	-222	2155
15	L16	591	-2155	55	CZ1	-402	2155
16	L17	874	-2155	56	CI	-586	2155
17	L18	1056	-2155	57	CZ2	-768	2155
18	L19	1280	-2155	58	VG	-1016	2155
19	L20	1504	-2155	59	OP00	-1246	2155
20	L21	1728	-2155	60	OPN0	-1498	2155
21	L22	1952	-2155	61	OPP0	-1749	2155
22	L23	2176	-2155	62	OP01	-2001	2155
23	L24	2624	-2155	63	OPN1	-2253	2155
24	L25	2766	-1862	64	OPP1	-2625	2155
25	L26	2766	-1638	65	V _{SSA}	-2766	1960
26	L27	2766	-1414	66	V _{SS}	-2766	1708
27	L28	2766	-1190	67	P0.0	-2766	1456
28	L29	2766	-966	68	P0.1	-2766	1204
29	L30	2766	-742	69	P0.2	-2766	952
30	OSC2	2766	-518	70	P0.3	-2766	700
31	OSC1	2766	-336	71	P1.0	-2766	448
32	V _{DD}	2766	-132	72	P1.1	-2766	196
33	$\overline{\text{XT}}$	2766	154	73	P1.2	-2766	-56
34	XT	2766	378	74	P1.3	-2766	-308
35	V _{SS2}	2766	602	75	P2.0	-2766	-560
36	C2	2766	826	76	P2.1	-2766	-812
37	C1	2766	1050	77	P2.2	-2766	-1064
38	V _{SS3}	2766	1232	78	P2.3	-2766	-1316
39	V _{SS1}	2766	1456	79	L0/P3.0	-2766	-1568
40	BD	2766	1694	80	L1/P3.1	-2766	-1834

PIN DESCRIPTIONS

Basic Functions

Function	Symbol	Pin		Pad	Type	Description
		GA	TB			
Power Supply	V _{DD}	32	30	32	—	0 V power supply.
	V _{SS1}	39	37	39	—	Bias output for driving LCD (–1.5 V).
	V _{SS2}	35	33	35	—	Negative power supply
	V _{SS3}	38	36	38	—	Bias output for driving LCD (–3.0 V). Bias output for driving LCD (–4.5 V).
	V _{SS}	66	64	66	—	Negative power supply for I/O port interface.
	C1	37	35	37	—	Pins for connecting a capacitor for generating LCD driving bias
	C2	36	34	36	—	
	V _{SSL}	44	42	44	—	Negative power supply for internal logic (An internally generated constant voltage is present at this pin.)
	V _{SSA}	65	63	65	—	Negative power supply for A/D converter: Externally connects to V _{SS2} .
V _{DDA}	46	44	46	—	0 V power supply for A/D converter: Externally connects to V _{DD} .	
Oscillation	XT	34	32	34	I	Low-speed clock oscillation input and output pins: Connect to a crystal (32.768 kHz).
	\overline{XT}	33	31	33	0	
	OSC1	31	29	31	I	High-speed clock oscillation input and output pins: Connect to an oscillation resistor (R _{OS}).
	OSC2	30	28	30	0	
Test	$\overline{TST1}$	41	39	41	I	Input pins for testing.
	$\overline{TST2}$	42	40	42	I	These pins are internally pulled up to V _{DD} .
Reset	\overline{RESET}	43	41	43	I	System reset input pin. Setting this pin to "L" level puts this device into a reset state. Then, setting this pin to "H" level starts executing an instruction from address 000H. This pin is internally pulled up to V _{DD} .

Basic Functions (continued)

Function	Symbol	Pin		Pad	Type	Description	
		GA	TB				
Ports	P0.0	67	65	67	I/O	4-bit input-output port (P0):	
	P0.1	68	66	68	I/O	Following can be specified for each bit by the port 0 control registers 0 to 3 (P00CON to P03CON): (1) input or output, (2) pull-up/pull-down resistor input or high impedance input, and (3) NMOS open drain output or CMOS output.	
	P0.2	69	67	69	I/O		
	P0.3	70	68	70	I/O		
	Ports	P1.0	71	69	71	I/O	4-bit input-output port (P1):
		P1.1	72	70	72	I/O	Following can be specified for each bit by the port 1 control registers 0 to 3 (P10CON to P13CON): (1) input or output, (2) pull-up/pull-down resistor input or high impedance input, and (3) NMOS open drain output or CMOS output.
		P1.2	73	71	73	I/O	
		P1.3	74	72	74	I/O	
	Ports	P2.0	75	73	75	I/O	4-bit input-output port (P2):
		P2.1	76	74	76	I/O	Following can be specified for each bit by the port 2 control registers 0 to 3 (P20CON to P23CON): (1) input or output, (2) pull-up/pull-down resistor input or high impedance input, and (3) NMOS open drain output or CMOS output.
		P2.2	77	75	77	I/O	
		P2.3	78	76	78	I/O	
Buzzer	BD	40	38	40	0	Output pin for the buzzer driver	
A/D Converter	AIN0	48	46	48	I/O	Analog voltage input pins. Each of these pins can be switched to provide a constant current output by AD control register 0 (ADCON0).	
	AIN1	49	47	49	I/O		
	AIN2	50	48	50	I/O		
	AIN3	51	49	51	I/O		
	RA	52	50	52	—	Current-adjusting resistor connection pin.	
	RI	53	51	53	—	Pin for connecting resistor for integration.	
	RCM	54	52	54	—	Common connection pin for resistor for integration, capacitor 1 for offset compensation, and capacitor for integration.	
	CZ1	55	53	55	—	Pin for connecting capacitor 1 for offset compensation.	
	CI	56	54	56	—	Pin for connecting capacitor for integration.	
	CZ2	57	55	57	—	Pins for connecting capacitor 2 for offset compensation.	
	VG	58	56	58	—		
	VrA	47	45	47	—	Reference voltage for A/D conversion (internally generated constant voltage).	
	VOF	45	43	45	I	Pin for connecting resistor for voltage amplification circuit offset adjustment.	
	OPP0	61	59	61	I	Analog micro-voltage input pins.	
	OPP1	64	62	64	I		
	OPN0	60	58	60	I	Pins for connecting resistor for voltage amplification factor adjustment.	
OPN1	63	61	63	I			
OPO0	59	57	59	0			
OPO1	62	60	62	0			

Basic Functions (continued)

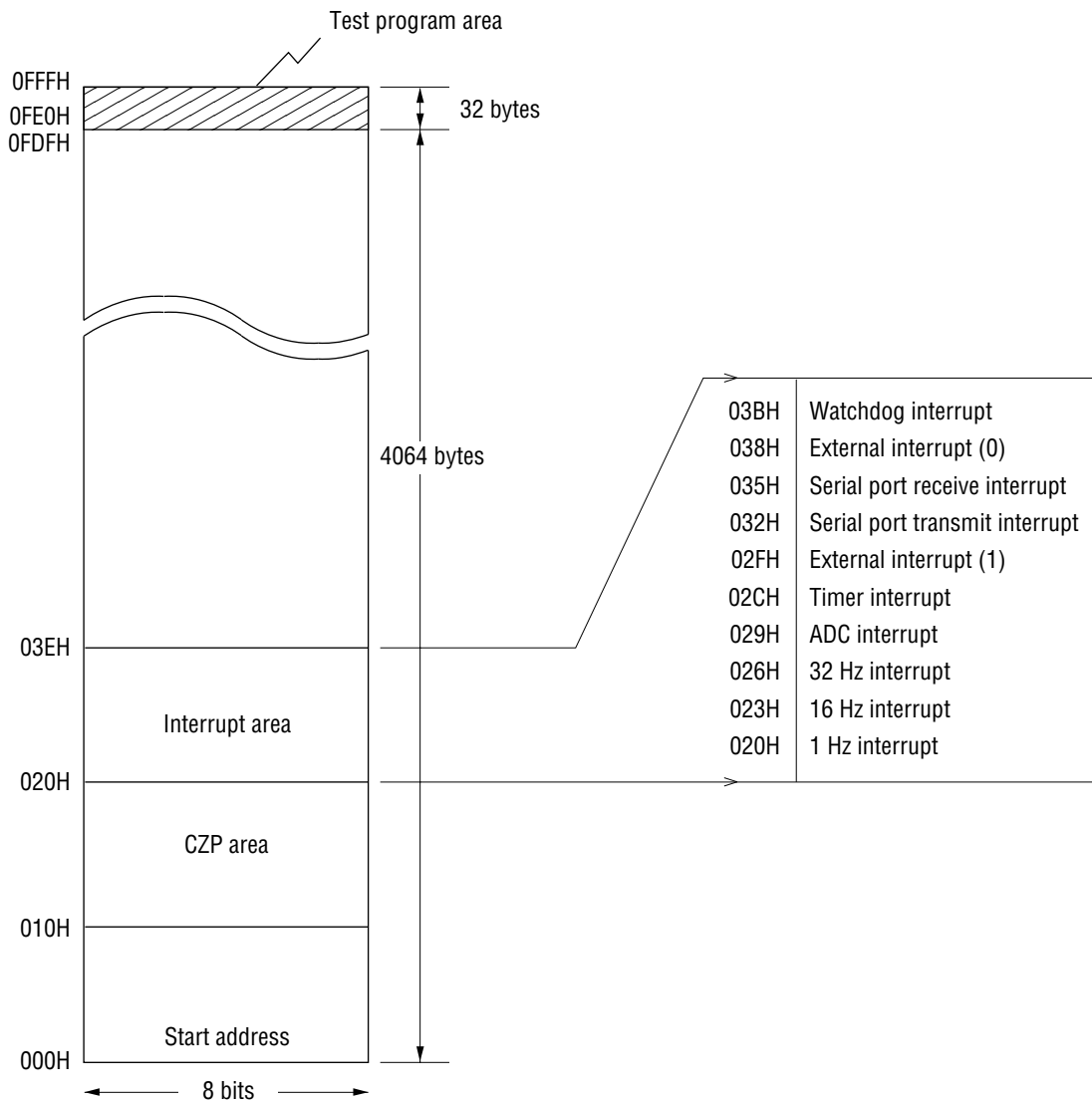
Function	Symbol	Pin		Pad	Type	Description
		GA	TB			
LCD Drivers	L0/P3.0	79	77	79	0	LCD segment and common signals output pins.
	L1/P3.1	80	78	80	0	Functions as output ports by mask option.
	L2/P3.2	1	79	1	0	
	L3/P3.3	2	80	2	0	
	L4/P4.0	3	1	3	0	
	L5/P4.1	4	2	4	0	
	L6/P4.2	5	3	5	0	
	L7/P4.3	6	4	6	0	
	L8	7	5	7	0	LCD segment and common signals output pins.
	L9	8	6	8	0	
	L10	9	7	9	0	
	L11	10	8	10	0	
	L12	11	9	11	0	
	L13	12	10	12	0	
	L14	13	11	13	0	
	L15	14	12	14	0	
	L16	15	13	15	0	
	L17	16	14	16	0	
	L18	17	15	17	0	
	L19	18	16	18	0	
	L20	19	17	19	0	
	L21	20	18	20	0	
	L22	21	19	21	0	
	L23	22	20	22	0	
	L24	23	21	23	0	
	L25	24	22	24	0	
	L26	25	23	25	0	
	L27	26	24	26	0	
	L28	27	25	27	0	
	L29	28	26	28	0	
L30	29	27	29	0		

Secondary Functions

Function	Symbol	Pin		Pad	Type	Description
		GA	TB			
External Interrupts	P0.0	67	65	67	I	Level-triggered external interrupt input pins. The change of input signal level causes an interrupt to occur.
	P0.1	68	66	68		
	P0.2	69	67	69		
	P0.3	70	68	70		
	P1.0	71	69	71		
	P1.1	72	70	72		
	P1.2	73	71	73		
	P1.3	74	72	74		
	P2.0	75	73	75		
	P2.1	76	74	76		
	P2.2	77	75	77		
	P2.3	78	76	78		
Serial Port	P0.1	68	66	68	I	Receive data input pin (RXD) of serial port.
	P2.0	75	73	75	I/O	Transmit clock input-output pin (TXC) of serial port.
	P2.1	76	74	76	I/O	Receive clock output pin (RXC) of serial port.
	P2.2	77	75	77	O	Transmit data output pin (TXD) of serial port.
Timer	P0.0	67	65	67	I	Capture trigger input pin of timer.
	P0.2	69	67	69	I	External clock input pin (TMC) of timer.
	P2.3	78	76	78	O	Timer overflow flag output pin (TMO) of timer.

MEMORY MAPS

Program Memory



Program Memory Map

Address 000H is the instruction execution start address by the system reset.

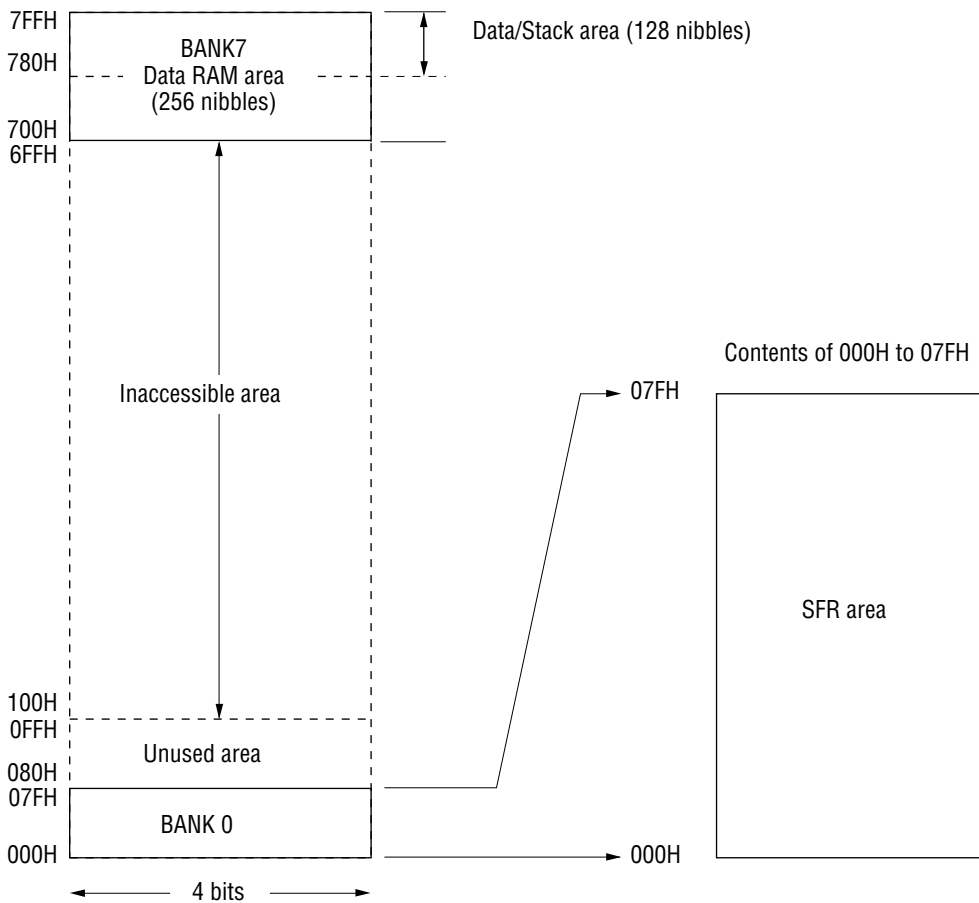
The CZP area from address 010H to address 01FH is the start address for the CZP subroutine of 1-byte call instruction.

The start address of interrupt subroutine is assigned to the interrupt address from address 020H to 03DH.

The user area has 4064 bytes of address 000H to address 0FDFH. No program can be stored in the test program area.

Data Memory

The data memory area consists of 8 banks and each bank has 256 nibbles (256 × 4 bits). The data RAM is assigned to BANK 7 and peripheral ports are assigned to BANK 0.



Data Memory Map

Half the data RAM area (128 nibbles) is shared by the stack area. The stack is a memory starting from address 7FFH toward the low-order addresses where 4 nibbles are used by Subroutine Call Instruction and 8 nibbles are used by an interrupt.

The addresses 080H to 0FFH of BANK 0 are not assigned as the data memory, so access to these addresses has no effect. Moreover, it is impossible to access BANK 1 to BANK 6.

ABSOLUTE MAXIMUM RATINGS

(V_{DD} = V_{DDA} = 0 V)

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage 1	V _{SS1}	T _a = 25°C	-2.0 to +0.3	V
Power Supply Voltage 2	V _{SS2}	T _a = 25°C	-4.0 to +0.3	V
Power Supply Voltage 3	V _{SS3}	T _a = 25°C	-5.5 to +0.3	V
Power Supply Voltage 4	V _{SSL}	T _a = 25°C	-4.0 to +0.3	V
Power Supply Voltage 5	V _{SS}	T _a = 25°C	-5.5 to +0.3	V
Power Supply Voltage 6	V _{SSA}	T _a = 25°C	-4.0 to +0.3	V
Input Voltage 1	V _{IN1}	V _{SS2} Input, T _a = 25°C	V _{SS2} - 0.3 to +0.3	V
Input Voltage 2	V _{IN2}	V _{SS} Input, T _a = 25°C	V _{SS} - 0.3 to +0.3	V
Input Voltage 3	V _{IN3}	V _{SS1} Input, T _a = 25°C	V _{SS1} - 0.3 to +0.3	V
Input Voltage 4	V _{IN4}	V _{SSA} Input, T _a = 25°C	V _{SSA} - 0.3 to +0.3	V
Output Voltage 1	V _{OUT1}	V _{SS2} Output, T _a = 25°C	V _{SS2} - 0.3 to +0.3	V
Output Voltage 2	V _{OUT2}	V _{SS3} Output, T _a = 25°C	V _{SS3} - 0.3 to +0.3	V
Output Voltage 3	V _{OUT3}	V _{SS} Output, T _a = 25°C	V _{SS} - 0.3 to +0.3	V
Output Voltage 4	V _{OUT4}	V _{SS1} Output, T _a = 25°C	V _{SS1} - 0.3 to +0.3	V
Storage Temperature	T _{STG}	—	-55 to +125	°C

RECOMMENDED OPERATING CONDITIONS

(V_{DD} = V_{DDA} = 0 V)

Parameter	Symbol	Condition	Range	Unit
Operating Temperature	T _{OP}	—	-40 to +85	°C
Operating Voltage	V _{SS2} V _{SSA}	V _{SS2} = V _{SSA}	-3.6 to -2.6	V
	V _{SS}	—	-5.25 to (0.8•V _{SS2} , -2.6 max.)*	V
External 700 kHz RC Oscillator Resistance	R _{OS}	—	90 to 300	kΩ
Crystal Oscillation Frequency	f _{XT}	—	30 to 66	kHz

* Indicates that the value of V_{SS} is 80% of V_{SS2} and should not exceed -2.6 V.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = V_{DDA} = 0 V, V_{SS2} = V_{SS} = -3.0 V, T_a = -40 to +85°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
V _{SS1} Voltage	V _{SS1}	C _a , C _b , C ₁₂ = 0.1 μF +100% -50%	-1.7	-1.5	-1.3	V	1
V _{SS3} Voltage	V _{SS3}	C _a , C _b , C ₁₂ = 0.1 μF +100% -50%	-4.7	-4.5	-4.3	V	
V _{SSL} Voltage	V _{SSL}	—	-2.1	-1.5	-0.6	V	
Crystal Oscillation Start Voltage	V _{STA}	Oscillation start time: within 5 seconds	—	—	-2.6	V	
Crystal Oscillation Hold Voltage	V _{HOLD}	—	—	—	-2.6	V	
Crystal Oscillation Stop Detection Time	T _{STOP}	—	0.1	—	1000	ms	
Internal Crystal Oscillator Capacitance	C _G	—	10	15	20	pF	
External Crystal Oscillator Capacitance	C _{GEX}	When external C _G used	10	—	30	pF	
Internal Crystal Oscillator Capacitance	C _D	—	10	15	20	pF	
Internal 700k RC Oscillator Capacitance	C _{OS}	—	8.0	12	16	pF	
700k RC Oscillation Frequency	f _{OSC}	External resistor R _{OS} = 100 kΩ V _{SS2} = -2.6 to -3.6 V	520	700	910	kHz	
POR Generation Voltage	V _{POR1}	When V _{SS2} is between V _{POR1} and -3.0 V	-0.7	—	0	V	
POR Non-generation Voltage	V _{POR2}	No POR when V _{SS2} is between V _{POR2} and -3.0 V	-3.0	—	-2.0	V	

Notes: 1. "POR" denotes Power On Reset.

2. "T_{STOP}" indicates that if the crystal oscillator stops over the value of T_{STOP}, the system reset occurs.

DC Characteristics (continued)

(V_{DD} = V_{DDA} = 0 V, V_{SS2} = V_{SS} = -3.0 V, T_a = -40 to +85°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Supply Current 1	I _{DD1}	CPU in halt state (700k RC oscillation halt)	—	1.2	4.5	μA	1
Supply Current 2	I _{DD2}	CPU in operating state (700k RC oscillation halt)	—	5.0	15	μA	
Supply Current 3	I _{DD3}	CPU in operating state (700k RC oscillation in operation)	—	400	800	μA	
Supply Current 4	I _{DD4}	CPU in halt state (700k RC oscillation halt),	—	200	300	μA	
		A/D converter in operating state	—	400	600	μA	

DC Characteristics (continued)

($V_{DD} = V_{DDA} = 0\text{ V}$, $V_{SS1} = V_{SSL} = -1.5\text{ V}$, $V_{SS2} = V_{SS} = V_{SSA} = -3.0\text{ V}$, $V_{SS3} = -4.5\text{ V}$,
 $T_a = -40\text{ to }+85^\circ\text{C}$ unless otherwise specified)

Parameter (Pin Name)	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Output Current 1 (P0.0 to P0.3) (P1.1 to P1.3) (P2.0 to P2.3)	I_{OH1}	$V_{OH1} = -0.5\text{ V}$	-6.0	-2.0	-0.7	mA	2
	I_{OL1}	$V_{OL1} = V_{SS} + 0.5\text{ V}$	0.7	2.0	6.0	mA	
	I_{OH1S}	$V_{SS} = -5\text{ V}$, $V_{OH1S} = -0.5\text{ V}$	-9.0	-3.0	-1.0	mA	
	I_{OL1S}	$V_{SS} = -5\text{ V}$, $V_{OL1S} = V_{SS} + 0.5\text{ V}$	1.0	3.0	9.0	mA	
Output Current 2 (BD)	I_{OH2}	$V_{OH2} = -0.7\text{ V}$	-6.0	-2.0	-0.7	mA	
	I_{OL2}	$V_{OL2} = V_{SS2} + 0.7\text{ V}$	0.7	2.0	6.0	mA	
Output Current 3 (RI, CI, OPO0, OPO1)	I_{OH3}	$V_{OH3} = -0.5\text{ V}$	-3.0	-1.2	-0.2	mA	
	I_{OL3}	$V_{OL3} = V_{SS} + 0.5\text{ V}$	15	3.0	100	μA	
Output Current 4 (When L0 to L7 are configured as output ports)	I_{OH4}	$V_{OH4} = -0.5\text{ V}$	-1.5	-0.6	-0.15	mA	
	I_{OL4}	$V_{OL4} = V_{SS} + 0.5\text{ V}$	0.15	0.6	1.5	mA	
	I_{OH4S}	$V_{SS} = -5\text{ V}$, $V_{OH4S} = -0.5\text{ V}$	-2.0	-0.7	-0.2	mA	
	I_{OL4S}	$V_{SS} = -5\text{ V}$, $V_{OL4S} = V_{SS} + 0.5\text{ V}$	0.2	0.7	2.0	mA	
Output Current 5 (OSC2)	I_{OH5}	$V_{OH5} = -0.5\text{ V}$	-6.0	-2.0	-0.7	mA	
	I_{OL5}	$V_{OL5} = V_{SS2} + 0.5\text{ V}$	0.7	2.0	6.0	mA	
Output Current 6 (L0 to L30)	I_{OH6}	$V_{OH6} = -0.2\text{ V}$ (V_{DD} level)	—	—	-4.0	μA	
	I_{OMH6}	$V_{OMH6} = V_{SS1} + 0.2\text{ V}$ (V_{SS1} level)	4.0	—	—	μA	
	I_{OMH6S}	$V_{OMH6S} = V_{SS1} - 0.2\text{ V}$ (V_{SS1} level)	—	—	-4.0	μA	
	I_{OML6}	$V_{OML6} = V_{SS2} + 0.2\text{ V}$ (V_{SS2} level)	4.0	—	—	μA	
	I_{OML6S}	$V_{OML6S} = V_{SS2} - 0.2\text{ V}$ (V_{SS2} level)	—	—	-4.0	μA	
	I_{OL6}	$V_{OL6} = V_{SS3} + 0.2\text{ V}$ (V_{SS3} level)	4.0	—	—	μA	
Output Leakage Current (P0.0 to P0.3) (P1.0 to P1.3) (P2.0 to P2.3)	I_{OOH}	$V_{OH} = V_{DD}$	—	—	0.3	μA	
	I_{OOL}	$V_{OL} = V_{SS2}$	-0.3	—	—	μA	

DC Characteristics (continued)

($V_{DD} = V_{DDA} = 0\text{ V}$, $V_{SS1} = V_{SSL} = -1.5\text{ V}$, $V_{SS2} = V_{SS} = V_{SSA} = -3.0\text{ V}$, $V_{SS3} = -4.5\text{ V}$,
 $T_a = -40\text{ to }+85^\circ\text{C}$ unless otherwise specified)

Parameter (Pin Name)	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Input Current 1 (P0.0 to P0.3) (P1.0 to P1.3) (P2.0 to P2.3)	I_{IH1}	$V_{IH1} = V_{DD}$ (when pulled down)	30	90	300	μA	3
	I_{IL1}	$V_{IL1} = V_{SS}$ (when pulled up)	-300	-90	-30	μA	
	I_{IH1S}	$V_{IH1} = V_{DD}$, $V_{SS} = -5\text{ V}$ (when pulled down)	80	250	800	μA	
	I_{IL1S}	$V_{IL1} = V_{SS} = -5\text{ V}$ (when pulled up)	-800	-250	-80	μA	
	I_{IH1Z}	$V_{IH1} = V_{DD}$ (in a high impedance state)	0	—	1.0	μA	
	I_{IL1Z}	$V_{IL1} = V_{SSA}$ (in a high impedance state)	-1.0	—	0	μA	
Input Current 2 (OPPO, OPP1, OPNO, OPN1, VOF)	I_{IL2}	$V_{IL2} = V_{SSA}$ (when pulled up)	-300	-90	-30	μA	
	I_{IH2Z}	$V_{IH2} = V_{DD}$ (in a high impedance state)	0	—	1.0	μA	
	I_{IL2Z}	$V_{IL2} = V_{SSA}$ (in a high impedance state)	-1.0	—	0	μA	
Input Current 3 (VrA)	I_{IL3}	$V_{IL3} = V_{SSA}$ (ENADC = 0)	-375	-250	-125	μA	
	I_{IH3}	$V_{IH3} = V_{rA} + 30\text{ mV}$ (ENADC = 1)	0.6	1.0	—	mA	
Input Current 4 (OSC1)	I_{IL4}	$V_{IL4} = V_{SS2}$ (when pulled up)	-300	-110	-10	μA	
	I_{IH4Z}	$V_{IH4} = V_{DD}$ (in a high impedance state)	0	—	1.0	μA	
	I_{IL4Z}	$V_{IL4} = V_{SS2}$ (in a high impedance state)	-1.0	—	0	μA	
Input Current 5 (RESET, TST1, TST2)	I_{IH5}	$V_{IH5} = V_{DD}$	0	—	1.0	μA	
	I_{IL5}	$V_{IL5} = V_{SS2}$	-3.0	-1.5	-0.75	mA	
Input Current 6 (RCM, CZ1, CZ2, AIN0 to AIN3, RA)	I_{IH6Z}	$V_{IH6} = V_{DD}$ (in a high impedance state)	0	—	1.0	μA	
	I_{IL6Z}	$V_{IL6} = V_{SSA}$ (in a high impedance state)	-1.0	—	0	μA	
Input Voltage 1 (P0.0 to P0.3) (P1.0 to P1.3) (P2.0 to P2.3) (OSC1)	V_{IH1}	—	-0.6	—	0	V	4
	V_{IL1}	—	-3.0	—	-2.4	V	
	V_{IH1S}	$V_{SS} = -5\text{ V}$	-1.0	—	0	V	
	V_{IL1S}	$V_{SS} = -5\text{ V}$	-5.0	—	-4.0	V	
Input Voltage 2 (OSC1, RESET, TST1, TST2)	V_{IH2}	—	-0.6	—	0	V	
	V_{IL2}	—	-3.0	—	-2.4	V	

DC Characteristics (continued)

($V_{DD} = V_{DDA} = 0\text{ V}$, $V_{SS1} = V_{SSL} = -1.5\text{ V}$, $V_{SS2} = V_{SS} = V_{SSA} = -3.0\text{ V}$, $V_{SS3} = -4.5\text{ V}$,
 $T_a = -40\text{ to }+85^\circ\text{C}$ unless otherwise specified)

Parameter (Pin Name)	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Hysteresis Width (P0.0 to P0.3) (P1.0 to P1.3) (P2.0 to P2.3)	ΔV_{T1}	—	0.2	0.5	1.0	V	4
	ΔV_{T1S}	$V_{SS} = -5\text{ V}$	0.25	1.0	1.5	V	
Hysteresis Width (RESET, TST1, TST2)	ΔV_{T2}	—	0.2	0.5	1.0	V	
Input Pin Capacitance (P0.0 to P0.3) (P1.0 to P1.3) (P2.0 to P2.3)	C_{IN}	—	—	—	5.0	pF	1

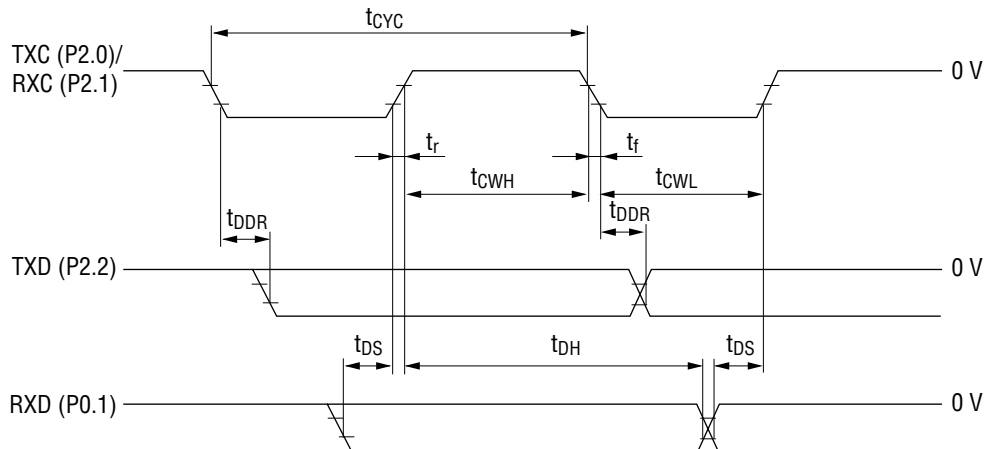
AC Characteristics (Serial Interface, Serial Port)(V_{DD} = 0V, V_{SS2} = -3.0 V, V_{SS} = -5.0 V, Ta = -40 to +85°C unless otherwise specified)

(1) Synchronous Communication

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
TXC/RXC Input Fall Time	t _f	—	—	—	1.0	μs
TXC/RXC Input Rise Time	t _r	—	—	—	1.0	μs
TXC/RXC Input "L" Level Pulse Width	t _{cWL}	—	0.8	—	—	μs
TXC/RXC Input "H" Level Pulse Width	t _{cWH}	—	0.8	—	—	μs
TXC/RXC Input Cycle Time	t _{cYC}	—	2.0	—	—	μs
TXC/RXC Output Cycle Time	t _{cYC1(0)}	CPU operating at 32.768 kHz	—	30.5	—	μs
TXD Output Delay Time	t _{DDR}	Output load capacitance 10 pF	—	—	0.4	μs
RXD Input Setup Time	t _{DS}	—	0.5	—	—	μs
RXD Input Hold Time	t _{DH}	—	0.8	—	—	μs

Synchronous communication timing

("H" level = -1.0 V, "L" level = -4.0 V)



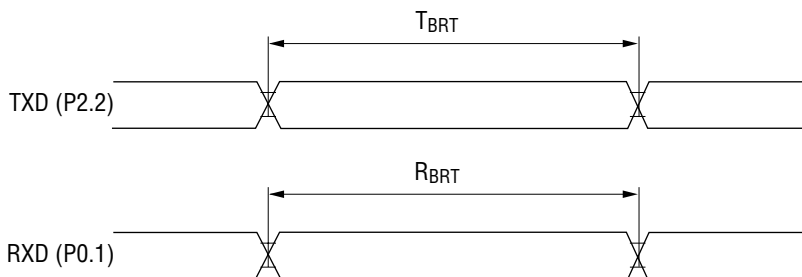
(2) UART Communication

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Transmit Baud Rate	T_{BRT}	$T_{BRT} = 1/f_{BRT}$ $T_{CR} = 1/f_{OSC}$	$T_{BRT} - T_{CR}$	T_{BRT}	$T_{BRT} + T_{CR}$	s
Receive Baud Rate	R_{BRT}	$R_{BRT} = 1/f_{BRT}$	$R_{BRT} \times 0.97$	R_{BRT}	$R_{BRT} \times 1.03$	s

f_{BRT} : Baud rates (1200, 2400, 4800, 9600 bps)

UART communication timing

("H" level = -1.0 V, "L" level = -4.0 V)



A/D Converter Characteristics

($V_{DD} = V_{DDA} = 0\text{ V}$, $V_{SS2} = V_{SS} = V_{SSA} = -3\text{ V}$, $T_a = -40\text{ to }+85^\circ\text{C}$, $V_{rA} = -1.2\text{ V}$, at execution of 12-bit A/D conversion, unless otherwise specified)

Parameter (Pin Name)	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Analog Input Voltage Range (AIN0 to AIN3)	V_{AIN}	—	-1.2	—	-0.4	V	5
Analog Input Voltage Range (OPP0, OPP1) (VOF)	V_{OPP}	—	-1.6	—	-0.4	V	
Resolution	—	—	—	—	$12 + S^*$	bits	
Linearity Error	—	—	-1	—	+1	LSB	
Zero Scale Error	—	—	-2	—	+2	LSB	
Full Scale Error	—	—	-16	—	+16	LSB	
VrA Voltage (VrA)	V_{rA}	$T_a = 25^\circ\text{C}$	-1300	-1200	-1100	mV	
VrA Temperature Coefficient	—	—	-8.0	—	+2.0	mV/°C	
VG Voltage (VG)	V_G	$T_a = 25^\circ\text{C}$	-867	-800	-733	mV	
RA Voltage (RA)	V_{RA}	$T_a = 25^\circ\text{C}$	-440	-400	-360	mV	

* "S" indicates a sign bit.

Voltage Amplification Circuit Characteristics

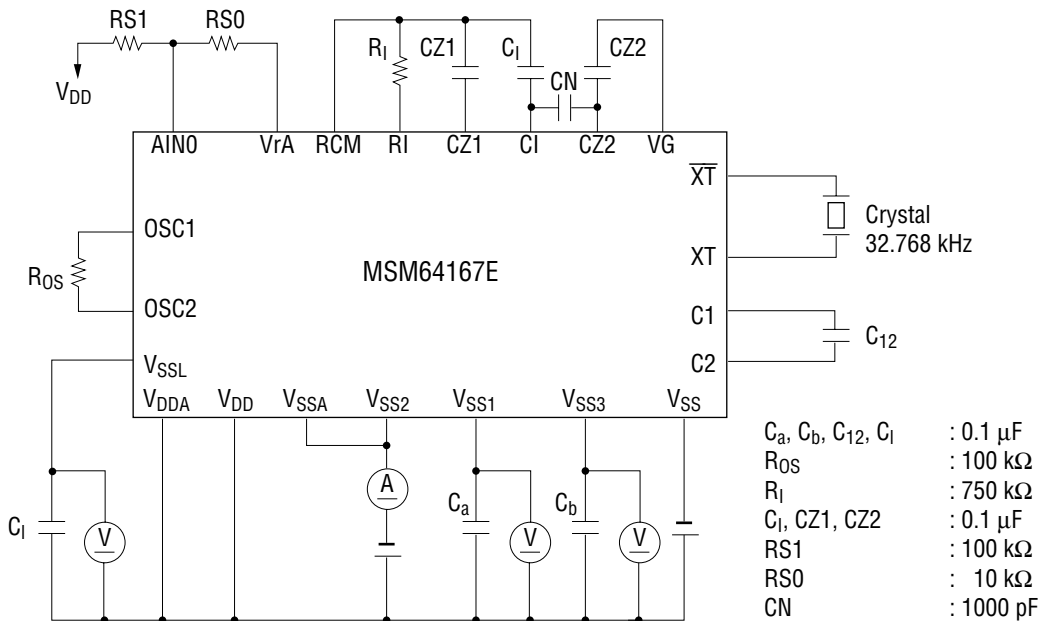
($V_{DD} = V_{DDA} = 0\text{ V}$, $V_{SS2} = V_{SS} = V_{SSA} = -3\text{ V}$, $T_a = -40\text{ to }+85^\circ\text{C}$ unless otherwise specified)

Parameter (Pin Name)	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Amplifier Gain Error (*1)	E_g (*2)	$V_{OPP1} - V_{OPP0} = 10\text{ mV}$, Gain = 40 $E_g = \frac{(V_{OP01} - V_{OP00}) / (V_{OPP1} - V_{OPP0})}{\text{Gain}} - 1$	-3.0	-1.5	0	%	5
Level Shift Error (*1)	EI	$EI = \frac{(V_{AIN3} - V_{VOF})}{(V_{OP01} - V_{OP00})} - 1$	-4	—	+4	%	
Amplifier Offset Voltage	V_{offA}	OPP0 = OPP1 = VOF = -0.8 V, OP00 = OPN0, OP01 = OPN1, $V_{offA} = V_{OP01} - V_{OP00}$	-20	—	+20	mV	
Level Shift Offset Voltage	V_{offL}	OP00 = OP01 = VOF = -0.8V, $V_{offL} = V_{AIN3} - V_{VOF}$	-30	—	+30	mV	

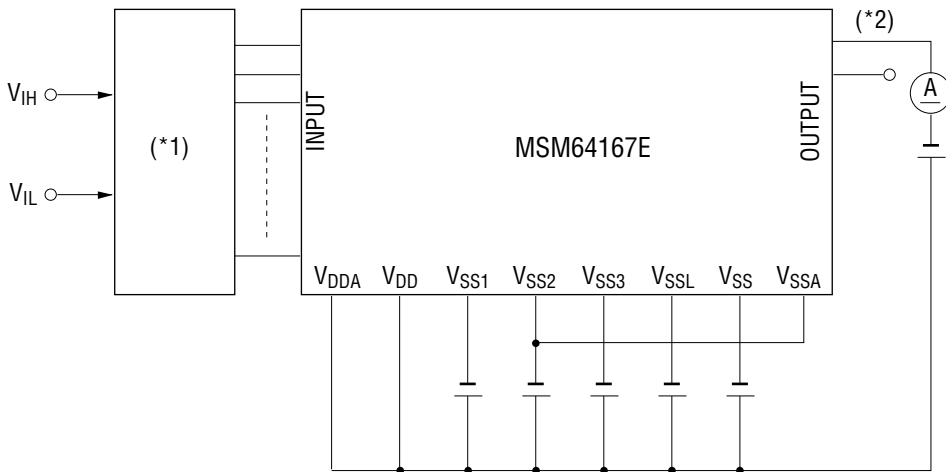
*1 Errors caused by offset voltage are excluded.

*2 Errors decrease in proportion to gain.

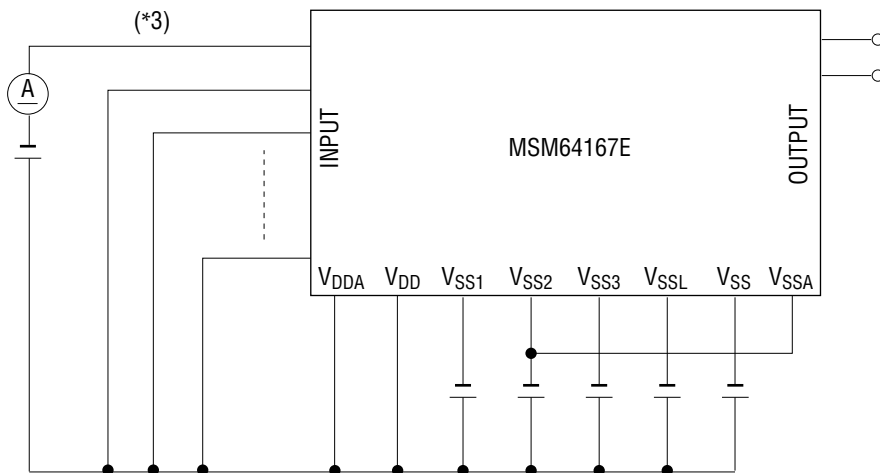
Measuring circuit 1



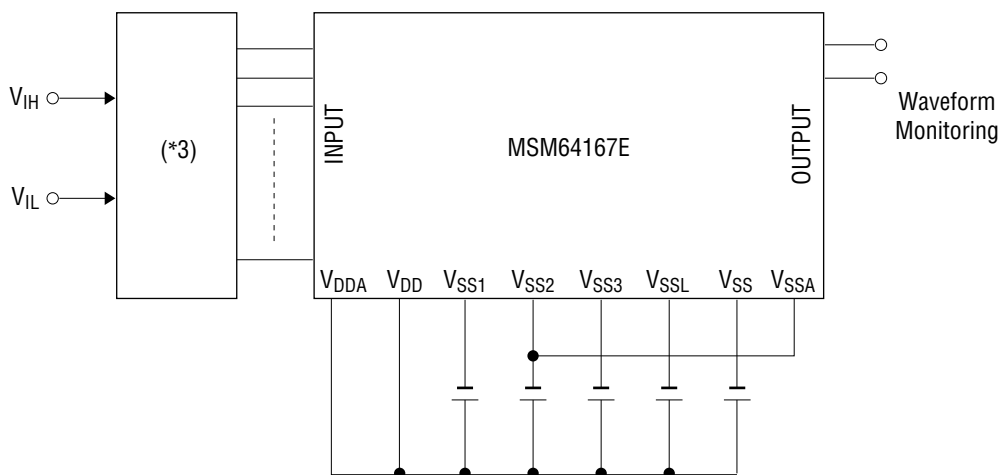
Measuring circuit 2



Measuring circuit 3

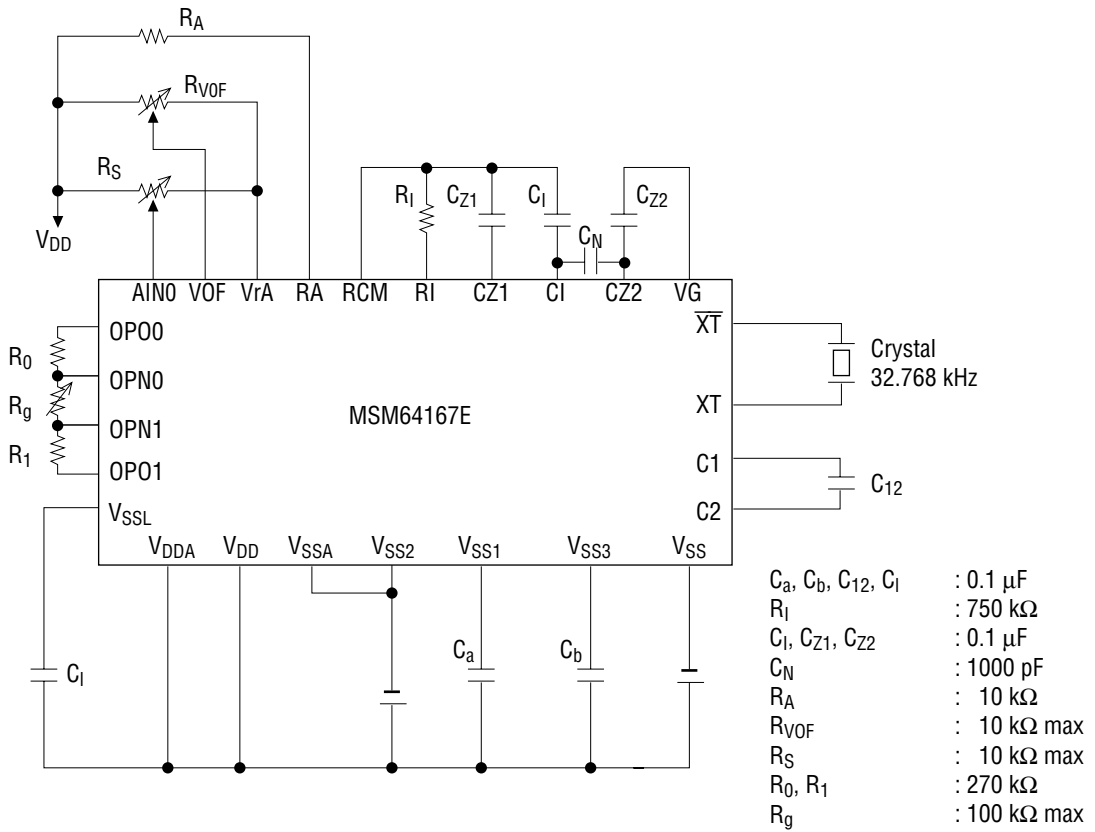


Measuring circuit 4



- *1 Input logic circuit to determine the specified measuring conditions.
- *2 Measured at the specified output pins.
- *3 Measured at the specified input pins.

Measuring circuit 5



FUNCTIONAL DESCRIPTION

CPU Peripheral Functions

• A/D converter (ADC)

The MSM64167E has a 4-channel input dual-slope type A/D converter. In dual-slope A/D conversion, the relationship between integral voltage and time is given by:

$$V_{in}/V_r = t_1/t_2$$

where,

t_1 = given time for which an analog input voltage is integrated

V_r = reference voltage

V_{in} = voltage resulted from charging for t_1

t_2 = time required to discharge the voltage, from V_r to V_{in}

From the above equation, V_{in} is found.

The range of V_{in} is -0.8 ± 0.4 V. The A/D converter resolution time is programmable. The A/D converter has a preamplifier for amplifying a microvoltage. It is suited to applications such as thermometers, pressure gauges, and hygrometers.

• LCD driver (LCD)

The MSM64167E has a built-in LCD driver for 31 outputs.

The LCD driver consists of 31×4 -bit display registers (DSPR0-30), the Display Control Register (DSPCON), a 31-output LCD driver circuit, and a bias generation circuit (BIAS).

There are three types of driving methods: 1/4 duty, 1/3 duty and 1/2 duty. Software selects the duty mode.

A mask option can select either a common driver or a segment driver for each LCD driver pin. A mask option can also specify assignment of each bit of the display register to each segment. All the display registers must be selected by a mask option.

L0 to L7 of the LCD driver can be configured to be output ports by a mask option.

The relationship between the duty, the bias method, and the maximum segment number follows:

1/4 duty 1/3 bias method ----- 108 segments

1/3 duty 1/3 bias method ----- 84 segments

1/2 duty 1/2 bias method ----- 58 segments

• Port (P0, P1, P2)

The MSM64167E has three input-output ports (P0, P1, P2) with 4 bits each. Each bit of the ports can be configured to be (1) an input or output, (2) pull-up/pull-down resistor input or high impedance input, and (3) NMOS open drain output or CMOS output. A change in the input level of each pin of P0 and P1 generates an external interrupt 0 request, and a change in the input level of each pin of P2 generates an external interrupt 1 request.

The serial port function and the timer function are assigned as the secondary functions.

• Buzzer driver (BD)

The MSM64167E has a built-in buzzer driver with 2 buzzer output frequencies and 4 buzzer output modes. Each buzzer output is selected by the Buzzer Control Register (BDCON) and the Buzzer Frequency Control Register (BFCON).

• Serial port (SIOP)

The MSM64167E has a serial port (SIOP). The serial port is a synchronous/asynchronous selectable serial communication port. The transmit section and the receive section are independent of each other, which allows simultaneous operation of transmission and receiving.

• Watchdog timer (WDT)

The MSM64167E has a built-in watchdog timer to detect CPU malfunction. The watchdog timer is composed of a 6-bit watchdog timer counter (WDTC) to count a 16 Hz output and a watchdog timer control register (WDTCON) to reset WDTC.

• Timer (TM)

The MSM64167E contains a 16-bit timer (TM). The timer has three operation modes: auto-reload mode, capture mode, and clock frequency measuring mode. It counts at 32.768 kHz or 700 kHz or by an external clock. The timer is used for pulse generation, time measurement, etc., and is also used as an A/D conversion counter at A/D conversion and as a baud rate generator at serial communication.

• Clock generation circuit (2CLK)

The MSM64167E has a clock generation circuit (2CLK) that generates clocks of two types: low-speed and high-speed. The circuit consists of a 32.768 kHz crystal oscillation circuit, a 700 kHz RC oscillation circuit, and a clock control section. This circuit generates the system clock (CLK), crystal oscillation clock (32.768 kHz), and RC oscillation clock (700 kHz).

The system clock is the basic operation clock of the CPU, and the crystal oscillation clock is the basic operation clock of the time-base counter and the buzzer driver. The crystal oscillation clock and RC oscillation clock are supplied to the timer to become a timer clock.

The system clock frequency is switched between 32.768 kHz (output of the crystal oscillation circuit) and 700 kHz (output of the RC oscillation circuit) based on the contents of the frequency control register (FCON).

Note: The oscillation frequency of the RC oscillation circuit varies depending on the value of external resistor (R_{OS}), operating voltage (V_{SS2}), and ambient temperature (T_a).

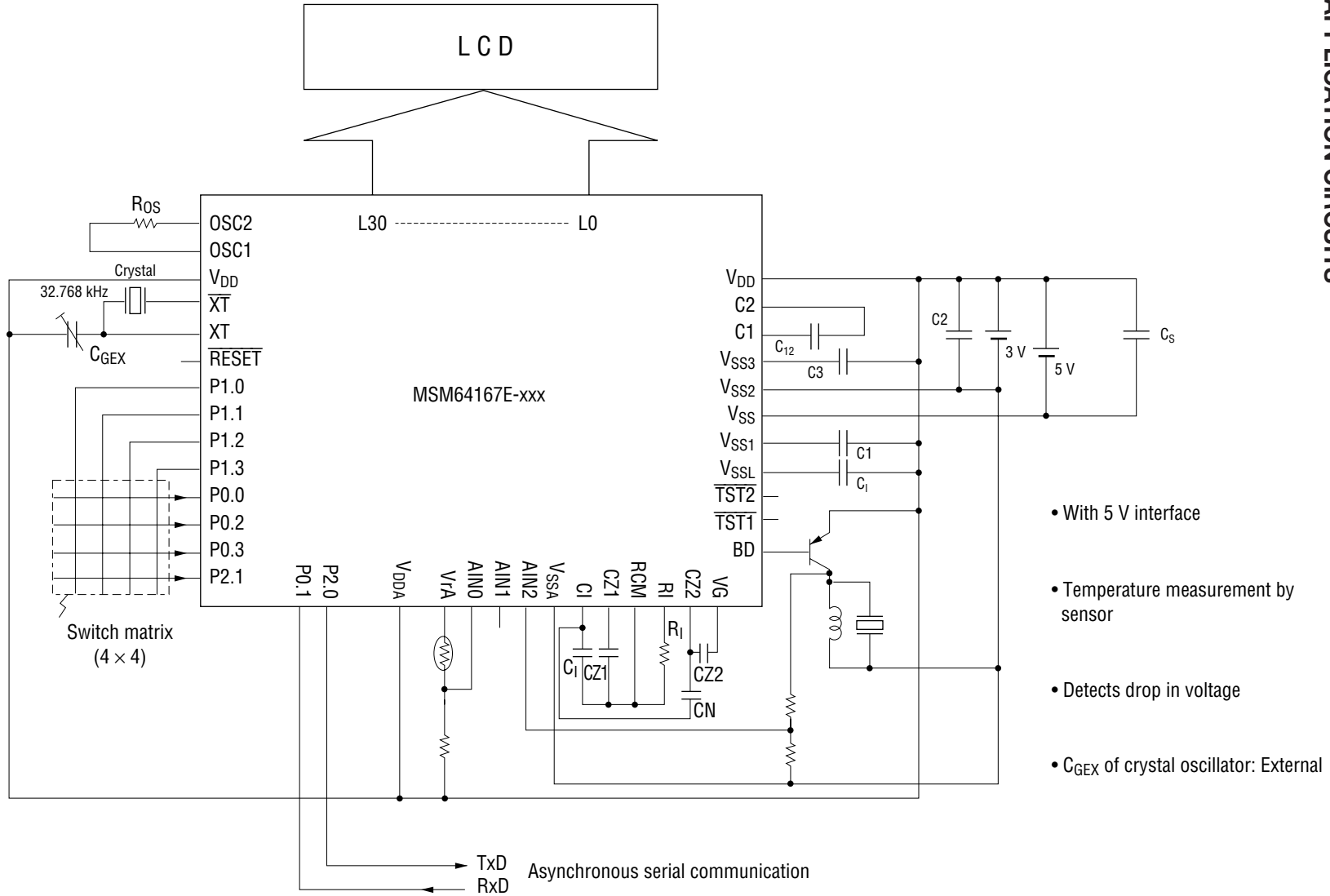
• Time base counter (TBC)

The MSM64167E has a built-in time base counter (TBC) that generates clocks to be supplied to internal peripheral circuits. The time base counter is composed of 15 binary counters. The count clock of the time base is driven by the oscillation clock (32.768 kHz) of the crystal oscillation circuit. The output of the time base counter is used for the buzzer driver, the system reset circuit, the timer, the watchdog timer, the time base interrupt, the sampling clocks of each port, and the LCD driver.

• Interrupt (INTC)

The MSM64167E has ten interrupt sources (10 vector addresses), of which two are external interrupts from ports and eight are internal interrupts.

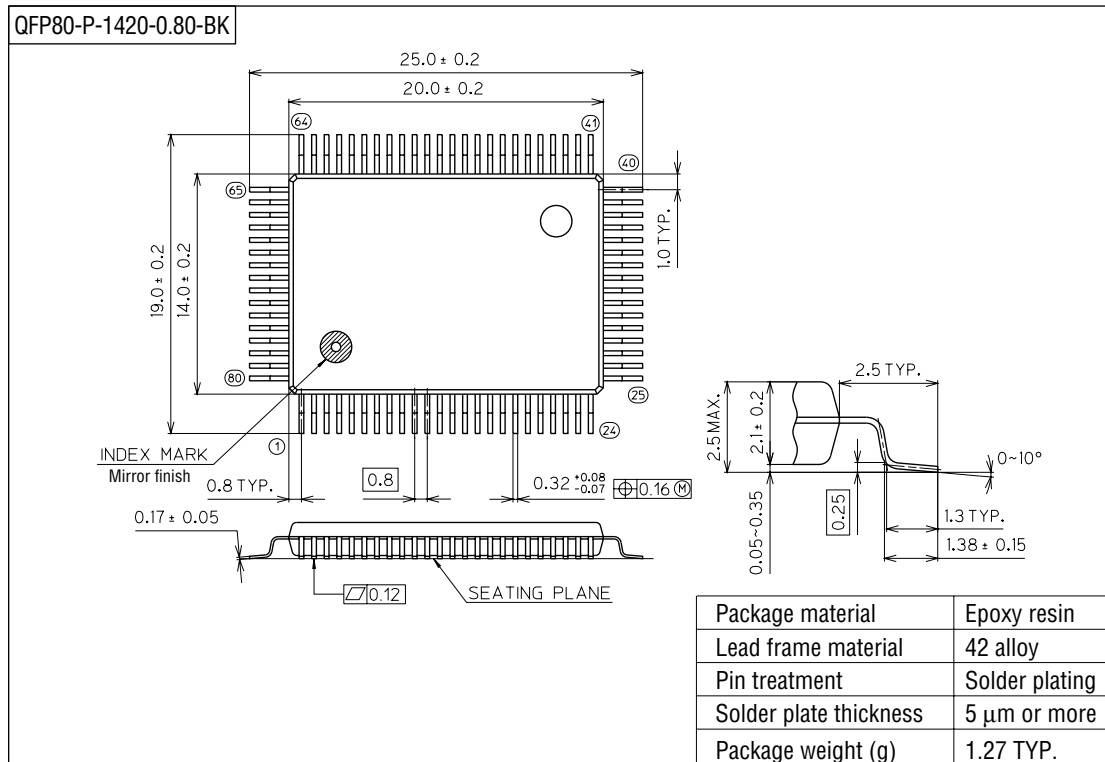
Of the ten interrupt sources, only the watchdog interrupt cannot be disabled (non-maskable interrupt). The other nine interrupts are controlled by the master interrupt enable flag (MI) and the interrupt enable registers (IE0, IE1, and IE2). When an interrupt condition is met, the CPU branches to a vector address corresponding to the interrupt source.



APPLICATION CIRCUITS

PACKAGE DIMENSIONS

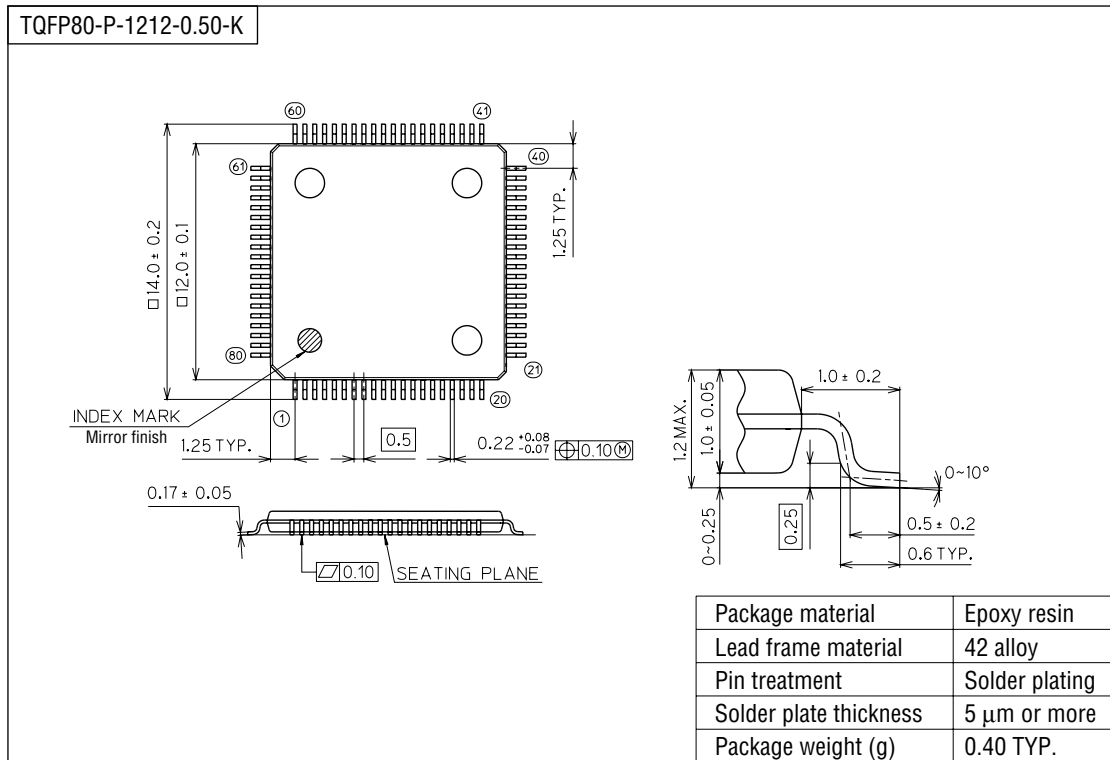
(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, TQFP, LQFP, SOJ, QFJ (PLCC), SHP, and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)



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