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# MSM6698

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## 80-DOT COMMON DRIVER

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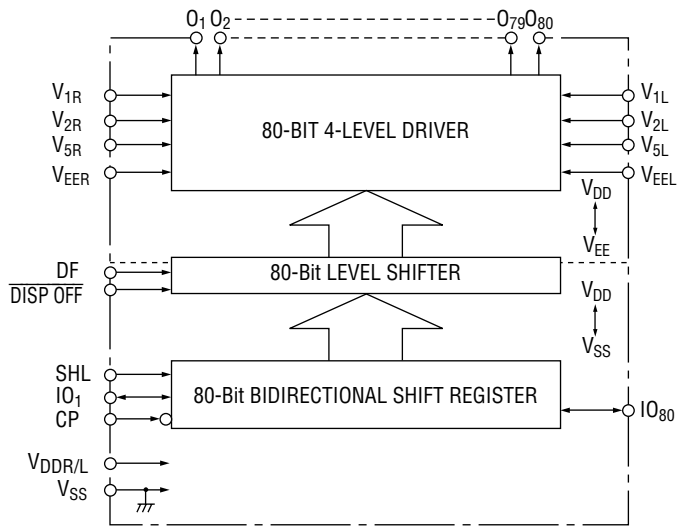
### GENERAL DESCRIPTION

The MSM6698 is a dot matrix LCD common driver. Fabricated in CMOS technology, the device consists of an 80-bit bi-directional shift register, 80-bit level shifter, and 80-bit 4-level driver. The MSM6698 is equipped with 80 LCD output pins. By connecting more than two MSM6698s in series, this LSI is applicable to a wide LCD panel.

### FEATURES

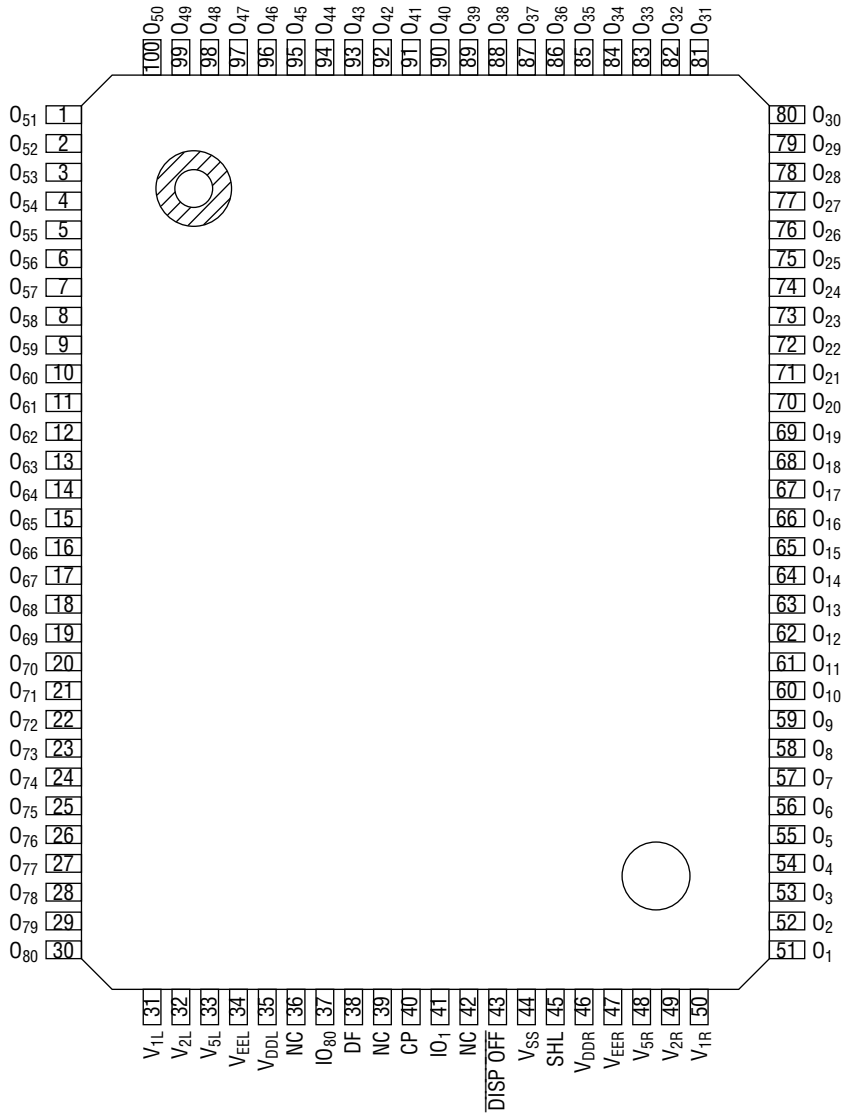
- Logic supply voltage : 2.7 to 5.5 V
- LCD drive voltage : 18 to 28 V
- Applicable LCD duty : 1/64 to 1/240
- Interface with MSM6599B (80-dot segment driver)
- Package:  
100-pin plastic QFP (QFP100-P-1420-0.65-K) (Product name: MSM6698GS-K)

**BLOCK DIAGRAM**



Note:  $V_{DDR/L}$  indicates an abbreviation of  $V_{DDR}$  and  $V_{DDL}$ .

**PIN CONFIGURATION (TOP VIEW)**



NC : No connection

**100-Pin Plastic QFP**

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage (1)	$V_{DD}$	$T_a = 25^{\circ}\text{C}$	-0.3 to +6.5	V
Power Supply Voltage (2)	$V_{DD} - V_{EE} *1$	$T_a = 25^{\circ}\text{C}$	0 to 30	V
Input Voltage	$V_I$	$T_a = 25^{\circ}\text{C}$	-0.3 to $V_{DD} + 0.3$	V
Storage Temperature	$T_{STG}$	—	-55 to +150	$^{\circ}\text{C}$

\*1  $V_1 > V_2 > V_5 > V_{EE}$ ,  $V_{EE} + 10\text{V} \geq V_5 > V_{EE}$ ,  $V_{DD} \geq V_1 > V_2 \geq V_{DD} - 10\text{V}$ ,  $V_{DD} = V_{DDR} = V_{DDL}$ ,  
 $V_1 = V_{1R} = V_{1L}$ ,  $V_2 = V_{2R} = V_{2L}$ ,  $V_5 = V_{5R} = V_{5L}$ ,  $V_{EE} = V_{EER} = V_{EEL}$

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Condition	Range	Unit
Power Supply Voltage (1)	$V_{DD}$	—	2.7 to 5.5	V
Power Supply Voltage (2)	$V_{DD} - V_{EE} *1$	No load	14 to 28	V
		During LCD drive	18 to 28	V
Operating Temperature	$T_{op}$	—	-20 to +75	$^{\circ}\text{C}$

\*1  $V_1 > V_2 > V_5 > V_{EE}$ ,  $V_{EE} + 7\text{V} \geq V_5 > V_{EE}$ ,  $V_{DD} \geq V_1 > V_2 \geq V_{DD} - 7\text{V}$ ,  $V_{DD} = V_{DDR} = V_{DDL}$ ,  
 $V_1 = V_{1R} = V_{1L}$ ,  $V_2 = V_{2R} = V_{2L}$ ,  $V_5 = V_{5R} = V_{5L}$ ,  $V_{EE} = V_{EER} = V_{EEL}$

## ELECTRICAL CHARACTERISTICS

### DC Characteristics

( $V_{DD} = 2.7$  to  $5.5V$ ,  $T_a = -20$  to  $+75^\circ C$ )

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	$V_{IH}$ *1	—	$0.8V_{DD}$	—	$V_{DD}$	V
"L" Input Voltage	$V_{IL}$ *1	—	$V_{SS}$	—	$0.2V_{DD}$	V
"H" Input Current	$I_{IH}$ *1	$V_I = V_{DD}$ , $V_{DD} = 5.5V$	—	—	1	$\mu A$
"L" Input Current	$I_{IL}$ *1	$V_I = 0V$ , $V_{DD} = 5.5V$	—	—	-1	$\mu A$
"H" Output Voltage	$V_{OH}$ *2	$I_O = -0.2mA$ , $V_{DD} = 2.7V$	$V_{DD} - 0.4$	—	—	V
"L" Output Voltage	$V_{OL}$ *2	$I_O = 0.2mA$ , $V_{DD} = 2.7V$	—	—	0.4	V
ON Resistance	$R_{ON}$ *4	$V_{DD} - V_{EE} = 25V$ $ V_N - V_O  = 0.25V$ *3	—	—	2.0	$k\Omega$
Logic Supply Current	$I_{SS}$	$f_{CP} = 28kHz$ , $V_{DD} = 3.0V$	—	—	50	$\mu A$
LCD Supply Current	$I_{EE}$	$V_{DD} - V_{EE} = 25V$ , No load	—	—	300	
Input Capacitance	$C_I$	$f = 1MHz$	—	—	—	pF

\*1 Applicable to CP,  $IO_1$ ,  $IO_{80}$ , SHL, DF,  $\overline{DISP OFF}$ .

\*2 Applicable to  $IO_1$ ,  $IO_{80}$ .

\*3  $V_N = V_{DD}$  to  $V_{EE}$ ,  $V_2 = 1/16 (V_{DD} - V_{EE})$ ,  $V_5 = 15/16 (V_{DD} - V_{EE})$ ,  $V_{DD} = V_1$ ,  $V_{DD} = 4.5V$   
 $V_{DD} = V_{DDR} = V_{DDL}$ ,  $V_1 = V_{1R} = V_{1L}$ ,  $V_2 = V_{2R} = V_{2L}$ ,  $V_5 = V_{5R} = V_{5L}$ ,  $V_{EE} = V_{EER} = V_{EEL}$

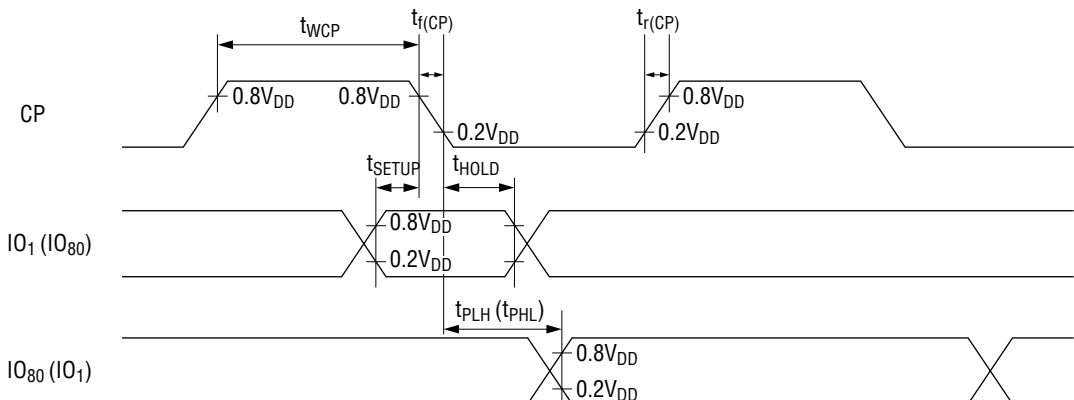
\*4 Applicable to  $O_1$  to  $O_{80}$

### Switching Characteristics

( $V_{DD} = 2.7$  to  $5.5V$ ,  $T_a = -20$  to  $+75^\circ C$ ,  $C_L = 15pF$ )

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H", "L" Propagation Delay Time	$t_{PLH}$ , $t_{PHL}$	—	—	—	3	$\mu s$
Clock Frequency	$f_{CP}$	—	—	—	1	MHz
CP Pulse Width	$t_{WCP}$	—	63	—	—	ns
Data Setup Time $IO_1$ ( $IO_{80}$ ) $\rightarrow$ CP	$t_{SETUP}$	—	100	—	—	ns
Data Hold Time CP $\rightarrow IO_1$ ( $IO_{80}$ )	$t_{HOLD}$	—	100	—	—	ns
Rise / Fall Time of CP	$t_r$ (CP), $t_f$ (CP)	—	—	—	20	ns

Note1: When display control by the  $\overline{DISPOFF}$  pin is performed, CP rise and fall time must be  $\leq 1 \mu s$ .



## FUNCTIONAL DESCRIPTION

### Pin Functional Description

#### • IO<sub>1</sub>, IO<sub>80</sub>, SHL

IO<sub>1</sub> and IO<sub>80</sub> are I/O pins of the 80-bit bi-directional shift register. The shift direction can be selected by the SHL pin. Set the SHL pin to "H" or "L" level during power-on. Table 1 gives functions of IO<sub>1</sub>, IO<sub>80</sub>, and SHL.

Table 1

SHL	Shift direction	I/O Pins	Input, output	Function
L	O <sub>1</sub> → O <sub>80</sub>	IO <sub>1</sub>	Input	The scanning data from the LCD controller LSI is input into IO <sub>1</sub> synchronized with the clock pulse. *1
		IO <sub>80</sub>	output	Shift register contents output pin. The scanning data which was input into IO <sub>1</sub> is output from IO <sub>80</sub> with 80-bit delay, synchronized with the clock pulse.
H	O <sub>80</sub> → O <sub>1</sub>	IO <sub>80</sub>	Input	The scanning data from the LCD controller LSI is input into IO <sub>80</sub> synchronized with the clock pulse. *1
		IO <sub>1</sub>	output	Shift register contents output pin. The scanning data which was input into IO <sub>80</sub> is output from IO <sub>1</sub> with 80-bit delay, synchronized with the clock pulse.

\*1 The combination of the scanning data, IO<sub>1</sub> or IO<sub>80</sub>, and the LCD driving output, O<sub>1</sub> - O<sub>80</sub>, is shown in the table below.

Scanning data	LCD driving output
"H"	Select level (V <sub>1</sub> , V <sub>EE</sub> )
"L"	Non-Select level (V <sub>2</sub> , V <sub>5</sub> )

- **CP**

This is a clock pulse input pin of the 80-bit bidirectional shift register. Scan data is shifted at the falling edge of a clock pulse.

- **DF**

This is an alternate signal input pin for LCD driving, which generally inputs a frame inversion signal.

- **$\overline{\text{DISP OFF}}$**

This is an input pin to control the output pins  $O_1$  to  $O_{80}$ . During low signal input, signals on the  $V_1$  level are output from the output pins  $O_1$  to  $O_{80}$ . See the Truth Table.

- **$O_1$  to  $O_{80}$**

4-level driver outputs of this IC device, directly corresponding to each bit of the bidirectional shift register. Any of four levels  $V_1$ ,  $V_2$ ,  $V_5$ , and  $V_{EE}$  is selected and output combining the DF signal with shift register data (see the Truth Table).

These outputs are connected to the Common side on the LCD panel.

- **$V_{DDR}$ ,  $V_{DDL}$ ,  $V_{SS}$**

These are power supply pins of this IC. Both the  $V_{DDR}$  and  $V_{DDL}$  pins are normally 2.7 to 5.5 V.  $V_{SS}$  is a grounding pin, which is normally 0 V.

- **$V_{1L}$ ,  $V_{2L}$ ,  $V_{5L}$ ,  $V_{EEL}$ ,  $V_{1R}$ ,  $V_{2R}$ ,  $V_{5R}$ ,  $V_{EER}$**

These are LCD drive bias voltage pins. The  $V_1$  pin may be separated from the  $V_{DD}$  pin. Bias power is supplied from an external source.

### Truth Table

DF	Shift register data	$\overline{\text{DISP OFF}}$	Driver Output ( $O_1$ to $O_{80}$ )
L	L	H	$V_2$
L	H	H	$V_{EE}$
H	L	H	$V_5$
H	H	H	$V_1$
×	×	L	$V_1$

× : Don't care

### NOTES ON USE (when turning power ON and OFF)

The LCD drivers of this IC requires a high voltage. When a high voltage is applied to them with the logic power supply floating, excess current flows. This may damage the IC. Be sure to carry out the following power-ON and power-OFF sequences.

When turning power ON:

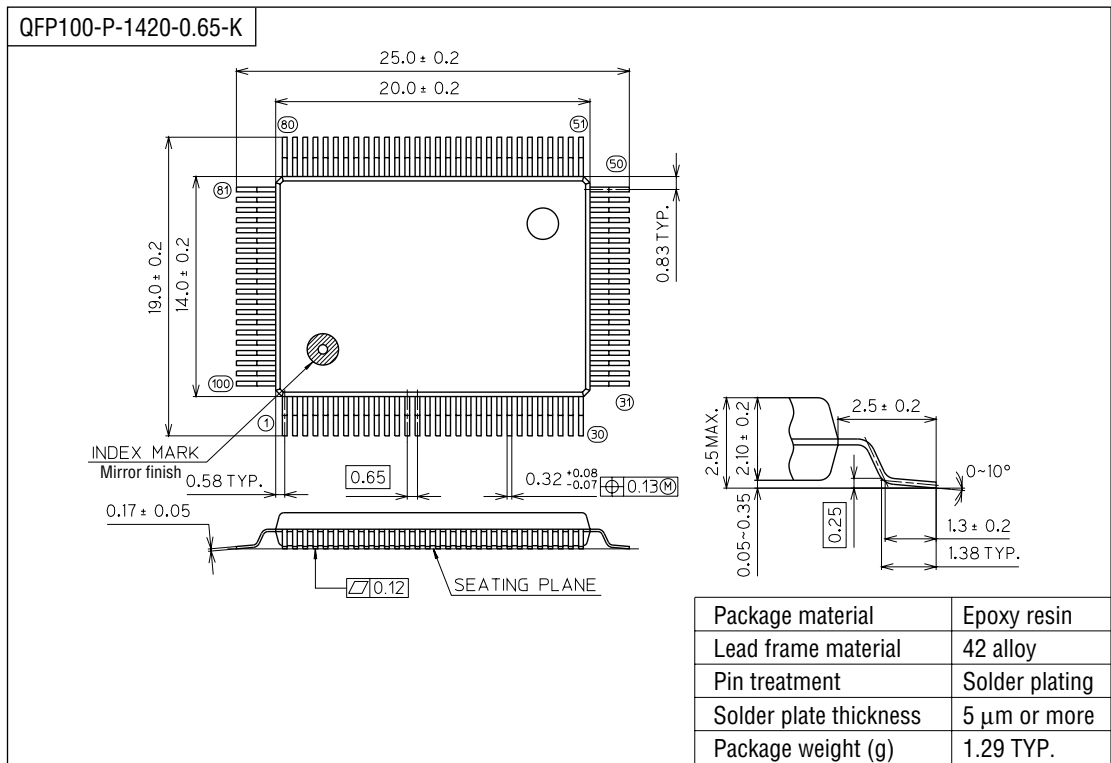
First turn on the logic circuits, then the LCD drivers, or turn on both of them at the same time.

When turning power OFF:

First turn off the LCD drivers, then the logic circuits, or turn off both of them at the same time.

**PACKAGE DIMENSIONS**

(Unit : mm)



**Notes for Mounting the Surface Mount Type Package**

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).