OKI Semiconductor

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MSM6778

120-DOT COMMON DRIVER (TAB)

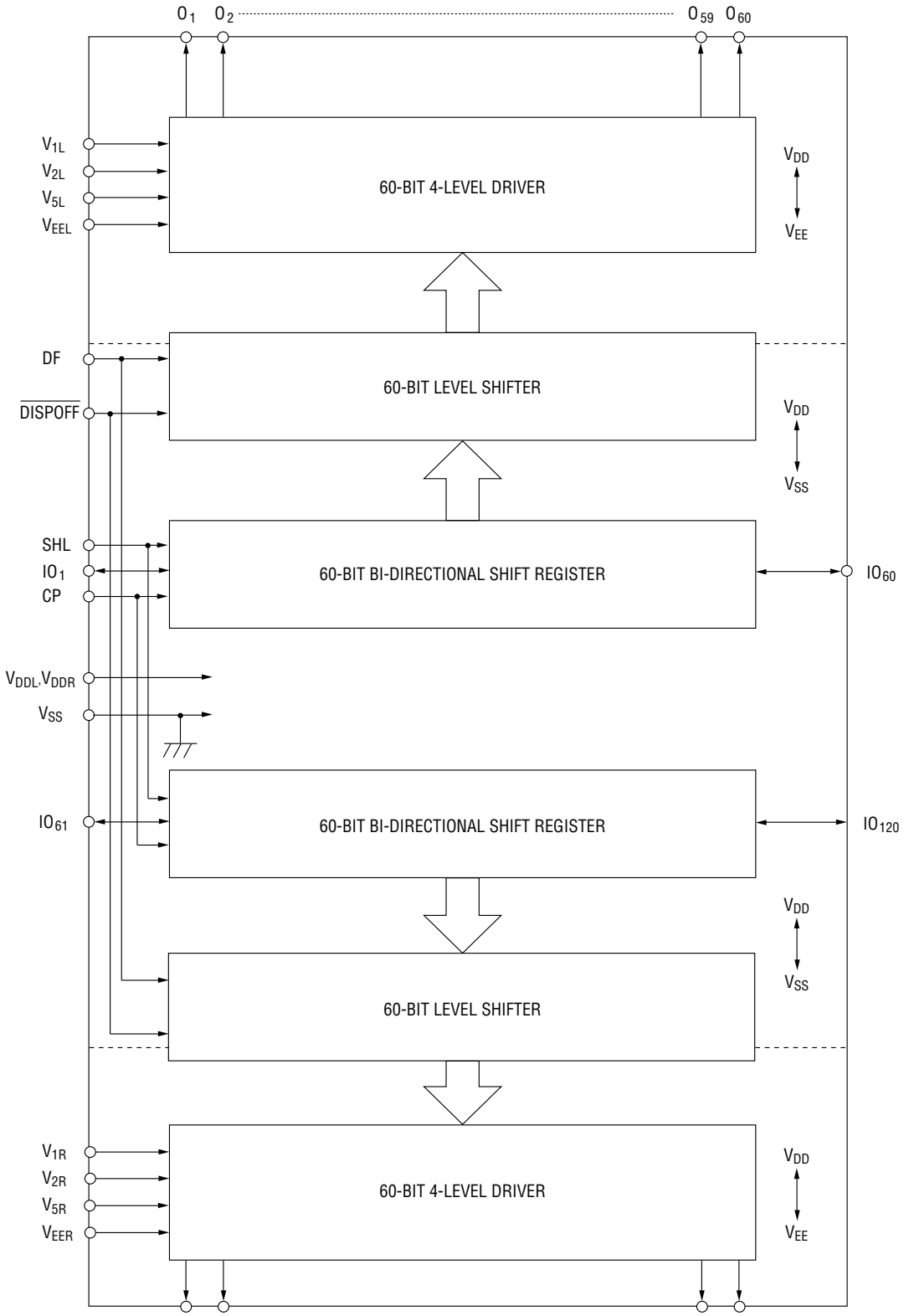
GENERAL DESCRIPTION

The MSM6778 is a dot-matrix LCD common driver. Fabricated in CMOS technology, the device contains two 60-bit bidirectional shift registers, two 60-bit level shifters, and two 60-bit 4-level drivers.
The MSM6778 has 120 LCD outputs. The number of LCD outputs can be increased by cascading MSM6778 devices, using cascade-connected I/O pins. The bias voltage which specifies a drive level can optionally be supplied externally. The MSM6778 is suitable for various types of LCD panel.

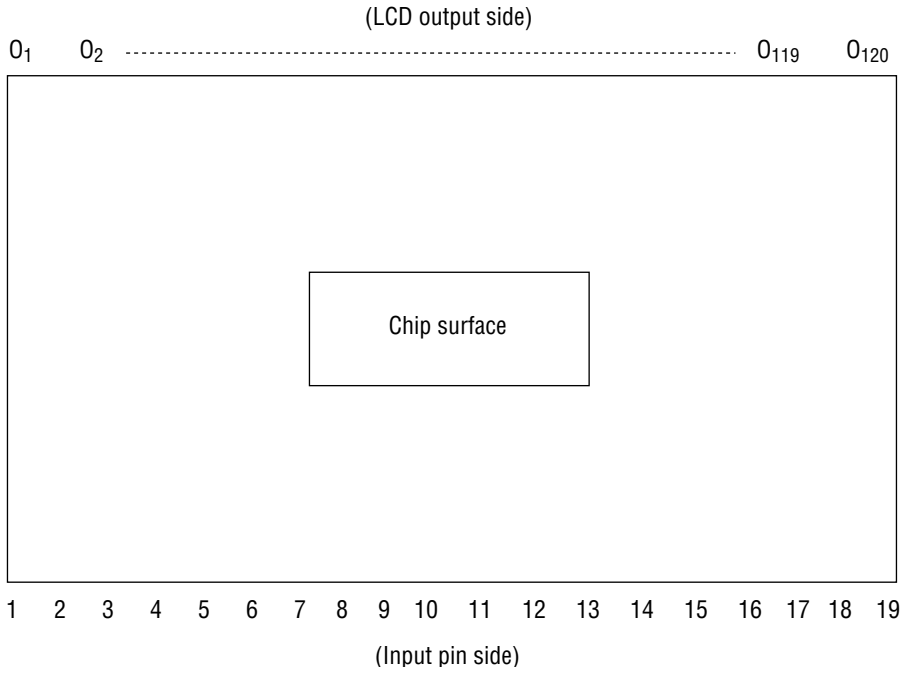
FEATURES

- Logic supply voltage : 2.7 V to 5.5 V
- LCD drive voltage : A wide range from 18 V to 28 V
- Applicable LCD duty : 1/100 to 1/256
- The bias voltage can be externally supplied.
- Structure:
  35mm-wide Tape Automated Bonding (TAB) film (Product name: MSM6778AV-Z-01)
  Tin-plating

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



Input Pin Name

Pin	Symbol	Pin	Symbol
1	V_{1L}	11	IO_{61}
2	V_{2L}	12	IO_{120}
3	V_{5L}	13	DF
4	V_{EEL}	14	CP
5	V_{DDL}	15	V_{DDR}
6	SHL	16	V_{EER}
7	V_{SS}	17	V_{5R}
8	$\overline{DISPOFF}$	18	V_{2R}
9	IO_1	19	V_{1R}
10	IO_{60}		

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage (1)	V_{DD}	Ta=25°C	–0.3 to +6.5	V
Power Supply Voltage (2)	V_{DD}–V_{EE}*	Ta=25°C	0 to 30	V
Input Voltage	V_I	Ta=25°C	–0.3 to V_{DD}+0.3	V
Storage Temperature	T_{STG}	—	–30 to +85	°C

* $V_1>V_2>V_5>V_{EE}$, $V_{DD}\geqq V_1>V_2\geqq V_{DD}-10V$, $V_{EE}+10V\geqq V_5>V_{EE}$
$V_{DD}=V_{DDL}=V_{DDR}$, $V_1=V_{1L}=V_{1R}$, $V_2=V_{2L}=V_{2R}$, $V_5=V_{5L}=V_{5R}$, $V_{EE}=V_{EEL}=V_{EER}$

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Power Supply Voltage (1)	V_{DD}	—	2.7 to 5.5	V
Power Supply Voltage (2)	V_{DD}–V_{EE}*	No load	14 to 28	V
		During liquid crystal driving	18 to 28	V
Operating temperature	T_{op}	—	–20 to +75	°C

* $V_1>V_2>V_5>V_{EE}$, $V_{DD}\geqq V_1>V_2\geqq V_{DD}-7V$, $V_{EE}+7V\geqq V_5>V_{EE}$
$V_{DD}=V_{DDL}=V_{DDR}$, $V_1=V_{1L}=V_{1R}$, $V_2=V_{2L}=V_{2R}$, $V_5=V_{5L}=V_{5R}$, $V_{EE}=V_{EEL}=V_{EER}$

Note: Unlike mold packages, The Tape Carrier Package (TCP) cannot shield a light. Please shield a light to secure the electrical characteristics.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD}=2.7 to 5.5 V, Ta= –20 to +75°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH} *1	—	0.8 V_{DD}	—	—	V
"L" Input Voltage	V_{IL} *1	—	—	—	0.2 V_{DD}	V
"H" Input Current	I_{IH} *1	$V_I=V_{DD}$, V_{DD}=5.5 V	—	—	1	µA
"L" Input Current	I_{IL} *1	V_I=0 V, V_{DD}=5.5 V	—	—	–1	µA
"H" Output Voltage	V_{OH} *2	I_O=–0.2 mA, V_{DD}=2.7 V	V_{DD}–0.4	—		V
"L" Output Voltage	V_{OL} *2	I_O=0.2 mA, V_{DD}=2.7 V	—	—	0.4	V
ON Resistance	R_{ON} *4	V_{DD}–V_{EE}=25 V, *3 I V_N–V_O I=0.25 V	—	—	2.0	kΩ
Supply Current	I_{DD} *5	CP=28 kHz, V_{DD}=3.0 V	—	—	60	µA
	I_{EE} *5	V_{DD}–V_{EE}=25 V, No load	—	—	400	µA
Input Capacitance	C_I	f=1 MHz	—	—	—	pF

*1 Applicable to pins CP, IO_1,IO_{60},IO_{61}, IO_{120}, SHL, DF, $\overline{DISPOFF}$
*2 Applicable to pins IO_1, IO_{60}, IO_{61}, IO_{120}
*3 $V_N=V_1$, V_2, V_5, V_{EE}, V_2=1/16 (V_{DD}–V_{EE}), V_5=15/16 (V_{DD}–V_{EE})
*4 Applicable to pins O_1 to O_{120}
*5 I_{DD} shows the supply current between V_{DD} and V_{SS}. I_{EE} shows the supply current between V_{DD} and V_{EE}.

Note: The above values are guaranteed when TCP is protected from light.

Switching Characteristics

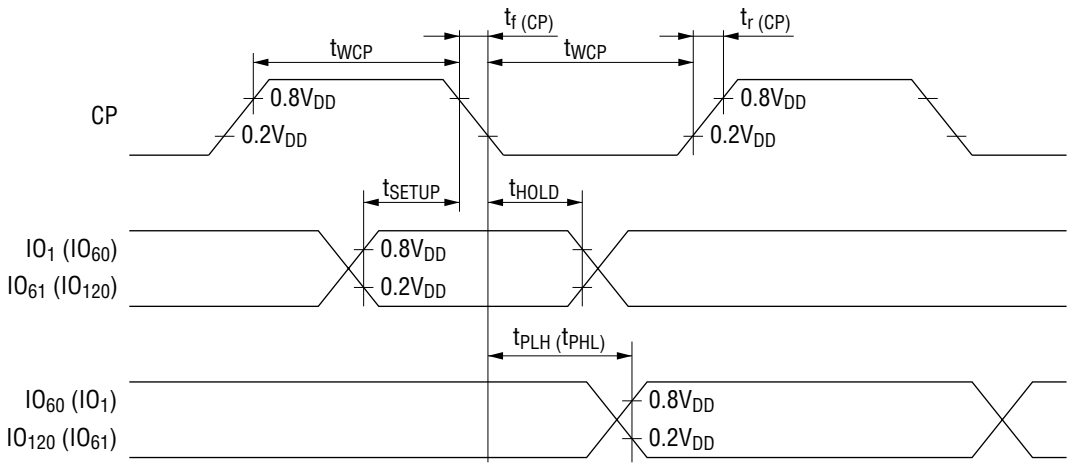
(V_{DD}=2.7 to 5.5 V, Ta= –20 to +75°C, C_L=15 pF)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
IO_1, IO_{61} (IO_{60}, IO_{120}) "H", "L" Propagation Delay Time	t_{PLH} t_{PHL}	—	*1	—	3	µs
Clock Frequency	f_{CP}	—	—	—	1	MHz
CP Pulse Width	t_{WCP}	—	63	—	—	ns
Data Setup Time IO_1, IO_{61} → CP (IO_{60}, IO_{120} → CP)	t_{SETUP}	—	100	—	—	ns
Data Hold Time CP → IO_1, IO_{61} (CP → IO_{60}, IO_{120})	t_{HOLD}	—	100	—	—	ns
CP Rise, Fall Time	$t_{r\ (CP)}$ $t_{f\ (CP)}$	—	—	—	20	ns

*1 The relationship between t_{PLH} (t_{PLH}) Min. and t_{HOLD} Min. satisfies the operation in a cascade connection state.

Note 1: When display is controlled by $\overline{DISPOFF}$ pin, CP rise and fall time must be ≦ 1 µs.

Note 2: The above values are guaranteed when TCP is protected from light.



FUNCTIONAL DESCRIPTION

Pin Functional Description

• IO_1, IO_{60}, IO_{61}, IO_{120}
These are I/O pins of the two 60-bit bidirectional shift registers.

• SHL
This pin selects the shift direction of the two 60-bit bidirectional shift registers.
Set this pin to "H" or "L" level during power-on.

SHL	Shift Direction	I/O pins		Function
L	$O_1 \rightarrow O_{60}$	IO_1, IO_{61}	Input	IO_1 and IO_{61} are data input pins for the shift register. The entered data is read in at the falling edge of a clock pulse. The data is output from IO_{60} and IO_{120} behind the number of bits (60) of the shift register.
	$O_{61} \rightarrow O_{120}$	IO_{60}, IO_{120}	Output	
H	$O_{60} \rightarrow O_1$	IO_{60}, IO_{120}	Input	IO_{60} and IO_{120} are data input pins for the shift register. The entered data is read in at the falling edge of a clock pulse. The data is output from IO_1 and IO_{61} behind the number of bits (60) of the shift register.
	$O_{120} \rightarrow O_{61}$	IO_1, IO_{61}	Output	

• CP
This is a clock pulse input for the two 60-bit bidirectional shift registers. Scan data is shifted at the falling edge of a clock pulse.

• DF
This is a synchronous signal input for alternate signal for LCD driving.

• $\overline{\text{DISPOFF}}$
This is an input used to control the output levels of O_1 to O_{120}. During low level input, the V_1 level is output from the output pins O_1 to O_{120} independently of the data of the shift register. See the truth table.

• O_1 to O_{120}
These are outputs for the 4-level drivers, which correspond directly to each bit of the shift register. One of the four levels V_1, V_2, V_5, and V_{EE} is selected and output depending on the combination of the shift register data and a DF signal. See the Truth Table.

• V_{1L}, V_{2L}, V_{5L}, V_{EEL}, V_{1R}, V_{2R}, V_{5R}, V_{EER}
These are LCD drive bias voltage inputs.

• V_{DDL}, V_{DDR}, V_{SS}
These are power supply pins for the device. V_{DD} is usually from 2.7 V to 5.5 V and V_{SS} is 0 V.

Truth Table

DF	SHIFT REGISTER DATA	DISPOFF	DRIVER OUTPUT (O_1 to O_{120})
L	L	H	V_2
L	H	H	V_{EE}
H	L	H	V_5
H	H	H	V_1
X	X	L	V_1

X : Don't care

NOTES ON USE (when turning the power ON or OFF)

The LCD drivers of this IC require a high voltage. For this reason, if a high voltage is applied to the LCD drivers with the logic power supply floating, excess current flows. This may damage the IC.
Be sure to follow the sequence below when turning the power ON or OFF.
Power ON : Logic circuits ON → LCD drivers ON, or both ON at a time
Power OFF : LCD drivers OFF → logic circuits OFF, or both OFF at a time