OKI Semiconductor
This version: Jan. 1998
Previous version: Nov. 1996

MSM6926/27/46/47 Application Notes

ITU-T V.21/ITU-T V.23 Based Single Power Supply FSK Modem

APPLICATION NOTE

1. AN INTRODUCTION TO THE MODEM

These days reflect our so-called communication era, and the data processing industry has been growing at a tremendous rate, particularly in the area using the existing telephone networks. The modems are playing an important role as an interface to computer systems which communicate by a public or dedicated data transmission networks. Taking early notice of the significance of data communications, OKI has been engaged since many decades in the development and manufacturing of data communication-related equipments. This application note introduces and explains OKI's latest development in this field, the CMOS Single-chip modem series, MSM6926, MSM6927, MSM6946, and MSM6947. Before entering details of this new series, let us first see what a modem is all about.

1) What is a modem?
2) Modem communication systems
3) Modem types and modulation/demodulation methods

1) What is a Modem?

Figure 1-1 shows a typical data communication system using modems. The basic role of a modem is to convert digital logic signals "1" and "0" into analog equivalent that can be passed through a telephone line, and vice versa.
A data signal (digital signal) from a data terminal is once converted into an analog audio signal and is transmitted to the modem of a receiving terminal utilizing the public telephone network. At the receiving end, the analog audio signal thus received is then converted by its modem into a corresponding digital signal and conveyed to the receiving data terminal.
In this way, two distant data terminals can communicate for the exchange of data by means of modems.
The telephone line allows transmission of analog audio signals exclusively, but the digital data signal, as such, cannot be passed through. For this reason, modems are required as an interface to existing analog transmission lines.
Referring to Figure 1-1, modulation and demodulation means the conversion of digital signals into analog and vice-versa, and will be detailed in the chapter "MODES TYPES AND MODULATION/DEMODULATION METHODS". The duplexer transmits a signal to the telephone line or receives it from the telephone line, and is not designed to receive a previously transmitted signal. Usually, it uses a hybrid transformer or hybrid resistor circuit consisting of two operational amplifiers, resistors and a line transformer.

2) Modem Communication Systems

The modem communication systems are largely divided into modes of operation. One is called the full duplex system, and the other the half-duplex system. The telephone line is a balanced two-wire circuit, and usually is called the 2-Wire (2W) line. The full-duplex and half-duplex are terms which conform to the common use of this 2-Wire line.

a) 4-Wire full-duplex communication

The 4-Wire full-duplex communication is another widely practiced method in which two dedicated telephone lines are used for transmission and reception, respectively. This method provides transmission and reception simultaneously, but requires two telephone lines.

b) 2-Wire half-duplex communication

The 2-Wire half-duplex communication is a method which links two terminals in either direction, but only one direction at a time. Namely, when one terminal is transmitting, the other must operate in the receiving mode. This limitation may be a drawback for certain applications.

c) 2-Wire full-duplex communication

The 2-Wire full-duplex communication is a method in which duplexers or the like are used to permit two distant terminals to work in both directions simultaneously through a 2-Wire line. This method is more economical compared with 2-Wire half-duplex.
The above three methods are schematically shown in Figure 1-2.

3) Modem Types and Modulation/Demodulation Methods

Table 1-1 shows a classification of modems.
The modems can also be classified by transmission speeds. Within 300 bps to 9600 bps, low-speed modems usually employ FSK (frequency shift keying) method, medium-speed modems PSK (phase shift keying), and high-speed modems QAM (phase quadrature amplitude modulation).
The ITU-T and BELL in the table stand for European and U.S. standards, respectively.
What are FSK, PSK and QAM, then?
Figure 1-3 shows the operating principles of FSK and PSK. In the FSK system, logic data signals "1" and "0" are modulated with frequencies; for example, "1" is modulated with a lower frequency (f_L), while "0" is modulated with a higher frequency (f_H).
In the PSK system, the frequency is constant, and the modulation is carried out by assigning phase 0° to say "1" and phase –180° to "0". (Two-phase phase shift keying) The QAM system is a complex one in which PSK and AM are combined. BY way of example, frequencies and phase angles assigned in FSK and PSK are shown in Table 1-2.
When referring to the modem modulation systems, we must speak of two important terms. One is the modulation rate (baud rate) and the carrier frequency. In the FSK system, the transmission speed and modulation rate are equal. This is because carrier frequencies are in one to one correspondence to logic values "1" and "0".
Where four phase angles are assigned to two data digits (that is, four 2-bit values) as in the 4-phase PSK system, the modulation rate becomes half of the transmission speed.
In the 4-phase PSK system (1200 bps), for example, the modulation rate is 600 bauds. In the FSK system (300 bps), on the other hand, the modulation rate is 300 bauds.
You remember that the 2-Wire full-duplex communication is subject to limitations in its implementation. This is because a group-wise communication system using the originate mode and answer mode as shown in Table 1-2 must be employed. In any modulation system whether FSK or PSK, a number of harmonics are produced by modulation.

In case of FSK, for example, if logic states "1' and "0" — these are called mark and space, respectively — are modulated in the originate mode specified in ITU-T V. 21, one is easily tempted to consider that 980 Hz and 1180 Hz alone appear. In actuality, however, there can appear many other frequency components, and their range is called the frequency band. The bandwidth of signal allowed to pass through a public telephone line is limited to a range of 0.3 kHz to 3.4 kHz.
This bandwidth is called the voice band. In the group-wise communication system, this voice band is divided into two bands: the lower frequency band which is assigned to the originate mode channel and the higher frequency band which is assigned to the answer mode channel. These two bands can be used independently each other. For each of these bands, a modulation rate and a carrier frequency are selected so that the resultant frequency components will be included in its frequency band.
In the FSK system, the maximum allowable modulation rate is ordinarily 300 baud. Should it be set at 1200 baud, the frequencies developed will occupy too wide a band to be accommodated in the voice band.
Namely, the 1200 baud FSK system cannot be realized in the full-duplex transmission form.
All these are summed up in Figure 1-4.
Full-duplex transmission cannot be made if bands are overlapped as shown in Figure 1-4 (b). As shown in Figure 1-4 (c), the 1200-baud FSK system is allowed to have only one channel.
As explained above, the 2-Wire full-duplex communication system is one in which the bi-directional data transmission between two terminals is carried out simultaneously by using channels assigned to transmission and reception previously.
Figure 1-5 shows a typical group-wise full-duplex communication system, which is common to both FSK and PSK systems. In the QAM system, frequency components are spread over a wide range, and the group-wise full-duplex communication system cannot be used. At present, efforts are being made to implement the QAM full-duplex communication system by the echo cancelling technique.

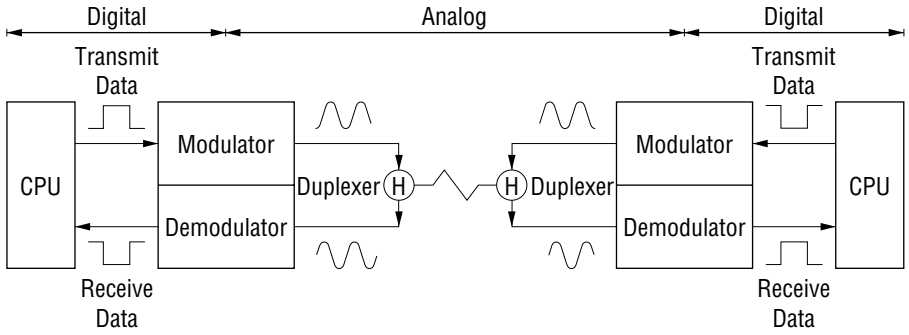


Figure 1-1 Typical Modem System

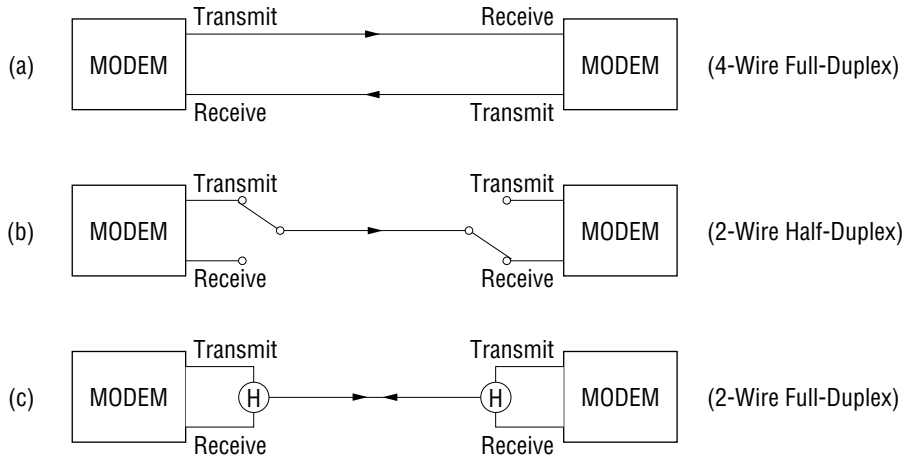


Figure 1-2 Modem Communication System

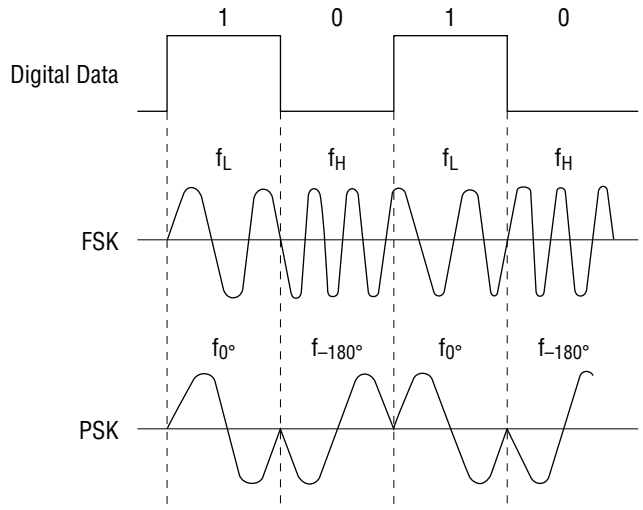


Figure 1-3 Modulated Waveforms

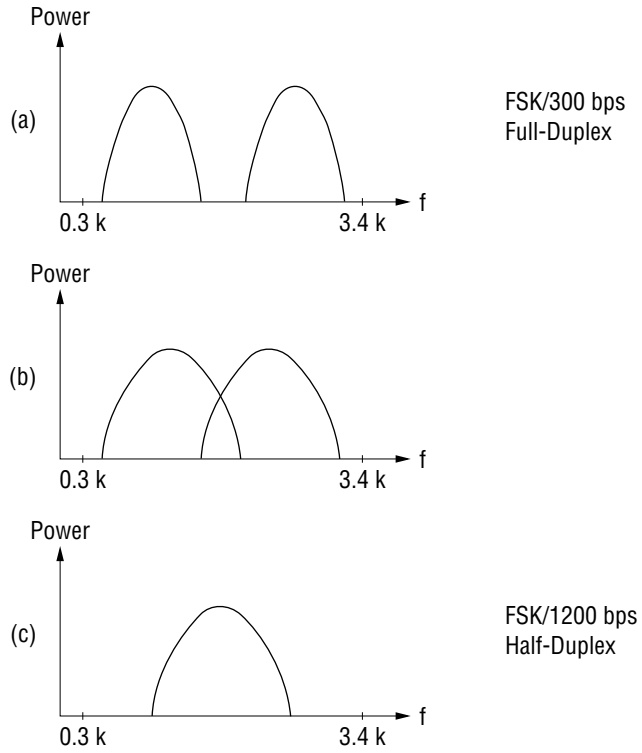


Figure 1-4 Division of Voice Frequency Band

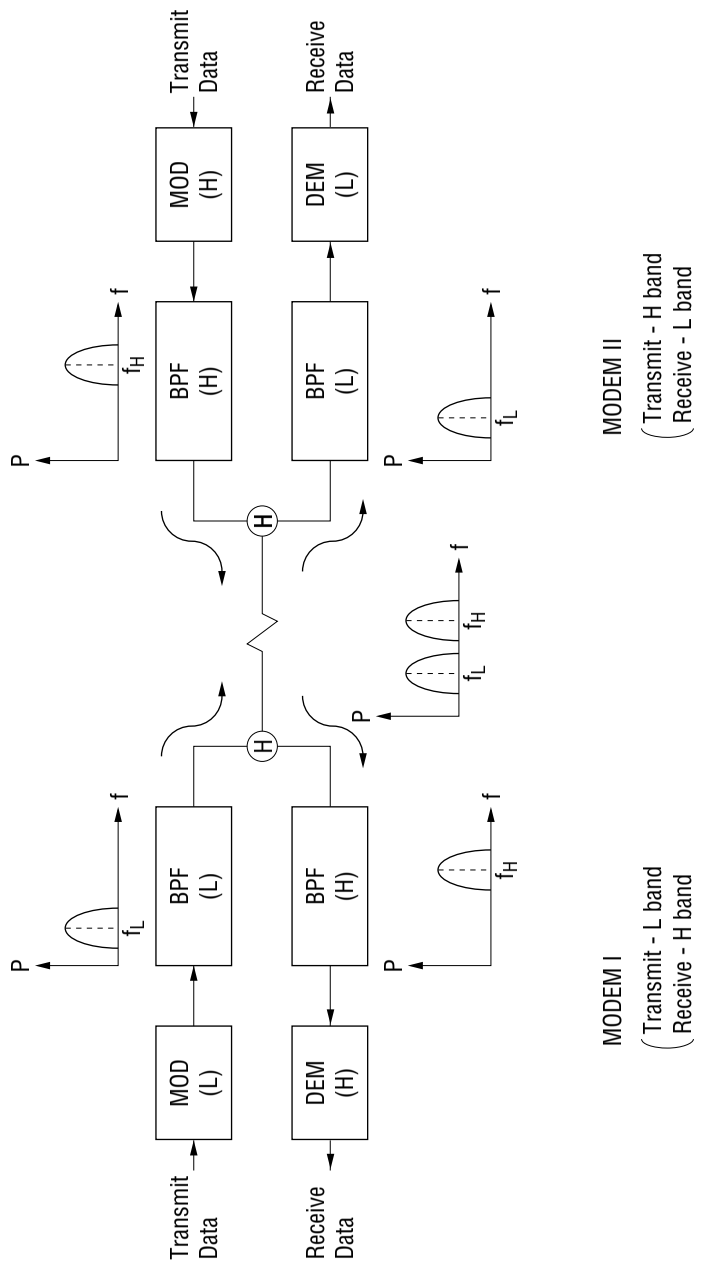


Figure 1-5 Group-wise Full-Duplex Communication System

Table 1-1 Transmission Speeds and Modulation Systems

(Voice-band modem according to ITU-T Recommendations)

Data Rate	Modulation	Baud Rate	Carrier Frequency	Bandwidth	Synchronization	Equalizer	ITU-T V-series	Similar BELL Standard
300 bps	FSK	300 baud	1080 ±100 Hz 1750 ±100 Hz	300 Hz	Asynchronous (Full Duplex)	Fixed	V.21	103
1200	4-phase PSK	600	1200 Hz 2400 Hz	1200 Hz	Synchronous/ Asynchronous (Full Duplex)		V.22	212
1200	FSK	1200	1700 ±400 Hz	1200 Hz	Asynchronous (Half Duplex)		V.23	202
2400	4-phase PSK	1200	1800 Hz	1200 Hz (3 dB down)	Synchronous (Half Duplex)		V.26 V.26 bis	201
4800	8-phase PSK	1600	1800 Hz	1600 Hz (3 dB down)		Automatic	V.27 V.27 bis V.27 ter	208
9600	16-phase QAM	2400	1700 Hz	2400 Hz (3 dB down)			V.29	209

Note: In practice, the occupied bandwidth for 2400 - 9600 bps are as follows to improve the receiving performances.

2400 bps — 2400 Hz (100% Roll-off)
4800 bps — 2400 Hz (50% Roll-off)
9600 bps — 2640 Hz (10% Roll-off)

Table 1-2 Correspondence of Digital Data to Analog Value

MODE	FSK (300 bps)			4-phase PSK (1200 bps)				
	Transmit Data bit	ITU-T V.21	Bell 103	Carrier Frequency	Data bit pair	ITU-T V.22 MODES 1-4	ITU-T V.22 MODE 5	Bell 212A
ORIGINATE	Mark "1"	980 Hz	1270 Hz	2400 Hz 1200 Hz	0 0	90°	270°	90°
	Space "0"	1180 Hz	1070 Hz		0 1	0°	180°	0°
ANSWER	Mark "1"	1650 Hz	2225 Hz		1 0	180°	0°	180°
	Space "0"	1850 Hz	2025 Hz		1 1	270°	90°	270°

2. MODEM DESIGN AND OPERATION

1) Modem Design

Illustrated here is a modem designed with MSM6946.
A block diagram of modem is shown in Figure 2-1.
It is provided with an automatic answering function in addition to basic functions. The automatic answering function performs ringing signal detection, control logic operation, and dc loop current control.
Figure 2-2 shows an elementary circuit design using MSM6946, and Table 2-1 is a parts list.
U2 is a dual operational amplifier, and provides an interface circuit with the telephone line.
U3 and U4 are level converters. They perform mutual conversions of the TTL level to and from the ±12 V level required for RS-232C.
U5 is used to drive indicators showing four statuses (power ON, carrier detect, received data, transmit data).
There are five switches in the circuit. SW1 is a power switch; SW2 is an originate (calling) mode/answer (called) mode selector switch; SW3 is used to turn the modem into a (remote) digital loopback mode, in which the transmit data (XD) and the request to send ($\overline{RS1}$) are looped back to the received data (RD) and the clear to send ($\overline{CS}$) respectively, and at the same time the serial data obtained by demodulating of the received FSK signal is input to the transmitter as transmit data within the chip, subjected to FSK modulation and sent back to the telephone line; SW4 is used to switch the telephone line to either the telephone handset or the transformer for modem operation; and SW5 is used to enable the automatic answering mode.
LED comes alight when both the established call connection and off-hook states are detected.
U6 is a photo coupler used to detect at ringing signal, and protects the modem circuit from surge voltages which may appear in the telephone line.
U7 is used for dc loop current control.
U8 is a dual D type flip-flop; one half is used to latch the dc loop current control signal, and another half to latch the data for which the off-state of the received carrier is detected.
U9 is a dual one-shot multivibrator, which is used to squelch the modem output for about 2 seconds (billing delay) necessary in the automatic answering and call connecting sequence and also to provide a sequence to turn off DSR (off-hook) and cut off the dc loop when the received carrier is not detected in about 10 seconds after connection of the modem to the telephone line.
U10 is a quad two input AND gate used in the automatic answering control circuit.
U11 is a dual one-shot multivibrators, one half is a 0.1-sec retriggerable one-shot that is clear the latch to disconnect the telephone line.
Figure 2-2 shows a modem directly connected to a telephone line. Note that the illustrated scheme is not approved by the authority for the purpose of test or development. A typical direct connection scheme (called DAA — direct access arrangement) is shown in Figure 2-3.

2) Modem Operation

In case of manual calling, the modem is placed in the originate and voice mode (telephone line connected to the telephone handset), and a call is made using the telephone handset.
When an answer is detected (i. e. an answer mark tone is heard), the modem is placed in the data mode (the telephone line connected to the modem), and the indicator will light up showing that a carrier signal from the answering modem is received.
In the automatic answering mode, the modem is required to follow the procedures before starting transmission and reception. The following shows a call establishment sequence. See Figure 2-4.

(1) A call is placed to remote modem.
(2) Ringing is detected at answering end.
(3) Answering modem enables DSR and goes off-hook upon completion of ringing.
(4) Answering modem waits two seconds for billing delay.
(5) Then, the transmitter is turned on, and an answer mode mark tone (2225 Hz) is sent forward toward the originating modem.
(6) The mark answer tone is received by the originating modem and the originating modem is placed in a data mode where DSR is enabled.
(7) At the originating modem, CD (carrier detect) is turned on after a carrier detect on-delay time.
(8) Then, the originating modem releases the squelch for the transmitter, initiates the transmission of mark tone in the originate mode, and starts counting CS (clear to send) delay time. (Data transmit state is not yet achieved here).
(9) Upon reception of the mark tone (1270 Hz) from the originating modem, the answering modem turns on CD after a carrier detect on-delay time.
(10) Then, CS is turned on, enabling the answering modem to start data communication.
(11) The originating modem enters into a data communication state after a CS delay time.

In the automatic answering mode, the call connection is aborted when no response is obtained within a specified time or when the received carrier is lost for more than a specified time.
A power supply for the modem is easily available with an AC adaptor for stepping down 100 Vac to 12 Vac.
In Figure 2-2, three power supplies (+12 V, –12 V and +5 V) are used. The –12 V power supply is used for the level converter only, and can be dispensed with if the modem is to be connected to a computer via UART.
One of the most important performances of the modem is the bit error rate, which represents the ratio of number of error bit to the total number of data bit. The bit error rate is measured using the test circuit illustrated in Figure 2-5 and the S/N ratio as a parameter defined at the receiver input.
A transmit data in a 511 bit pseudo-random bit pattern is applied to the transmitter to generate an FSK signal. The signal is added with noise from a white noise source via attenuators, and is connected to the received signal input terminal of the modem to be measured.

The noise level (N) is usually measured through a voice frequency band-pass filter (BPF) to determine an S/N ratio.
The bit error rate is determined by comparing transmitted data and received data with each other and by counting the error bit in the serial received data stream.
An example of measured bit error rate characteristics is shown in Figure 2-6.

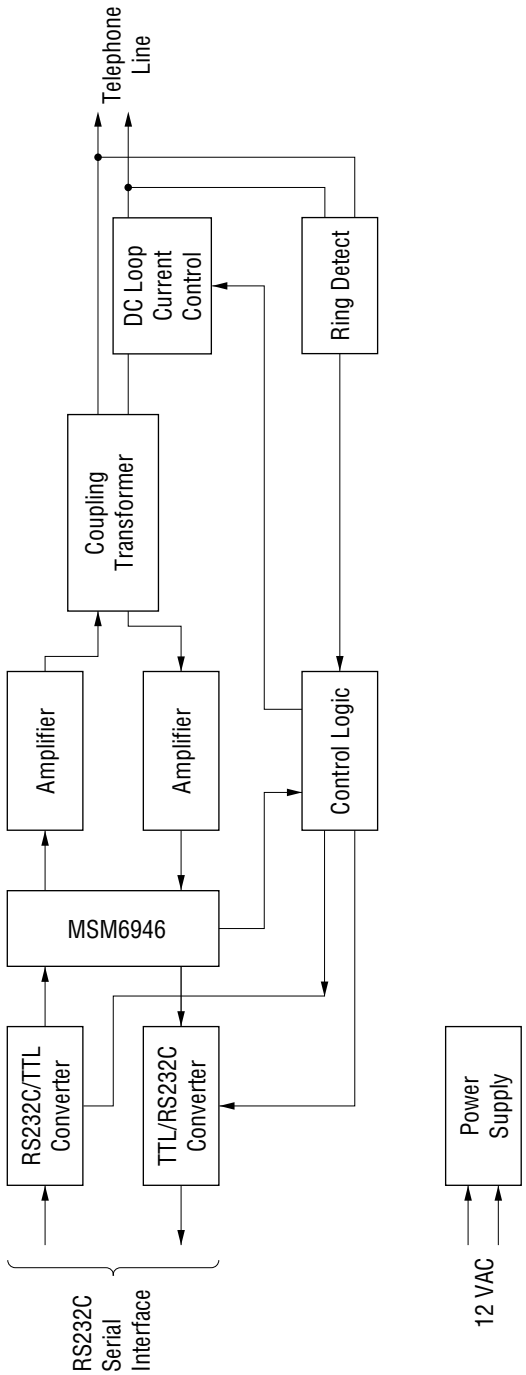


Figure 2-1 Block Diagram of Modem with Automatic Answer

Table 2-1 Parts Table for Figure 2-2

U_1	MSM6946RS	U_6	4N25	$V_{1,2}$	V39Z
U_2	LM747CN HA17458PS	U_7	RRD51A05 (D)	T	TAMURA SEISAKUSHO DP101
U_3	DS1488N SN75188 HD75188	U_8	MM74C74	Z_1 to Z_4	IN5242
U_4	DS1489N SN75189 HD75189	U_9, U_{11}	CD4538BC MSM4538RS	Z_5	IN5231
U_5	CD4049C MSM4049RS	U_{10}	MM74C08 MSM4081RS	CRYSTAL	KINSEKI HC-43/U

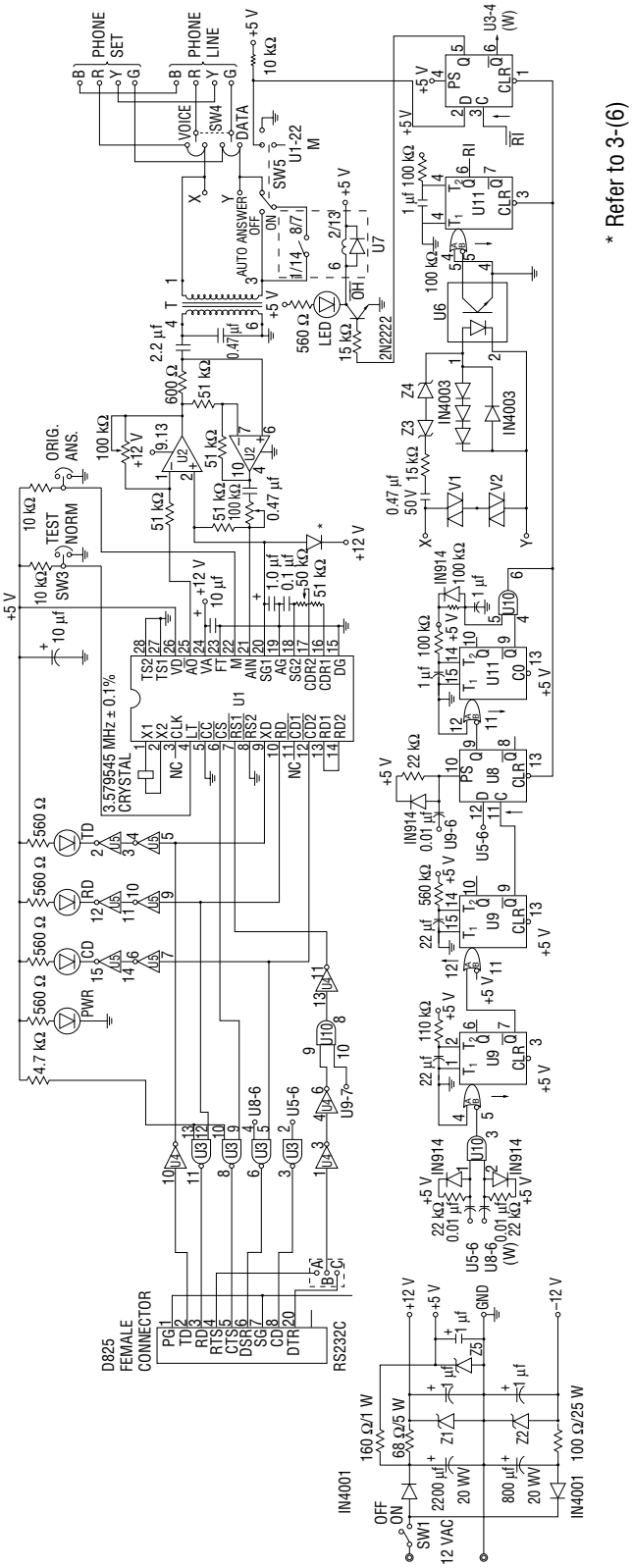


Figure 2-2 An Circuit Design Using Single-Chip Modem (with Automatic Answer)

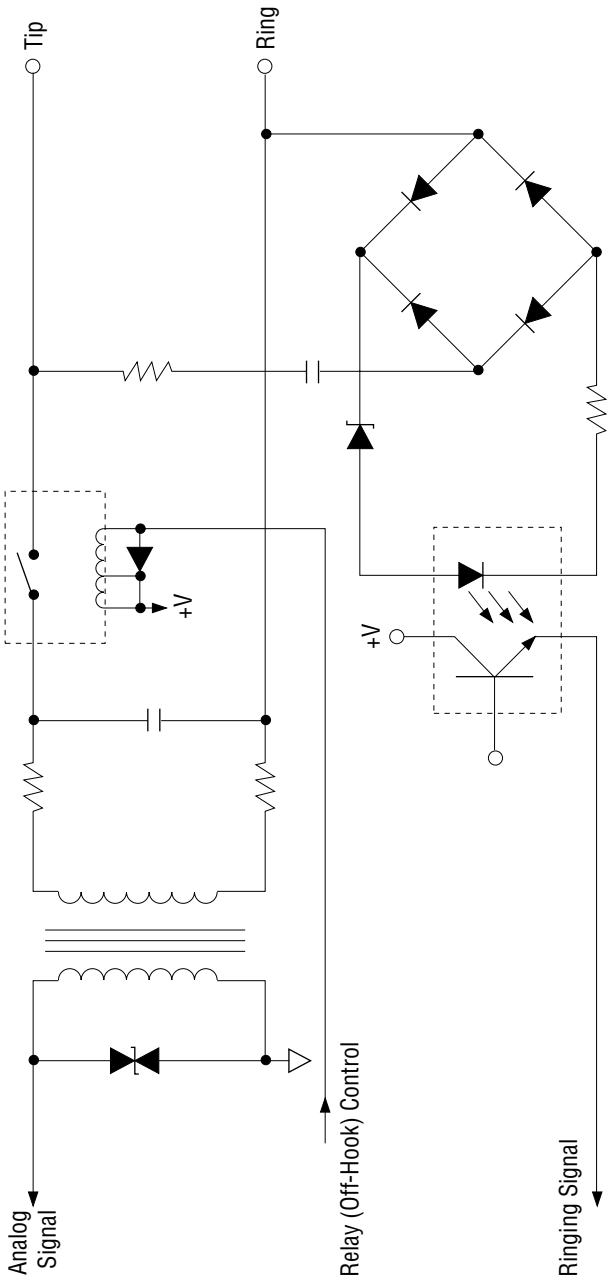


Figure 2-3 A Schematic Diagram of a Typical DAA

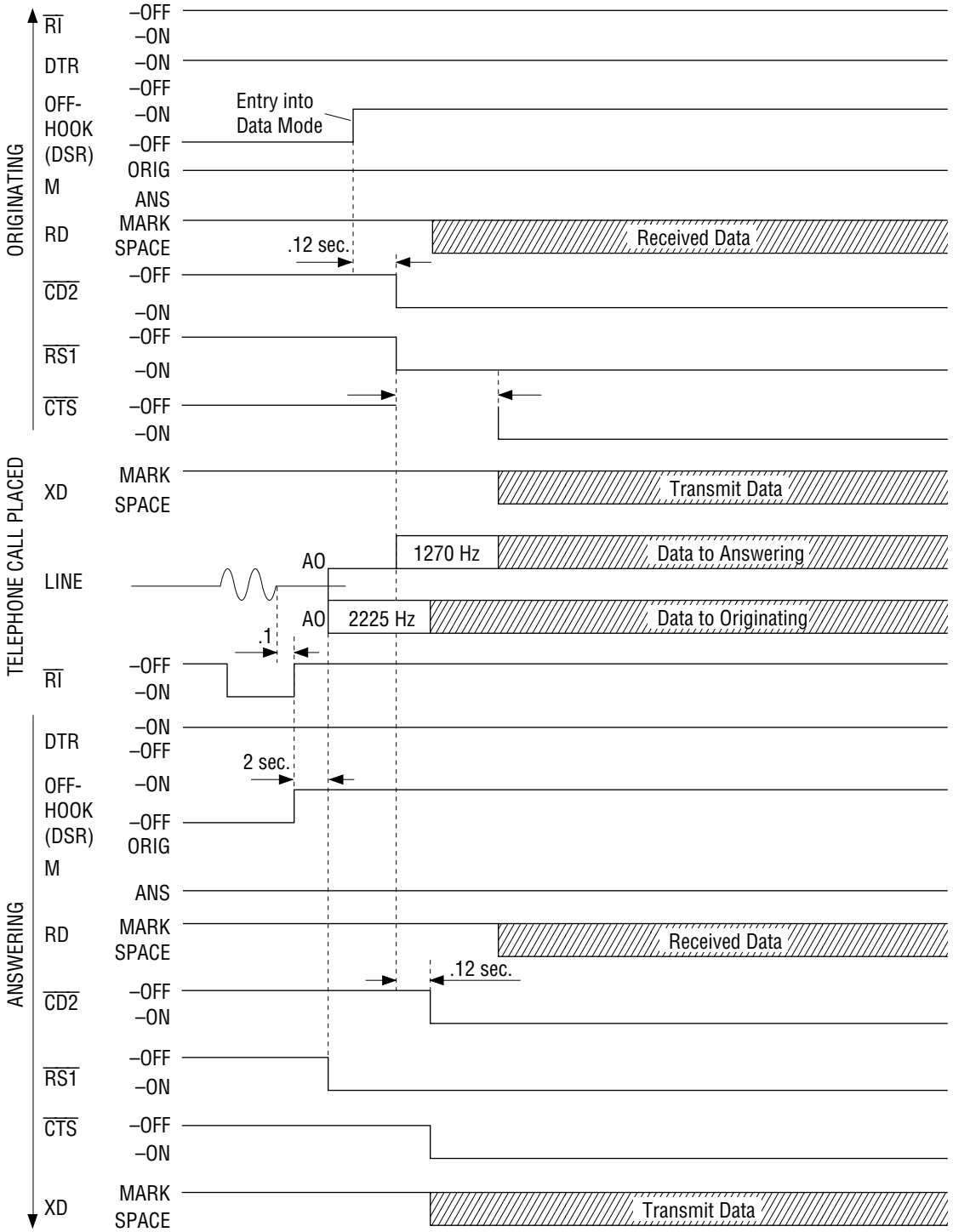


Figure 2-4 Call Establishment Sequence with Automatic Answer

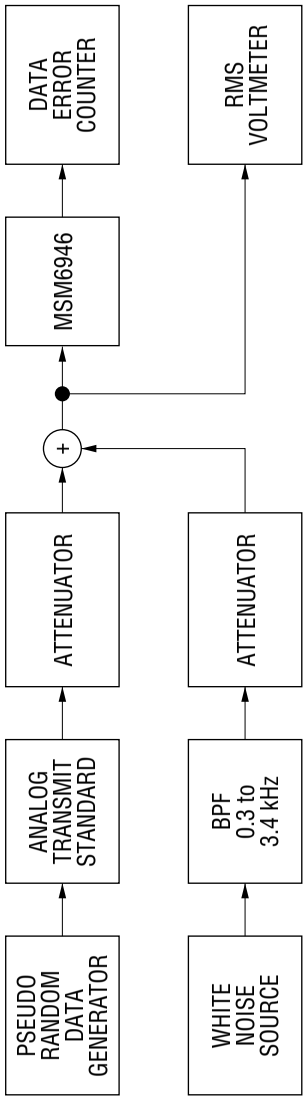


Figure 2-5 Modem Test Set

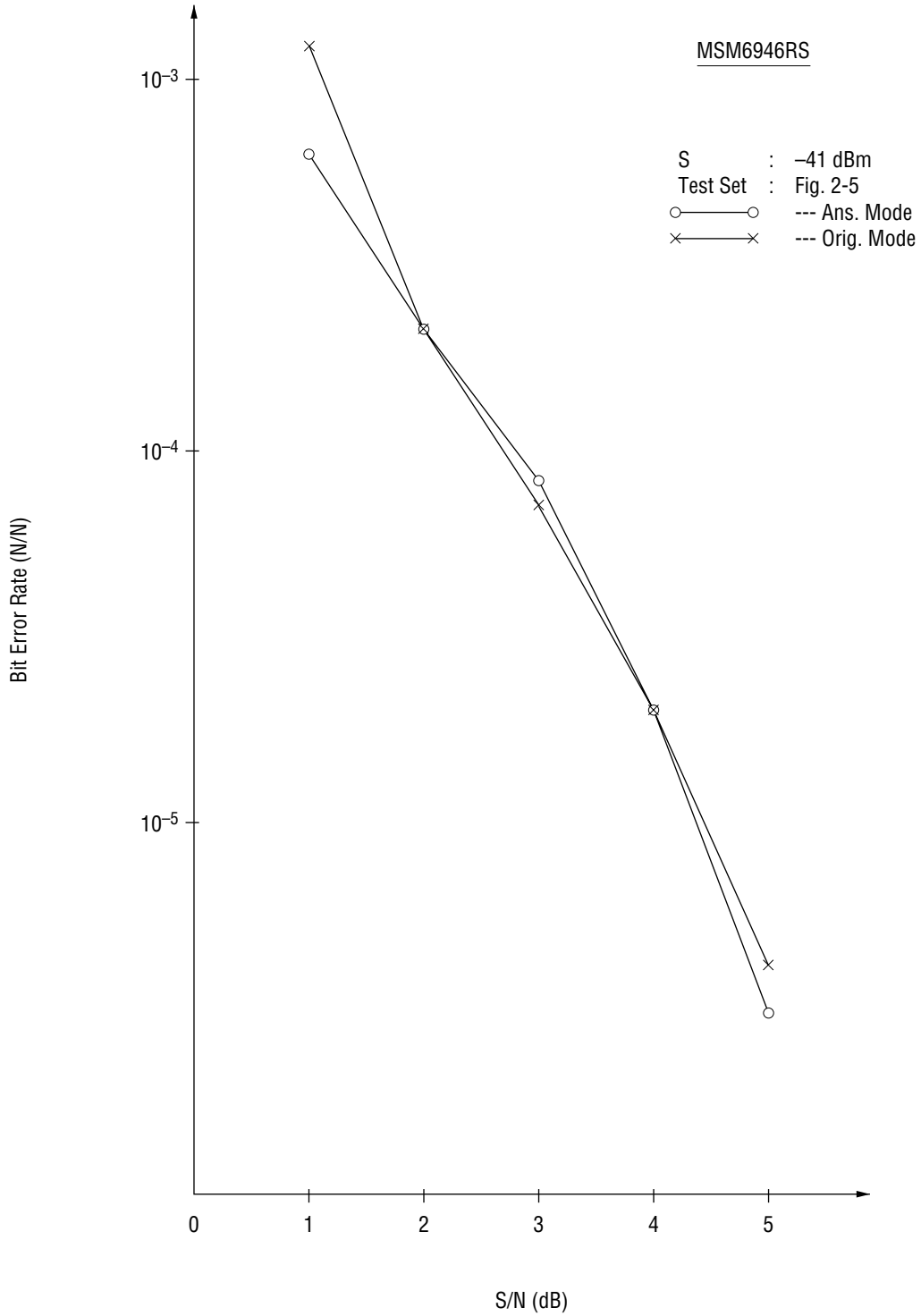


Figure 2-6 Measured Bit Error Rate Characteristics

APPENDIX

(Standard interface, and the control of modems used for public switched network)

Table 2-2 shows typical interface circuit for usual low speed asynchronous full-duplex modem. The clear-to-send signal is slightly different in meaning from modem to modem. In BELL 103, this signal means that a carrier signal from a remote modem is received; namely, that the transmission channel is in good working order. It is used synonymous with CD (carrier detect). On the other hand, when a half-duplex modem like a 1200 bps FSK modem is used on a public switched network at which the full-duplex communication is capable, the clear-to-send signal serves just as a delayed signal of the request-to-send.
In this case, the clear-to-send signal remains to be an indication that the data communication is likely to be capable. When applying a modem on a public switched network, interface circuits — data terminal ready (DTR) and ringing indicator (RI) — are necessary.
These two circuits plus carrier detect circuit (CD) are minimum requisites to the control of public switched network by a modem.
These functions will be well understood when compared with the operating sequence of a usual telephone.

Usual telephone		Low-speed asynchronous full-duplex modem
Ringing	⟷ (RI)	Ringing Indicator
Going off-hook	⟷ (DTR)	Data Terminal Ready ON
Response by far-end calling party	⟷ (CD)	Received Carrier Detect ON

The data terminal ready (DTR) shows a state that the modem is powered on, connected to the data transmission line, and is not in the test mode, and that it is ready to operate.
DTR is rarely used for asynchronous transmission in North America, but is used widely in Europe.

- Except from "Technical Aspects of Data Communication", written by John E. McNamara, the copyright is under Digital Equipment Corporation.

Table 2-2 Typical Interface Circuits for Low Speed Modem

Interface Circuit		Function	Symbol in Figure 2-2
EIA	ITU-T		
AA	101	Protective Ground	PG
AB	102	Signal Ground	SG
BA	103	Transmitted Data	TD
BB	104	Received DATA	RD
CA	105	Request to Send	RTS
CB	106	Clear to Send	CTS
CC	107	Data Set Ready	DSR
CD	108/1	Connect Data Set to Line	DTR
	108/2	Data Terminal Ready	
CF	109	Received Line Signal Detector	CD
CE	125	RING Indicator	RI

Note 1 : In the case of full-duplex modem used for public switched network, the request-to-send (RTS) circuit is usually unnecessary.

Note 2 : Unless otherwise specified by the Post, Telephone and Telegraph Authority (PTT), the low speed asynchronous modem interface is enough with either CD or CTS circuit, whichever is available.

Note 3 : Unless otherwise specified by the PTT, the modem interface with the minimum equipped functions need not to be provided with DSR circuit.

3. HINTS AND PRECAUTIONS ON USE

Unlike to general-purpose memories and logical gates, the single-chip modem LSI is hard to use. For example...

- Handling of analog quantity over a wide range of signal levels.
- Use of functions which defy standardization or common applications.
- Full use of the technology for switched capacitor whose characteristics are highly susceptible to deterioration due to power noise.

Accordingly, its use is accompanied by limitations and at the same time special know-how. These are explained hereunder, and additional information will be published in due course. Whenever designers look at an IC, most of them are too readily tempted to associate it with digital operations. As a result, they are liable to set its operating conditions in a rough manner. However, the LSI for this modem series has highly delicate functions which in the past have been implemented with discrete components or hybrid-ICs provided with adjust circuits or trimmers, and utmost attention should be paid to its using conditions so as to elicit its maximum performance.

1) Pin Connections for MSM6926/6946/6927/6947

The following shows the terminals with different functions.

Table 3-1 Different Pin Functions for 4-kind of Modem LSIs.

Device	Pin 22	Pin 27	Pin 28
MSM6926	M (Answer/Originate)	TS1 (Timer Selection)	TS2 (Timer Selection)
MSM6946			
MSM6927	$\overline{SQ}$ (2-Wire/4-Wire)		
MSM6947		TS (Timer Selection)	$\overline{ATE}$ (Answer Tone)

The operating conditions are assumed as follows.
- Use of internal timers.
- 2-Wire use (as in the public switched network)

In this case, the differences in connection between the devices are as follows.

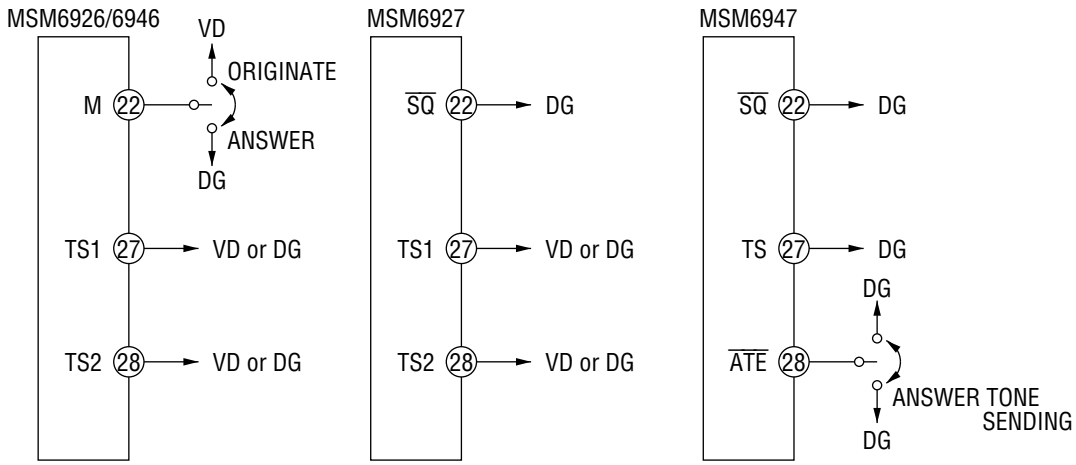
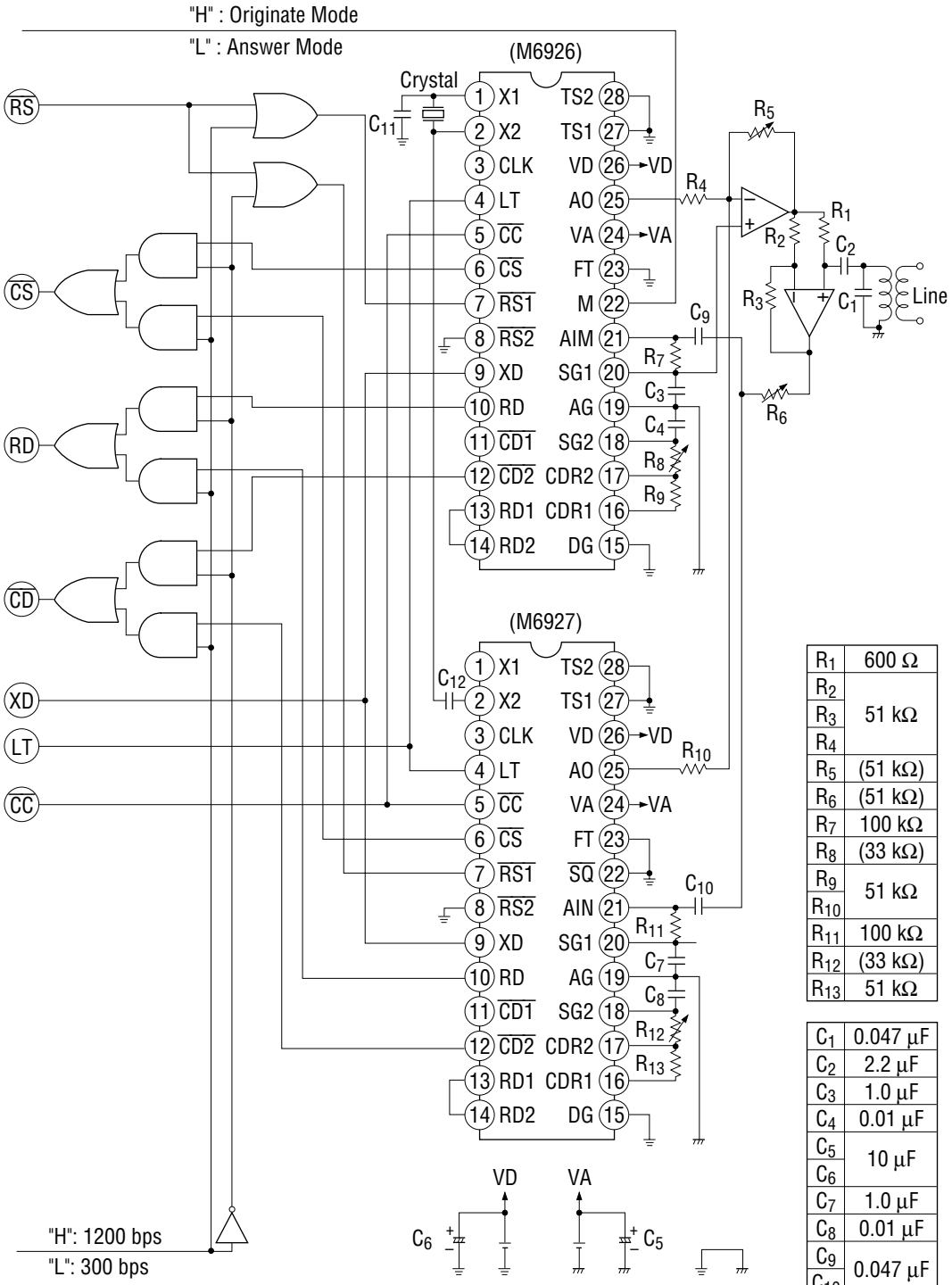


Figure 3-1 The Differences in Connection between the Devices

For other pins, the devices are used in the same manner.

2) MSM6926 and MSM6927 for 2-speed operation

Figure 3-2 introduces a circuit employing a 6926 and a 6927 for 2-speed operation.



R_1	600 Ω
R_2	51 kΩ
R_3	
R_4	
R_5	(51 kΩ)
R_6	(51 kΩ)
R_7	100 kΩ
R_8	(33 kΩ)
R_9	51 kΩ
R_{10}	
R_{11}	100 kΩ
R_{12}	(33 kΩ)
R_{13}	51 kΩ

C_1	0.047 µF
C_2	2.2 µF
C_3	1.0 µF
C_4	0.01 µF
C_5	10 µF
C_6	
C_7	1.0 µF
C_8	0.01 µF
C_9	0.047 µF
C_{10}	
C_{11}	10 pF
C_{12}	200 pF

Figure 3-2

3) Setting of the Carrier Detect Level

In a single-chip modem LSI, the receive carrier detect ON and OFF levels can be set within the range of –43 to –48 dBm by adjusting the ratio of the external resistors R_8 and R_9.

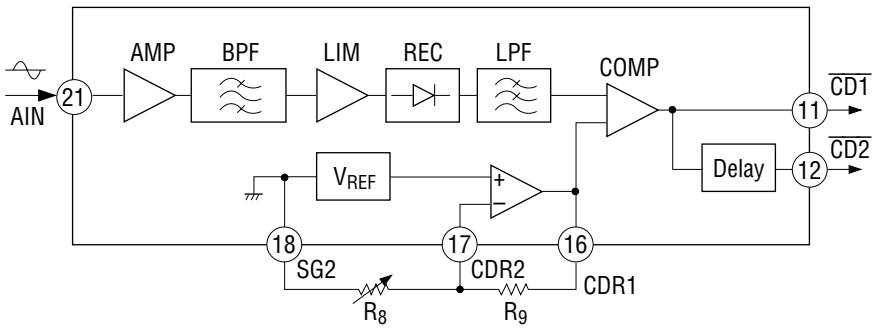


Figure 3-3

After adjustment, the voltage between Pin 16(CDR1) and Pin 18(SG2) will be about 3 V. Since the input signal level refers to LSI Pin 21 (AIN) of the LSI, it may have to be amplified when attenuated by a line transformer, etc.

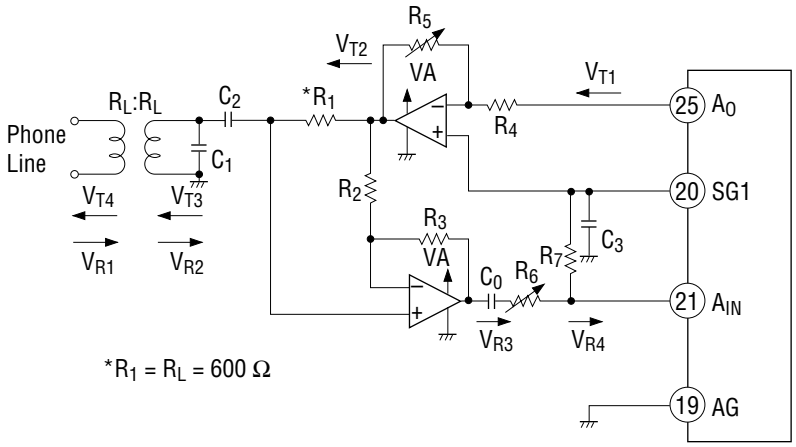
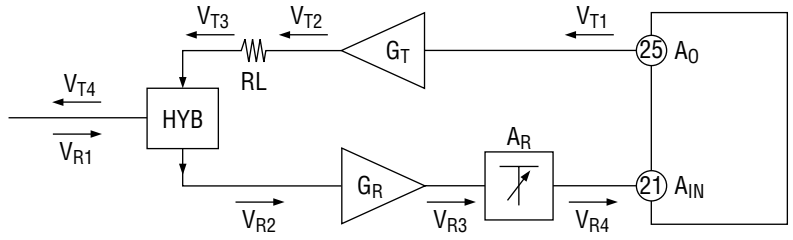


Figure 3-4

Figure 3-5 is a simplified drawing of Figure 3-4.



G_R	$1 + \frac{R_3}{R_2}$	2 ≡ +6 dB	Typical Design Values
A_R	$\frac{R_7}{R_6 + R_7}$	1/2 ≡ –6 dB	
G_T	$\frac{R_5}{R_4}$	1 ≡ 0 dB	

Figure 3-5

Accordingly, if the loss across the line transformer is 0 dB, the following equation applies;

$V_{R4} = V_{R1} \bullet G_R \bullet A_R = V_{R1}$
$V_{T4} = V_{T1} \bullet G_T \bullet 1/2 = V_{T1} - 6$ dB

If the maximum received signal level is –6 dBm, the level at AIN terminal is –6 dBm. The transmit level will be 0 dBm because it is attenuated by 6 dB by R_1 and the transformer impedance R_L (both 600 Ω).
If the line transformer produces a loss of 2 dB in both directions, it is required to reduce R_6 (from the typical value of 51 kΩ to about 30 kΩ) to compensate the received level at AIN.
Additionally in order to keep the transmit signal level at the typical value of 0 dBm, it is required to increase R_5 (from the typical value of 51 kΩ to approx. 64 kΩ).

Note:

$$20 \log \frac{R_7}{R_6' + R_7} = 20 \log \frac{51}{30 + 51} \simeq -4.0 \text{ dB} = (-6) + \underline{\underline{2 \text{ dB}}}$$

$$20 \log \frac{R_5'}{R_4} = 20 \log \frac{64}{51} = 2.0 \text{ dB} = (0) + \underline{\underline{2 \text{ dB}}}$$

If R_6 is fixed at the typical value of 51 kΩ, and if the line transformer causes a 2 dB loss, the received signal level of –6 to –48 dBm is shifted by 2 dB to –8 to –50 dBm at AIN terminal. It is therefore only required to lower the carrier detection level (by increasing R_8 from the typical value of 33 kΩ to 51 kΩ) by 2 dB.
In this case, the maximum received signal level at AIN is –8 dBm, and the carrier detect ON/OFF level is within the range of –45 to –50 dBm. This method, however is not recommendable because the S/N ratio will be slightly deteriorated. Anyway, operation is possible, although hysteresis width, etc. cannot be warranted. It should also be noted that the carrier detect ON delay time becomes longer and the OFF delay time shorter.

4) Transmission and Reception Timing

The operation timing is shown below.

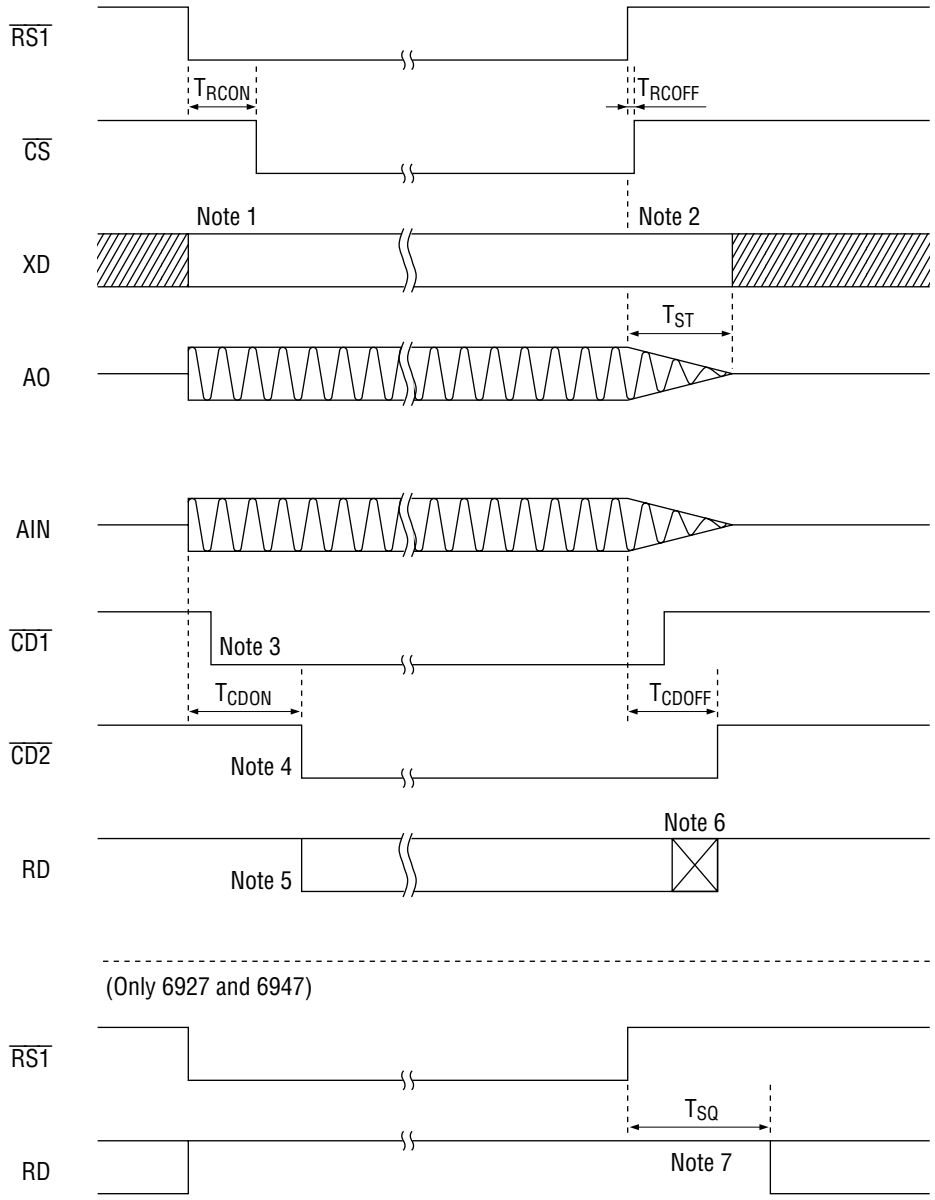


Figure 3-6 Timing Waveform

Note 1: From the time when $\overline{RS1}$ has become "L", a modulated waveform is generated at $\overline{AO}$ in accordance with "H" or "L" at XD.

Note 2: Even when $\overline{RS1}$ has attained "H", the modulated waveform maintains at $\overline{AO}$ during the soft turn-off period (T_{ST}) in accordance with "H" or "L" at XD, while its amplitude gradually attenuates.

Note 3: $\overline{CD1}$ is the terminal where the carrier detect signal is output without logical delay. The ON and OFF delay times at $\overline{CD1}$ change depending on the received signal level (AIN) and the differential voltage of the comparator in the detection circuit (VR=CDR1 terminal voltage—SG2 terminal voltage), etc. This is the reason for which the response characteristics of analog reception filter, limiter and carrier detector are significant factors. Typical characteristics are shown in Figure 3-7 through 3-10.

Note 4: $\overline{CD2}$ is the terminal where the output carrier detect signal is logically delayed by the internal delay circuit. The delay time provided by the internal delay circuit depends on the clock frequency, and is stable. Typical delay times are shown in Table 3-3. T_{CDON} and T_{CDOFF} values are indicated in Figure 3-7 through 3-10 and Table 3-3.

Note 5: When $\overline{CD2}$ is "H", RD is hold at "H" level (Mark hold).

Note 6: When the input level decreases after $\overline{CD1}$ goes "H' and the carrier detect circuit turned off, the demodulator will stop its operation.
During the period from the suspension of demodulation to the point of time when $\overline{CD2}$ becomes "H", the RD output becomes "H" in case of MSM6926, 6927 and 6947, and "L" in case of MSM6946 respectively.

Note 7: MSM6927 and MSM6947 has a built-in receive squelch delay timer, which is enabled by setting SQ terminal to "L". (It is used for the 2-Wire communication).
During transmission in the half-duplex mode ($\overline{RS1}$ = "L"), RD and $\overline{CD2}$ are fixed at "H", and even after $\overline{RS1}$ changes to "H". RD and $\overline{CD2}$ are kept at "H" during the squelch time (T_{SQ}) to avoid data errors in the demodulated data stream due to transient response at the time of sudden cut-off transmit signal. Table 3-4 shows the actual measurements.

Table 3-2 RS/CS Timing Measurement by Devices ($\overline{RS1} \rightarrow \overline{CS}$)

MSM6926

TS2	TS1	T_{RC} ON	T_{RC} OFF
0	0	402 ms	0.2 µs
0	1	30 ms	0.2 µs
1	0	350 ms	0.2 µs
1	1	External	External

MSM6927

TS2	TS1	T_{RC} ON	T_{RC} OFF
0	0	201 ms	0.3 µs
0	1	29 ms	0.3 µs
1	0	73 ms	0.2 µs
1	1	External	External

MSM6946

TS2	TS1	T_{RC} ON	T_{RC} OFF
0		198 ms	0.2 µs
1		External	External

MSM6947

TS	T_{RC} ON	T_{RC} OFF
0	180 ms	0.2 µs
1	External	External

Table 3-3 CD Timing Measurement by Devices ($\overline{CD1} \rightarrow \overline{CD2}$)

MSM6926

TS2	TS1	$\overline{CD2}$/ON	$\overline{CD2}$/OFF
0	0	301 ms	21 ms
0	1	4 ms	21 ms
1	0	152 ms	4 ms
1	1	External	External

MSM6927

TS2	TS1	$\overline{CD2}$/ON	$\overline{CD2}$/OFF
0	0	7.5 ms	5.2 ms
0	1	7.5 ms	5.2 ms
1	0	7.5 ms	5.2 ms
1	1	External	External

MSM6946

TS2	TS1	$\overline{CD2}$/ON	$\overline{CD2}$/OFF
0		102 ms	8 ms
1		External	External

MSM6947

TS	$\overline{CD2}$/ON	$\overline{CD2}$/OFF
0	14.5 ms	9.9 ms
1	External	External

Table 3-4 MSM6927/6947 Received Data Squelch Delay Timing Measurements

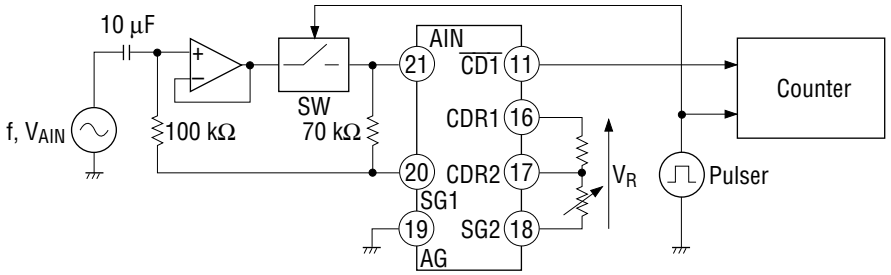
MSM6927

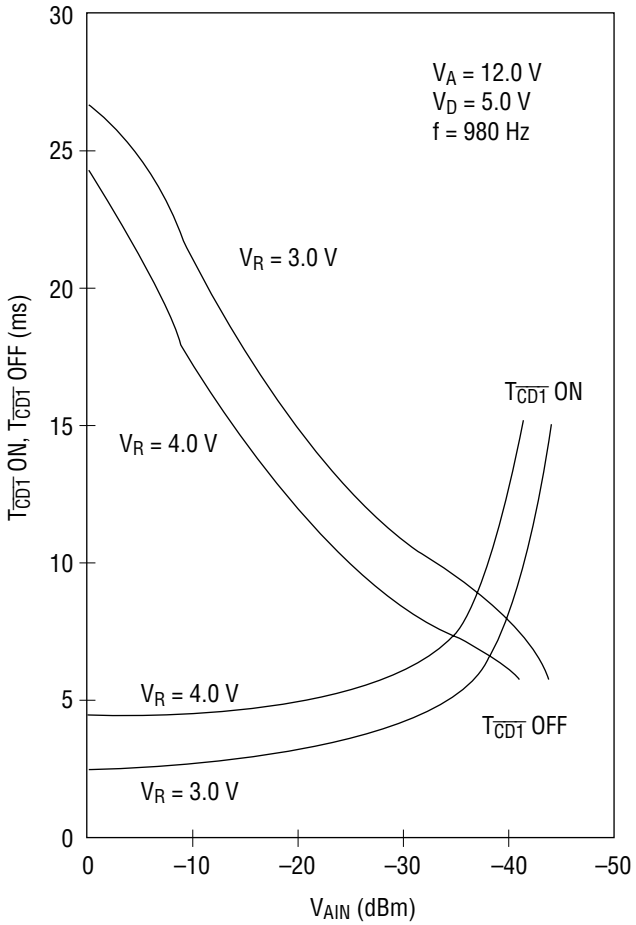
$\overline{SQ}$	TS2	TS1	TSQ
0	0	0	150 ms
0	0	1	150 ms
0	1	0	40 ms

MSM6947

$\overline{SQ}$	TS	TSQ
0	0	151 ms

Measuring Circuit





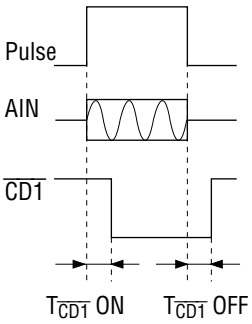


Figure 3-7 MSM6926 $\overline{\text{CD1}}$ Delay Time Characteristics

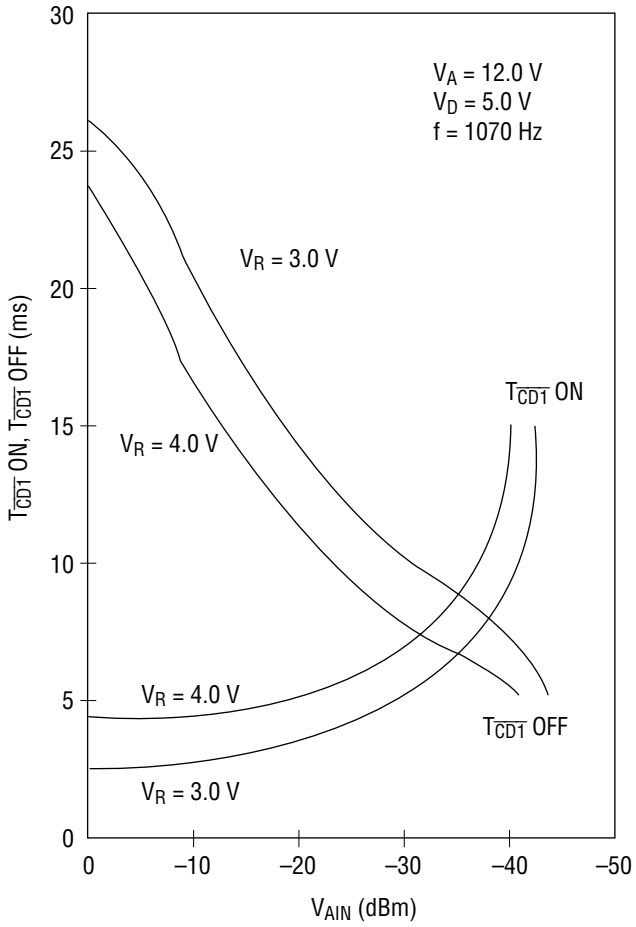


Figure 3-8 MSM6946 $\overline{CD1}$ Delay Time Characteristics

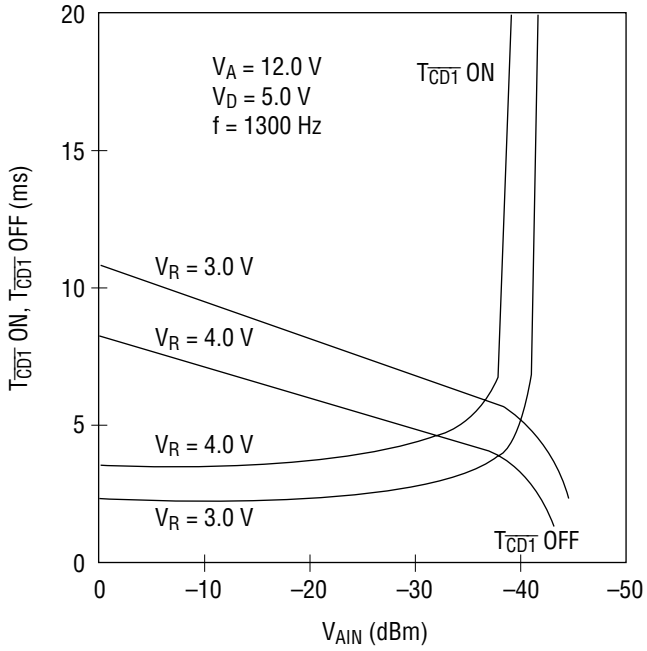


Figure 3-9 MSM6927 $\overline{CD1}$ Delay Time Characteristics

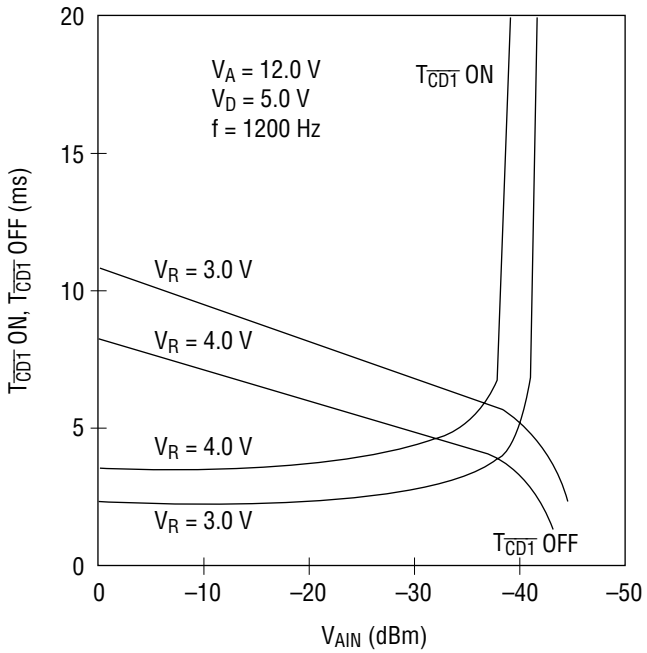


Figure 3-10 MSM6947 $\overline{CD1}$ Delay Time Characteristics

5) A Simple Configuration Example of External Timer

The external timers shown in the data sheet have many gates. For a simple configuration of a timer circuit, refer to Figures 3-11 and 3-12. When using MSM6926, 6946 or 6927, apply an "H" level to TS1 (Pin 27) and TS2 (Pin 28). When using MSM6947, apply an "H" level to TS (Pin 27). In this mode, external timer circuits can be added.

a) 300 bps (MSM6926/6946)

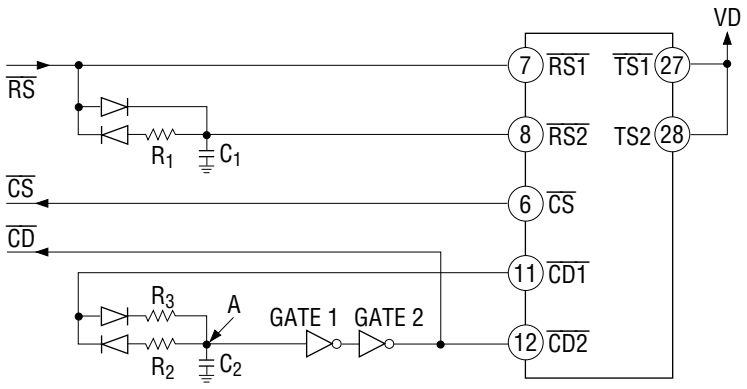
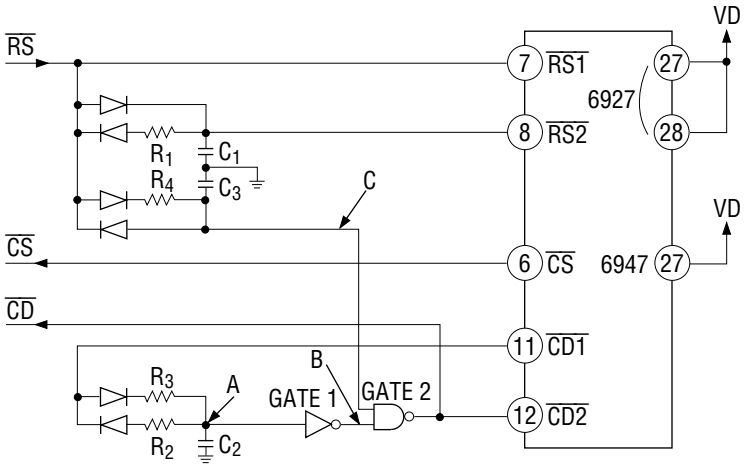


Figure 3-11

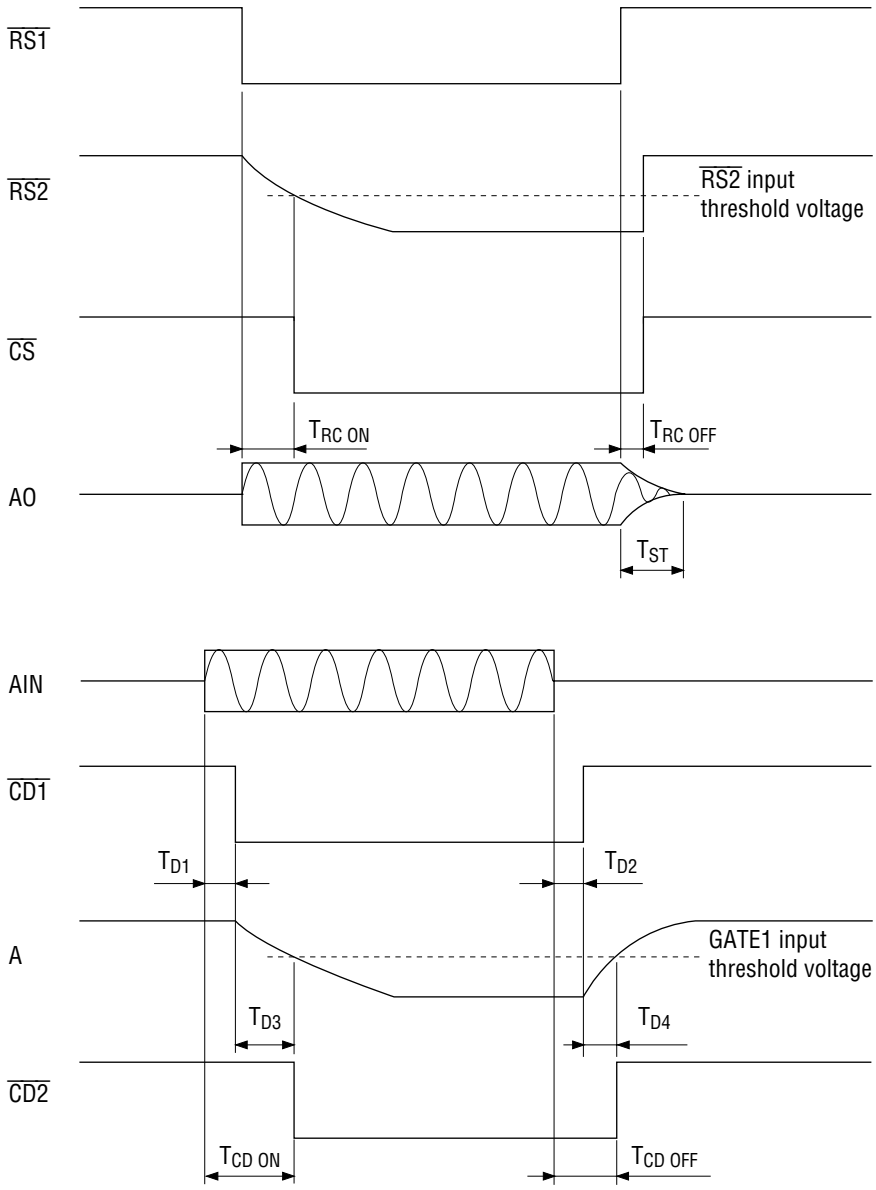
b) 1200 bps (MSM6927/6947) – 2-Wire circuit



Note: Same as (a) in case of 4-Wire circuit.

Figure 3-12

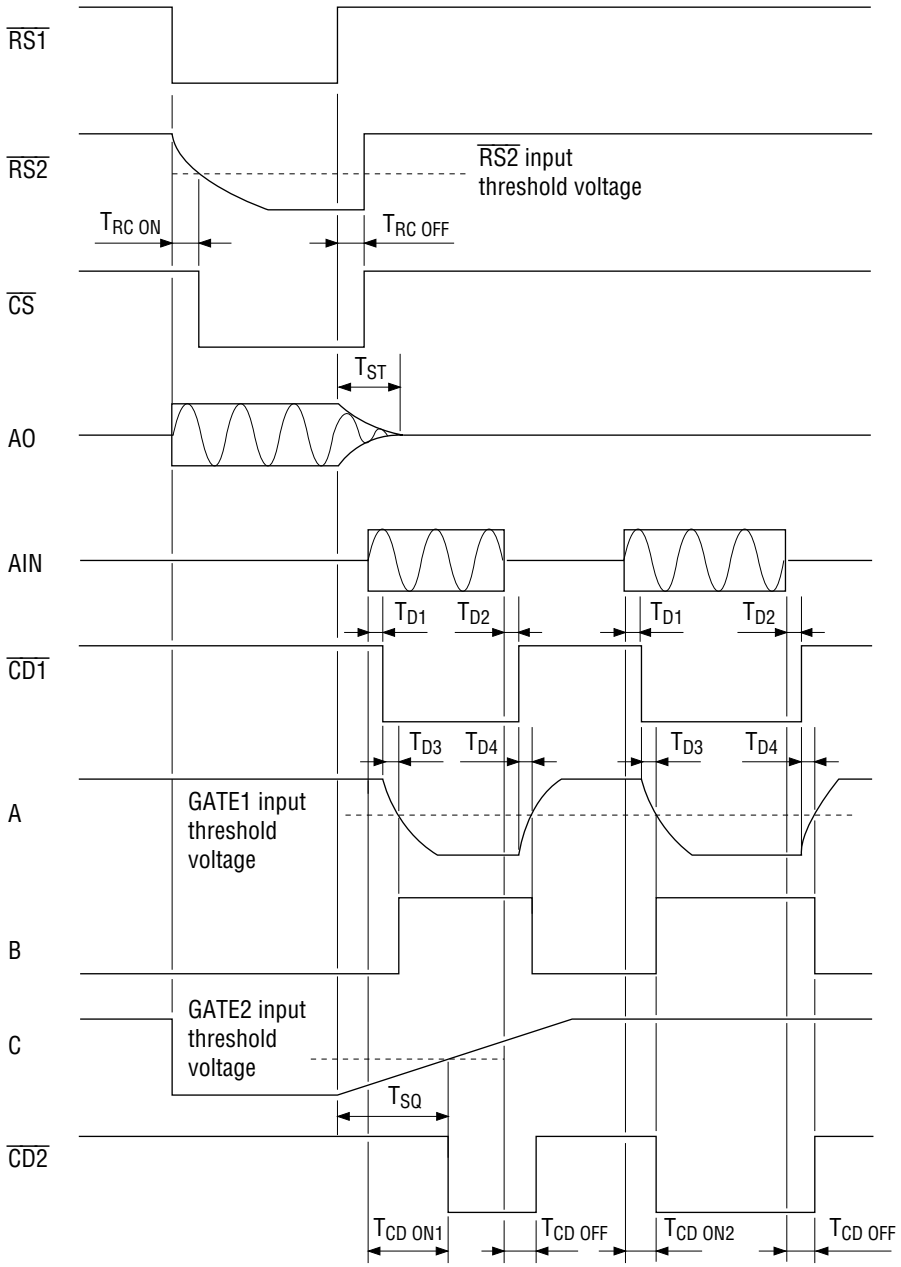
c) MSM6926/6946 timing diagram



Notes: 1. Transmission and reception are perfectly independent from each other.
2. $T_{RC\ ON} \propto R_1 \bullet C_1$, depends on $\overline{RS2}$ input threshold voltage.
$T_{RC\ OFF} \cong 0$
T_{D1}, T_{D2} : depend on the transient response of analog circuits such as reception filter, especially on the received signal level.
$T_{D3} \propto R_2 \bullet C_2$, $T_{D4} \propto R_3 \bullet C_2$, both depend on the threshold voltage at GATE1 input.
$T_{CD\ ON} = T_{D1} + T_{D3}$, $T_{CD\ OFF} = T_{D2} + T_{D4}$

Figure 3-13

d) MSM6927/6947 timing diagram (2-Wire facilities)



Note: $T_{RC\ ON} \propto R_1 \bullet C_1$, depends on $\overline{RS2}$ input threshold voltage.
$T_{RC\ OFF} \cong 0$
T_{D1}, T_{D2}, depend on the transient response of analog circuits such as reception filter, especially on the received signal level.
$T_{D3} \propto R_2 \bullet C_2$, $T_{D4} \propto R_3 \bullet C_2$, both depend on GATE1 input thresholde voltage.
$T_{SQ} \propto R_4 \bullet C_3$, depends on GATE2 input threshold voltage.
$T_{CD\ ON2} = T_{D1} + T_{D3}$, $T_{CD\ OFF} = T_{D2} + T_{D4}$

Figure 3-14

6) Circuit to Prevent Latch-up Due to Power Supply Noise

The LSIs for single chip modem series have a high immunity against latch-up, but are vulnerable against severe noise in the power supply.

Add a diode as illustrated in Figure 3-15.
For best protection, provide a zener diode (to 15 V) and a choke coil.

There is no restriction in whether to apply the 12 V source or 5 V source first.

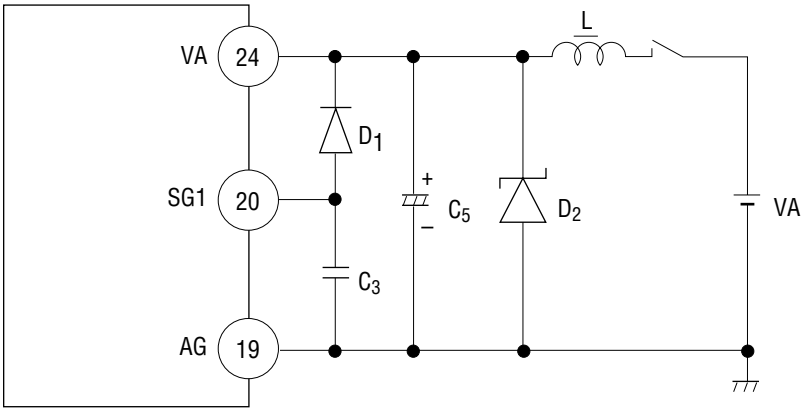


Figure 3-15

7) How to Apply Clock Pulses

a) Clock circuit when two one-chip modems are used

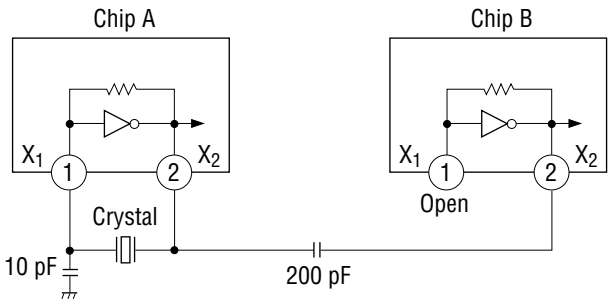


Figure 3-16

b) How to use an external clock circuit

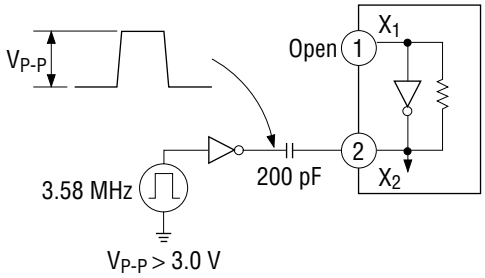


Figure 3-17

8) Line Equalization Circuit for 1200 bps FSK Modem

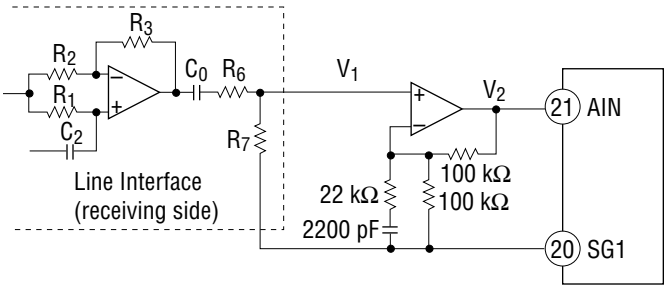


Figure 3-18 An Example of Line Equalization Circuit

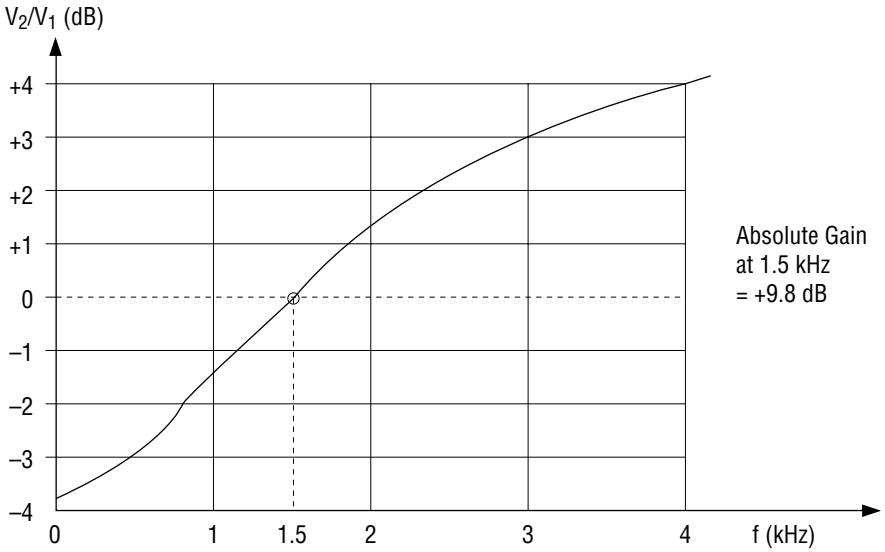


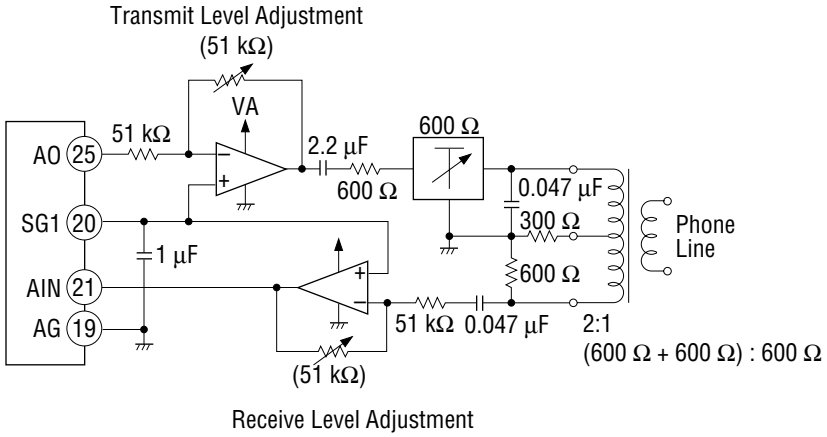
Figure 3-19 Frequency Characteristics of Line Equalization Circuit

The line equalization circuit shown in Figure 3-18 has a gain of +9.8 dB at 1.5 kHz. The input level at AIN terminal is adjusted by varying R_6 and R_7, which have a typical value of 51 kΩ. R_6 is set at 91 kΩ, and R_7 at 15 kΩ respectively. $(R_7/R_6 + R_7) \cong 1/7)$

This line equalization circuit can also be used on the transmitting side, but its frequency characteristics should be selected case by case.

9) Circuit Interfacing Using a Variable Analog Attenuator

a) In case of hybrid transformer



Notes: 1. AIN signal level should not exceed –6 dBm.
2. The value of resistors and capacitors are recommended values.

Figure 3-20 Circuit Using an Attenuator (No. 1)

b) In case of a line transformer plus hybrid circuit consisting of resistors and OP amps

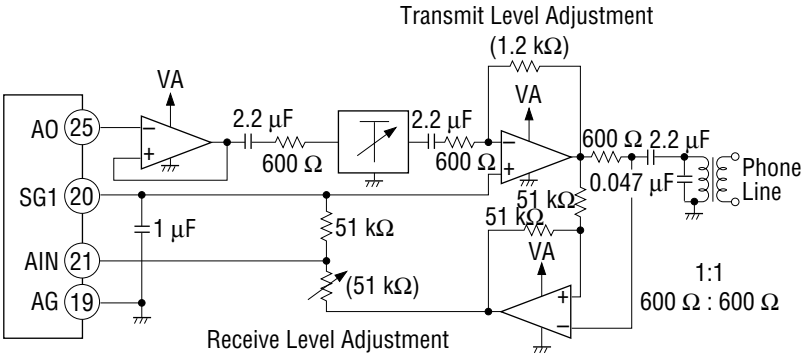


Figure 3-21 Circuit Using an Attenuator (No. 2)

c) 1200 bps 2-wire half-duplex communication

In this case, transmission and reception are not carried out simultaneously, the circuit becomes simpler than that compared with a) and b).

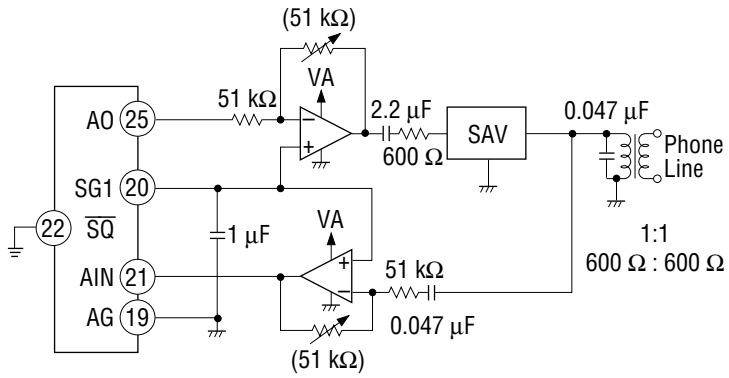


Figure 3-22 Circuit Using an Attenuator (No. 3)

In 2-Wire operation, $\overline{SQ}$ (Pin 22) is set to digital "L".
Under this condition, when sending the transmission carrier ($\overline{RS1}$ = digital "0"), the carrier detection is disabled and the received data is held in the "mark" state, independent of the signal entering AIN (received analog signal input).

Reference

In the half-duplex operation, the preceding hybrid circuit is unnecessary. The circuit using a variable analog attenuator has been shown in Figure 3-22, and a circuit without an attenuator is shown in Figure 3-23.

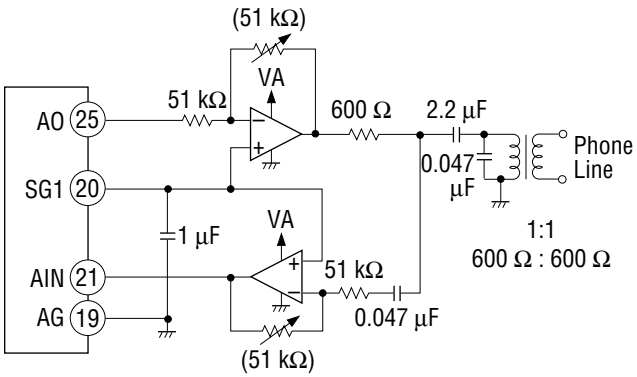


Figure 3-23 Line Interface Circuit for Half-Duplex Operation

10) Deterioration of Characterisitcs Due to Power Supply Noise

If both power supplies and particularly the VA supply contain noise, degraded characteristics are as follows.

1 Narrowing in the range of received signal levels
2 Narrowing of the hysteresis width of the carrier detect level
3 Increased bit error rate

There are two major reasons for these phenomena.

a) The internal signal ground is provided as a VA/2 potential.

Accordingly, half of the noise amplitude V_N, superimposed on VA, appears on the signal ground, and IC internal analog signal processing is carried out with reference to SG1 (Pin 20) containing this $V_{N/2}$ noise.
Both the transmit and received signals are connected to the telephone line via a transformer. Usually, the transformer operates with reference to 0 V, which is equal to the potential of AG. Please refer to the circuit in Figure 3-24.

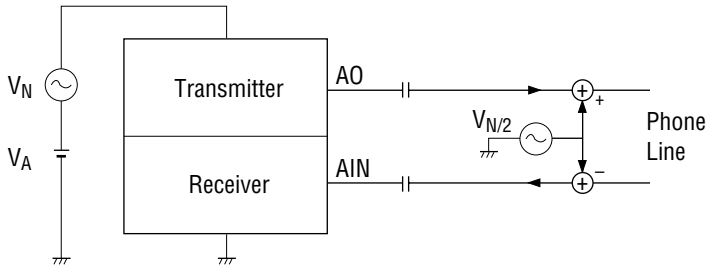


Figure 3-24 Equivalent Model Showing Noise, V_N in the Power Supply

b) Deterioration of characteristics due to crosstalk noise voltage from VA into the operational amplifier output, etc. via the power line of the operational amplifier and capacitor switches on the chip.

The problems do not only result in increase in noise level, but also the noise level in the voice band may be increased significantly because of the aliasing effect inherent in the switched capacitor method that plays a key role in the modem chip. The degree of deterioration in characteristics due to the combined appearance of noise and aliasing effect depends on the noise frequency, as demonstrated by the frequency characteristics in Figure 3-25 measured on MSM6926. In Figure 3-25, a sinusoidal noise voltage was superimposed on VA, and its levels (V_{P-P}) at which erroneous operations came up were measured and plotted. At around 1.5 kHz to 2 kHz deterioration occurred, because that noise frequency band interfaces with the received carrier frequency band. The modem chip uses 56 kHz as a sampling clock signal for the switched capacitor filter, and it is found that the aliasing effect makes it liable for the erroneous operations caused with respect to the superimposed signals represented by nearly all multiples of the clock frequency.

It is therefore necessary to minimize VA noise through a bypass capacitor, etc. Noise superimposed on the digital circuit power supply, V_D (+5 V), does not lead directly to this kind of deterioration. In the modem chip, however, analog and digital circuits are resident together, and noise on V_D may enter into the analog circuit via the reverse bias junction.

Accordingly, it is also important to reduce the noise level at V_D.

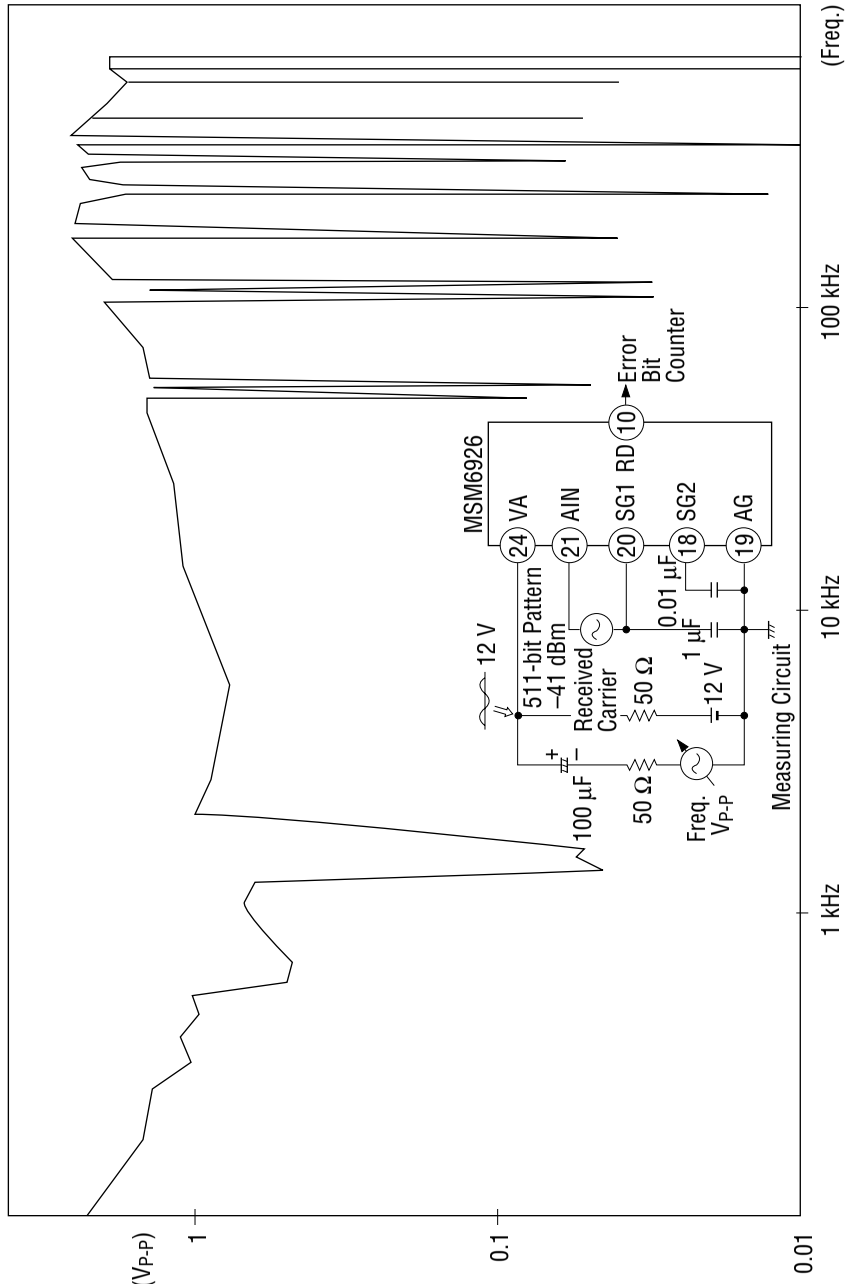


Figure 3-25 Frequency Characteristics of Power Supply Noise Level Responsible for Erroneous Operations

11) Tone Dialer Connection Circuit

Connect the tone dialer MK5089 (Mostek), MSM6234 (OKI), etc. as illustrated in Figure 3-26.

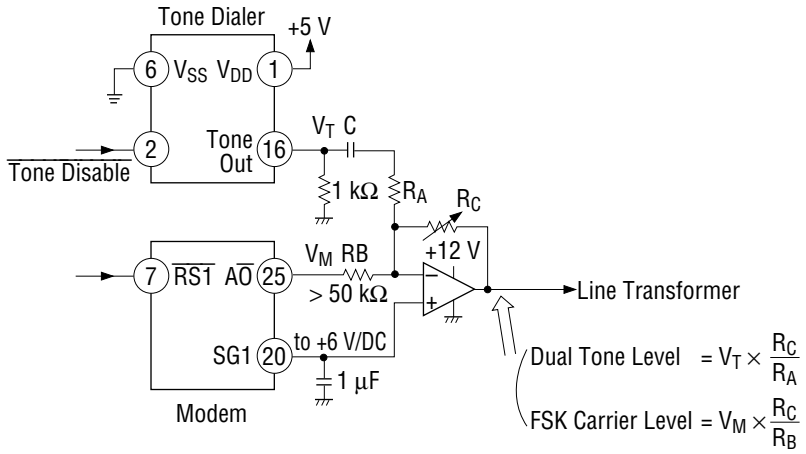


Figure 3-26 Tone Dialer Connection Circuit

The operational amplifier operates with SG1 potential (approx. +6 V) as a signal ground, therefore requires an AC coupling. If out-of-voice band noise in the tone dialer output is so serious as to require its elimination, a circuit as illustrated in Figure 3-27 works effectively.

C_T must be selected to obtain a proper time constant.

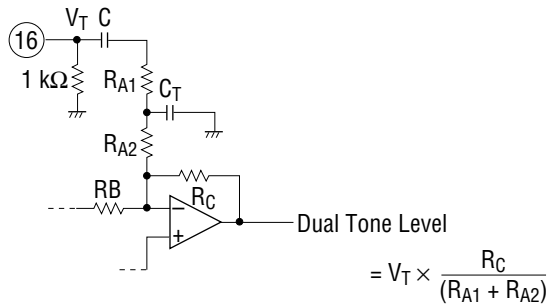


Figure 3-27 Circuit for Eliminating Noise Outside of Dual Tone Band

12) Considerations for Duplexer (Line Hybrid Circuit)

In case of full-duplex systems, a duplexer plays an important role. Its purpose is to help reject transmit signal energy from the receive signal.

Theoretically, a duplexer can be adjusted to achieve infinite rejection (no existence of cross-talk) – where the phase and amplitude of the inverting and non-inverting signals cancel through the duplexer OP-Amps. In practice, however, telephone line impedances vary enough such that only about 10 to 15 dB of rejection can be expected. To attain this rejection, it is recommended that the duplexer components (R_1, R_2, R_3 and C_1 in Figure 3-28) be tuned for the impedance and loss characteristics of the particular type of transformer being used.
This will minimize the impedance variation of the line.

Once these component values have been determined for a particular transformer type, further trimming is usally unnecessary on a board-to-board basis. A recommended procedure for balancing the duplexer which was used in finding the values in Figure 3-28, is as follows.

a) A recommended procedure for balancing the duplexer

(1) First, put the $\overline{RSI}$ input to VD (transmit squelch). Next, connect a 600 Ω signal source to points A and B (in case of MSM6926, 0 dBm and 980 Hz.) Tune R_1 until the loss at point A and B is exactly 6 dB. This allows maximum power transfer through the transformer.

(2) With R_1 at this new value, replace the signal source with a 600 Ω resistor at point A and B. Now output the transmit signal from A_0 (V_0) via OPA1 at the same frequency.

(3) Now tune R_3 until the signal out of A_0 reaches a minimum at OPA2 output terminal (V_2). Then tune C_1 until a new, lower minimum is reached which should be around 30 dB.

The phase and amplitude of the two signal components have now been matched for the best rejection over the spread of telephone line.

A crosstalk characteristic of the duplexer adjusted in steps (1) through (3) is shown in Figure 3-29. It was obtained by measuring the V_0-to-V_2 transfer characteristic with the modem chip and the duplexer disconnected from each other.

The duplexer has the attenuation pole at about 1420 Hz when a line impedance is ideal 600 Ω.

b) Characteristics on a practical line

Figure 3-29 also shows the practical characteristics of the duplexer connected to existing telephone lines.

These are represented by V_0-to-V_2 transfer characteristics; it should be noticed that the receive signal level at AIN terminal (V_3) will be lower than V_2 by about 6 dB typically because of the existence of R_6 and R_7.

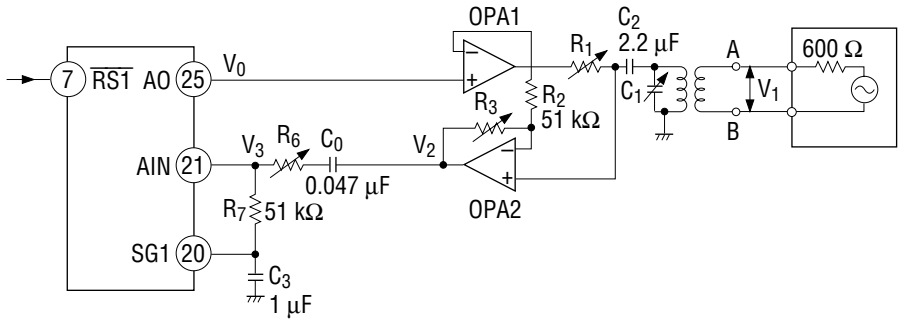


Figure 3-28 Duplexer (Line Hybrid Circuit) Considerations

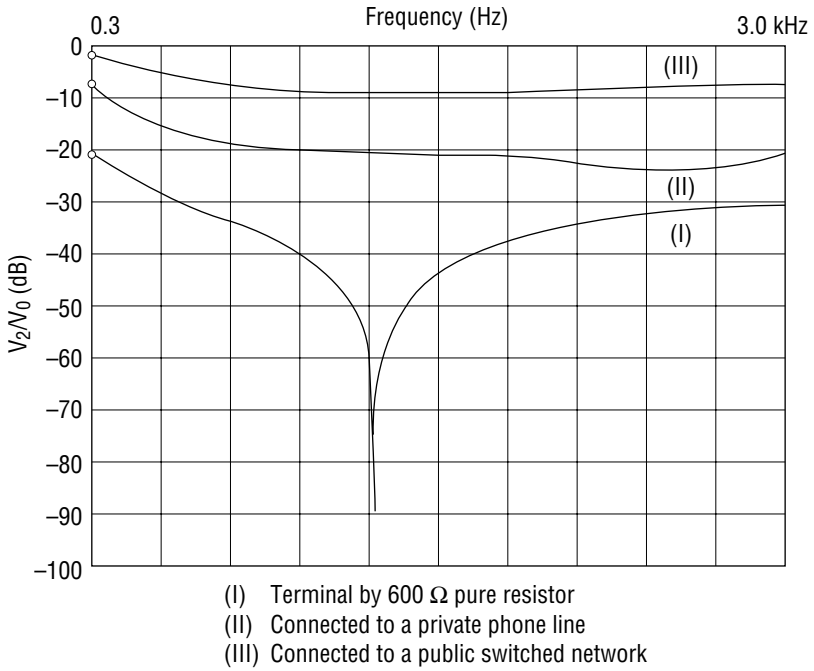


Figure 3-29 Experimental Cross-Talk Characteristics

c) Allowable crosstalk level

We investigated how the receiver characteristics would be affected by crosstalk. The measuring circuit used is shown in Figure 3-30, and the characteristics obtained are shown in Figures 3-31 and 3-32. For example, if MSM6946 (Bell 103) is to operate in originate mode (M = 1) with a bit error rate (BER) of 10^{-4} or less for a receive signal level of –43 dBm or greater, these figures argue that the crosstalk level should be held down below –3 dBm.

Next, it should be noticed that not only the AC signal crosstalk, but also the DC voltage on AIN terminal deteriorate the performance, becuase the DC voltage makes the receiver's dynamic range to be narrow.

This is the reason for which capacitor C_0 shown in Figure 3-28 is necessary. Capacitor C_0 prevents the DC offset voltage on A_0 from being conveyed to AIN terminal.

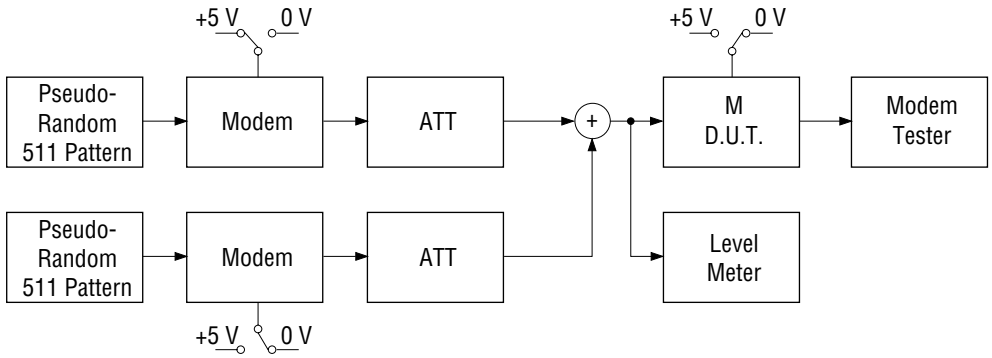


Figure 3-30 Test Set Examining the Influence of Cross-Talk

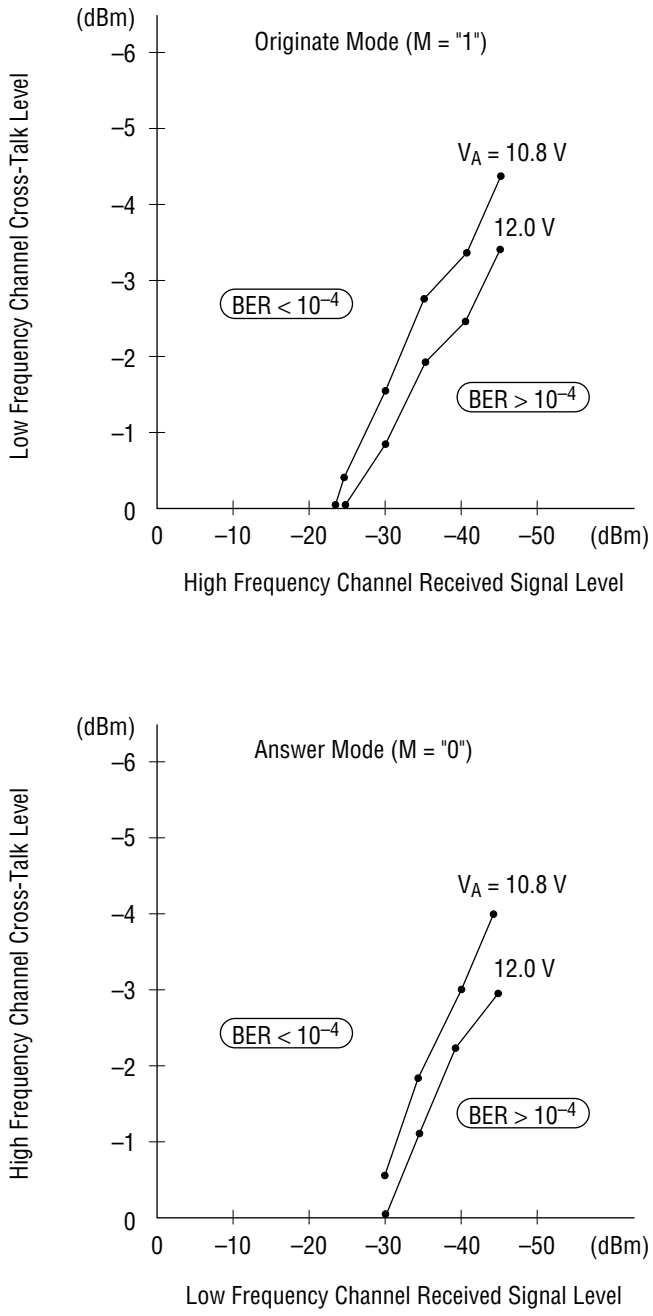


Figure 3-31 Deterioration of Bit Error Rate by Cross-Talk (MSM6926)

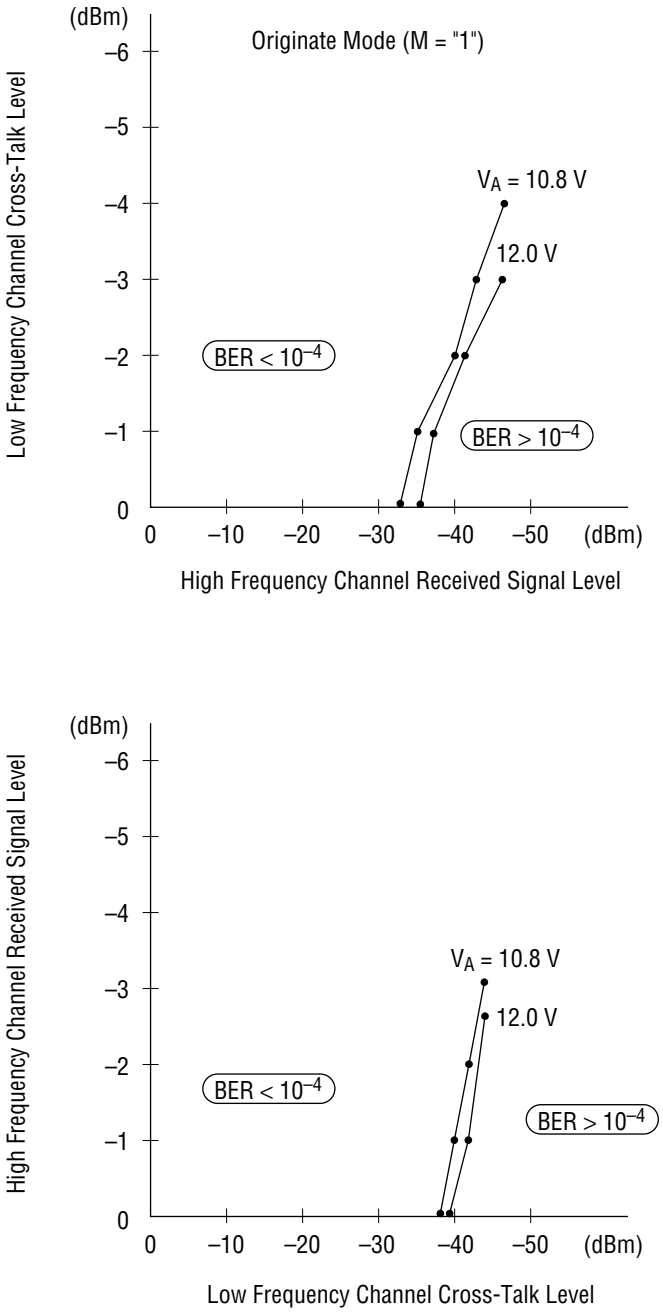


Figure 3-32 Deterioration of Bit Error Rate by Cross-Talk (MSM6946)

d) Consideration

(1) With reference to the circuit shown in Figure 3-28, if no transformer loss is present, the receive signal will be amplified twice (+6 dB) at the output of OPA2. Accordingly, it is reduced to a half (–6 dB) through R_6 and R_7 before input to AIN terminal. Assuming that the V_0-toV_2 transfer ratio is –8 dB (See Figure 3-29), the crosstalk level at AIN terminal is calculated as follows, because V_0 is +6 dBm.

+6 dBm*1 –8 dB*2 –6 dB*3 = –8 dBm*4

*1: tansmit level at A_0 terminal, V_0
*2: V_0-to-V_2 transfer ratio
*3: attenuation by R_6 and R_7
*4: crosstalk signal level at AIN terminal

According to Figure 3-32, it can be seen that the cross-talk of –8 dBm is not a problem for the system performance.

(2) In case a series resistance or other detrimental impedance in the telephone line causes a signal transmission loss through the transformer, the performance will be degraded as compared with the case discussed in (1) above.
For example, if a both-way transmission loss is 4 dB and V_0-to-V_2 transfer ratio remains to be –8 dB, the crosstalk level at AIN terminal is calculated as follows.

(+6 dBm + 4 dB*1) –8 dB –6 dB + 4 dB*2 = 0 dBm

*1: compensation for loss through transformer in the transmit direction (an additional gain of 4 dB to be given to OPA1)
*2: compensation for loss through transformer in the receive direction (loss through the R_6-R_7 attenuator to be reduced by 4 dB)

When MSM6946 (Bell 103) is operated in the high-frequency channel receiving mode (M = 1), Figure 3-32 tells that if the crosstalk level is 0 dBm, the bit error rate will run in excess of 10^{-4} unless the receive signal level is greater than –33 dBm.

(3) The greater the ratio of the transmit signal level to the maximum receive signal level is, the more will be aggravated the degradation of the system performance due to crosstalk.

4. CHECK POINTS FOR TROUBLE SHOOTINGS

1) Basic Examinations

- V pin 15, V pin 19 = 0 V
- V pin 24 = +12 V ±10%
- Are there any noise on pin 24? If the noise is not negligible; modem performances are easy to be deteriorated.
- V pin 26 = +5 V ±5%
- V pin 20 = 1/2 • (V pin 24)
  The load resistance connected to pin 20 must be more than 50 kΩ and any other voltage potentials must not input to this pin.
- V pin 18 = V pin 20 + 0.7
- V pin 16 = V pin 18 + 3.0
- VDC (pin 21) = V pin 20
- Any external components should not be connected to pin 1 and pin 2 except a 3.58 MHz crystal resonator.
- Pin 3 outputs a pulse train of which frequency is about 874 Hz.
- Pin 13 should be connected to pin 14.
- Pin 23 should be connected to digital "0" level.
- The analog transmit signal on pin 25 swings keeping its DC potential at about half of VA (pin 24). The load resistance connected to pin 25 must be more than 50 kΩ.
- The fun-out number of digital output pins are less than two.

Note: Checks should be performed with direct touching to pins.

2) Checks for Signal Transmiting

2-1. Common checks

- Pin 4 and Pin 7 should be connected to digital "0" level.
- Pin 6 outputs digital "0" level.
- Transmit data is input to the chip through pin 9 (XD).

2-2. MSM6926 and MSM6946

- Operating mode is determined using pin 22-originate or answer mode.
- Pin 27 and Pin 28 should be connected to digital "0" level.

2-3. MSM6927

- Pin 27 and Pin 28 should be connected to digital "0" level.

2-4. MSM6947

- Pin 27 should be connected to digital "0" level.
- Pin 28 should be connected to digital "1" level.

Signal transmiting ought to be performed after checks shown above if the chip is not out of order.

3) Checks for Signal Receiving

3-1. Common checks

- Pin 4 and Pin 7 should be connected to digital "0" level.
- The receive signal level should be within –6 and –43 dBm at the point of Pin 21 (AIN).
- Pin 11 and Pin 12 output the digital "0" state during the chip operates as a receiver.
- Pin 10, Pin 13 and Pin 14 show the same digital output data.

3-2. MSM6926 and MSM6946

- Confirm the carrier frequencies transmited through Pin 25 according to the operating modes.

3-3. MSM6927 and MSM6947

- Pin 7 should be connected to digital "1" level.
- Pin 22 should be connected to digital "0" level.
- Pin 22 ($\overline{SQ}$) is connected to digital "1" level when the operation on 4-wire facilities or the self test is required.

Signal receiving ought to be performed after checks shown above if the chip is not out of order.