OKI Semiconductor
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MSM7503

Multi-Function PCM CODEC

GENERAL DESCRIPTION

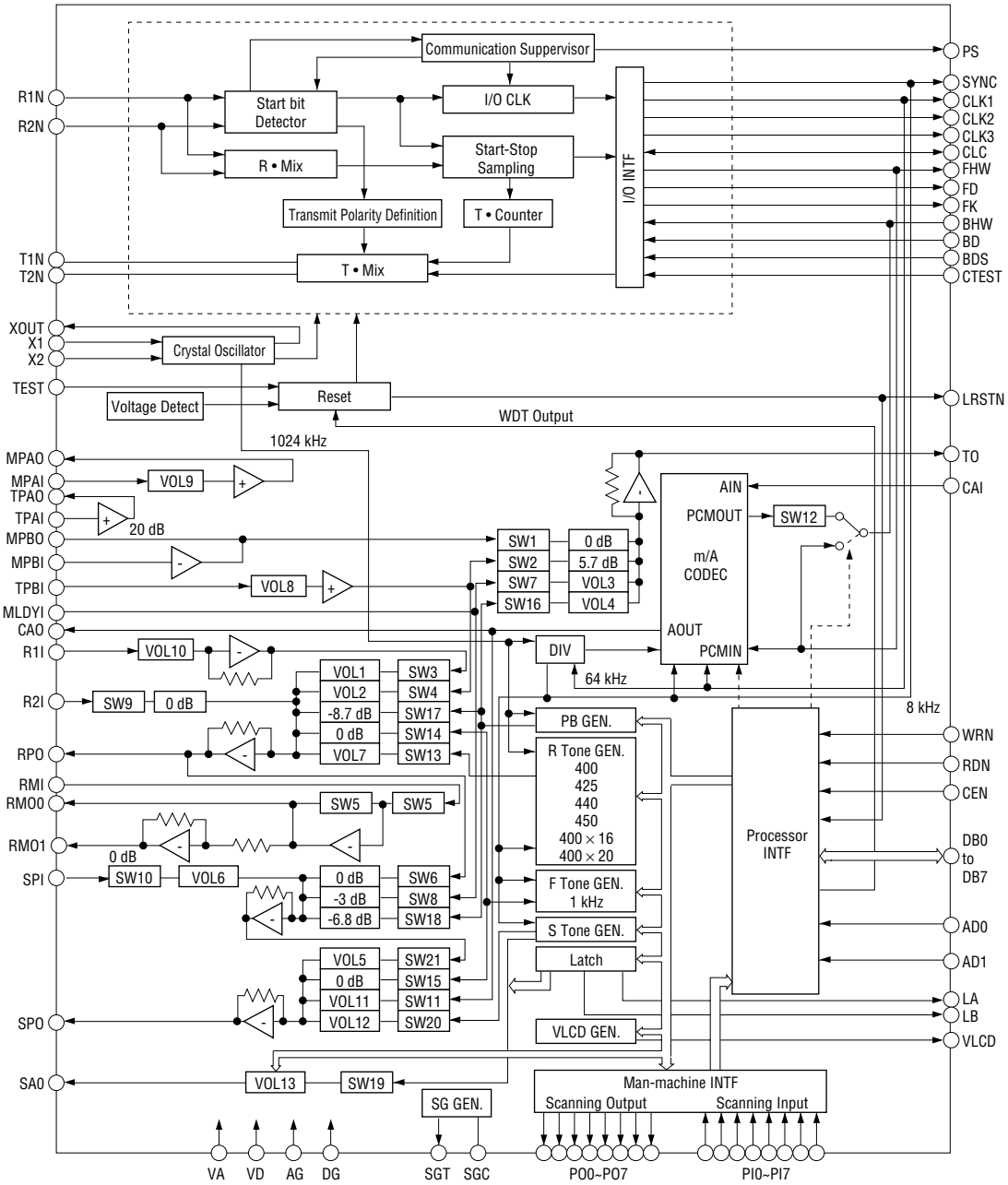
The MSM7503 is a high performance, low power CODEC LSI device integrating a 2-wire time division transmission (ping-pong transmission) interface function and has a basic function of man-machine interface to that of the MSM7502.
The MSM7503 operates from single 5 V power supply and is ideal for digital telephone terminals such as pushbutton telephone sets and digital PBXs.
The MSM7503 ping-pong transmission interface supports a bidirectional communication of up to 800 m long on the 2-wire twisted pair line, and can send and receive voice data at 64 kbps and control data at 16 kbps.
The man-machine interface consists of analog speech path, key-scanner, tone generators, CODEC meeting the μ/A companding law, and processor interface, which are controlled via 8-bit data buses.

FEATURES

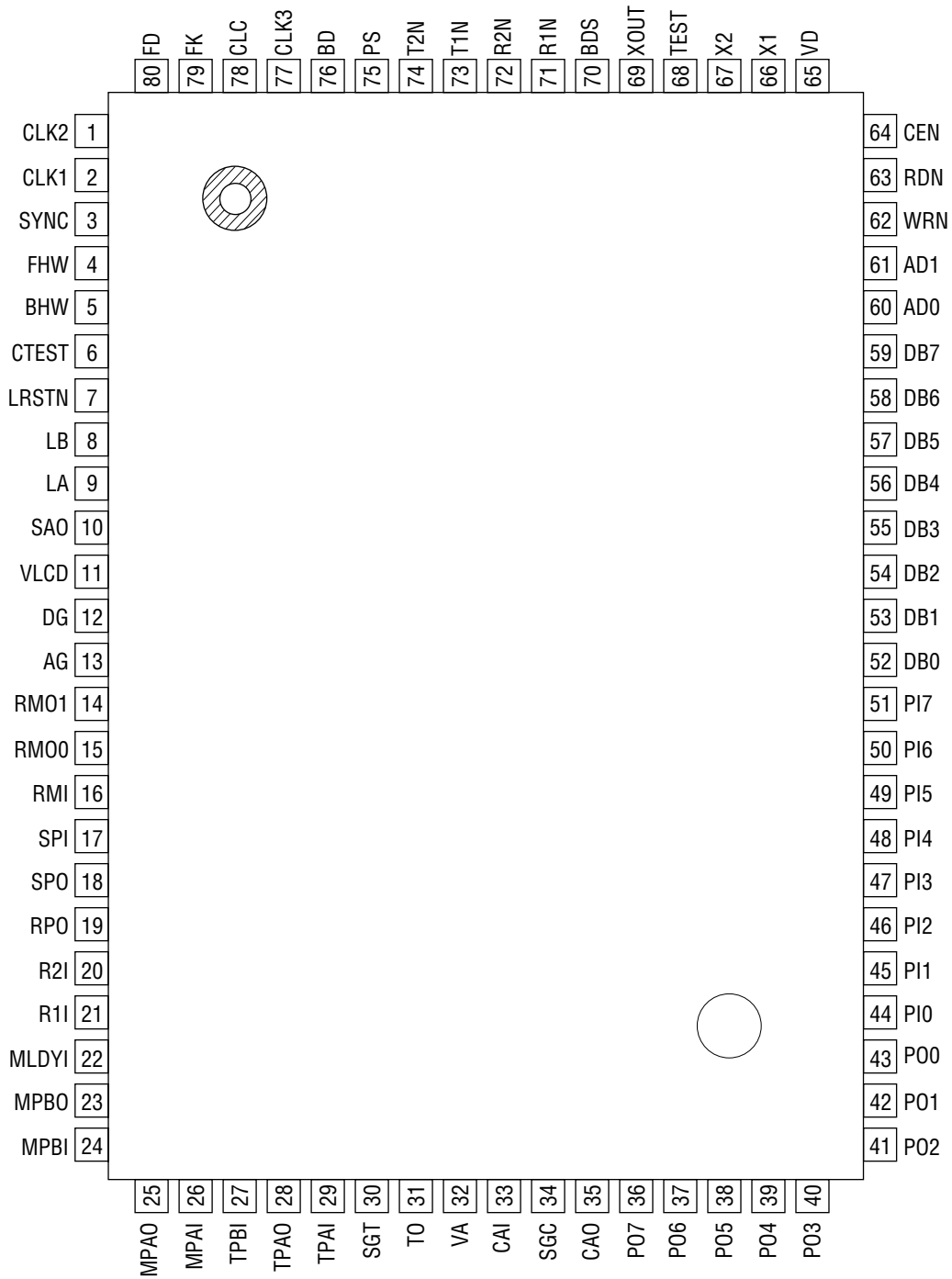
- Single +5 V Power Supply
- Low Power Dissipation
  - Power ON Mode : 50 mW Typ. 100 mW Max.
  - Power Down Mode : 15 mW Typ. 30 mW Max.
- Pin-Pong Transmission : Burst of 8 kHz, Transmission of 256 kbps, AMI coding, 2-wire time division transmission
- Transmission data configuration
  - : Transmit Start bit (1 bit), K-bit (1 bit), Control bit (2 bits), Voice bit (8 bits), DC balance bit (1 bit), totalling 13 bits
  - Receive Sync bit (4 bits), K-bit (1 bit), Control bit (2 bits), Voice bit (8 bits), DC balance bit (1 bit), totalling 16 bits
- Control Data Interface supports synchronous and asynchronous communications
- Built-in Power-on Reset by the power supply voltage monitoring
- Output of the ping-pong transmission monitoring signal
- CODEC complied by the ITU-T companding law
- Calling Tone Interval : Controlled by processor
- Calling Tone Combination : Controlled by processor, 6 modes
- Calling Tone Volume : Controlled by processor, 4 modes
- Ringing Tone Interval : Controlled by processor
- Ringing Tone Frequency : Controlled by processor, 6 modes
- Ringing Tone Level : Controlled by processor, 4 levels
- Built-in PB Tone Generator
- Built-in Speech path Control Switches
- General Latch Output for External Control : 2 bits
- Watch-dog Timer : 500 ms

- Scanning I/O
  - Output : 8 bits
  - Input : 8 bits
- Direct Connection to Handset : 1.2 kΩ driving available
- Built-in Pre-amplifier for Loud-speaker
- Hand-free Interface
- μ-law/A-law Switchable CODEC
- LCD Deflection Angle Voltage : Controlled by processor, 8 levels
- Package:
  80-pin plastic QFP (QFP80-P-1420-0.80-BK) (Product name : MSM7503GS-BK)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



80-Pin Plastic QFP

PIN AND FUNCTIONAL DESCRIPTIONS

LA, LB

General latch outputs for external control.
Statuses of these outputs are controlled via the processor interface. Refer to the description of the control data for details. These outputs provide the capability to drive one TTL.

DG

Digital Ground.
DG is separated from the analog ground AG inside the device. But, DG should be connected as close to the AG pin on PCB as possible.

AG

Analog Ground.

SA0

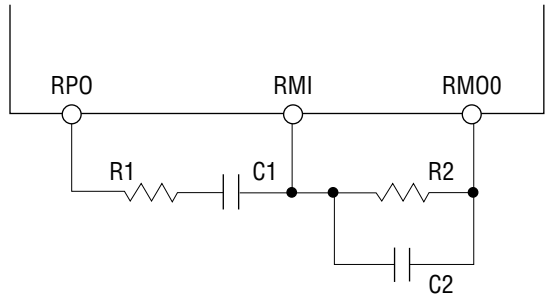
Sounder (calling tone) driving outputs.
Through processor control, the calling tone volume is selectable from 4 levels and one of six tone combinations is selectable. Initially, the calling tone volume is set at a maximum and the tone combination is set at a 16 Hz Wamble tone by a combination of 1 kHz and 1.3 kHz.
The SA0 outputs pulse waveforms using DG as a reference potential.

RMI, RMO0, RMO1

Receive main amplifier input and outputs.
RMI is the inverted input and RMO0 and RMO1 are the outputs of the receive main amplifier. The output signal on RMO1 is inverted against RMO0 by a gain 1 (0 dB), so the earphone of a handset is directly connected between RMO0 and RMO1. During the system power down, the RMO0 and RMO1 outputs are in a high impedance state. The receive main amplifier gain is determined by a resistor connected between RPO and RMI, and a resistor connected between RMI and RMO0. The receive main amplifier gain varies between 0 and +20 dB in effect. A piezo-receiver with an impedance greater than 1.2 kΩ is available.

If the adjusting of receive path frequency characteristics is required, insert the following circuit for adjustment. During the whole system Power ON, the speech path from RMI to RMO0 and RMO1 is disconnected and the output of RMO0 and RMO1 is at the SG level (VA/2). The speech path is provided by processor control.

A circuit example for adjustment of frequency characteristics



Main amplifier gain without capacitors

$$G = \frac{R2}{R1}$$

SPI

Addition input of speaker amplifier.
The typical gain between SPI and SPO is 0 dB. But, the 2-stage gain amplifier allows to set up a gain between 0 dB and –18 dB in a 6 dB step, or a gain between 0 dB and –28 dB in a 4 dB step through processor control. The input resistance of SPI is typically 20 kΩ to 150 kΩ (it varies by gain setting).

SPO

Output of pre-amplifier for speaker.
Since the driving capability is 2.4 V_{PP} for the load of 20 kΩ, SPO can not directly drive a speaker. During the whole system power down mode, SPO is at an analog ground level. During the whole system power on mode, SPO is in a non-signal state (SG level), and a receive voice signal, R-tone, F-tone, hold acknowledge tone, PB signal acknowledge tone, and sounder tone are output from the speaker by processor control.

When the speaker is used as a sounder, the sounder tone is output via the SPO pin by connecting the SPI input with the sounder output (SA0 or SA1). In addition, when the AD-converted sounder tone is sent from the main device, the sounder tone is output via the SPO pin since the CAO pin for CODEC output is internally connected.

R1I, R2I, RPO

R1I and R2I are for the inputs and RPO is for the output of the receive pre-amplifier.
Normally, R1I is connected via an AC-coupling capacitor to the CODEC analog output (CAO), and R2I is used as the mixing signal input pin.
The typical gain between R1I and PRO is –6 dB. Through processor control, gains are variable from –14 dB to 0 dB in 2 dB steps. In addition, the receive pad can control the gain of –9, –6, –3, or 0 dB. The gain between R2I and RPO is fixed to 0 dB.
During the whole system power-on mode, the RPO output is in non-signal state, and speech signal, R-tone, F-tone, PB acknowledge tone, side tone signal are output by processor control.
During the whole system power-down mode, the RPO output is the analog ground level.
The input resistance of R1I is typically between 20 kΩ and 100 kΩ (it varies by gain setting). The input resistance of R2I is typically 20 kΩ.

MLDYI

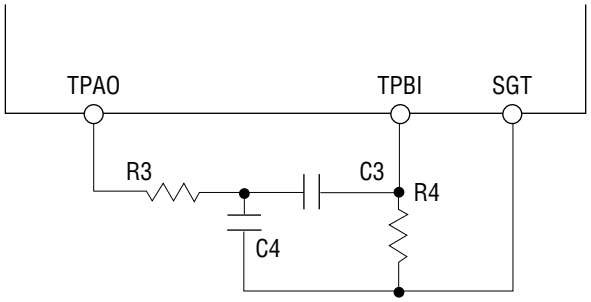
Hold tone signal input.
For example, the output of external melody IC is connected to this pin. Through processor control, the signal applied to MLDYI is output from the TO output pin as a hold tone on the transmit path, and from the SPO output pin as a hold acknowledge tone on the receive path. The typical gain between MLDYI and TO is –2 dB. Through processor control, a gain between –2 dB and –11 dB is also settable at 3 dB steps. The typical gain between MLDYI and SPO is –3 dB. Through processor control, a gain between –3 dB to –31 dB is also settable at 4 dB steps. MLDYI is a high impedance input, so insert an about 100 kΩ bias resistor between MLDYI and SGT.

TPBI, TO

TPBI is the input and TO is the output of the transmit pre-amplifier (B).
When the handset is used, TPBI is connected to the transmit pre-amplifier (A) output pin (TPAO). If adjustment of frequency characteristics on the transmit path is required, insert a circuit for adjustment of characteristic between TPAO and TPBI. Through processor control, the signal applied to this pin is output via the TO pin on the transmit path and its side tone via the RPO pin. During the whole system power down mode, TO is at an analog ground level. The typical gain between TPBI and TO is +17.7 dB. Through processor control, a gain between +17.7 dB and +8.7 dB is also settable at 3 dB steps.

The typical gain between TPBI and RPO is +3.0 dB. Through processor control, a gain between –9 dB and +9 dB is variable in 3 dB steps. Changing the gain between TPBI and TO may change the gain between TPBI and RPO. TPBI is a high impedance input, so insert an about 100 kΩ resistor between TPBI and SGT.

A circuit example for adjustment of frequency characteristics



MPAI, MPAO

Handfree microphone pre-amplifier (A) input and output.
MPAI is the input and MPAO is the output. The speech path between MPAI and MPAO is always active regardless of processor control. During the whole system power saving mode, MPAO is at an analog ground level. The gain between MPAI and MPAO is typically +20 dB. Through processor control, gains between +14 dB and +11 dB are also settable. MPAI is a high impedance input, so insert an about 100 kΩ between MPAI and SGT.

MPBI, MPBO

The handfree microphone (B) input and output.
MPBI is the inverted input and MPBO is the output. With an external resistor, the amplifier gain is adjusted in the range between –25 dB and +25 dB. A signal on the MPBO is output via the TO pin through processor control. During the whole system power down mode, MPBO is at an analog ground level. The gain between MPBO and TO is fixed to 0 dB.

TPAI, TPAO

The transmit pre-amplifier (A) input and output.
TPAI is the input and TPAO is the output. TPAI should be connected to the microphone of handset via an AC-coupling capacitor if the DC offset appears at a transmit signal (offset from SGT). The transmit path from TPAI to TPAO is always active regardless of processor control. During the whole system power down mode, TPAO is at an analog ground level. The gain between TPAI and TPAO is fixed to 20 dB.

SGT

Transmit path signal ground.
SGT outputs half the supply voltage. During the whole power down mode, SGT output is in a high impedance state.

SGC

Bypass capacitor connecting pin for a signal ground level.
Insert a 0.1 μF high performance capacitor between SGC and AG.

VA, VD

+5 V power supply.
VA is for an analog circuit and VD is for a digital circuit. Both VA and VD should be connected to the +5 V analog path of the system.

CAI, CAO

CODEC analog input and output.
CAI is the analog input of CODEC to be connected to the TO pin. If the DC offset voltage on the TO signal is great, CAI should be connected via AC-coupling capacitor. At this time, insert an about 100 kΩ bias resistor between CAI and SGT.

CAO is the analog output of CODEC. CAO should be connected to R1I via AC-coupling capacitor.
A bias resistor is not required to R1I. During the whole system or CODEC power down mode, CAO is at the SG voltage level.

PO0, PO1, PO2, PO3, PO4, PO5, PO6, PO7

Scanning outputs.
These output pins need external pull-up resistors because of their open- drain circuits. But, when these are used in combination with PI0 to PI7, pull-up resistors are not required. Through processor control, these outputs can be set open or to digital "0". Initially, these outputs are set at an opened state.

PI0, PI1, PI2, PI3, PI4, PI5, PI6, PI7

Scanning inputs. In the READ mode, data on PI0 to PI7 can be read out of the processor via data bus (DB0 to DB7).
Since these inputs are pulled up inside the IC, external resistors are not required.

DB0, DB1, DB2, DB3, DB4, DB5, DB6, DB7

Data bus I/O pins.
These pins are configured as an output during the READ mode only and as an input during other modes.

T1N, T2N

Line transmit signal output.
Signals which consist of a total of 13 bits configured by the start bit (fixed at "1"), the K bit (fixed at "1"), the D bits (control data of two bits), the transmit B bits (eight for voice and data) and the DC bit (1 bit for the DC balance) at the bit rate of 256 kHz are output in burst mode from the T1N pin and the T2N pin in turn at intervals of 125 µsec. These output signals become the AMI code with a duty of 50% in the line coding configuration by connecting to the line via a transformer etc. In the output timing of the T1N and T2N pins, the top bit of the signal is output after receiving a 16-bit signal.

R1N, R2N

Line receive signal input.
Line signals (50% duty AMI code) which consist of a total of 16 bits configured by the frame synchronous bits (four bits with "1"), the K bit (one bit for polling), the D bits (control data of two bits), the receive B bits (eight bits for voice and data), and the DC bit (bit for DC balance) have been transmitted in burst mode at the bit rate of 256 kHz at interval of 125 µsec. These signals should be input in the R1N pin and the R2N pin after separating then into the polarity of "+" and "–".

SYNC

Synchronous signal (8 kHz) output.
This synchronous signal is generated by dividing the oscillator output of 8.192 MHz, applying the frame synchronous bit included in the line signal as a reference phase. This signal also sent to the tone generator and the CODEC inside the device. All timing signals of the CODEC are synchronized by this signal.

CLK1

64 kHz CLK signal output synchronized to the SYNC signal output.
This signal is connected to the CODEC inside the device and is used as a bit clock for receiving and sending the PCM I/O data from and to the ping-pong transmission interface. When an external signal is input to the BHW pin, or when the FHW pin outputs signals for the external circuit, the timing should be set by the CLK1 signal. This signal is always output in the power ON mode.

CLK2

16 kHz CLK signal output synchronized to the SYNC signal output.
This signal can be used for the input or output of the control signal (BD input or FD output) of 16 kbps. This signal is always output in the power ON mode.

CLK3

CLK signal output of 256 kHz synchronized to the SYNC signal.
This signal can be used when the control signal of 16 kHz is input or output from or to the external device by the start-stop synchronization. This signal is always output in the power ON mode.

CLC

Control signal input for phase-inverting the 256 kHz CLK signal which is output form the CLK3 pin.
If the reference phase is set by setting CLC to "0", the CLK signal of 256 kHz is phase-inverted against the reference phase by setting CLC to "1".

FHW

The output of the extracted B-bit (8-bit sequence) from receive signals which are input to R1N and R2N.
This signal is output synchronizing to the rising edge of a CLK1 (64 kHz) output signal beginning with the rising edge of a SYNC output signal.
Since this pin is connected to the D/A converter of the CODEC inside device, the B bits of receive signals are decoded to analog signals.

BHW

Input to the B bit slot of line signals transmitted from the T1N and T2N pins.
The input signal to this pin must be synchronized to the CLK1 output signal (64 kHz) beginning with the rising edge of the SYNC output signal. The input signal is shifted at the falling edge of CLK1.
In the case of inserting the voice data into the transmit B bit, the PCM output of the CODEC is connected to this input pin, and inserting the voice data into the B bit slot is enabled by setting SW12 to ON through processor control. In this case the BHW pin is used as an output pin, so external signals can not be input to this pin. This is an input and output pin of an open drain type with a pulled-up resistance of 5 kΩ.

FD

The signal output of the extracted Control bit (2-bit sequence at 16 kbps) from line signals which are input to the R1N and R2N pins.
This signal is output synchronizing to the rising edge of a CLK2 output signal beginning with the rising edge of the SYNC output signal.
FD is an output pin of an open drain type with a pulled-up resistance of about 10 kΩ.

FK

The signal output of the extracted K bit (8 kbps) from the line receive signals which are input to the R1N and R2N pins.
This signal is output synchronizing to the rising edge of a SYNC output signal. FK is an output pin of an open drain type with a pulled-up resistance of about 10 kΩ.

BD

Input to the D bit (2-bit sequence at 16 kbps) of line signals transmitted from the T1N and T2N pins. When the BDS control pin is in "0", this pin enters the synchronous mode and data must be input to this pin synchronizing with CLK2 (16 kHz).
When the BDS control pin is set to "1", this pin enters the asynchronous data input mode and the asynchronous data of 11 bits including the start bit and stop bit can be input at data rate of 16 kbps.

BDS

Control signal input for selection of the synchronous mode or asynchronous mode for control data (D-bit) input.
When being at "0" level, this pin enters the synchronous data input mode, when being at "1" level, this pin enters the asynchronous data input mode.

PS

Monitoring signal output for the state of the ping-pong transmission. When frames are synchronized (in normal operation) after receiving more than three consecutive frame synchronous signals which are included in the line receive signal sequence, this pin outputs "1".
Otherwise, this pin outputs "0". PS is an output of an open drain type with pulled-up resistance of about 10 kΩ.

X1, X2

CLK oscillator circuit input and output. X1 is input and X2 is output. A crystal oscillator of 8.192 MHz should be connected between X1 and X2. If the frequency deviation in CLK oscillation is great with respect to the receive data rate, the noise of the CODEC increases. The oscillation frequency deviation in CLK should be kept in ±20 ppm or less.

XOUT

8.192 MHz CLK signal output.
If capacitance load is given to the output, the current consumption will increase. About 0.03 mA / pF.

AD0, AD1

Address data inputs for the internal control registers.
Addressing of the internal control registers is executed by AD0 and AD1 and sub address data, DB7 and DB6.

	AD1	AD0	DB7	DB6	Function
WRITE	0	0	0	0	ON/OFF controls of sounder, R-Tone, F-Tone
			0	1	Level/Frequency controls of sounder, R-Tone
			1	0	PB tone control
			1	1	Controls of internal speech path switch and general latch Watchdog timer reset
	0	1	0	0	Controls of receive gain and side tone gain
			0	1	Controls of transmit hold tone, PB tone, handfree input, handset inputs gain
			1	0	Controls of speaker pre-amplifier gain and additional speaker gain
			1	1	Controls of receive PAD and incoming tone input gain
	1	0	—	—	Scanning output control
	1	1	0	0	Scanning interrupt reset
	1	1	0	1	LCD deflection angle control voltage setting
	1	1	1	0	Power ON/OFF control
	1	1	1	1	CODEC control (Controls of companding law and digital loop)
READ	1	0	—	—	Scanning data read-out

WRN

Write signal for internal control registers.
Data on the data bus is written into the registers at the rising edge of WRN under the condition of digital "0" of CEN (Chip Enable). While CEN is in digital "1" state, WRN becomes invalid. The Write cycle is a minimum of 2 µs regardless of the presence or absence of clock signals.

RDN

Read signal input to read PI0 to PI7 out of the processor.
When CEN and RDN are in digital "0" state, the digital values on PI0 to PI7 are output onto the data buses DB0 to DB7. While CEN is in digital "1" state, the RDN signal becomes invalid.

CEN

Chip Enable signal input.
When CEN is in digital "0" state, WRN and RDN are valid.

VLCD

By processor control, VLCD outputs a DC voltage between 0 and 1.4 V is about 0.2 V step. This is used to control the deflection angle of the LCD display. VLCD has the internal resistance value of about 1 kΩ, so the external load of over 100 kΩ should be used. During initialized state, VLCD outputs the voltage of 0 V.

LRSTN

Reset signal output for external circuit.
This reset signal output pin goes to "0" level when the power supply is approximately more than 4.0 V or when the TEST pin is at digital "0" level and the watchdog timer (WDT) outputs a signal. The WDT output does not affect the LSRTN output when TEST pin is at digital "1" level.
The LRSTN signal is also used as a reset signal for internal registers.
When LRSTN is at "0" level, all internal control registers are initialized.
The internal WDT outputs a 500 ms cycle signal when the LRSTN is at digital "1" and the processor does not send a timer reset signal.
Refer to the figure 1 for the output timing of this output.

TEST

Control signal input for deciding valid/invalid of reset control from the internal WDT output. When this input pin is at digital "0" level, the LRSTN output goes to "0" level. When this input pin is at "1" level, the internal WDT does not affect the LSRTN output.

CTEST

Test pin for shipment testing.
This pin should be set to "0" level.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	AG, DG = 0 V	0 to 7	V
Analog Input Voltage	V_{AIN}	AG, DG = 0 V	–0.3 to V_{DD} + 0.3	V
Digital Input Voltage	V_{DIN}	AG, DG = 0 V	–0.3 to V_{DD} + 0.3	V
Storage Temperature	T_{STG}	—	-55 to 150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage		V_D	VA, VD (Voltage must be fixed)	4.75	5.0	5.25	V
Operating Temperature Range		Ta	—	–10	25	70	°C
Input High Voltage		V_{IH}	All Digital Input Pins	2.2	—	V_{DD}	V
Input Low Voltage		V_{IL}	All Digital Input Pins	0	—	0.8	V
Digital Input Rise Time		t_{lr}	All Digital Input Pins	—	—	50	ns
Digital Input Fall Time		t_{lf}	All Digital Input Pins	—	—	50	ns
Digital Output Load		R_{DL}	PO0 to PO7	10	—	—	kΩ
		C_{DL}	PO0 to PO7	—	—	100	pF
			Other digital output pins except PO0 to PO7	—	—	10	
Crystal Oscillator	Oscillating Frequency			—	8.192	—	MHz
	Allowable Frequency Deviation		25°C ±3°C	–50	—	50	ppm
	Temperature Characteristics			–50	—	50	ppm
	Equivalent Series Resistance			—	—	80	Ω
	Production Load Capacitance			—	16	—	pF

Recommend Operating Conditions (Analog Interface)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Analog Load Resistance	R_{AL}	TPAO, MPAO, MPBO, TO, RPO, SPO, CAO		20	—	—	kΩ
		RMO0, RMO1 with respected to SG Level		0.6	—	—	
Analog Load Capacitance	C_{AL}	TPAO, MPAO, MPBO, TO, RPO, SPO, CAO		—	—	30	pF
		RMO0, RMO1		—	—	70	nF
Allowable Analog Input Offset Voltage	V_{off}	TPAI, TPBI, MPAI	With respect to SG	–10	—	10	mV
		MLDY		–50	—	50	
		R1I, R2I, SPI		–25	—	25	
		CAI		–100	—	100	

Recommended Operating Conditions (Processor Digital Interface)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Write Pulse Period	P_W	WRN	See Fig.2	2000	—	—	ns
Write Pulse Width	T_W	WRN		100	—	—	ns
Read Pulse Width	T_R	RDN		200	—	—	ns
Address Data Setup Time	t_{AW1}	AD0, AD1→WRN		80	—	—	ns
	t_{AR1}	AD0, AD1→RDN		80	—	—	ns
Address Data Hold Time	t_{AW2}	WRN→AD0, AD1		50	—	—	ns
	t_{AR2}	RDN→AD0, AD1		50	—	—	ns
CEN Setup Time	t_{CW1}	CEN→WRN		80	—	—	ns
	t_{CR1}	CEN→RDN		80	—	—	ns
CEN Hold Time	t_{CW2}	WRN→CEN		50	—	—	ns
	t_{CR2}	RDN→CEN		50	—	—	ns
Data Setup Time	t_{DW1}	DB0 to 7→WRN		110	—	—	ns
Data Hold Time	t_{DW2}	WRN→DB0 to 7		20	—	—	ns

Recommended Operating Conditions (Ping-Pong transmission Interface)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
B Signal Set-up Time	T_{SBHW}	BHW Input	See Fig. 3	50	—	—	ns
B Signal Hold Time	T_{HBHW}	BHW Input	See Fig. 3	50	—	—	ns
D Signal Set-up Time	T_{SBD}	BD Input	See Fig. 4	50	—	—	ns
D Signal Hold Time	T_{HBD}	BD Input	See Fig. 4	50	—	—	ns
Receive Data Cycle Time	T_{CB}	R1N, R2N	See Fig. 5	—	3.906	—	µs
Receive Data Width	T_{WB}	Width of "L" at R1N and R2N	See Fig. 5	1.35	1.953	2.5	µs
Receive Flame Cycle Time	T_{FM}	—	See Fig. 5	—	125	—	µs

ELECTRICAL CHARACTERISTICS

DC and Digital Interface Characteristics

(V_{DD} = 5 V ±5%, Ta = –10°C to 70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Current	I_{DD1}	Operating Mode (No Signal, Sounder OFF)	—	10	20	mA
	I_{DD2}	Whole system Power Down	—	3	6	mA
	I_{DD3}	CODEC Power Down	—	7	14	mA
Power Supply Voltage Detection	V_{th}	Power Supply Voltage at LRSTN = 1, See Fig. 1	3.9	—	—	V
Power Supply Voltage Non-Detection	V_{tl}	Power Supply Voltage at LRSTN = 0, See Fig. 1	—	—	3.8	V
Input High Voltage	V_{IH}	—	2.2	—	V_{DD}	V
Input Low Voltage	V_{IL}	—	0.0	—	0.8	V
High Input Leakage Current	I_{IH}	Digital Pins except for PI0 to PI7	—	—	2.0	µA
		PI0 to PI7 (Internal Pull-up Pins)	—	—	2.0	µA
Low Input Leakage Current	I_{IL}	Digital Pins except for PI0 to PI7	—	—	0.5	µA
		PI0 to PI7 (Internal Pull-up Pins)	10	—	25	µA
Digital Output High Voltage	V_{OH}	Output Pins 1 *1 I_{OH} = 0.1 mA	2.4	—	V_{DD}	V
		Output Pins 2 *2 I_{OH} = 1.6 mA	2.4	—	V_{DD}	
		All Output Pins I_{OH} = 1 µA	3.8	—	V_{PP}	
Digital Output Low Voltage	V_{OL}	I_{OL} = –1.6 mA	0.0	—	0.4	V
Digital Output Leakage Current	I_O	DB0 to DB7 (Write Mode)	—	—	10	µA
Analog Output Offset Voltage	V_{off}	TPAO, MPAO	–200	—	200	mV
		MPBO, TO, CAO, RPO, RMO0, RMO1, SPO	–100	—	100	
Input Capacitance	C_{IN}	—	—	5	—	pF
Analog Input Resistance	R_{IN}	TPAI, TPBI, MLDYI, RMI, MPAI, MPBI	—	10	—	MΩ
		R1I, R2I, SPI	10	—	—	kΩ
		CAI (fin : < 4 kHz)	—	1	—	MΩ
SG Voltage	—	—	VA/2 –0.05	VA/2	VA/2 +0.05	V
SG Drive Current	I_{SGF}	FORCE Current	1.0	1.5	—	mA
	I_{SGS}	SINK Current	0.3	0.5	—	
Equivalent Pull-up Resistance	R_{PULL}	PI0 to PI7, V_I = 0 V	200	370	500	kΩ

Notes: *1 BHW, FK, FD, PS
*2 SYNC, CLK1, CLK2, CLK3, T1N, T2N, XOUT, LA, LB, LRSTN, DB0 TO DB7

Digital Interface Characteristics

(V_{DD} = 5 V ±5%, Ta = –10°C to 70°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Digital Output (Latch) Delay Time	$t_{pd\ LA}$	WR→LA, LB	See Fig. 2	0.2	—	1.5	µs
Key Scanning Output Delay Time	$t_{pd\ scn}$	WR→PO0 to PO7 Pull-up resistance 10 kΩ	See Fig. 2	0.2	—	1.5	µs
Digital Output (Data) Delay Time	$t_{pd\ data}$	RD→DB0~DB7	See Fig. 2	10	20	100	ns
Delay Time of Power Supply Voltage Detect	t_{dRST1}	LRSTN 0→1	See Fig. 1	—	128	—	ms
	t_{dRST2}	LRSTN 1→0		—	0.01	—	µs
Delay Time of LRSTN due to WDT	T_{WDT}		See Fig. 1	—	500	—	ms
	t_{dRST3}			—	0.85	—	µs
	t_{WRST}			—	1.7	—	
CLK Output Delay Time	t_{dSCK1}	SYNC→CLK1	See Fig. 3	366	—	488	ns
	t_{sSCK2}	SYNC→CLK2	See Fig. 4	366	—	488	
	t_{dSCK3}	SYNC→CLK3		366	—	488	
B Signal Delay Time	t_{dFHW}	CLK1→FHW	See Fig. 3	—	10	—	ns
D Signal Output Delay Time	t_{dFD}	CLK2→FD See Fig. 4	L→H	—	340	—	ns
			H→L	—	10	—	
K Signal Output Delay Time	t_{dFK}	See Fig. 4	L→H	—	740	—	ns
			H→L	—	500	—	
SYNC Output Frequency	f_{SYNC}			—	8	—	kHz
SYNC Output Width	T_{WSYNC}			—	16.6	—	µs
CLK1 Output Frequency	f_{CLK1}			—	64	—	kHz
CLK2 Output Frequency	f_{CLK2}			—	16	—	kHz
CLK3 Output Frequency	f_{CLK3}			—	256	—	kHz
CLK Output Duty Ratio	—	CLK1, CLK2, CLK3		—	50	—	%
Line Output Signal Width	t_{WF}	T1N, T2N "L" Width	See Fig. 5	—	1.953	—	µs
Clock Output Jitter Width		SYNC, CLK1, CLK2 CLK3 When use Xtal		—	250	—	ns

AC Characteristics 1 (CODEC)

(V_{DD} = 5 V ±5%, Ta = –10°C to 70°C)

Parameter	Symbol	Freq. (Hz)	Level (dBm0)	Condition	Min.	Typ.	Max.	Unit
Transmit Frequency Response	Loss T1	60	0		20	27	—	dB
	Loss T2	300			–0.20	0.07	0.20	
	Loss T3	1020			Reference			
	Loss T4	2020			–0.15	–0.03	0.20	
	Loss T5	3000			–0.15	0.06	0.20	
	Loss T6	3400			0.0	0.38	0.80	
Receive Frequency Response	Loss R1	300	0		–0.15	–0.03	0.20	dB
	Loss R2	1020			Reference			
	Loss R3	2020			–0.15	–0.02	0.20	
	Loss R4	3000			–0.15	0.15	0.20	
	Loss R5	3400			0.0	0.56	0.80	
Transmit Signal to Distortion Ratio	SD T1	1020	3	*1	35	43.0	—	dB
	SD T2		0		35	41.0	—	
	SD T3		–30		35	38.0	—	
	SD T4		–40		29	31.0	—	
	SD T5		–45		24	26.5	—	
Receive Signal to Distortion Ratio	SD R1	1020	3	*1	37	43.0	—	dB
	SD R2		0		37	41.0	—	
	SD R3		–30		37	40.0	—	
	SD R4		–40		30	34.0	—	
	SD R5		–45		25	31.0	—	
Transmit Gain Tracking	GT T1	1020	3		–0.3	0.01	0.3	dB
	GT T2		–10		Reference			
	GT T3		–40		–0.3	–0.05	0.3	
	GT T4		–50		–0.5	0.05	0.4	
	GT T5		–55		–1.2	0.30	1.2	
Receive Gain Tracking	GT R1	1020	3		–0.3	0.0	0.3	dB
	GT R2		–10		Reference			
	GT R3		–40		–0.3	–0.10	0.3	
	GT R4		–50		–0.5	–0.30	0.5	
	GT R5		–55		–1.2	–0.40	1.2	
Idle Channel Noise	Nidle T	—	—	AIN = SG *1 μ	—	–73.5	–70	dBm0p
				AIN = SG *1 A	—	–71	–68	
	Nidle R	—	—	*1 *2	—	–78.0	–75	
Absolute Amplitude	AV T	1020	0	CAI → BHW	0.5671	0.6007	0.6363	Vrms
	AV R			FHW → CAO	0.5671	0.6007	0.6363	
Absolute Delay Time	Td	1020	0	CAI → CAO BCLOCK = 64 kHz	—	0.58	0.60	ms

Notes: *1 The Psophometric weighted filter is used
*2 PCMIN input: idle CODE

AC Characteristics 1 (CODEC) (Continued)

(V_{DD} = 5 V ±5%, Ta = −10°C to 70°C)

Parameter	Symbol	Freq. (Hz)	Level (dBm0)	Condition	Min.	Typ.	Max.	Unit
Transmit Group Delay	t_{gd} T1	500	0	*3	—	0.19	0.75	ms
	t_{gd} T2	600			—	0.12	0.35	
	t_{gd} T3	1000			—	0.02	0.125	
	t_{gd} T4	2600			—	0.05	0.125	
	t_{gd} T5	2800			—	0.08	0.75	
Receive Group Delay	t_{gd} R1	500	0	*3	—	0.0	0.75	ms
	t_{gd} R2	600			—	0.0	0.35	
	t_{gd} R3	1000			—	0.0	0.125	
	t_{gd} R4	2600			—	0.09	0.125	
	t_{gd} R5	2800			—	0.12	0.75	
Crosstalk Attenuation	CR T	1020	0	CAI → CAO	70	78	—	dB
	CR R			FHW → BHW CAO left open	75	86	—	
Discrimination Out-of-band Signal	DIS	4.6 kHz to 72 kHz	−25	0 to 4000 Hz	30	32.0	—	dB
Out-of-band Signal Spurious	S	300 to 3400	0	4.6 kHz to 100 kHz	—	−37.5	−35	dBm0
Intermodulation Distortion	IMD	fa = 470 fb = 320	−4	2fa−fb	—	−52	−35	dBm0
Power Supply Noise Rejection Ratio	PSR T	0 to 50 kHz	50 mV_{pp}	*4	25	30	—	dB
	PSR R							

Notes: *3 The minimum value of group delay only is defined as the reference value
*4 Measurement at the idle channel noise

AC Characteristics 2 (Transmit Path)

(V_{DD} = 5 V ±5%, Ta = –10°C to 70°C)

Parameter	Symbol	Freq. (Hz)	Level (dBV)	Condition	Min.	Typ.	Max.	Unit
Pre-Amp Gain	GTPA	1020	–24.0	TPAI-TPAO	18.0	20.0	22.0	dB
Transmit Path Gain	GTPB1			TPBI-TO Set at typical gain	15.7	17.7	19.7	dB
Transmit Path Gain Setting (VOL8)	RG1TPB			Setting, –3 dB than typical gain	–5.0	–3.0	–1.0	dB
	RG2TPB			Setting, –6 dB than typical gain	–8.0	–6.0	–4.0	
	RG3TPB			Setting, –9 dB than typical gain	–11.0	–9.0	–7.0	
Microphone Pre-Amp Gain	GMPA	1020	–24.0	MPAI-MPAO Set at typical gain	18.0	20.0	22.0	dB
Microphone Pre-Amp Gain Setting (VOL9)	RG1MPA			Setting, –6 dB than typical gain	–8.0	–6.0	–4.0	dB
	RG2MPA			Setting, –9 dB than typical gain	–11.0	–9.0	–7.0	
Additional Transmit Signal Gain	GTMX	1020	–4.0	MPBO-TO	–2.0	0.0	2.0	dB
Cross Talk Attennation at Microphone Signal Path	TMX OFF	1020	–24	MPAI-TO	50	60	—	dB
In-Channel PB Signal Output Level	VPBT1	—	—	TO per wave set at typical gain	–19.4	–17.4	–15.4	dBV
In-Channel PB Signal Output Level Setting (VOL4)	GPBT1	—	—	Setting, –3 dB than typical gain	–5.0	–3.0	–1.0	dB
	GPBT2			Setting, –6 dB than typical gain	–8.0	–6.0	–4.0	
	GPBT3			Setting, –9 dB than typical gain	–11.0	–9.0	–7.0	
In-Channel PB Signal Frequency Deviation	DfPBT	—	—		–1.0	—	1.0	%
In-Channel PB Signal Distortion	THDPBT	—	—	In-band Distortion	—	–35	–30	dB
Hold Tone Path Gain	GPAT	1020	–4.0	MLDYI-TO Set at typical gain	–4.0	–2.0	0.0	dB
Hold Tone Path Gain Setting (VOL3)	RG1PAT			Setting, –3 dB than typical gain	–5.0	–3.0	–1.0	dB
	RG2PAT			Setting, –6 dB than typical gain	–8.0	–6.0	–4.0	
	RG3PAT			Setting, –9 dB than typical gain	–11.0	–9.0	–7.0	
Idle Channel Noise	NiTPA	—	—	TPAI:Terminated in 510 Ω Measured at TO TPAO-TPBI Directly connected Set at typical gain *5	—	–70	—	dBV
Maximum Output Voltage Swing	VOT	1020	—	TPAO, TO, MPAO, MPBO R_L = 20 kΩ	2.4	—	—	V_{pp}

Note: *5 Noise band width: 0.3 to 3.4 kHz, non weighted

AC Characteristics 3 (Receive Path)

(V_{DD} = 5 V ±5%, Ta = –10 to 70°C)

Parameter	Symbol	Freq. (Hz)	Level (dBV)	Condition		Min.	Typ.	Max.	Unit
Receive Signal Path Gain	GRPA	1020	–4.0	Typical gain is set between R1I and RPO		–8.0	–6.0	–4.0	dB
Receive Signal Path Gain Setting (VOL1)	RGRPA1			Setting, than typical gain	–8 dB	–10.0	–8.0	–6.0	dB
	RGRPA2				–6 dB	–8.0	–6.0	–4.0	
	RGRPA3				–4 dB	–6.0	–4.0	–2.0	
	RGRPA4				–2 dB	–4.0	–2.0	0.0	
	RGRPA5				2 dB	0.0	2.0	4.0	
	RGRPA6				4 dB	2.0	4.0	6.0	
	RGRPA7				6 dB	4.0	6.0	8.0	
Receive PAD Gain Setting (VOL10)	RGPAD1			Setting, than typical gain	–3 dB	–5.0	–3.0	–1.0	dB
	RGPAD2				–6 dB	–8.0	–6.0	–4.0	
	RGPAD3				–9 dB	–11.0	–9.0	–7.0	
Additional Receive Signal Path Gain	GRMX	1020	–4.0	R2I and RPO		–2.0	0.0	2.0	dB
Side Tone Path Gain	GSIDE	1020	–14.0	Typical gain is set betweenTPBI and RPO		1.0	3.0	5.0	dB
Side Tone Path Gain Setting (VOL2)	RGSIDE1			Setting, than typical gain	6 dB	4.0	6.0	8.0	dB
	RGSIDE2				3 dB	1.0	3.0	5.0	
	RGSIDE3				–3 dB	–5.0	–3.0	–1.0	
	RGSIDE4				–6 dB	–8.0	–6.0	–4.0	
	RGSIDE5				–9 dB	–11.0	–9.0	–7.0	
	RGSIDE6				–12 dB	–14.0	–12.0	–10.0	
Speaker Pre-Amp Gain	GSP	1020	–4.0	Typical gain is set between RPO and SPO		–2.0	0.0	2.0	dB
Speaker Pre-Amp Gain Setting (VOL5)	RGSP1			Setting, than typical gain	–4 dB	–6.0	–4.0	–2.0	dB
	RGSP2				–8 dB	–10.0	–8.0	–6.0	
	RGSP3				–12 dB	–14.0	–12.0	–10.0	
	RGSP4				–16 dB	–18.0	–16.0	–14.0	
	RGSP5				–20 dB	–22.0	–20.0	–18.0	
	RGSP6				–24 dB	–26.0	–24.0	–22.0	
	RGSP7				–28 dB	–30.0	–28.0	–26.0	
Additional Speaker Input Path Gain	GSPI	1020	–4.0	Typical gain is set between SPI and SPO		–2.0	0.0	2.0	dB

AC Characteristics 3 (Receive Path) (Continued)

(V_{DD} = 5 V ±5%, Ta = –10°C to 70°C)

Parameter	Symbol	Freq. (Hz)	Level (dBV)	Condition		Min.	Typ.	Max.	Unit
Additional Speaker Input Path Gain Setting (VOL6)	RGSPI1	1020	–4.0	Setting, than typical gain	–6 dB	–8.0	–6.0	–4.0	dB
	RGSPI2				–12 dB	–14.0	–12.0	–10.0	
	RGSPI3				–18 dB	–20.0	–18.0	–16.0	
Hold Acknowledge Tone Path Gain	GPAR	1020	–4.0	Typical gain is set between MLDYI and SPO		–5.0	–3.0	–1.0	dB
PB Acknowledge Tone Output Level	VPBRP	—	—	RPO per wave		–32.1	–30.1	–28.1	dBV
	VPBSP			SPO per wave Set at typical gain		–30.2	–28.2	–26.2	dBV
PB Acknowledge Tone Frequency Difference	DfPBR	—	—	RPO, SPO		–1.0	—	1.0	%
PB Acknowledge Tone Distortion	THDPBR	—	—	RPO, SPO		—	–35	–30	dB
Incoming Tone Speaker Output Path Gain	GCAO	1020	–20	Typical gain is set between CAO and SPO		–2.0	0.0	2.0	dB
Incoming Tone Speaker Output Path Gain Setting (VOL11)	RGCAO1			Setting, than typical gain	–10 dB	–12.0	–10.0	–8.0	dB
	RGCAO2				–20 dB	–22.0	–20.0	–18.0	
Idle Channel Noise	NiRPO	—	—	R1I:SG, Measured at RPO Set at typical gain.		—	–86.0	—	dBV
	NiSPO	—	—	R1I:SG, Measured at SPO Set at typical gain.		—	–89.0	—	dBV
	NiRMO	—	—	R1I:SG, Gain 0 dB RMO0, RMOB *5		—	–86.0	—	dBV
Maximum Output Amplitude	VOR	—	—	RPO, SPO RL = 20 kΩ		2.4	—	—	V_{pp}
Maximum Output Amplitude	VOR	1020	—	Resister of 1.2 kΩ between RMO0 and RMO1 Measurement at each output		3.6	—	—	V_{pp}
Cross Talk Attennation between Transmit Path and Receive Path	RX to TX	1020	–4	Between R1I and TO		4.5	55	—	dBV

Note: *5 Noise band width : 0.3 kHz to 3.4 kHz, non weighted

AC Characteristics 4 (Ringing Tone)

(V_{DD} = 5 V ±5%, Ta = –10°C to 70°C)

Parameter	Symbol	Condition			Min.	Typ.	Max.	Unit
R-Tone Output Amplitude (VOL7)	VRTO	RPO	Level Setting 1		63	90	117	mV_{pp}
			Level Setting 2		84	120	156	
			Level Setting 3		105	150	195	
			Level Setting 4		126	180	234	
F-Tone Output Amplitude	VFTRP	RPO			112	160	208	mV_{pp}
	VFTSP	SPO			7.5	11.0	14.5	
S-Tone Output Amplitude (VOL12)	VSTSP	SPO	Gain Setting	0 dB	154	220	286	mV_{pp}
				–10 dB	49	70	91	
				–20 dB	12	17	22	
Frequency Deviation	D_{fT}	—			–0.5	—	–0.5	%

AC Characteristics 4 (Sounder Output Circuit)

(V_{DD} = 5 V ±5%, Ta = –10°C to 70°C)

Parameter	Symbol	Freq. (Hz)	Level (dBV)	Condition		Min.	Typ.	Max.	Unit
Sounder Tone Output Amplitude (VOL13)	VST1	—	—	Reference level of DG RLSA0 is 40 kΩ or more.	Vol.1	3.5	4	—	V
	VST2				Vol.2	1	1.2	1.5	
	VST3				Vol.3	0.25	0.44	0.6	
	VST4				Vol.4	0.2	0.27	0.35	
Output Resistance	ROSA0	—				—	2	—	kΩ
Output Load	RLSA0	With respect to DG				40	—	—	kΩ

LCD Defelection Angle Control Voltage Output

(V_{DD} = 5 V ±5%, Ta = –10°C to 70°C)

Parameter	Symbol	Condition			Min.	Typ.	Max.	Unit
		DB2	DB1	DB0				
Output Voltage	VLCD	1	1	1	1.1	1.4	1.7	V
		1	1	0	0.9	1.2	1.5	
		1	0	1	0.7	1.0	1.3	
		1	0	0	0.5	0.8	1.1	
		0	1	1	0.3	0.8	0.9	
		0	1	0	0.2	0.4	0.6	
		0	0	1	0.15	0.2	0.4	
		0	0	0	0.0	0.0	0.05	
Output Resistance	ROLCD	—			—	1.0	—	kΩ
Output Load	RLLCD	To GND			100	—	—	kΩ

TIMING DIAGRAM

Reset Signal Output Timing

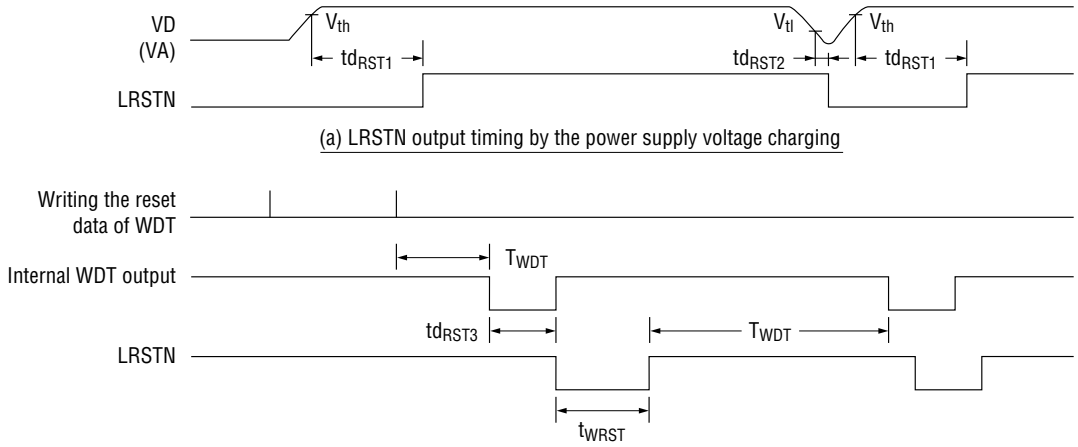


Figure 1

Processor Interface Timing

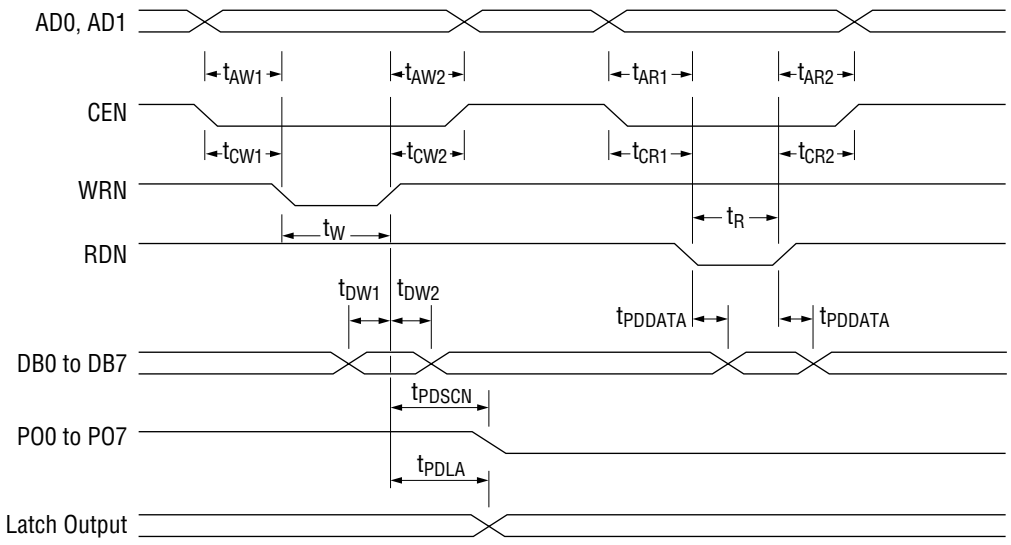


Figure 2

B-bit signal I/O Timing

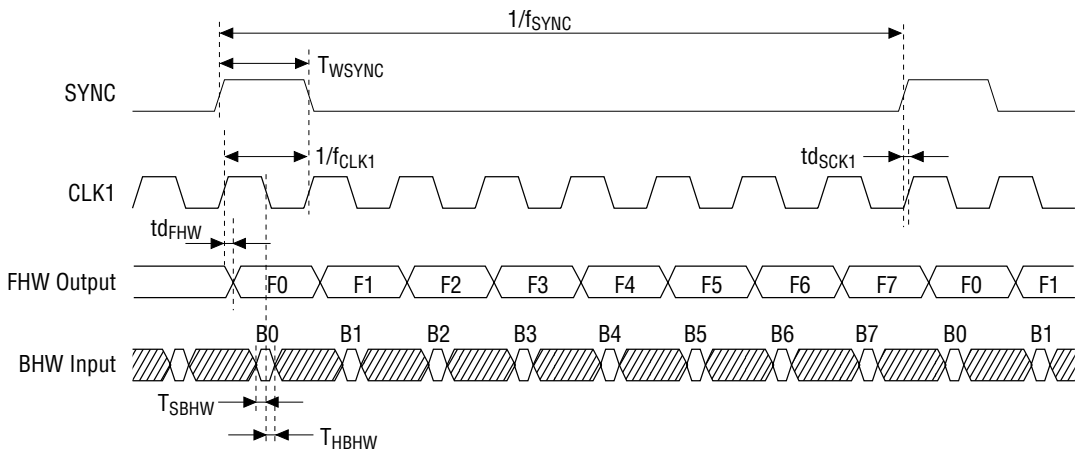


Figure 3

D-, K-bit Signal I/O Timing

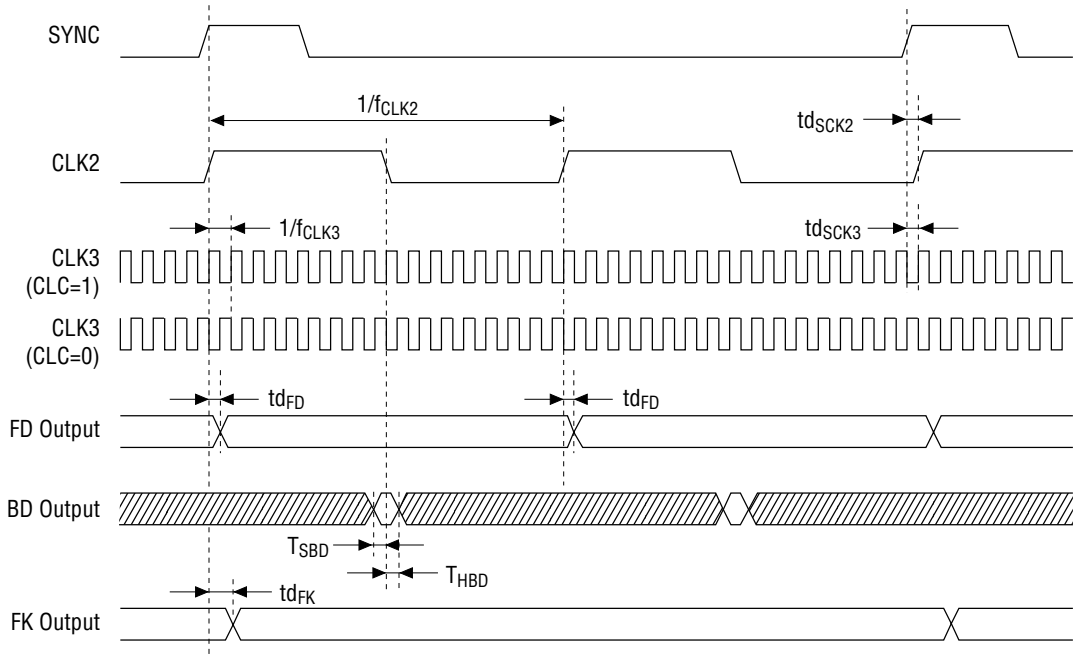


Figure 4

Ping-Pong Transmission Signal Timing

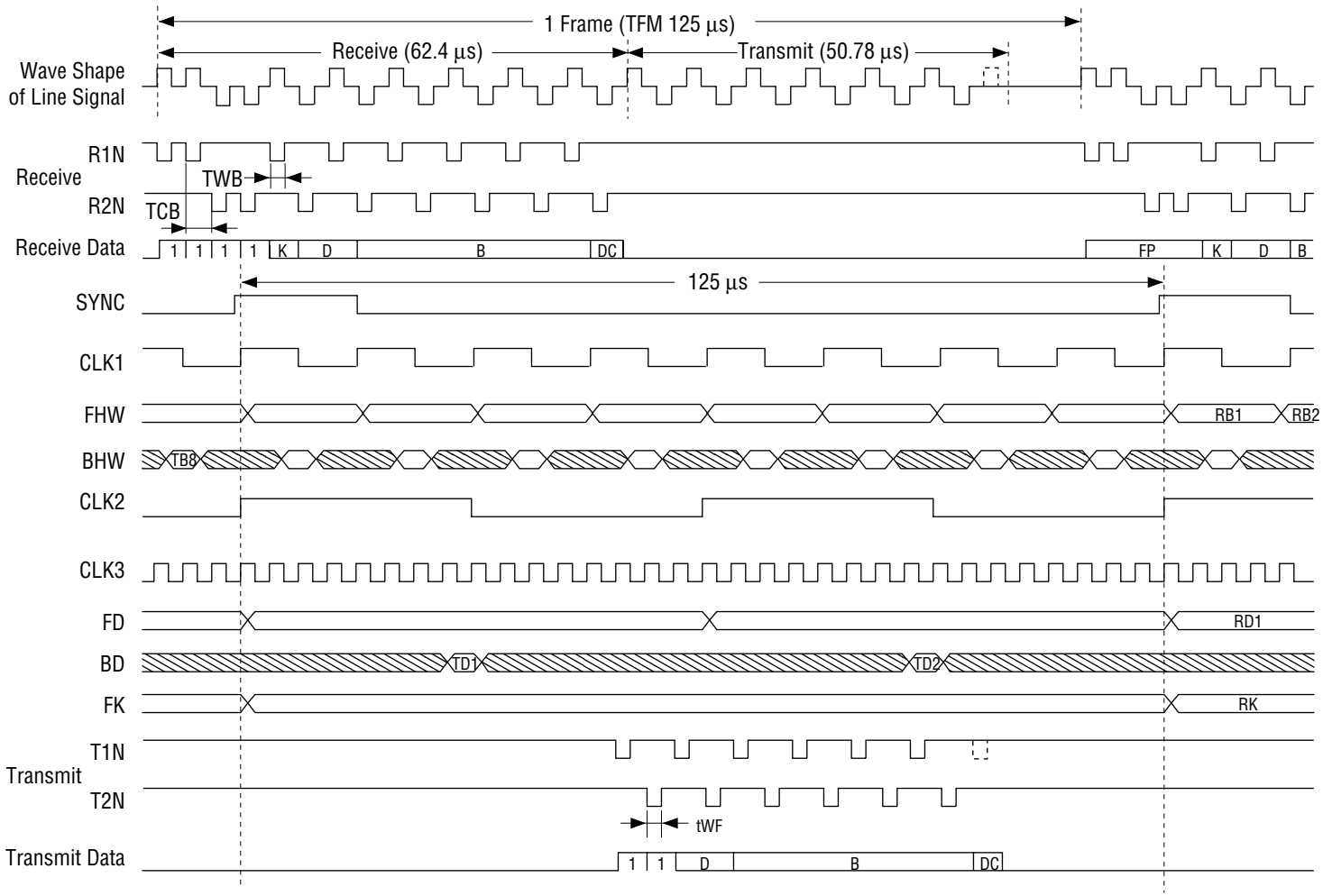


Figure 5

FUNCTIONAL DESCRIPTION

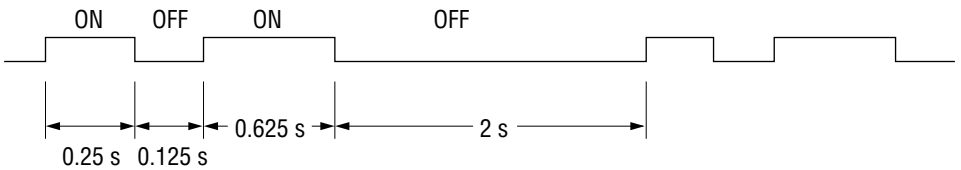
Control Data Description

Sounder Calling Tone and tone ON/OFF control

WRITE Mode
Address Data AD1 = 0, AD0 = 0

Control Data								Description for Control						Remarks
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0							
0	0	1	0	0	0	0	0	Sounder output	ON	SW19	ON			Tone Output: SA0
		0				0	0	Sounder output	OFF	SW19	OFF			
		1				0	1	Sounder output	ON	SW20	ON			Tone Output: SPO *1
		0				0	1	Sounder output	OFF	SW20	OFF			
		1				1	0	R-Tone	ON	SW13	ON			Tone Output: RPO
		0				1	0	R-Tone	OFF	SW13	OFF			
		1	0			1	1	F-Tone	ON(1 kHz)	SW14	ON,	SW15	OFF,	
		0				1	1	F-Tone	OFF	SW14	OFF,	SW15	OFF,	
		1	1			1	1	F-Tone	ON(1 kHz)	SW14	OFF,	SW15	ON,	Tone Output: SPO
		0				1	1	F-Tone	OFF	SW14	OFF,	SW15	OFF,	

*1: This Sounder Output is sent at the timing shown below.



Level and frequency control of sounder and R-tone

WRITE Mode
Address Data AD1 = 0, AD0 = 0

Control Data								Description for Control	Remarks
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
0	1	0	—	—	—	0	0	SA0 output sounder volume 1 (Large)	Sounder volume and tone are defind at a time. At the initial setting, sounder volume 1 and sounder combination tone 1 are set. SA0 sounder volume: VOL 13
						0	1	SA0 output sounder volume 2 (Middle)	
						1	0	SA0 output sounder volume 3 (Small 1)	
						1	1	SA0 output sounder volume 4 (Small 2)	
			0	0	0	—		Sounder combination tone 1 (16 Hz wamble tone with 1000 Hz/1333 Hz)	
			0	0	1			Sounder combination tone 2 (16 Hz wamble tone with 667 Hz/800 Hz)	
			0	1	0			Sounder combination tone 3 (8 Hz wamble tone with 800 Hz/1000 Hz)	
			1	0	0			Sounder combination tone 4 (Single tone of 1000 Hz)	
			1	0	1			Sounder combination tone 5 (Single tone of 800 Hz)	
			1	1	0			Sounder combination tone 6 (Single tone of 400 Hz)	
		1	—			0	0	R-Tone output level 1 (90 mV_{PP} at RPO output)	R-Tone output level = VOL 7 R-Tone output level and frequency are defined at a time. At the initial setting, output level 1 and a single 400 Hz tone are set.
						0	1	R-Tone output level 2 (120 mV_{PP} at RPO output)	
						1	0	R-Tone output level 3 (150 mV_{PP} at RPO output)	
						1	1	R-Tone output level 4 (180 mV_{PP} at RPO output)	
			0	0	0	—		R-Tone 400 Hz single tone	
			0	0	1			R-Tone 425 Hz single tone	
			0	1	0			R-Tone 440 Hz single tone	
			0	1	1			R-Tone 450 Hz single tone	
			1	0	0			R-Tone 400 Hz ON/OFF by 16 Hz	
			1	0	1			R-Tone 400 Hz ON/OFF by 20 Hz	

PB tone control

WRITE Mode
Address Data AD1 = 0, AD0 = 0

Control Data								Output PB Frequency			Remarks
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	PB	Low	High	
1	0	1	PBTC	0	0	0	0	1	697 Hz	1209 Hz	When PBTC = 0 SW16: ON SW17: ON SW18: OFF
				0	0	0	1	2	697	1336	
				0	0	1	0	3	697	1477	
				0	0	1	1	A	697	1633	PB tone is sent to the transmit path T0 and the receive path RPO.
				0	1	0	0	4	770	1209	
				0	1	0	1	5	770	1336	When PBTC = 1 SW16: OFF SW17: OFF SW18: ON
				0	1	1	0	6	770	1477	
				0	1	1	1	B	770	1633	
				1	0	0	0	7	852	1209	PB tone is sent to the receive path SPO only.
				1	0	0	1	8	852	1336	
				1	0	1	0	9	852	1477	
				1	0	1	1	C	852	1633	
				1	1	0	0	*	941	1209	
				1	1	0	1	0	941	1336	
				1	1	1	0	#	941	1477	
				1	1	1	1	D	941	1633	
		0	0	X	X	X	X	PB tone stop			SW16, SW17, SW18: OFF

SW control and timer reset

WRITE Mode
Address Data AD1 = 0, AD0 = 0

Control Data								Description for Control			Remarks
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0				
1	1	1	0	0	0	0	1	SW1	ON	Transmit handfree input	When hold tone or PB tone transmit is selected, these inputs are muted.
				0	0	1	0	SW2	ON	Transmit handset input	
				0	0	1	1	SW3	ON	Receive input	—
				0	1	0	1	SW4	ON	Side tone input	When Handfree input is selected, side tone is muted.
				0	1	1	0	SW5	ON	Receive main amplifier input	—
				0	1	1	1	SW6	ON	Receive speaker input	
				1	0	0	0	SW7	ON	Transmit path hold tone input	—
				1	0	0	1	SW8	ON	Receive path hold tone Acknowledge input	
				1	0	1	0	SW9	ON	Additional receive input	—
				1	0	1	1	SW10	ON	Additional speaker input	
				1	1	0	0	SW11	ON	Speaker DEC input	Speaker DEC input = CODEC AOUT
				1	1	0	1	SW12	ON	PCM output enable	—
				1	1	1	0	LA = 1		General Latch output for external control	
				1	1	1	1	LB = 1			
		0	0	Above codes				Above corresponding SW or latch is set to OFF or "0".			
		0	0	0	0	0	0	All of above SWs or latches are set to OFF or "0" at the initial setting stage.			
1	1	1	1	0	0	0	0	Watchdog timer is reset.			

Gain setting (receive gain, side tone gain)

WRITE Mode
Address Data AD1 = 0, AD0 = 0

Control Data								Description for Control	Remarks
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
0	0	—	—	—	0	0	0	Typical receive gain (–6dB)	Receive gain = VOL1 Side tone gain = VOL2 Receive gain and side tone gain are set at a time. At the initial setting, the typical gain is set.
					0	0	1	–8 dB than the typical gain	
					0	1	0	–6 dB than the typical gain	
					0	1	1	–4 dB than the typical gain	
					1	0	0	–2 dB than the typical gain	
					1	0	1	+2 dB than the typical gain	
					1	1	0	+4 dB than the typical gain	
					1	1	1	+6 dB than the typical gain	
		0	0	0	—			Typical side tone gain (–9 dB)	
		0	0	1				–12 dB than the typical gain	
		0	1	0				–9 dB than the typical gain	
		0	1	1				–6 dB than the typical gain	
		1	0	0				–3 dB than the typical gain	
		1	0	1				+3 dB than the typical gain	
		1	1	0				+6 dB than the typical gain	
		1	1	1				Side tone OFF (VOL2 max loss)	

Gain control (transmit hold tone, PB tone, microphone input, handset input)

WRITE Mode
Address Data AD1 = 0, AD0 = 1

Control Data								Description for Control	Remarks
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
0	1	0	0	—	—	0	0	Typical transmit hold tone gain (–2 dB)	Transmit hold tone gain = VOL3 Transmit PB tone gain = VOL4 Hold tone gain and PB tone gain are set at a time. At the initial setting, the typical gain is set.
						0	1	–3 dB with respect to the typical gain	
						1	0	–6 dB with respect to the typical gain	
						1	1	–9 dB with respect to the typical gain	
				0	0	—		Typical transmit PB tone gain (+4 dB)	
				0	1			–3 dB with respect to the typical gain	
				1	0			–6 dB with respect to the typical gain	
				1	1			–9 dB with respect to the typical gain	
			1	—	—	0	0	Typical handfree input gain (+20 dB)	Handfree input gain = VOL9 Handset input gain = VOL8 Handfree input gain and handset Input gain are set at a time. At the initial setting, the typical gain is set.
						0	1	–6 dB with respect to the typical gain	
						1	0	–9 dB with respect to the typical gain	
						1	1	—	
				0	0	—		Typical handset input gain (+12 dB)	
				0	1			–3 dB with respect to the typical gain	
				1	0			–6 dB with respect to the typical gain	
				1	1			–9 dB with respect to the typical gain	

Gain control (receive PAD, speaker)

WRITE Mode
Address Data AD1 = 0, AD0 = 1

Control Data								Description for Control	Remarks
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
1	0	1	—	—	0	0	0	Typical speaker pre-amp. gain (0 dB)	Speaker pre-amp. gain = VOL5 Additional speaker gain = VOL6 Speaker pre-amp. gain and additional speaker gain are set at a time. At the initial setting, SW21-OFF and the typical gain are set.
					0	0	1	-4 dB with respect to the typical gain	
					0	1	0	-8 dB with respect to the typical gain	
					0	1	1	-12 dB with respect to the typical gain	
					1	0	0	-16 dB with respect to the typical gain	
					1	0	1	-20 dB with respect to the typical gain	
					1	1	0	-24 dB with respect to the typical gain	
					1	1	1	-28 dB with respect to the typical gain	
			0	0	—			Typical additional speaker input path gain (0 dB)	
			0	1				-6 dB with respect to the typical gain	
			1	0				-12 dB with respect to the typical gain	
			1	1				-18 dB with respect to the typical gain	
		0	0	0	0	0	0	Speaker receive OFF(SW21 OFF)	
							1	Speaker receive ON (SW21 ON)	
1	1	0	0	—		0	0	Typical receive PAD gain (0 dB)	Receive PAD = VOL10 Incoming tone gain = VOL11, VOL12 Receive PAD and incoming tone gain are set at a time. At the initial setting, the typical gain is set.
						0	1	-3 dB with respect to the typical gain	
						1	0	-6 dB with respect to the typical gain	
						1	1	-9 dB with respect to the typical gain	
				0	0	—		Typical incoming tone gain (0 dB)	
				0	1			-10 dB with respect to the typical gain	
				1	0			-20 dB with respect to the typical gain	

Key scanning signal output control

WRITE Mode
Address Data AD1 = 1, AD0 = 0

Controlo Data								Description for Control
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Output Data								The data set on DB7 to DB0 are output on PO7 to PO0 respectively. Output data is held until next data is written. When the set data is set to "0", output data goes to "0", when set to "1", output pin is left open. At the initial setting, PO7 to PO0 are in open state.

Key scanning data read out

Read Mode
Address Data AD1 = 1, AD0 = 0

Contorol Data								Description for Control
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
PI7	PI6	PI5	PI4	PI3	PI2	PI1	PI0	Data input onto PI7 to PI0 are output onto DB7 to DB0.

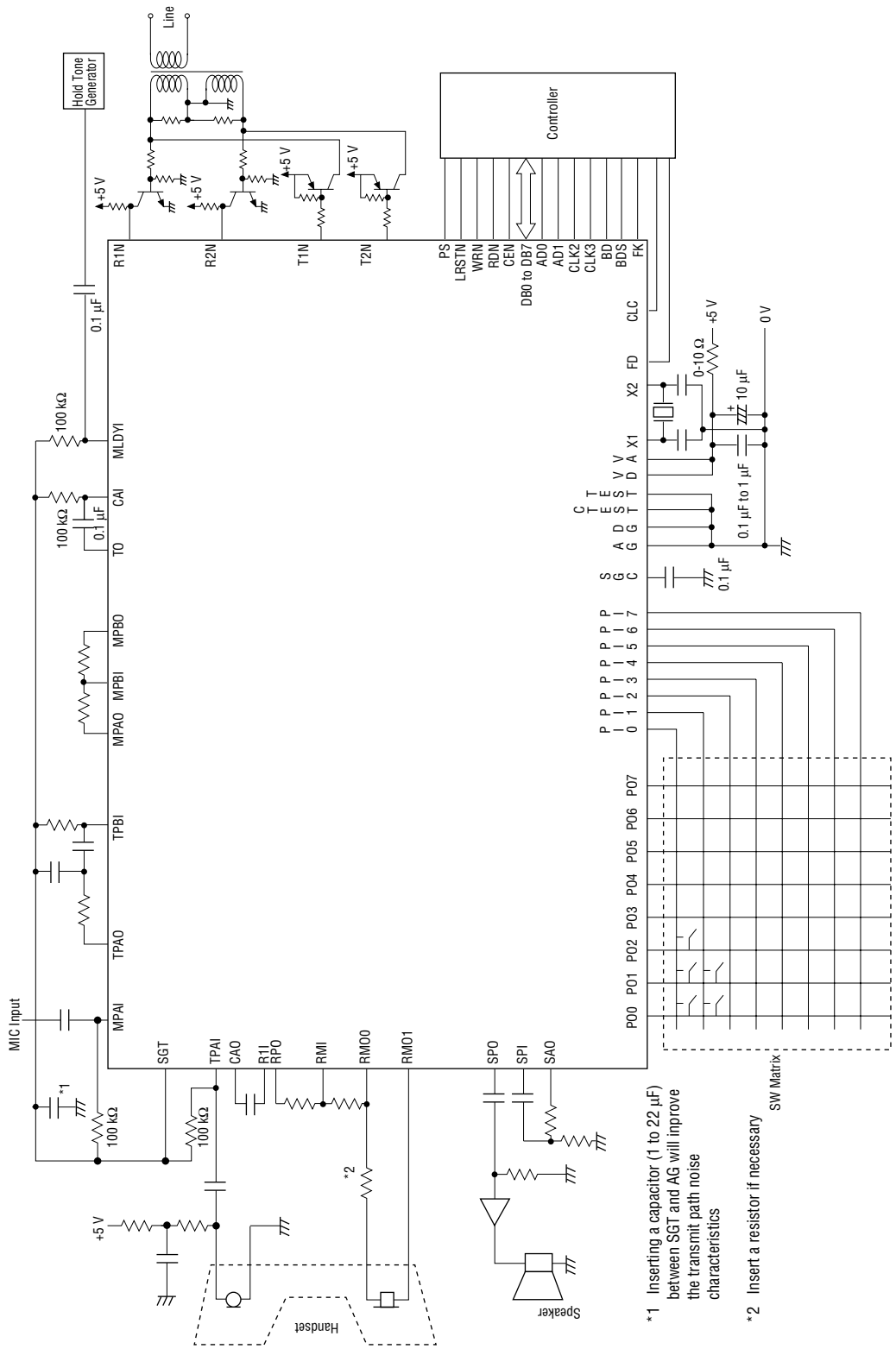
Special functions

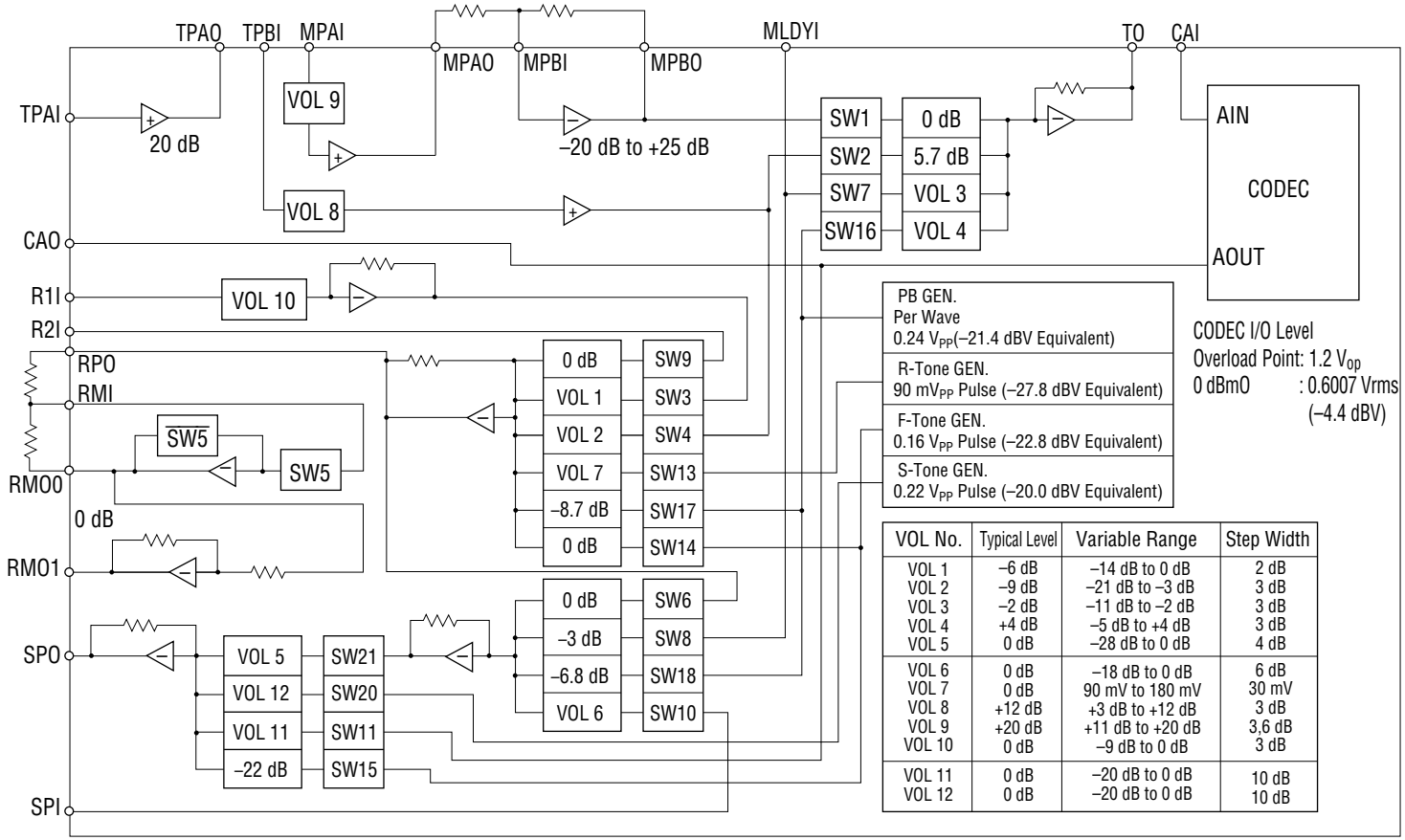
WRITE Mode
Address Data AD1 = 1, AD0 = 1

Contorol Data								Description for Control	Remarks
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
LCD Deflection Angle Control Voltage Output									
0	1	0	0	0	0	0	0	VLCD pin output voltage: 0.0 V	At the initial setting stage, set to 0 V.
					0	0	1	: 0.20 V	
					0	1	0	: 0.40 V	
					0	1	1	: 0.60 V	
					1	0	0	: 0.8 V	
					1	0	1	: 1.0 V	
					1	1	0	: 1.2 V	
					1	1	1	: 1.4 V	
Power Down Mode Control									
1	0	0	0	0	0	0	0	Analog, CODEC power down mode	At the initial setting stage, set to analog and CODEC power down mode. CODEC power ON/OFF control is valid in the analog and CODEC power ON mode.
						0	1	Analog, CODEC power ON mode	
						1	0	CODEC power down mode	
						1	1	CODEC power ON mode	
CODEC Control									
1	1	0	0	0	0	—	0	CODEC operates in μ-law	At the initial setting stage, set to μ-law, and FHW and BHW are normally connected. The componding law and the connection control are set at a time.
							1	CODEC operates in A-law	
						0	—	FHW and BHW are normally connected	
						1		BHW is connected to FHW	

*2: Even during the analog and CODEC power down mode, following functions are available, Key scanning data I/O, sounder outputs (SA0), WDT, and general latch output (LA, LB)

APPLICATION CIRCUIT





VOL No.	Typical Level	Variable Range	Step Width
VOL 1	–6 dB	–14 dB to 0 dB	2 dB
VOL 2	–9 dB	–21 dB to –3 dB	3 dB
VOL 3	–2 dB	–11 dB to –2 dB	3 dB
VOL 4	+4 dB	–5 dB to +4 dB	3 dB
VOL 5	0 dB	–28 dB to 0 dB	4 dB
VOL 6	0 dB	–18 dB to 0 dB	6 dB
VOL 7	0 dB	90 mV to 180 mV	30 mV
VOL 8	+12 dB	+3 dB to +12 dB	3 dB
VOL 9	+20 dB	+11 dB to +20 dB	3,6 dB
VOL 10	0 dB	–9 dB to 0 dB	3 dB
VOL 11	0 dB	–20 dB to 0 dB	10 dB
VOL 12	0 dB	–20 dB to 0 dB	10 dB

Note : (+) : The output signal is input with the same phase as

(–) : The output signal is with inverted phase.

RECOMMENDATIONS FOR ACTUAL DESIGN

- To assure proper electrical characteristics, use bypass capacitors with excellent high frequency characteristics for the power supply and keep them as close as possible to the VA and AG pins.

- Connect the AG pin and the DG pin each other as close as possible. Connected to the system ground with low impedance. If the AG and DG of the device are connected to different ground lines, the device may be latched up.

- Connect the VA pin and the VD pin as close together as possible and routed them to the analog 5 V power supply. If the VA and VD of the device are connected to different power supplies, the device may be latched up.

- Mount the device directly on the board when mounted on PCBs. Do not use IC sockets. If an IC socket is unavoidable, the short lead type socket is recommended.

- When mounted on a frame, electro-magnetic shielding should be recommended, if any electro-magnetic wave source such as power supply transformers is surrounding the device.

- Keep the voltage on the V_{DD} pin not lower than –0.3 V even instantaneously to avoid latch-up phenomenon when turning the power on.

- Use a low noise (particularly, low level type of high frequency spike noise or pulse noise) power supply should be used to avoid the erroneous operation and the degradation of the characteristics of these devices.

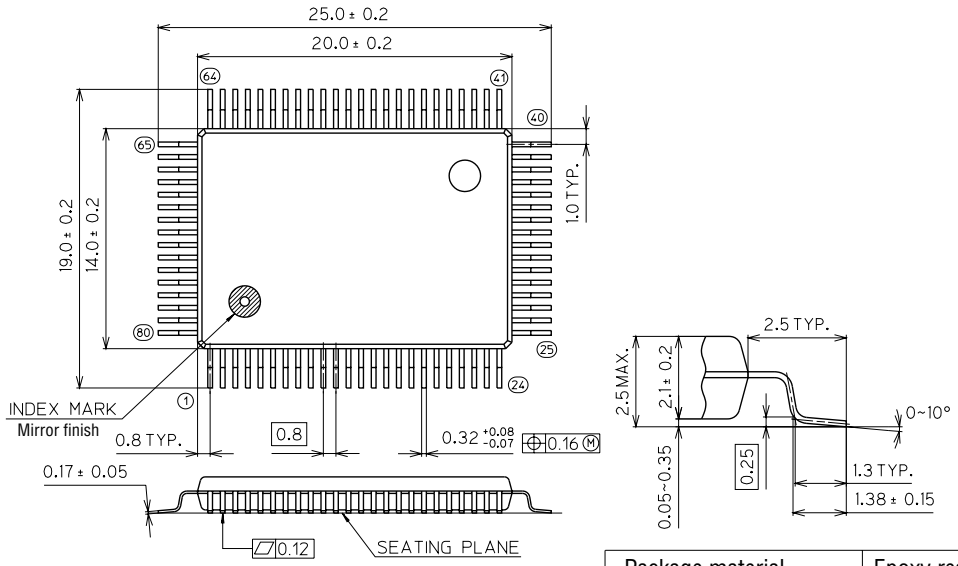
- Connect analog input pins and digital input pins that are not used to the SG pin and to GND, respectively.

- When the data is written differently from the data defined in the section, Control Data Description in Functional Description, the device is not guaranteed in normal operation.

PACKAGE DIMENSIONS

(Unit : mm)

QFP80-P-1420-0.80-BK



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 µm or more
Package weight (g)	1.27 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).