OKI Semiconductor

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Previous version: Nov. 1996

MSM7583

π/4 Shift QPSK MODEM

GENERAL DESCRIPTION

The MSM7583 is a CMOS IC for the π/4 shift QPSK modem developed for the digital cordless telephone systems.
The device, which contains one system of modulator and two systems of demodulater, is optimized for applications for cell stations in a cordless telephone system.

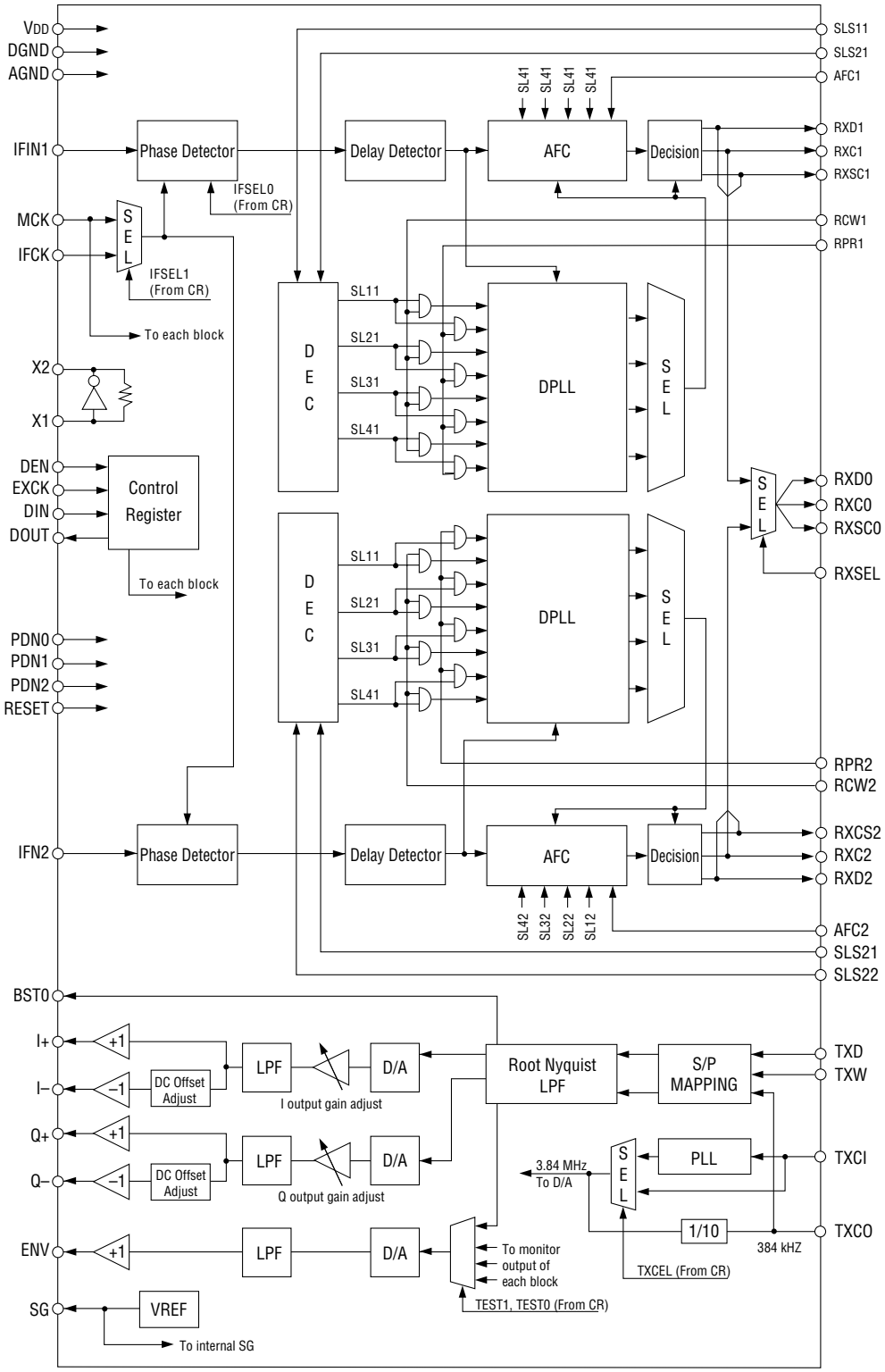
FEATURES

- Single +5 V Power Supply: 4.5 V to 5.5 V

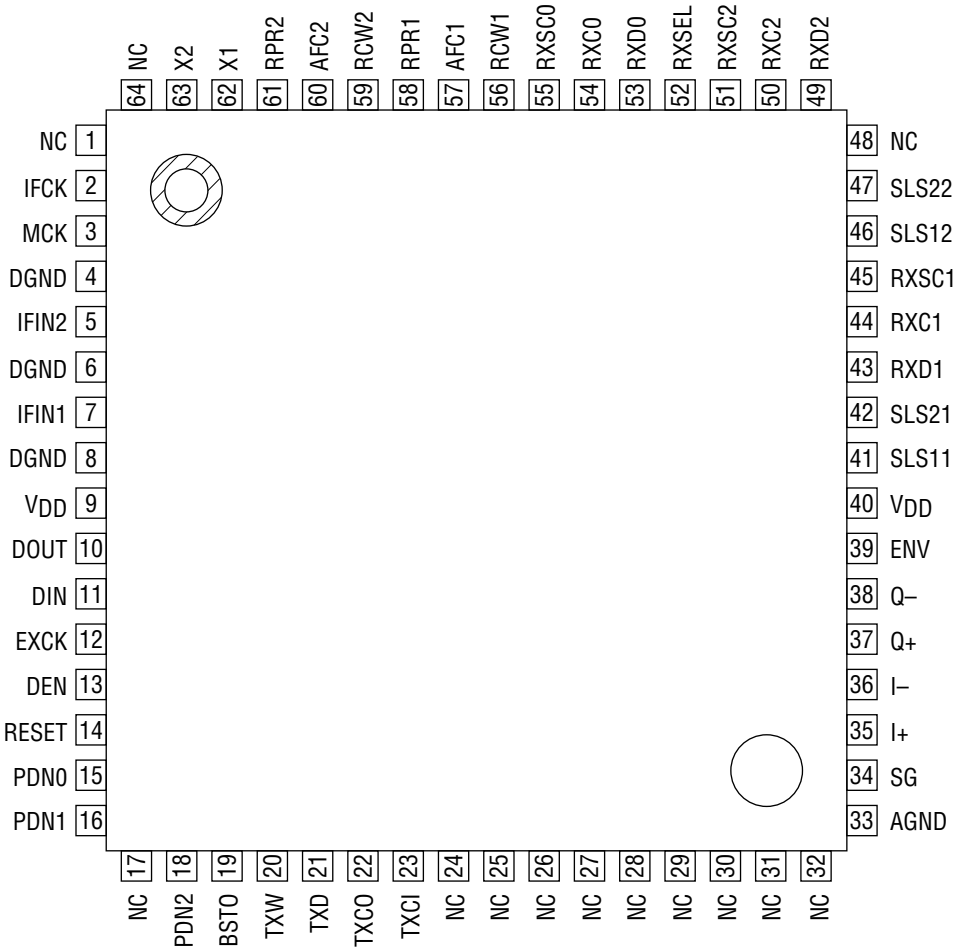
(Modulator Block)
- Built in Root Nyquist Filter for Baseband Limitting (50% Roll-off)
- Ramp Bit for Burst Signal Rise-up (Fall-down) : 2 Symbols
- Built-in D/A converters for Analog Outputs of Quadrature Signal I/Q Components and $\sqrt{I^2 + Q^2}$ (Analog) Power Envelope Output.
- Differential I/Q Analog Output Type
- I/Q Output, DC Offset/Amplitude Adjustable

(Demodulator Block)
- Built-in Diversity-corresponding Demodulation Circuit: 2 Systems
- Full Digital π/4 Shift QPSK Demodulation System
- Input IF Signal Frequency Selectable: 1.2/10.7/10.75/10.8 MHz
- Built-in Clock Recovery: 4 Circuits
- Transmit/Receive Independent Power-down Control capability
- Built-in Precise Analog Voltage Reference
- MCU Serial Interface for Mode Setting and Built-in Test Circuit
- Test Modes: Eye Pattern/AFC Compensating Signal/Phase Detection Signal Monitoring Capability
- Transmission Speed: 384 kbps
- Low Power Consumption
  Operating Mode: 16 mA Typ./Modulator (V_{DD} = 5.0 V)
  28 mA Typ./Demodulator (V_{DD} = 5.0 V)
  Whole Power-down Mode: 0.03 mA Typ. (V_{DD} = 5.0 V)
- Package:
  64-pin plastic QFP (QFP64-P-1414-0.80-BK)(Product name : MSM7583GS-BK)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



64-Pin Plastic QFP

NC : No connect pin

PIN AND FUNCTIONAL DESCRIPTIONS

TXD

Transmit data input for 384 kbps.

TXCI

Transmit clock input.
When the control register CR0 - B6 is "0", a 384 kHz clock pulse synchronous with TXD should be input to this pin. This clock pulse should be continuous because this device uses APLL to generate internal clock pulses.
When CR0 - B6 is "1", a 3.84 MHz clock pulse should be input to this pin. When the 3.84 MHz clock pulse is applied to TXCI, TXCO outputs a 384 kHz clock pulse, which is generated by dividing the TXCI input by 10. The transmit data, synchronous 384 kHz clock pulse, should be input to the TXD. In this case the device does not use APLL, and the 3.84 MHz clock pulse need not be continuous. (Refer to Fig. 1.)

TXCO

Transmit clock output.
When CR0 - B6 is "0", TXCO outputs the 384 kHz clock pulse (APLL output) for monitoring purposes. When CR0 - B6 is "1", this pin outputs a 384 kHz clock pulse generated by dividing the TXCI input by 10. (Refer to Fig. 1.)

TXW

Transmit data window signal input.
The transmit timing signal for the burst data is input to the device through this pin. If TXW pin is "1", modulation data is output. (Refer to Fig. 1.)

I+, I–

Quadrature modulation signal I component differential analog outputs.
The level of the outputs is 500 mVpp with 1.6 Vdc as center value. The output pin load conditions are: $R \geq 10\ k\Omega$, $C \leq 20$ pF. The gain of these pins can be adjusted using the control registers CR1 - B7 to B4, and the offset voltage at the I– pin can be adjusted using CR3 - B7 to B3.

Q+, Q–

Quadrature modulation signal Q component differential analog outputs.
The level of the outputs is 500 mVpp with 1.6 Vdc as center value. The output pin load conditions are: $R \geq 10\ k\Omega$, $C \leq 20$ pF. The gain of these pins can be adjusted using the control registers CR1 - B3 to B0, and the offset voltage at the Q– pin can be adjusted using CR4 - B7 to B3.

ENV

Quadrature modulation signal envelope ($\sqrt{I^2 + Q^2}$) output.

Its output level is 500 mVpp with 1.6 Vdc as a center value. The output pin load conditions are: R ≥ 10 kΩ , C ≤ 20 pF. The gain of this output can be adjusted using the control registers CR2 - B7 to B4.

This pin is also used to monitor eye pattern, AFC compensating signal, and phase detection of the demodulator block during the test mode. Refer to the description of the control register for details.

BSTO

Modulation burst window signal output.

The burst position for the I/Q baseband modulation output is output. (Refer to Fig. 1.)

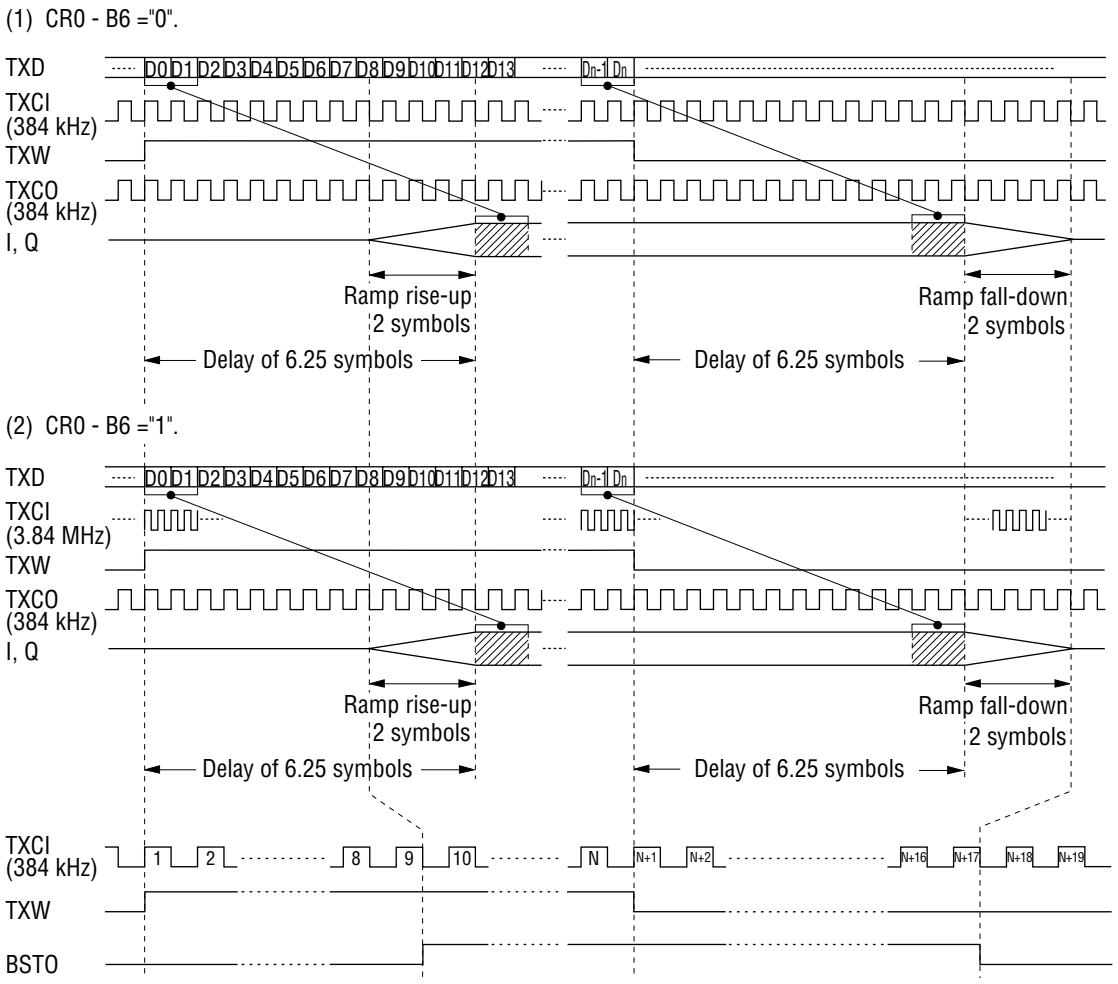


Figure 1 Transmitter Timing Diagram

SG

Internal reference voltage output.
The output voltage is about 2.0 V. A bypass capacitor should be connected between this pin and the AGND pin. The external SG voltage, if necessary should be used via buffer.

RESET

Control register reset.
When this pin is set to "0", the register is reset to the initial value.
The reset signal input width is 200 ns or more.

PDN0, PDN1, PDN2

Inputs for power-down control.
PDN0 controls the standby/communication modes, PDN1 controls the modulator, and PDN2 controls the demodulator. Refer to Table 1 for details.

Table 1 Power Down Control

	PDN0	PDN1	PDN2	Function	Mode
Standby Mode	0	—	0	All power-down.	Mode A
	0	—	1	Modulator power is off (VREF and PLL power is also off). Demodulator power is on.	Mode B
Communication Mode	1	0	0	Modulator power is off (VREF and PLL power is on). I and Q outputs are in a high-impedance state. Only demodulator clock recovery block power is on.	Mode C
	1	1	0	Modulator power is on. Only demodulator clock recovery block power is on.	Mode D
	1	0	1	Modulator power is off (VREF and PLL power is on). I and Q outputs are in a high-impedance state. Demodulator power is on.	Mode E
	1	1	1	Modulator power is on. Demodulator power is on.	Mode F

V_{DD}

+5 V power supply voltage.

AGND

Analog signal ground.

DGND

Digital signal ground.
AGND and DGND are not connected in the device. This pin should be tied to the AGND pin on the PCB as close as possible from the device.
AGND and DGND should be connected as close as prossible on the PC board.

MCK

Master clock input.
The clock frequency is 19.2 MHz.

IFIN1, IFIN2

Modulated signal inputs for the demodulator block.
Select the IF frequency from 1.2 MHz, 10.7 MHz, 10.75 MHz, and 10.8 MHz based on CR0 - B4 and B3. IFIN1 is for Channel 1, and IFIN2 for Channel 2.

IFCK

Clock signal input for demodulator block IF frequency (10.7 MHz or 10.75 MHz).
If the IF frequency is 10.7 MHz, 19.0222 MHz should be supplied. When it is 10.75 MHz, 19.1111 MHz should be supplied. When the IF frequency is 1.2 MHz or 10.8 MHz, set this pin to "0" or "1". (Refer to Fig. 2.)

X1, X2

Crystal oscillator connection pins.
When supplying a 19.0222 MHz or 19.1111 MHz clock to IFCK, use these pins. (Refer to Fig. 2.)

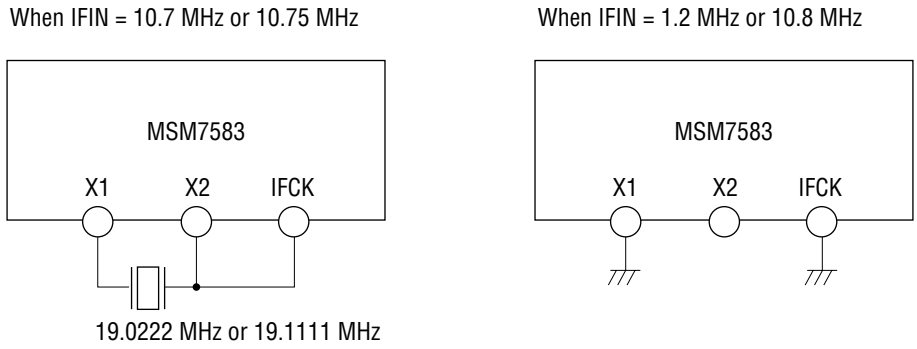


Figure 2 How to Use IFCK, X1, and X2

RXD1, RXC1, RXSC1

Channel 1 receive data, receive clock, and receive symbol clock output pins.
During power-on, these output pins are at the output level of the clock recovery circuit selected by a combination of SLS11 and SLS21 (described later). (Refer to Fig. 3.)

RXD2, RXC2, RXSC2

Channel 2 receive data, receive clock, and receive symbol clock output pins.
During power-on, these output pins are at the output level of the clock recovery circuit selected by a combination of SLS12 and SLS22 (described later). (Refer to Fig. 3.)

SLS11, SLS21, SLS12, SLS22

Receiver slot select signal pins of Channel 1 (SLS11, SLS21) and Channel 2 (SLS12, SLS22). The MSM7583 has four sets of clock recovery circuits and four AFC information storage registers. One of the sets is selected according to a combination of the signals at these pins. (Refer to Fig. 3.)

Channel 1 (SLS21, SLS11) = (0, 0): Slot 1, (0, 1): Slot 2
(1, 0): Slot 3, (1, 1): Slot 4

Channel 2 (SLS22, SLS12) = (0, 0): Slot 1, (0, 1): Slot 2
(1, 0): Slot 3, (1, 1): Slot 4

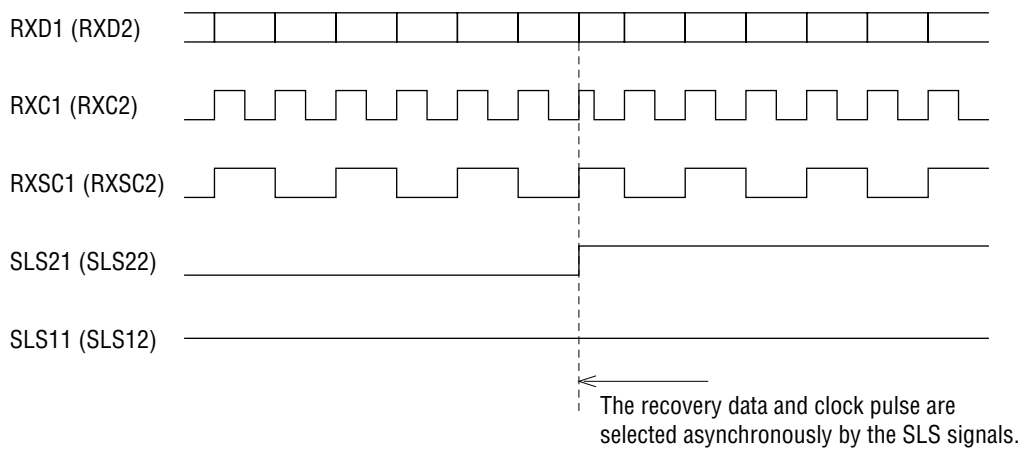


Figure 3 RXD, RXC, and RXSC Timing Diagram

RXD0, RXC0, RXSC0

Receive data, receive clock, and receive symbol clock outputs.
These pins are at the output level selected by RXSEL (described below).

RXSEL

Receive data, receive clock, and receive symbol clock select signal.
If this pin is set to "0", the output levels of Channel 1 RXD1, RXC1, and RXSC1 are selected to be output to RXD0, RXC0, and RXSC0. If this pin is set to "1", the output levels of Channel 2 RXD2, RXC2, and RXSC2 are selected to be output to RXD0, RXC0, and RXSC0.
Note that a hazard may sometime occur in RXDO, RXCO, and RXSCO because RXSEL selects asynchronously.

RPR1, RPR2

High-speed phase clock control signal input pin for the clock recovery circuit.
When each of the pins is "1", the clock recovery circuit starts in the high-speed phase clock mode. When the phase difference is less than a defined value, the circuit shifts to the low-speed phase clock mode automatically. When each of the pins is "0", the circuit is always in the low-speed phase clock mode. RPR1 is for Channel 1, and RPR2 for Channel 2.

AFC1, AFC2

AFC operation range specification signal inputs.
As shown in Fig. 4, the AFC information is reset when both AFC and RPR are set to "1". AFC operation starts at a certain period after the AFC information is reset. When RPR is set to "1", an average number of times that AFC sets to on is low. When RPR is "0", it is high. When AFC is "0", frequency error is not calculated, but the frequency is corrected using an error that is held. AFC1 is for Channel 1, and AFC2 for Channel 2.

RCW1, RCW2

Clock recovery circuit operation ON/OFF control signal inputs.
When this pin is "0", DPLL does not make any phase corrections. RCW1 is for Channel 1, and RCW2 for Channel 2.

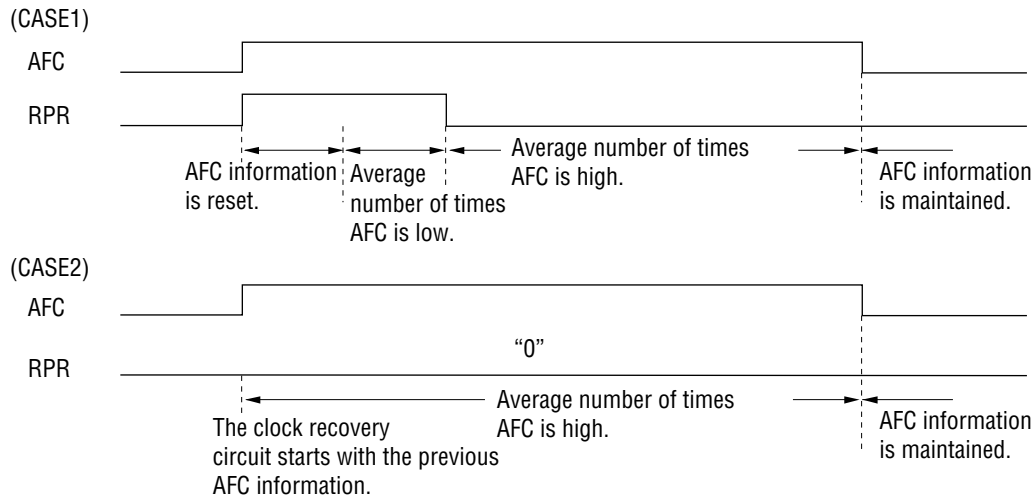


Figure 4 AFC Control Timing Diagram

DEN, EXCK, DIN, DOUT

Serial control ports for the microprocessor interface.
The MSM7583 contains a 6-byte control register. An external CPU uses these pins to read data from and write data to the control register. DEN is the "Enable" signal input pin. EXCK is a data shift clock pulse input pin. DIN is an address and data input pin. DOUT is a data output pin. Figure 5 shows an input/output timing diagram.

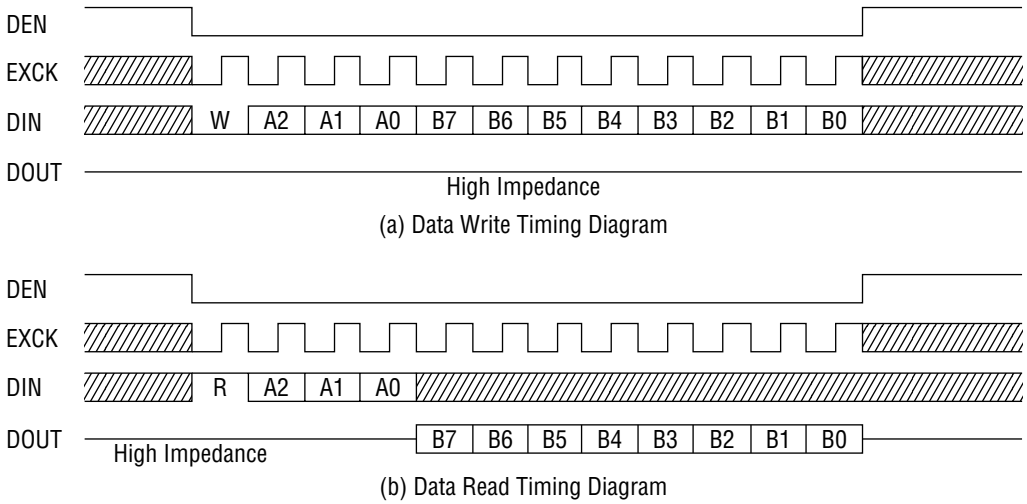


Figure 5 MCU Interface Input/Output Timing Diagram

The register map is shown below

Table 2 Control Register Map

Register	Address			Data								R/W
	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	
CR0	0	0	0	ENVPD	TXCSEL	MODOFF	IFSEL1	IFSEL0	ENVSEL	TEST1	TEST0	R/W
CR1	0	0	1	Ich GAIN3	Ich GAIN2	Ich GAIN1	Ich GAIN0	Qch GAIN3	Qch GAIN2	Qch GAIN1	Qch GAIN0	R/W
CR2	0	1	0	ENV GAIN3	ENV GAIN2	ENV GAIN1	ENV GAIN0	—	—	—	—	R/W
CR3	0	1	1	Ich Offset4	Ich Offset3	Ich Offset2	Ich Offset1	Ich Offset0	—	—	—	R/W
CR4	1	0	0	Qch Offset4	Qch Offset3	Qch Offset2	Qch Offset1	Qch Offset0	—	—	—	R/W
CR5	1	0	1	ICT7	ICT6	ICT5	ICT4	LOCAL INV1	LOCAL INV0	ICT1	ICT0	R/W

R/W : Read/Write enable

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	—	0 to 7	V
Digital Input Voltage	V_{DIN}	—	–0.3 to V_{DD} + 0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(V_{DD} = 4.5 V to 5.5 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	Voltage must be fixed	4.5	—	5.5	V
Operating Temperature	Ta	—	–25	+25	+70	°C
Input High Voltage	V_{IH}	All digital input pins	2.2	—	V_{DD}	V
Input Low Voltage	V_{IL}	All digital input pins	0	—	0.6	V
Master Clock Frequency	f_{MCK}	MCK	—	19.2	—	MHz
Modulator Input Frequency	f_{TXC1}	TXCI (when CR0 - B6 = "0")	—	384	—	kHz
	f_{TXC2}	TXCI (when CR0 - B6 = "1")	—	3.84	—	MHz
Demodulator Input Frequency	f_{IFCK1}	IFCK (when IFIN = 10.7 MHz)	–50 ppm	19.0222	+50 ppm	MHz
	f_{IFCK2}	IFCK (when IFIN = 10.75 MHz)	–50 ppm	19.1111	+50 ppm	MHz
Clock Duty Cycle	D_{CCK}	MCK, IFCK, TXCI	40	50	60	%
IF Input Duty Cycle	D_{CIF}	IFCK	45	50	55	%

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 4.5 V to 5.5 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Current	I_{DD1}	Mode A (when V_{DD} = 5.0 V)	—	0.03	0.06	mA
	I_{DD2}	Mode B (when V_{DD} = 5.0 V)	—	25.0	50.0	mA
	I_{DD3}	Mode C (when V_{DD} = 5.0 V)	—	8.5	17.0	mA
	I_{DD4}	Mode D (when V_{DD} = 5.0 V)	—	16.0	32.0	mA
	I_{DD5}	Mode E (when V_{DD} = 5.0 V)	—	28.0	56.0	mA
	I_{DD6}	Mode F (when V_{DD} = 5.0 V)	—	35.0	70.0	mA
Output High Voltage	V_{OH}	I_{OH} = 0.4 mA	2.8	—	V_{DD}	V
Output Low Voltage	V_{OL}	I_{OL} = –1.6 mA	0.0	—	0.4	V
Input Leakage Current	I_{IH}	—	—	—	10	µA
	I_{IL}	—	—	—	10	µA

Analog Interface Characteristics

(V_{DD} = 4.5 V to 5.5 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condtion	Min.	Typ.	Max.	Unit
Output Resistance Load	R_{LIQ}	I+, I–, Q+, Q–, ENV	10	—	—	kΩ
Output Capacitance Load	C_{LIQ}	I+, I–, Q+, Q–, ENV	—	—	20	pF
Output DC Voltage Level	V_{DC1}	I+, I–, Q+, Q– (TXW = 0)	1.55	1.6	1.65	V
	V_{DC2}	I+ (CR0 – B5 = 1) when not modulated	—	1.77	—	V
	V_{DC3}	Q+ (CR0 – B5 = 1) when not modulated	—	1.67	—	V
	V_{DC4}	ENV (TXW = 0)	—	1.35	—	V
	V_{DC5}	ENV (TXW = 1, CR0 – B2 = 0, TXD = 0)	—	1.72	—	V
	V_{DC6}	ENV (TXW = 1, CR0 – B2 = 1, TXD = 0)	—	1.63	—	V
Output AC Voltage Level	V_{AC}	I+, I–, Q+, Q– (TXW = 0 continuous input)	340	360	380	mV_{PP}
Offset Voltage Difference	V_{OFF}	Difference among I+, I–, Q+, and Q–	–20	—	+20	mV
Output DC Voltage Adjustment Level Range	DCVL	—	—	±45	—	mV
Output AC Voltage Adjustment Level Range	ACVL	—	—	±4	—	%
Out-of-band Spectrum	P600	600 kHz detuning (*)	60	—	—	dB
	P900	900 kHz detuning (*)	65	—	—	dB
Modulation Accuracy	EVM	—	—	1.0	3.0	% rms
Demodulator IF Input Level	IFV	IFIN input level	0.5	—	V_{DD}	V_{PP}
IFIN Input Impedance	RIF	—	—	20	—	kΩ
	CIF	—	—	5	—	pF
SG Output Voltage	VSG	—	—	2.0	—	V
SG Output Impedance	RSG	—	—	2	—	kΩ
SG warm-up Time	T_{SG}	SG↔AGND 0.1 µF (Rise Time to 90% of max. level.)	—	400	—	µs
Modulator D/A Conversion Sampling Frequency	F_{SDA}	—	—	1.92	—	MHz
Modulator D/A Conversion Offset Frequency	F_{CDA}	—	—	380	—	kHz

* Power attenuation at 600 kHz or 900 kHz ±96 kHz as referred to two times of the power in frequency band of 0 to 96 kHz

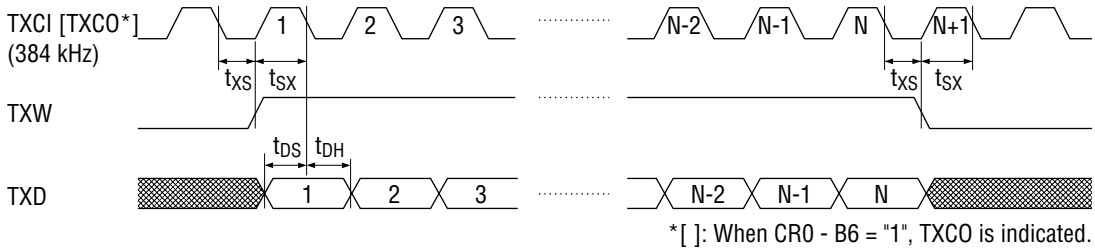
Digital Interface Characteristics

(V_{DD} = 4.5 V to 5.5 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condtion		Min.	Typ.	Max.	Unit
			Other				
Transmitter Digital Input/Output Setting Time	t_{SX} t_{XS}	C load = 50 pF	Fig. 6	200	—	—	ns
	t_{DS} t_{DH}			200	—	—	ns
	t_{XD1} t_{XD2}			0	—	200	ns
	t_{XD3} t_{XD4}			0	—	200	ns
Receiver Digital Input/Output Setting Time	t_{RD1}	C load = 50 pF	Fig. 7	0	—	200	ns
	t_{RD2}			0	—	200	ns
	t_{RS1} to t_{RS4}			10	—	—	µs
	t_{RW}			10	—	—	µs
Serial Port Digital Input/Output Setting Time	t_{M1}	C load = 50 pF	Fig. 8	50	—	—	ns
	t_{M2}			50	—	—	ns
	t_{M3}			50	—	—	ns
	t_{M4}			50	—	—	ns
	t_{M5}			100	—	—	ns
	t_{M6}			50	—	—	ns
	t_{M7}			50	—	—	ns
	t_{M8}			0	—	100	ns
	t_{M9}			50	—	—	ns
	t_{M10}			50	—	—	ns
	t_{M11}			0	—	50	ns
EXCK Clock Frequency	f_{EXCK}	—	EXCK	—	—	10	MHz

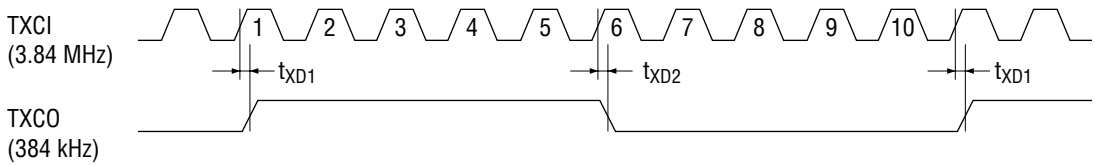
TIMING DIAGRAM

Transmit Data Input Timing



*[ ]: When CR0 - B6 = "1", TXCO is indicated.

Transmit Clock (TXCO) Output Timing (when CR0 - B6 = 1)



Transmit Burst Position Output (BSTO) Timing

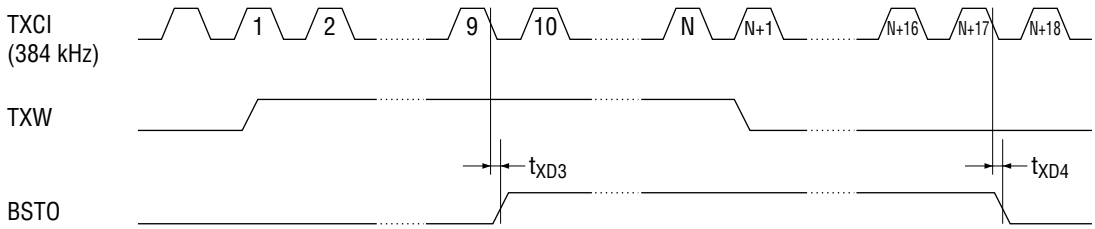


Figure 6 Transmit (Modulator) Digital Input/Output Timing

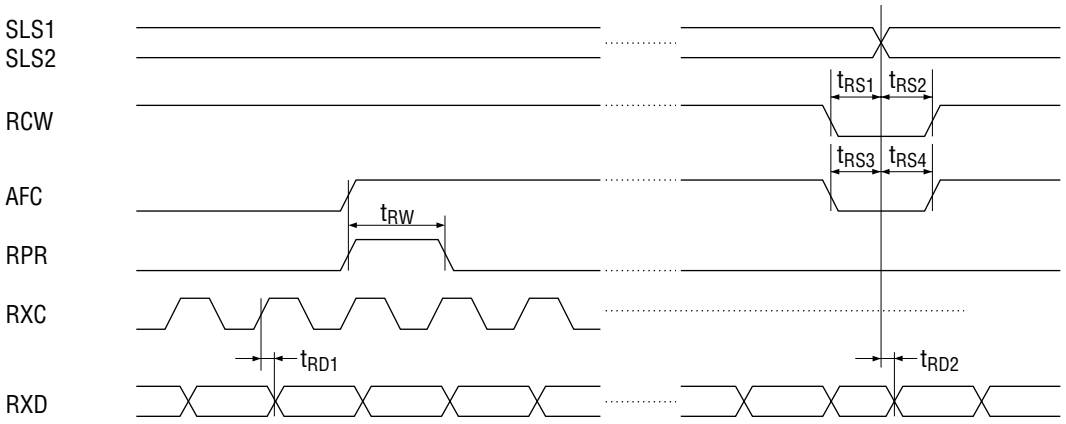


Figure 7 Receiver (Demodulator) Digital Input/Output Timing

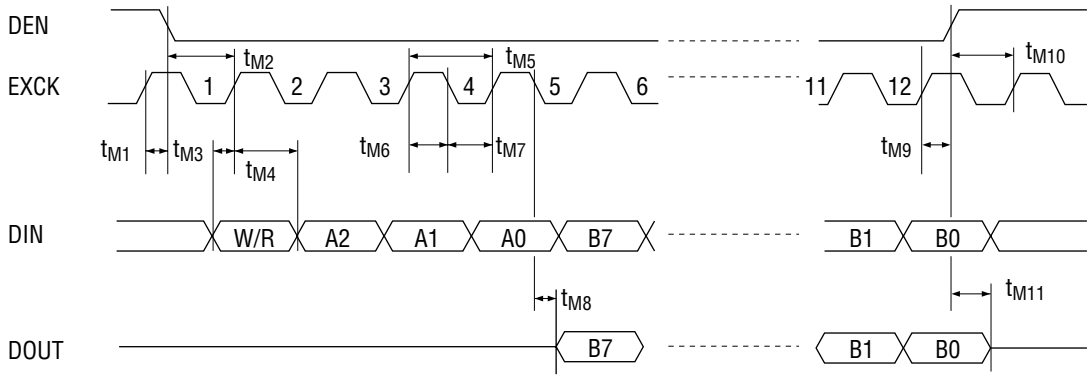


Figure 8 Serial Control Port Interface

FUNCTIONAL DESCRIPTION

Control Registers

(1) CR0 (basic operation mode setting)

	B7	B6	B5	B4	B3	B2	B1	B0
CR0	ENVPD	TXCSEL	MODOFF	IFSEL1	IFSEL2	ENVSEL	TEST1	TEST0
Initial value (*)	0	0	0	0	0	0	0	0

* The initial value is set when a reset signal is supplied at RESET.

B7: Transmit envelope output power down control
0/Envelope output ON
1/Envelope output OFF

B6: Transmit timing clock selection
0/TXCI input: 384 kHz.
TXCO output: 384 kHz output from APLL
Transmit data TXD is input in synchronization with the rising edge of TXCI (APLL is on.)
1/TXCI input: 3.84 MHz.
TXCO output: 384 kHz (one-tenth of the TXCI frequency)
Transmit data TXD is input in synchronization with the rising edge of TXCO (APLL is off.)

B5: Modulation on/off control
1/modulation OFF (with phase fixed)
0/modulation ON.

B4, B3: Receiver input IF frequency selection
(0, 0), (0, 1): 1.2 MHz
(1, 0) : 10.8 MHz
(1, 1) : 10.7 MHz/10.75 MHz

B2: Transmit envelope ($I^2 + Q^2$ or $\sqrt{I^2 + Q^2}$) output selection

When B1, B0 is (0, 0) : 0/$\sqrt{I^2 + Q^2}$ output
1/$I^2 + Q^2$ output
When B1, B0 is other than (0, 0) : 0/Channel 1 receive monitor output
1/Channel 2 receive monitor output

B1, B0: Test mode selection bits. Each monitor output is output to the transmit ENV pin.
(0, 0): transmit envelope ($I^2 + Q^2$ or $\sqrt{I^2 + Q^2}$) output
(0, 1): receiver phase detection signal output
(1, 0): receiver delay detection signal output
(1, 1): receiver internal AFC information output

(2) CR1 (I, Q gain adjustment)

	B7	B6	B5	B4	B3	B2	B1	B0
CR1	Ich GAIN3	Ich GAIN2	Ich GAIN1	Ich GAIN0	Qch GAIN3	Qch GAIN2	Qch GAIN1	Qch GAIN0
Initial value	0	0	0	0	0	0	0	0

B7 to B4: I+/I- output gain setting, in 3 mV steps (Refer to Table 3.)

B3 to B0: Q+/Q- output gain setting, in 3 mV steps (Refer to Table 3.)

(3) CR2 (ENV gain adjustment)

	B7	B6	B5	B4	B3	B2	B1	B0
CR2	ENV GAIN3	ENV GAIN2	ENV GAIN1	ENV GAIN0	—	—	—	—
Initial value	0	0	0	0	0	0	0	0

B7 to B4: ENV output gain setting, in 9 mV steps (Refer to Table 3.)

B3 to B0: Not used

Table 3 I, Q, and ENV Output Gain Values

CR1				I and Q Amplitude (value relative to the reference (1.000) at (0, 0, 0, 0))	CR2				ENV Amplitude (value relative to the reference (1.000) at (0, 0, 0, 0))
B7	B6	B5	B4		B7	B6	B5	B4	
B3	B2	B1	B0						
0	1	1	1	1.042	0	1	1	1	1.126
0	1	1	0	1.036	0	1	1	0	1.108
0	1	0	1	1.030	0	1	0	1	1.090
0	1	0	0	1.024	0	1	0	0	1.072
0	0	1	1	1.018	0	0	1	1	1.054
0	0	1	0	1.012	0	0	1	0	1.036
0	0	0	1	1.006	0	0	0	1	1.018
0	0	0	0	1.000	0	0	0	0	1.000
1	1	1	1	0.994	1	1	1	1	0.982
1	1	1	0	0.988	1	1	1	0	0.964
1	1	0	1	0.982	1	1	0	1	0.946
1	1	0	0	0.976	1	1	0	0	0.928
1	0	1	1	0.970	1	0	1	1	0.910
1	0	1	0	0.964	1	0	1	0	0.892
1	0	0	1	0.958	1	0	0	1	0.874
1	0	0	0	0.952	1	0	0	0	0.856

(4) CR3 (I– output offset voltage adjustment)

	B7	B6	B5	B4	B3	B2	B1	B0
CR3	Ich Offset4	Ich Offset3	Ich Offset2	Ich Offset1	Ich Offset0	—	—	—
Initial value	0	0	0	0	0	0	0	0

B7 to B3: I– output pin offset voltage adjustment (Refer to Table 4.)

B2 to B0: Not used

(5) CR4 (Q– output offset voltage adjustment)

	B7	B6	B5	B4	B3	B2	B1	B0
CR4	Qch Offset4	Qch Offset3	Qch Offset2	Qch Offset1	Qch Offset0	—	—	—
Initial value	0	0	0	0	0	0	0	0

B7 to B3: Q– output pin offset voltage adjustment (Refer to Table 4.)

B2 to B0: Not used

Table 4 I and Q Channel Offset Adjustment Values

CR3, CR4					I and Q offset	CR3, CR4					I and Q offset
B7	B6	B5	B4	B3	(mV)	B7	B6	B5	B4	B3	(mV)
0	1	1	1	1	+45	1	1	1	1	1	–3
0	1	1	1	0	+42	1	1	1	1	0	–6
0	1	1	0	1	+39	1	1	1	0	1	–9
0	1	1	0	0	+36	1	1	1	0	0	–12
0	1	0	1	1	+33	1	1	0	1	1	–15
0	1	0	1	0	+30	1	1	0	1	0	–18
0	1	0	0	1	+27	1	1	0	0	1	–21
0	1	0	0	0	+24	1	1	0	0	0	–24
0	0	1	1	1	+21	1	0	1	1	1	–27
0	0	1	1	0	+18	1	0	1	1	0	–30
0	0	1	0	1	+15	1	0	1	0	1	–33
0	0	1	0	0	+12	1	0	1	0	0	–36
0	0	0	1	1	+9	1	0	0	1	1	–39
0	0	0	1	0	+6	1	0	0	1	0	–42
0	0	0	0	1	+3	1	0	0	0	1	–45
0	0	0	0	0	0	1	0	0	0	0	–48

(6) CR5 (IC test)

	B7	B6	B5	B4	B3	B2	B1	B0
CR5	ICT7	ICT6	ICT5	ICT4	LOCAL INV1	LOCAL INV0	ICT1	ICT0
Initial value	0	0	0	0	0	0	0	0

B7 to B4: ICT7 to ICT4. Device test control bits.

B3, B2 : Local inverting mode setting bits. (Used when the phase of the demodulator IF input to this device is inverted.)
(1, 1) = local inverting mode
(0, 0) = normal mode

B1, B0 : ICT1, ICT0. Device test control bits.

Note: CR5 - B7 to B4, B1, and B0 are used to test the device. They should be set to "0" during normal operation.

State Transition Time

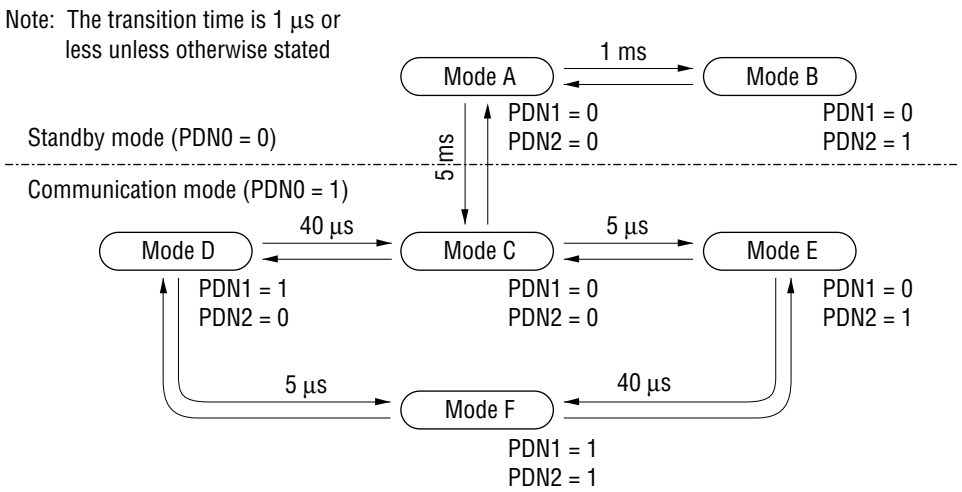


Figure 9 Power-Down State Transition Time

APPLICATION CIRCUIT

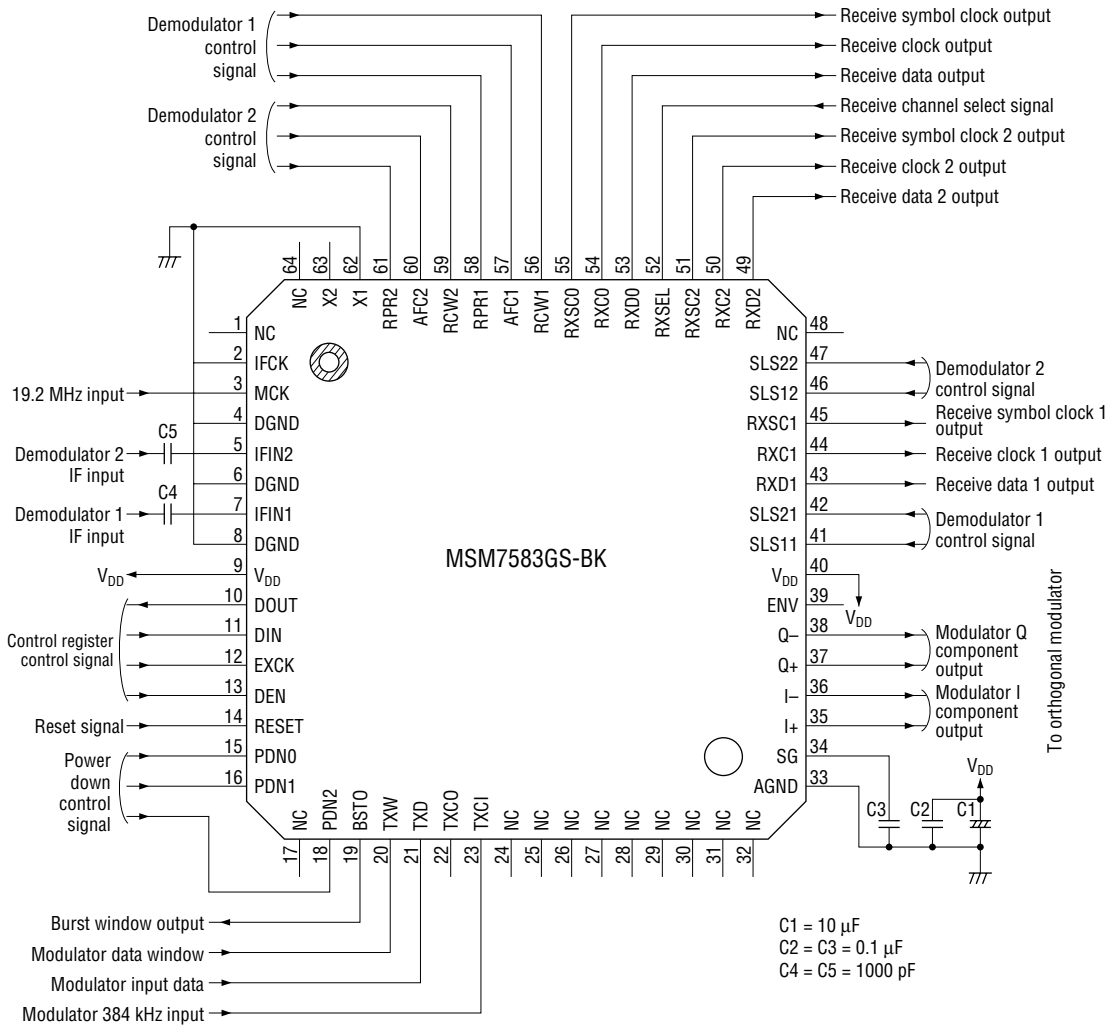
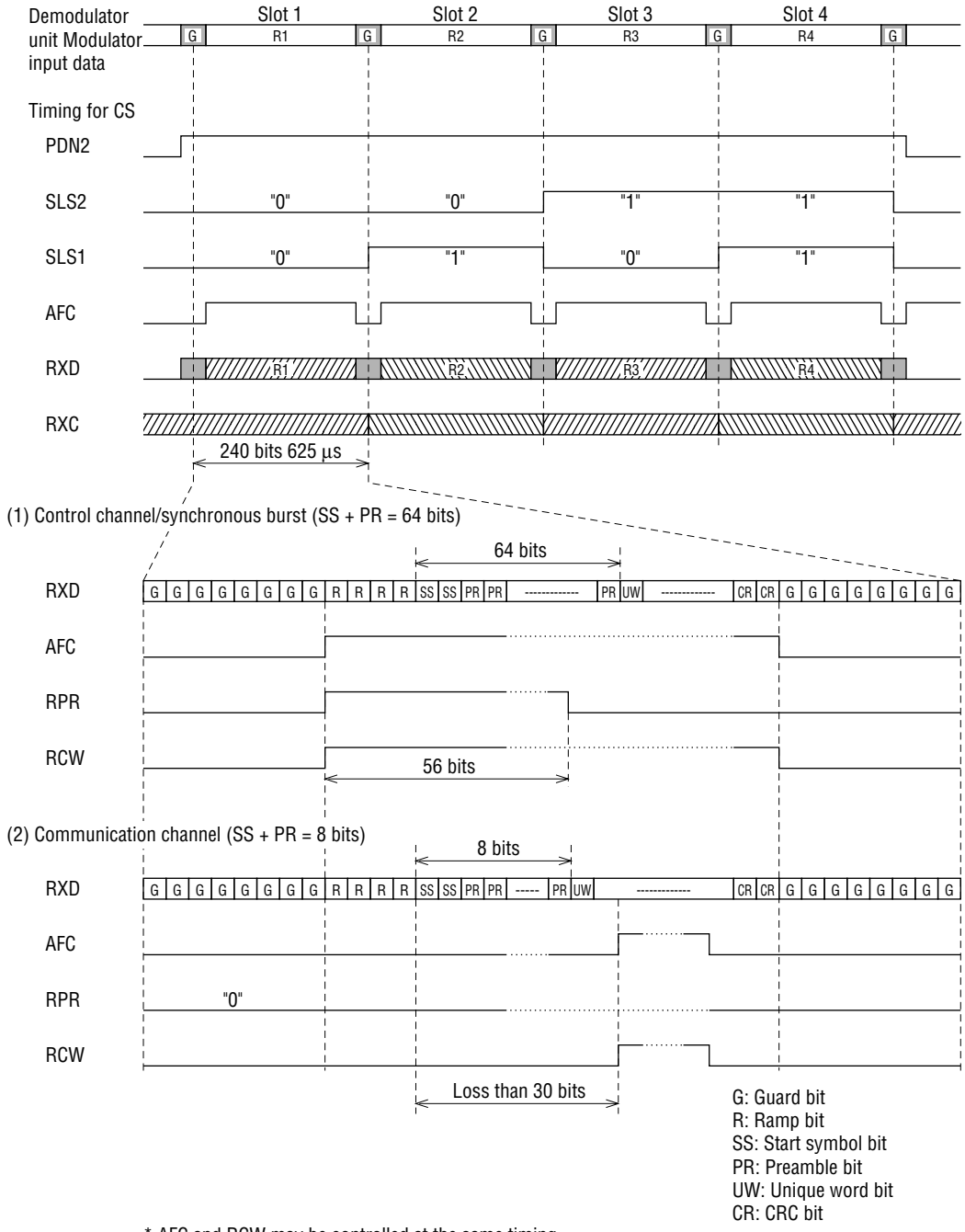


Figure 10 Example of Circuit Configuration

Demodulator Control Timing Diagram (Example)

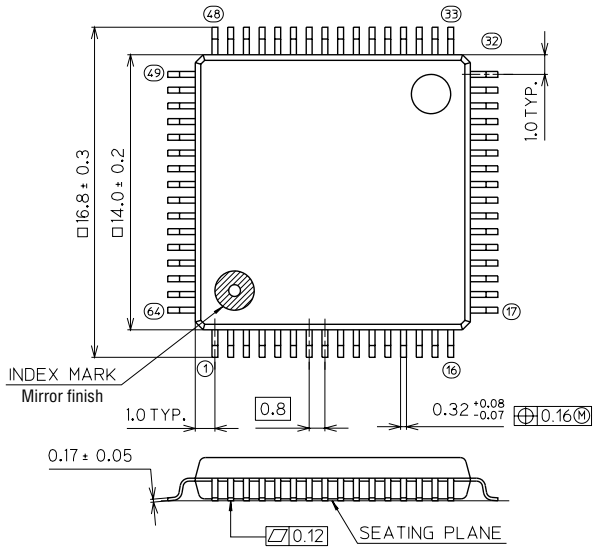


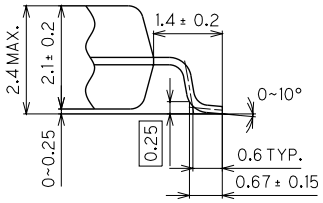
* AFC and RCW may be controlled at the same timing.

PACKAGE DIMENSIONS

(Unit : mm)

QFP64-P-1414-0.80-BK





Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 µm or more
Package weight (g)	0.87 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).