OKI Semiconductor

This version: Aug. 1999
Previous version: Dec. 1998

MSM7654

NTSC/PAL Digital Video Encoder

GENERAL DESCRIPTION

The MSM7654, which is a digital video encoder supporting NTSC/PAL formats, converts digital image data to an analog video signal.
The encoder can receive the digital image or RGB digital image signals conforming to ITU-R BT.601 as an input signal.
The encoder can output simultaneously the composite video and S-video signals, and it can also output the RGB analog signal by switching.
The encoder can control luminance (Y) signal output levels of the composite video and S-video signals.

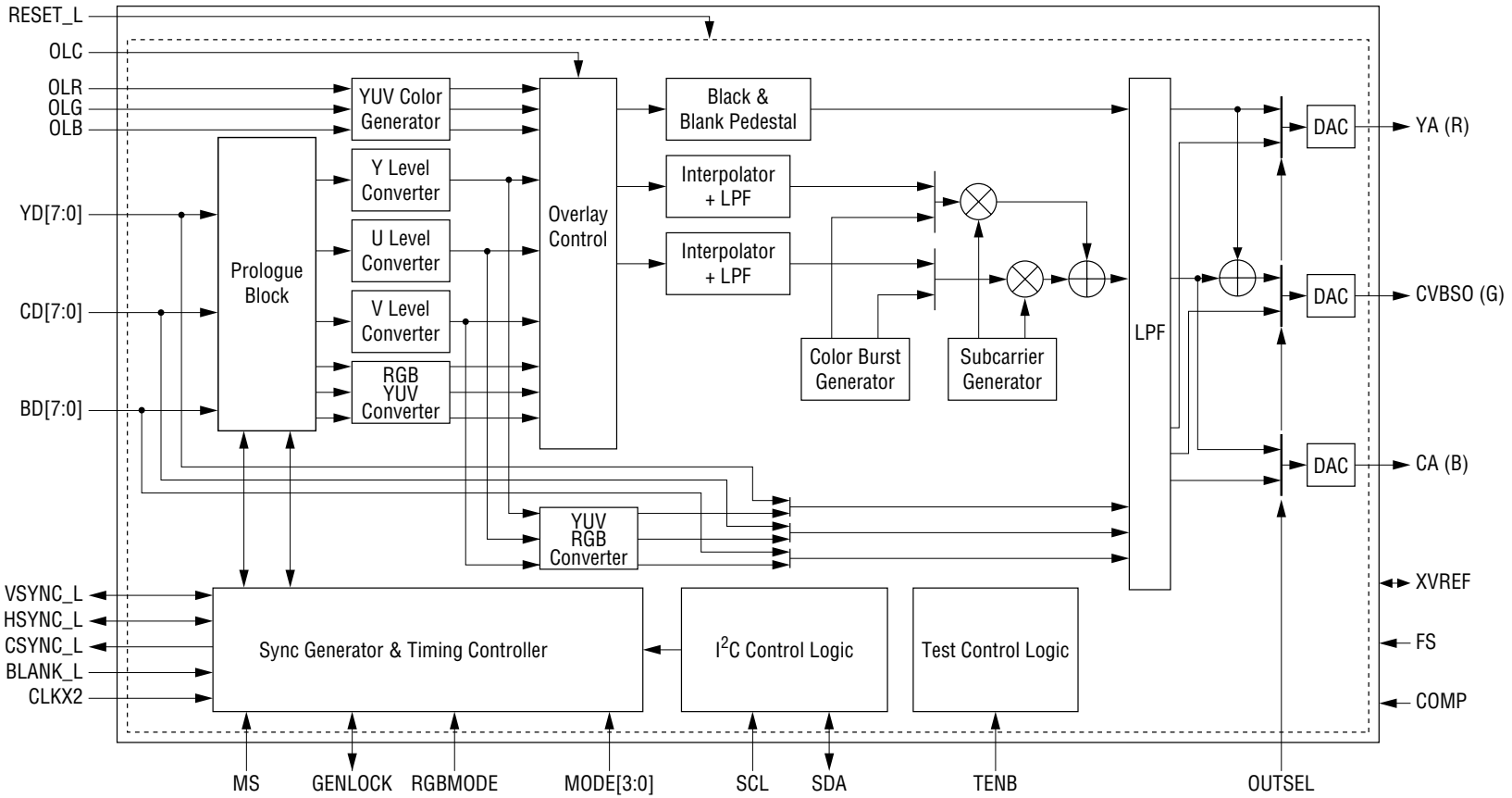
FEATURES

- Video signal system: NTSC/PAL
- Scanning system: interlaced/noninterlaced (NTSC : 262 lines/PAL : 312 lines)
- Input digital level: conforms to ITU-R BT.601 (CCIR601)
- Input-output timing: conforms to ITU-R BT.656 or ITU-R BT.624-4
- Input signal sampling ratio : Y:Cb:Cr = 4:2:2 or 4:1:1/R:G:B = 8:8:8
- Supported input interface
  - ITU-R BT.656
  - YCbCr format (8-bit input)
  - ITU-R BT.601 (8-bit (Y) + 8-bit (CbCr) input)
  - RGB (24-bit input)
- Pixel frequency (Sampling frequency) :
  - 12.272727 MHz (24.545454 MHz) : NTSC Square Pixel
  - 13.5 MHz (27 MHz) : NTSC/PAL ITU-R BT.601
  - 14.318182 MHz (28.636364 MHz) : NTSC 4Fsc
  - 14.75 MHz (29.5 MHz) : PAL Square Pixel
- Output format
  - Selectable composite & S-video or RGB
  - 37.5 Ω driving capability
- Master or slave operation (slave operation only in ITU-R BT.656 mode)
- Internal 3ch 10-bit DAC
- 3-bit title/graphics can be displayed (only for composite and S-video signals)
- Color bar function
- I^2C-bus host interface function
- Brightness level adjust of 100% to 68.75% (only for composite and S-video signals)
- GENLOCK control
- 3.3 V single power supply (each I/O pin is 5 V tolerable)
- Package
  64-pin plastic QFP (QFP64-P-1414-0.80-BK) (Product name: MSM7654GA)

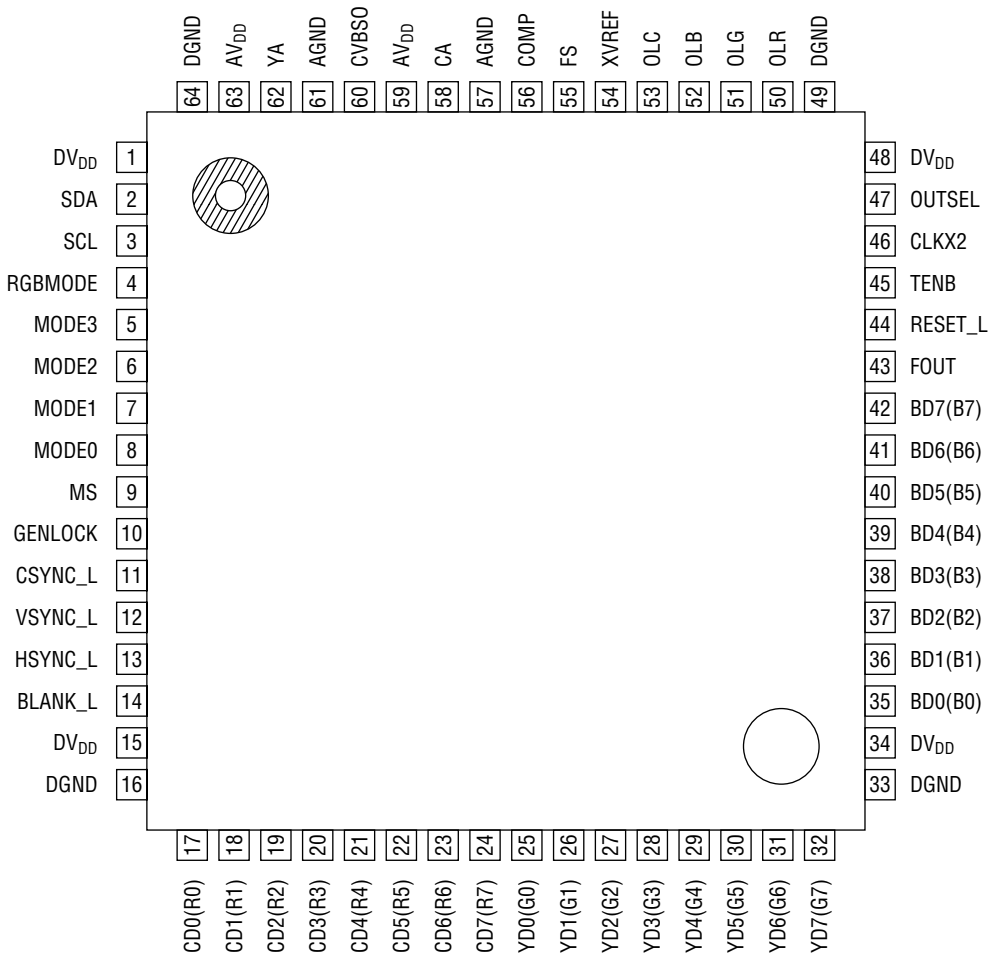
APPLICATIONS

- Video CD
- Video game equipment
- Electronic still cameras
- Video filing systems
- Video cameras
- Videophones
- Multimedia equipment
- Video printers
- Videoconferencing systems
- Scanners
- Video graphics boards
- Monitoring systems

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



64-Pin Plastic QFP

PIN DESCRIPTIONS

Pin	I/O	Symbol	Description
1		DV_{DD}	3.3 V digital power supply.
2	I/O	SDA	I^2C interface data bus.
3	I	SCL	I^2C interface clock bus.
4	I	RGBMODE	Input signal select pin. "0" : YCbCr / "1" : RGB, Internal pull-down.
5 to 8	I	MODE[3:0]	Operation mode select pin. However, sleep mode is valid while RGBMODE is "0". Internal pull-down. 0000 : NTSC ITU-R BT.656 0001 : NTSC 27 MHz YCbCr 0010 : NTSC 24.52 MHz Square Pixel 0011 : NTSC 28.64 MHz 4Fsc 0101 : NTSC 13.5 MHz YCbCr 0110 : NTSC 12.27 MHz 0111 : NTSC 14.32 MHz 1000 : PAL ITU-R BT.656 1001 : PAL 27 MHz YcbCr 1010 : PAL 29.5 MHz Square Pixel 1101 : PAL 13.5 MHz 1110 : PAL 14.75 MHz 1111 : Sleep Mode (Valid only when RGBMODE is "0")
9	I	MS	Master/slave operation selection in other modes than ITU-R BT.656. Internal pull-down. "1" : Master / "0" : Slave Only slave mode is selected in ITU-R BT.656 mode (input of "1" is invalid)
10	I/O	GENLOCK	GENLOCK signal I/O pin.
11	O	CSYNC_L	Composite sync output pin.
12	I/O	VSYNC_L	Vertical sync input/output pin (output mode in master mode/input mode in slave mode)
13	I/O	HSYNC_L	Horizontal signal input/output pin (output mode in master mode/input mode in slave mode)
14	I	BLANK_L	Composite blank signal input pin.
15		DVDD	3.3 V digital power supply.
16	I	DGND	Digital GND.
17 to 24	I	CD0 to CD7	8-bit digital image chrominance signal data input pins at pixel rate operation. Level conforms to ITU-R BT.601. R signal input pins in RGB input mode. CD7 is MSB. Fixed to "0" when not used.
25 to 32	I	YD0 to YD7	8-bit digital image data input pins at double pixel rate operation. 8-bit digital luminance signal data input pins at pixel rate operation. Level conforms to ITU-R BT.601. G signal input pins in RGB input mode. YD7 is MSB.
33		DGND	Digital GND
34		DVDD	3.3 V digital power supply
35 to 42	I	BD0 to BD7	B signal input pins in RGB input mode. Fixed to "0" when not used.
43	O	FOUT	Field information output pin (Odd Field : "1", Even Field : "0") (Polarity can be changed by the internal register.)
44	I	RESET_L	System reset pin.
45	I	TENB	Input pin for testing. Normally fixed to "0". Internal pull-down. The user cannot use this pin.
46	I	CLKX2	Clock input pin.

PIN DESCRIPTIONS (continued)

Pin	I/O	Symbol	Description
47	I	OUTSEL	Video output format select pin. "0" : S-Video & Composite / "1" RGB. Internal pull-down.
48		DV_{DD}	3.3 V digital power supply
49	I	DGND	Digital GND
50	I	OLR	Overlay text color (Red component).
51	I	OLG	Overlay text color (Green component).
52	I	OLB	Overlay text color (Blue component).
53	I	OLC	Transparent control signal. "1" indicates overlay signal.
54	I/O	XVREF	External reference voltage input pin for DAC or internal reference voltage output pin. (Reference voltage for DAC)
55	I	FS	DAC full scale adjustment pin.
56	I	COMP	DAC phase correction pin.
57		AGND	Analog GND.
58	O	CA	Analog color chrominance signal output pin or B (Blue) signal output pin.
59		AV_{DD}	3.3 V analog power supply.
60	O	CVBSO	Analog composite signal output pin or G (Green) signal output pin.
61		AGND	Analog GND.
62	O	YA	Analog luminance signal output pin or R (Red) signal output pin.
63		AV_{DD}	3.3 V analog power supply.
64		DGND	Digital GND.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	DV_{DD}	—	–0.3 to +4.5	V
	AV_{DD}	—	–0.3 to +4.5	
Digital Input Voltage	V_I	DV_{DD} = 3.3 V	–0.3 to +5.5	V
Analog Output Current	I_O	—	70	mA
Power Consumption	P_W	—	800	mW
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage (*1)	DV_{DD}	—	3.0	3.3	3.6	V
	AV_{DD}	—	3.0	3.3	3.6	
Operating Temperature 1	Ta1	DV_{DD} = AV_{DD} = 3.3 V	0	25	70	˚C
External Reference Voltage	Vrefex	DV_{DD} = AV_{DD} = 3.3 V, Ta = 25˚C	—	1.25	—	V
DA Current Setting Resistance	Riadj	(*2)	—	192.5	—	Ω
DA Output Load Resistance	R_L	(*3)	—	(75//75)	—	Ω

(*1) Supply an equal voltage to both DV_{DD} and AV_{DD}.
(*2) A volume control resistor of approx. 500 Ω is recommendable for adjusting the output current.
(*3) Indicates the value when Riadj = 192.5 Ω (typical value).

ELECTRICAL CHARACTERISTICS

DC Characteristics

(Ta = 0 to 70°C, DV_{DD} = 3.3 V ±0.3 V, AV_{DD} = 3.3 V ±0.3 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage (*1)	V_{IH}	—	2.2	—	—	V
"L" Input Voltage	V_{IL}	—	—	—	0.8	V
"H" Output Voltage	V_{OH}	I_{OH} = –4 mA (*2)	0.7DV_{DD}	—	—	V
"L" Output Voltage	V_{OL}	I_{OL} = 4 mA (*2)	—	—	0.4	V
Input Leak Current	I_I	V_I = GND to DV_{DD}	–10	—	+10	µA
Input Leak Current (with pull-down resistor)	I_{IH}	V_I = GND to DV_{DD}	20	—	250	µA
Output Leak Current	I_O	V_I = GND to DV_{DD} (*3)	–10	—	+10	µA
Power Supply Current (operating 1)	I_{DDO1}	R_L = 37.5 Ω	—	180	200	mA
Power Supply Current (operating 2)	I_{DDO2}	R_L = 75 Ω	—	140	160	mA
Power Supply Current (standby 1)	I_{DDS1}	CLKX2 = 0 MHz RESET_L = "0" R_L = 37.5 Ω	—	120	130	mA
Power Supply Current (standby 2)	I_{DDS2}	CLKX2 = 0 MHz RESET_L = "0" R_L = 75 Ω	—	60	65	mA
Power Supply Current (Sleep mode)	I_{DDSM}	MODE [3:0] = "1111" RGBMODE = "1"		1.0	2.0	mA
I²C-bus SDA Output Voltage	$SDAV_L$	Low level, I_{OL} = 3 mA	0	—	0.4	V
I²C-bus SDA Output Current	$SDAI_O$	During Acknowledge	3	—	—	mA
Internal Reference Voltage	Vrefin	—	—	1.25	—	V
DA Output Load Resistance	R_L	—		37.5		Ω
	R_L	—		75		Ω
Integral Linearity	SINL	—		±2		LSB
Differential Linearity	SDNL	—		±1		LSB

(*1) Up to 5.5 V can be input to the digital input pin (5 V tolerable)
(*2) VSYNC_L, HSYNC_L, GENLOCK, CSYNC_L, FOUT
(*3) SDA

AC Characteristics

(Ta = 0 to 70°C, DV_{DD} = 3.3 V ±0.3 V, AV_{DD} = 3.3 V ±0.3 V)

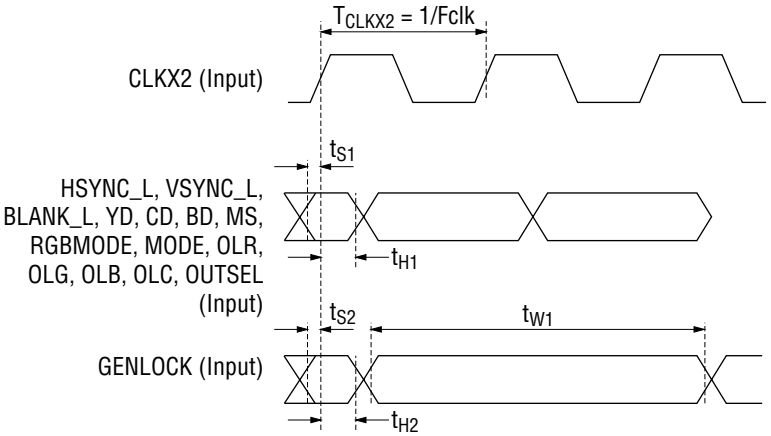
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CLKX2 Frequency (*1)	Fclk	PAL Square Pixel	—	29.5	—	MHz
		NTSC 4Fsc	—	28.636364	—	MHz
		NTSC Square Pixel	—	24.545454	—	MHz
		ITU-R BT.601/656	—	27.0	—	MHz
Input Data Setup Time 1	t_{S1}	—	2.5	—	—	ns
Input Data Setup Time 2	t_{S2}	—	0.0	—	—	ns
Input Data Hold Time 1	t_{H1}	—	10.0	—	—	ns
Input Data Hold Time 2	t_{H2}	—	11.08	—	—	ns
GENLOCK Minimum Pulse Width	t_{W1}	—	93.0	—	—	ns
Output Delay Time 1	t_{D1}	—	6.0	—	18.0	ns
Output Delay Time 2	t_{D2}	—	7.0	—	25.0	ns

(*1) If high precision is needed for sub-carrier/synchronization signals, clocks within ±100 ppm(typ.) should be provided.

TIMING DIAGRAMS (SWITCHING CHARACTERISTICS)

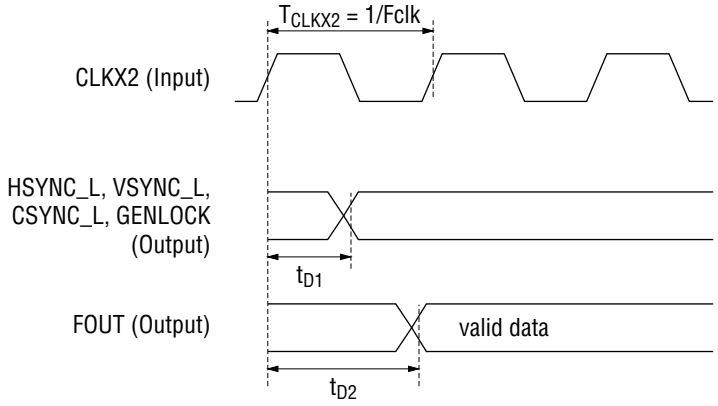
1) Setup/Hold Time

The input data is fetched in the encoder at the rising edge of CLKX2.
T_{CLKX2}: Input clock period



Input Timing

2) Output Delay Time



Output Timing

3) I²C-bus Interface Input/Output Timing

When writing to internal registers, written contents are set to the internal registers MR1 [7] and CR0 [2:1] during the vertical blanking period. On the other hand, written contents are immediately set to the other internal registers.

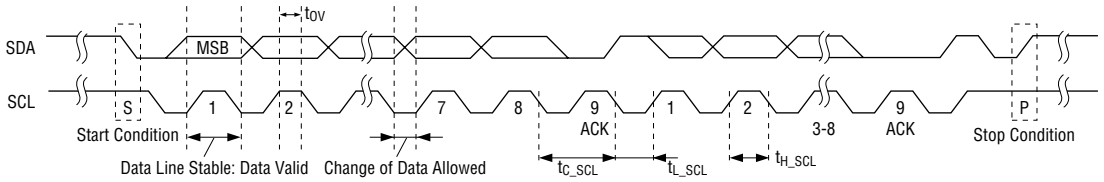
(Note) Data cannot be changed when SCL is "H". Data line can be changed only when SCL is "L".

The I²C-bus Interface Basic Input/Output Timing is shown below.

I²C-bus AC Characteristics

($Ta = 0$ to 70°C, $DV_{DD} = 3.3\ V \pm 0.3\ V$, $AV_{DD} = 3.3\ V \pm 0.3\ V$)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
I²C-bus Clock Cycle Time	t_{C_SCL}	Rpull_up = 4.7 kΩ	200	—	—	ns
I²C-bus High Level Cycle	t_{H_SCL}	Rpull_up = 4.7 kΩ	100	—	—	ns
I²C-bus Low Level Cycle	t_{L_SCL}	Rpull_up = 4.7 kΩ	100	—	—	ns
SDA-SCL Overlap Time	t_{OV}	Rpull_up = 4.7 kΩ	40	—	—	ns



I²C-bus Input/Output Basic Timing

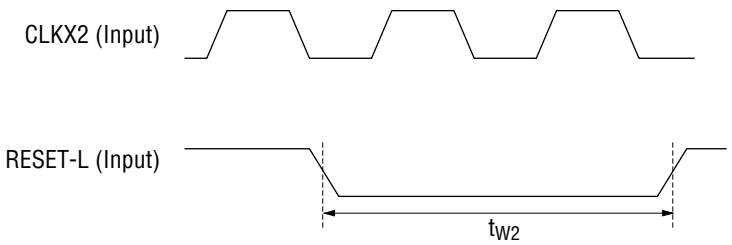
4) Reset Input Timing

The reset timing is asynchronous with the clock timing.

Reset AC Characteristics

($Ta = 0$ to 70°C, $DV_{DD} = 3.3\ V \pm 0.3\ V$, $AV_{DD} = 3.3\ V \pm 0.3\ V$)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Minimum Reset Pulse Width	t_{W2}	—	81.5	—	—	ns



Reset Timing

BLOCK FUNCTIONAL DESCRIPTION

- **Prologue Block**
  This block separates input data at the ITU-R BT.656 format into a luminance signal (Y) and a chrominance signal (Cb & Cr), and also generates information concerning sync signals HSYNC_L, VSYNC_L, and BLANK_L.
  This block separates input data at the 27 MHz YCbCr (8-bit input) format into a luminance signal (Y) and a chrominance signal (Cb & Cr).
  This block separates input data at the 13.5 MHz YCbCr (16-bit input) format into a chrominance signal Cb and a chrominance signal Cr.
  Of the processed input data, luminance and chrominance signals other than valid pixel data are replaced by 8'h10 and 8'h80 respectively.
  RGB signals are converted into luminance (Y) and chrominance (Cb & Cr) signals.

- **Y Limiter Block**
  This block limits the luminance input signal by clipping the lower limit of an input signal outside the ITU-R BT.601 Standard
  • Signals are limited to YD = 16 when YD < 16.
  • Signals are limited to YD = 254 when YD (input during a valid pixel period) = 255.
  In other cases, signals are fed as is to next processing.

- **C Limiter Block**
  This block limits the chrominance signal by clipping the upper and lower limits of the input signal outside the ITU-R BT.601 Standard.
  CD = 1 when CD = 0 is input during a valid pixel period.
  CD = 254 when CD = 255 is input during a valid pixel period.

- **Y Level Converter Block**
  Converts ITU-R BT.601 standard luminance signal level to DAC digital input level.

- **U Level Converter Block**
  Converts ITU-R BT.601 standard chrominance signal level to DAC digital input level.

- **V Level Converter Block**
  Converts ITU-R BT.601 standard chrominance signal level to DAC digital input level.

- **RGB YUV Level Converter Block**
  Converts RGB signals to YUV signals at a DAC digital input level.

- **YUV Color Generator Block**
  This block generates luminance and chrominance signals from overlay color signals OLR, OLG and OLB. The control signal (register CR0[3:1]) controls the output content and output level. The output content of overlay or color bar is selected with register CR0[3] and the output level of 100%, 75%, 50%, or 25% is selected with register CR0[2:1].

- **Overlay Control Block**
  This block selects input image data or YUV Color Generator output signals.
  It is determined by the level of the control signal (OLC, CR [3]), as shown below: (x : don't care)
  CR [3] = 1, OLC = x: Selects color bar signal (YUV Color Generator output signal).
  CR [3] = 0, OLC = 1: Selects overlay signal (YUV Color Generator output signal).
  CR [3] = 0, OLC = 0: Selects input image data.

- **YUV to RGB Converter Block**
  This block converts YUV signals separated by the prologue block into RGB signals.

- **Black & Blank Pedestal Block**
  This block adds sync signals at the luminance side to luminance signals.

- **Interpolator + LPF Block**
  This block executes data interpolation and the elimination of high frequency components by LPF for input chrominance signals.

- **I^2C Control Logic Block**
  This is the serial interface block based on I^2C standard of Phillips Corporation.
  Internal registers (MR0 and MR1) and command registers (CR0 and CR1) can be set from the master side.
  When writing to the internal registers other than MR1 [7] (black level control) and CR0 [2:1] (overlay level), written contents are immediately set to them. It is during the vertical blanking period that written contents are set to MR1 [7] and CR0 [2:1].

- **Sync Generator & Timing Controller Block**
  This block generates sync signals and control signals.
  This block operates in slave mode, which performs external synchronization, and in master mode, which internally generates sync signals.

- **Color Burst Generator Block**
  Outputs U and V components of amplitude of burst signals.

- **Subcarrier Generator Block**
  Executes color subcarrier generation.

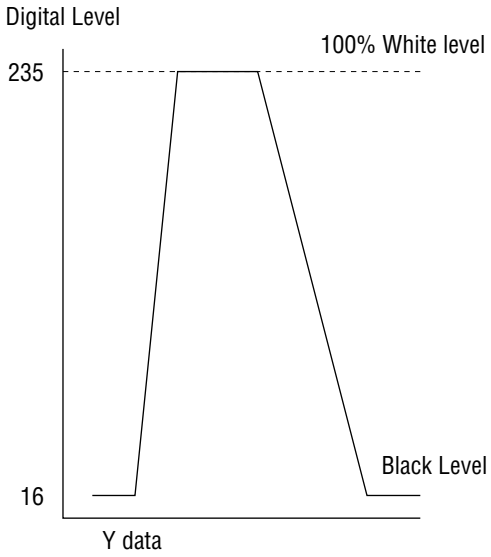
- **Low Pass Filter (LPF) Block**
  This block performs upsampling at CLKX2 for luminance signals and chrominance signals modulated with CLKX1 divided from CLKX2. Interpolation processing is executed in this process.

- **DAC Block**
  This block converts digital video signals to analog video signals with a 10-bit accuracy and outputs them. Since the analog output pins (YA, CVBSO, CA) are current outputs, these pins should be connected to external resistors. See "Analog output reference circuit in APPLICATION CIRCUIT EXAMPLE" for resistance values.

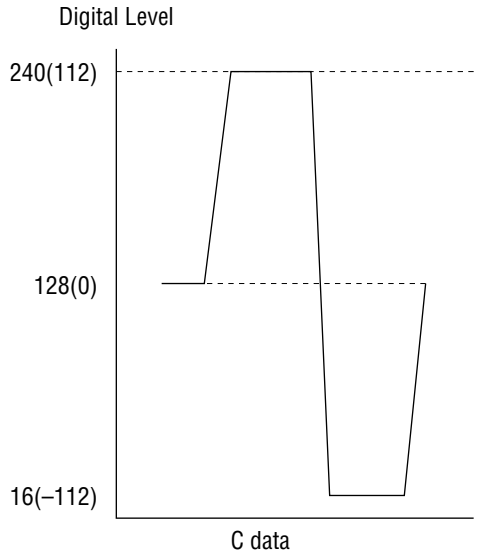
INPUT DATA FORMAT

1) Input Level 1 (YCbCr format)

The signal level specified by the ITU-R BT.601 is input.
When other signal levels than specified by the ITU-R BT.601 are input, the luminance signal level is clipped to 16 to 254 and the chrominance signal level to 1 to 254.
For chrominance signal input, the offset binary or 2's complement format is available by setting of internal register MR0[6].



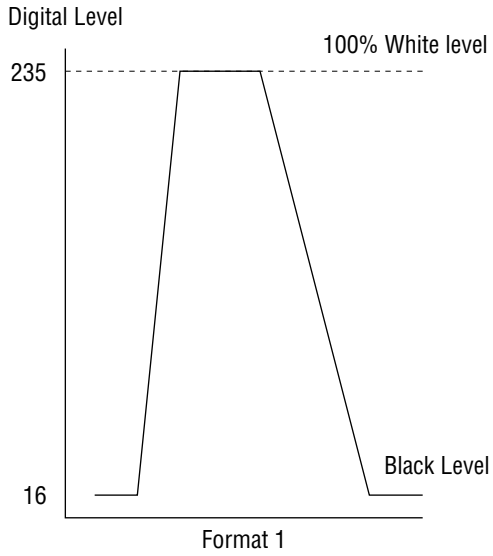
Input luminance signal level



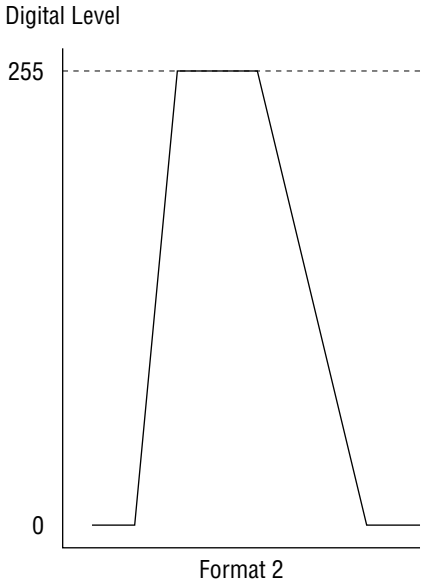
Input chrominance signal level

2) Input Level 2 (RGB format)

Two types of input level are available by setting of internal register MR1[5].



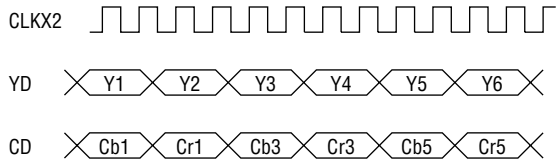
Input RGB signal level 1



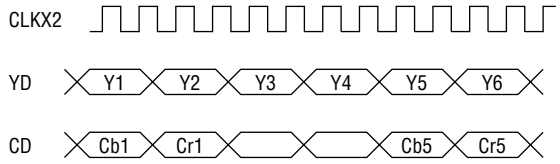
Input RGB signal level 2

3) Basic Pixel Sampling Ratio

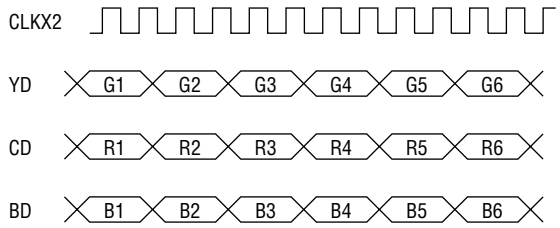
4:2:2 or 4:1:1 is supported. The internal register CR0[0] is used to control.



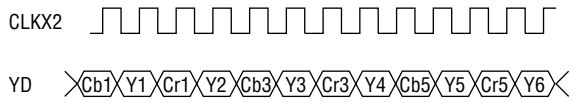
4:2:2 sampling at 8bit Y/8bit CbCr input



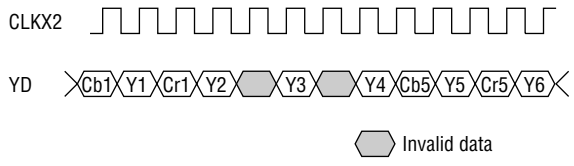
4:1:1 sampling at 8bit Y/8bit CbCr input



At RGB input



4:2:2 sampling at 8bit YCbCr input



4:1:1 sampling at 8bit YCbCr input

4) Scanning System

NTSC and PAL systems support both interlaced scanning and non-interlaced scanning.

NTSC	Interlaced	262.5 lines at 60 Hz
NTSC	Non-interlaced	262 lines at 60 Hz
PAL	Interlaced	312.5 lines at 50 Hz
PAL	Non-interlaced	312 lines at 50 Hz

In the master mode, it is possible to select the desired setting from the above settings by switching the internal registers. In the master mode, only odd fields can be consecutively scanned. In the slave mode, it is possible to consecutively output odd fields or even fields by using phase information from VSYNC_L and HSYNC_L.
Since either odd fields or even fields are consecutively output, the resolution is halved. However, setting of non-interlaced scanning eliminates flicker of the screen display which appears when moving of pictures is stopped in the interlaced scanning.

5) I²C Bus Format

The input format of I²C-bus interface is shown below.

S	Slave Address	A	Subaddress	A	Data 0	A	.....	Data n	A	P

Symbol	Description
S	Start condition
Slave Address	Slave address 1000100X. The 8th bit is write (0) signal.
A	Acknowledge. Generated by slave
Subaddress	Subaddress byte
Data n	Write to the address specified by the subaddress.
P	Stop condition

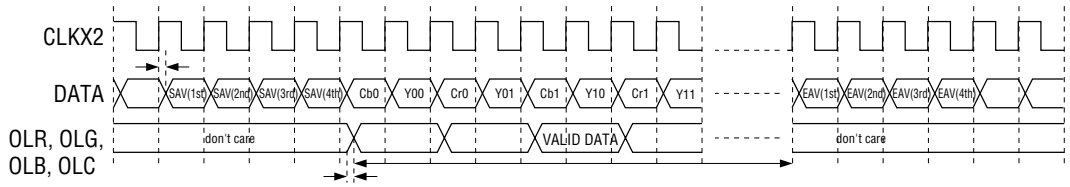
As described above, it is possible to write data from subaddress to subaddress continuously. Writing to discontinuous addresses is performed by repeating the Acknowledge and Stop condition formats after Data 0.

If one of the following matters occurs, the encoder will not return "A" (Acknowledge).

- The slave address does not match.
- A non-existent subaddress is specified.
- The write attribute of a register does not match "X" which is the 8th bit (LSB) of the slave address ("X" = 0 because this LSI is write only).

INPUT TIMING 1 (ITU-R BT.656 input)

The input data is fetched in the encoder at the rising edge of a clock pulse.



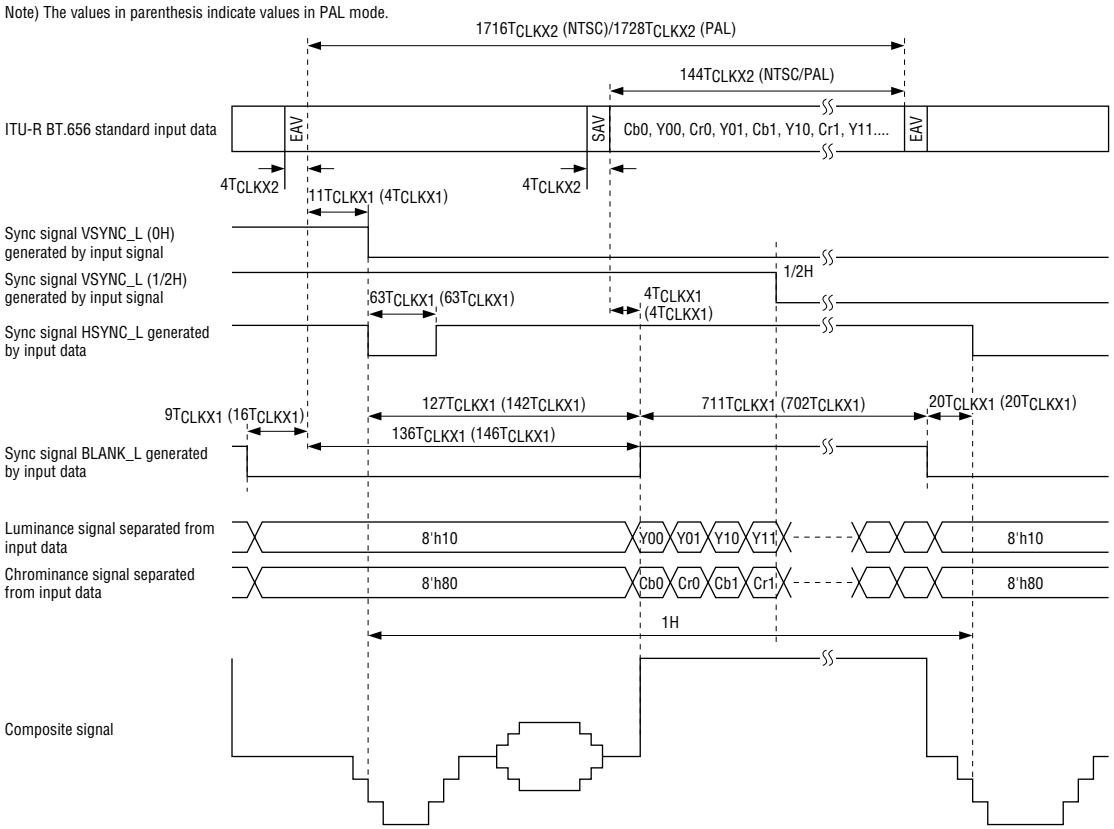
Input timing

Relationship Between Blank Signal and Input Image Data

The blank signal is generated by the ITU-R BT.656 standard input data. The input image data is valid when the blank signal is "H".

Valid Data Range

According to the ITU-R BT.656 standard, the pixel data immediately from SAV (4th word) to a fixed value before EVA is valid.
The following figure shows the relationship between the input data at the ITU-R BT.656 format and the sync, luminance, chrominance signals which are processed inside the encoder.



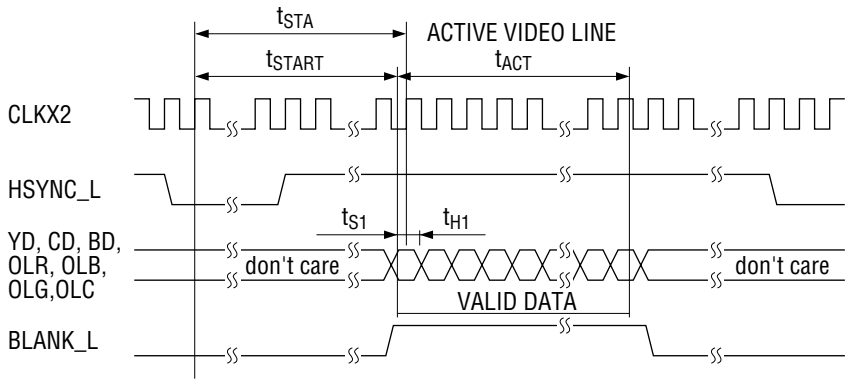
Relationship between input data and sync signal, luminance signal, chrominance signals

INPUT TIMING 2 (8bit Y/8bit CbCr input, 8bit YCbCr & RGB input)

Input Data Timing

Input data and sync signals are fed into the encoder at the rising edge of CLKX2.

Input data is handled as valid pixel data when t_{START} passes after the falling edge of HSYNC_L. Chrominance signal of input data at this time is regarded as Cb.



Video data input timing

Input data is recognized as valid pixel data when input signal BLANK_L is "H" in the t_{ACT} period. When BLANK_L is "H" during the blanking period, however, input data is not output as valid pixel data since processing to maintain blanking period is internally in-progress.

The values of t_{STA} differ slightly between in master mode and in slave mode. The values of t_{STA} are as follows.

In YCbCr format input mode, the values of t_{STA} are the same, in 8 bit (Y) + 8 bit (CbCr) mode, in 8 bit (YCbCr) mode, or in RGB mode.

In master mode

Operation mode	$t_{STA}(T_{CLKX2})$
ITU-R BT.601 NTSC	250
ITU-R BT.601 PAL	280
4 Fsc NTSC	266
Square pixel NTSC	228
Square pixel PAL	306

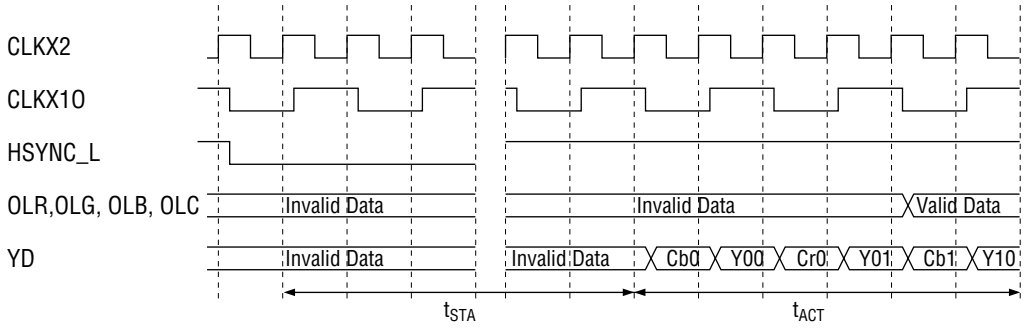
In slave mode

Operation mode	$t_{STA}(T_{CLKX2})$
ITU-R BT.601 NTSC	260
ITU-R BT.601 PAL	290
4 Fsc NTSC	276
Square pixel NTSC	238
Square pixel PAL	316

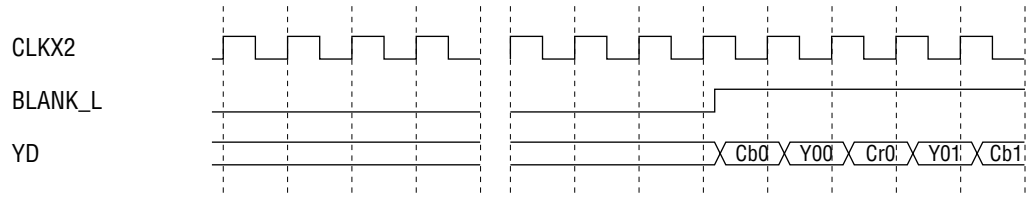
$t_{STA} - t_{S1} = t_{START}$

Input Timing at Double Speed Pixel Rate YCbCr Format

1) Timing of Input Data to HSYNC_L

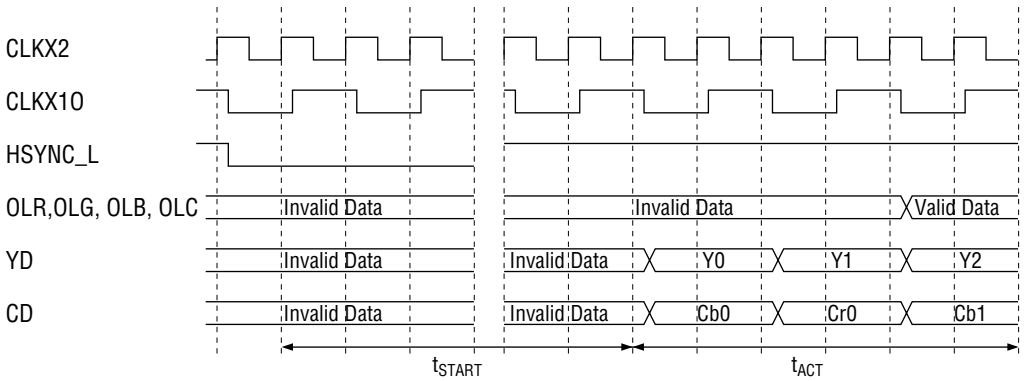


2) Input Timing when BLANK_L is Input

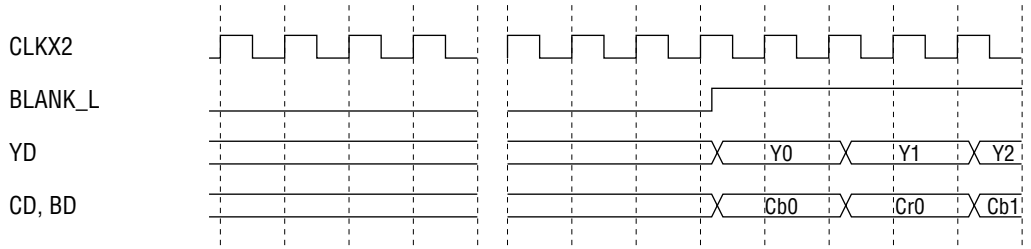


Input Timing at Pixel Rate and RGB YCbCr Format

1) Timing of Input Data to HSYNC_L



2) Input Timing when BLANK_L is Input

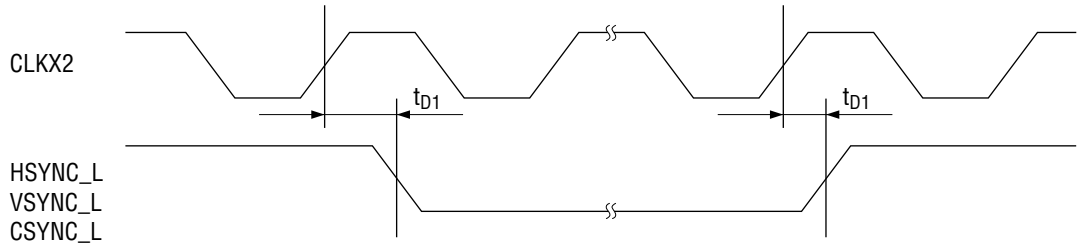


SYNC SIGNALS (VSYNC_L, HSYNC_L) I/O TIMING

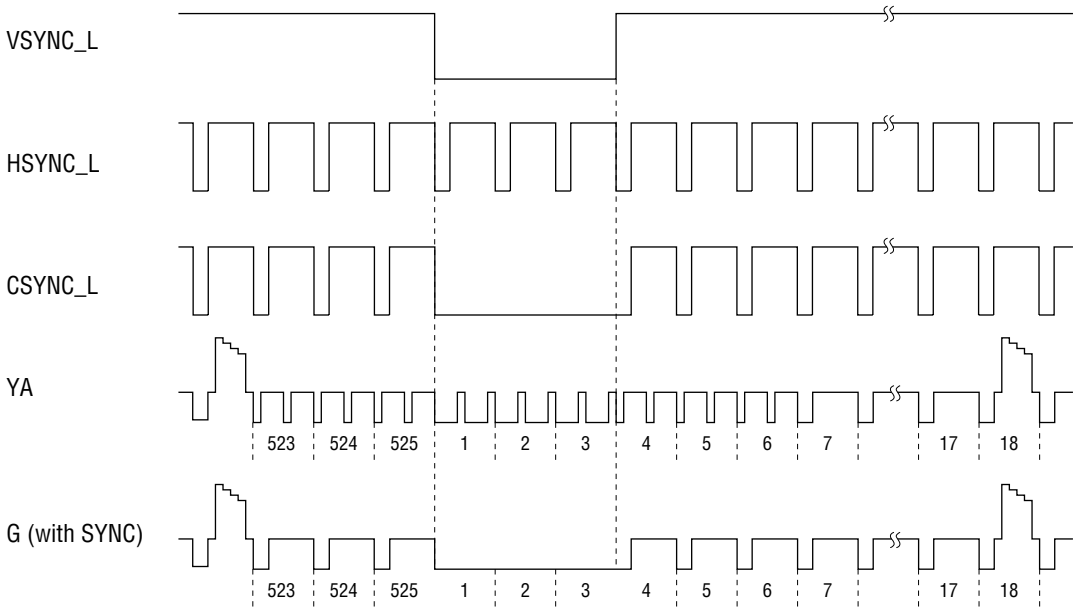
By setting the external terminal MS or internal register, this function enables either operation in the master mode in which the sync signals HSYNC_L and VSYNC_L are internally generated or operation in the slave mode in which the encoder operates by using the external HSYNC_L and VSYNC_L (See "SETTINGS OF EACH MODE" for switching between master mode and slave mode). The field is judged by using the generated HSYNC_L and VSYNC_L.

Master Mode

Output timing of HSYNC_L and VSYNC_L in master mode is as follows.



Output timing 1 of internal synchronization, HSYNC_L, VSYNC_L, and CSYNC_L



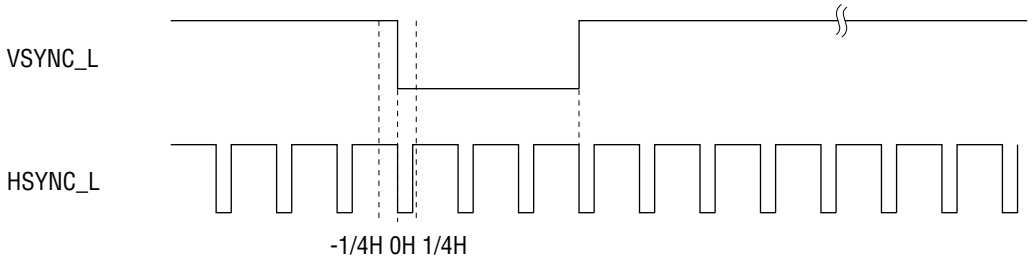
Output timing 2 of internal synchronization HSYNC_L, VSYNC_L, and CSYNC_L

Slave Mode

Input timing of VSYNC_L and HSYNC_L in slave mode is as follows.

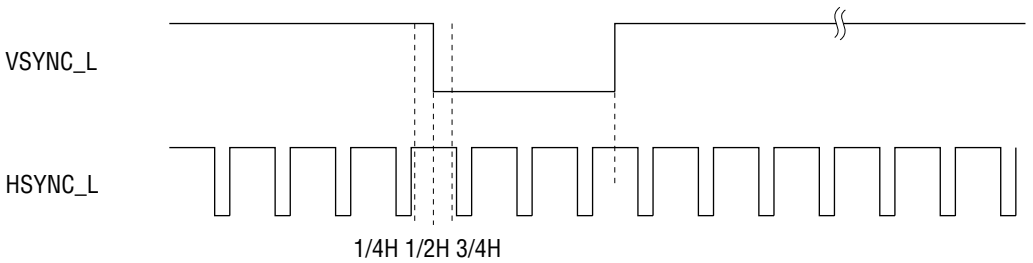
1) Odd field judgment

(1) If the encoder detects the VSYNC_L falling edge between -1/4H and 0H (not including 0H), it judges information with HSYNC_L and VSYNC_L as an odd field and normally operates.
(2) If the encoder detects the VSYNC_L falling edge between 0H and 1/4H (including 0H), it judges information with HSYNC_L and VSYNC_L as an odd field and normally operates.



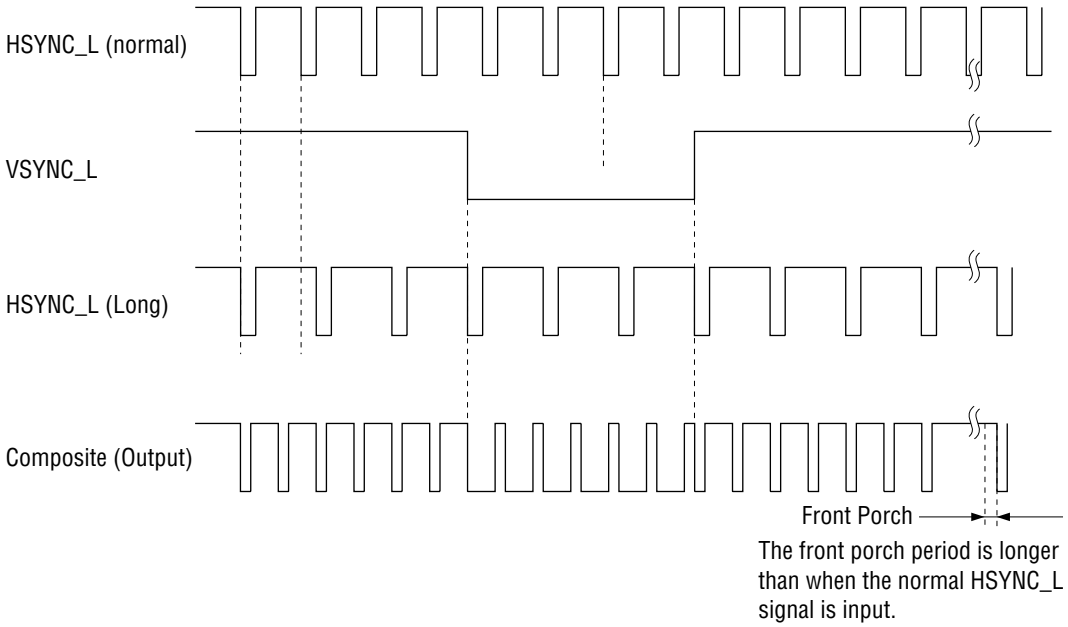
2) Even field judgment

(1) If the encoder detects the VSYNC_L falling edge between 1/4H and 1/2H (not including 1/2H), it judges information with HSYNC_L and VSYNC_L as an even field and normally operates.
(2) If the encoder detects the VSYNC_L falling edge between 1/2H and 3/4H (including 1/2H), it judges information with HSYNC_L and VSYNC_L as an even field and normally operates.



The normal vertical blanking periods cannot be obtained in the following cases:

(1) If the HSYNC_L peiod is longer than the standard, the vertical blanking period is output in the HSYNC_L period unless the pixel counter overflows in one line.
However, in the waveform the front porch period becomes longer.



When the pixel counter overflows, the encoder recognizes that the HSYNC_L signal has been input when the pixel counter becomes zero and the next line starts.
The following HSYNC_L signal resets the pixel counter again.
Therefore, inputting such a signal not only disturbs signals in the vertical blanking period but also causes abnormal operations in the horizontal period.

(2) If the HSYNC_L period is shorter than the standard, serrations may be lost.

(3) If the VSYNC_L period is longer than the standard, the vertical blanking period is output as shown below.

- If the number of lines is greater than the standard value, the first equalizing pulse period is longer.
- If the number of lines is equal to the standard value, the contents of output signals per line are normal.
- If the number of lines is smaller than the standard value, the first equalizing pulse period is shorter.

(4) If the VSYNC_L period is shorter than the standard, the vertical blanking period is output as shown below.

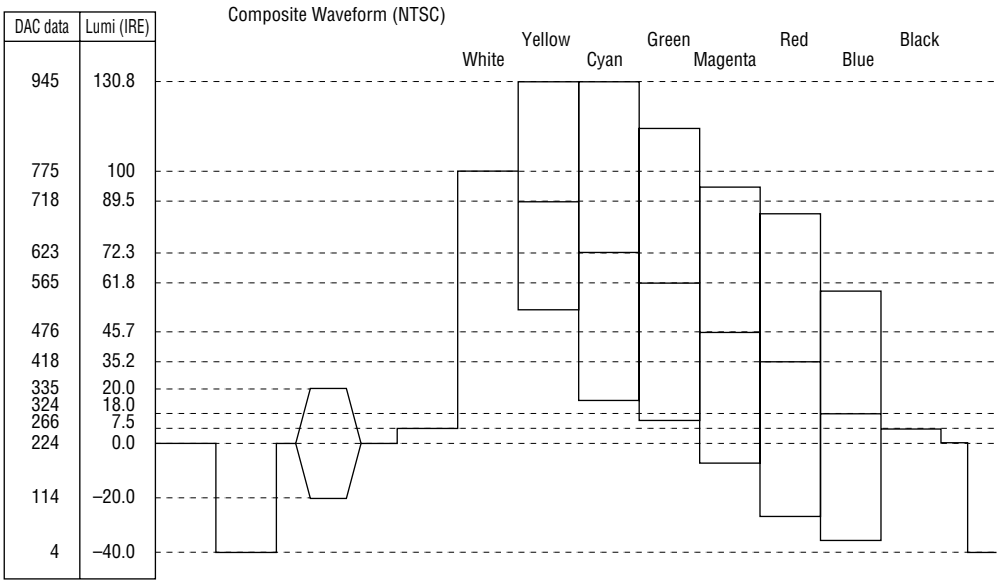
- If the number of lines is greater than the standard value, the first equalizing pulse period is longer.
- If the number of lines is equal to the standard value, the contents of output signals per line are normal.
- If the number of lines is smaller than the standard value, the first equalizing pulse period is shorter.

OUTPUT FORMAT

The timing conforms to the ITU-R BT.624-4 standard.
In the NTSC operation mode, the existence/non-existence of setup level is selected by setting of internal regsiters.

Data level on the DAC input terminal:
When the contents of 100% luminance order color bar are input into the encoder, the input level is as follows.

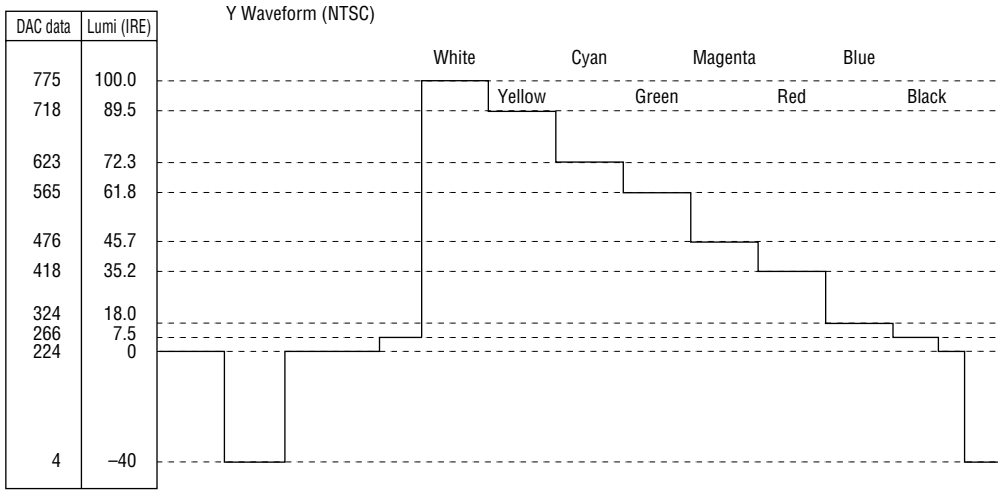
NTSC Composite Signal (Setup 7.5IRE)



NTSC Composite Signal (Setup 7.5)

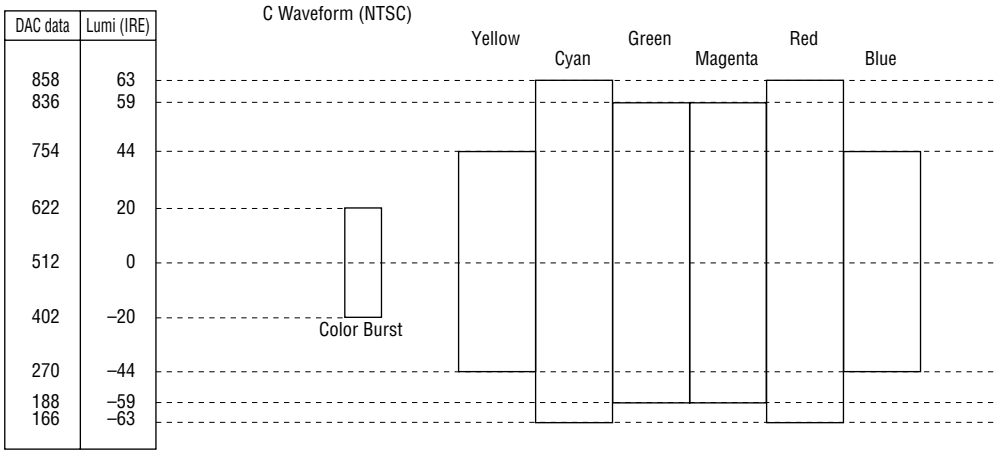
NTSC S-Video Signal (Setup 7.5IRE)

• Luminance (Y) signal output



NTSC Y Signal Output (Setup 7.5)

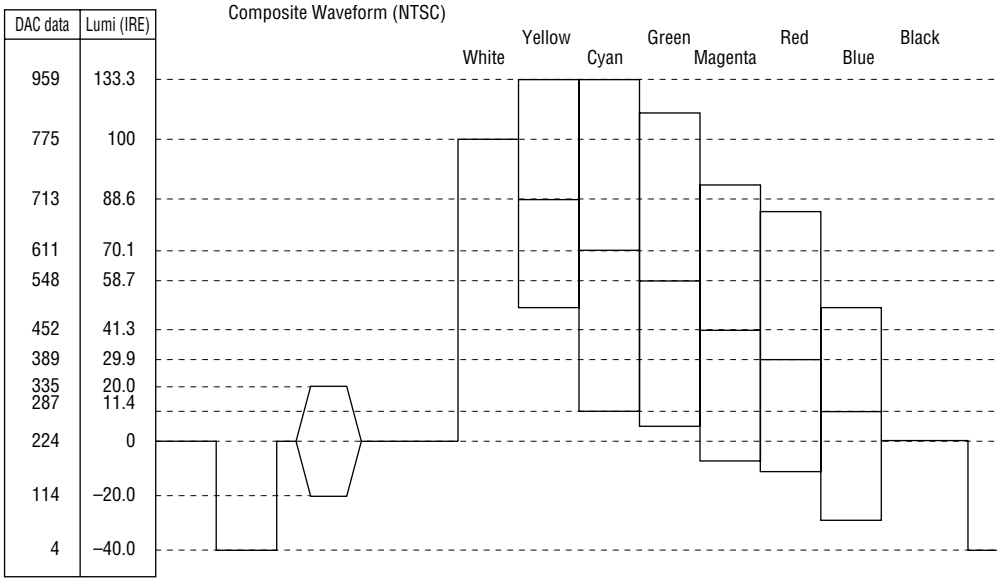
• NTSC chrominance (C) signal output



NTSC C Signal Output (Setup 7.5)

NTSC S-Video Signal (Setup 0IRE)

• Luminance (Y) signal output

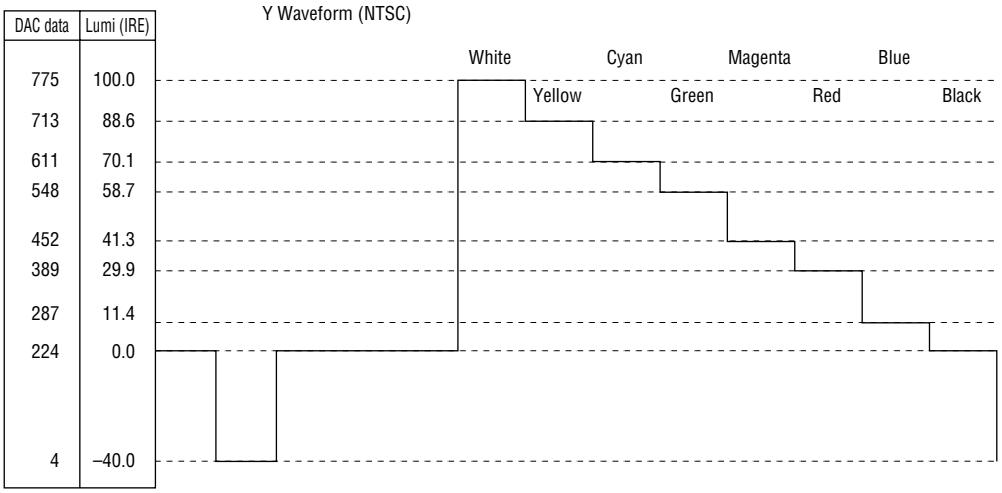


NTSC Composite Signal (Setup 0)

NTSC S-Video Signal (Setup 0IRE)

• Luminance (Y) signal output

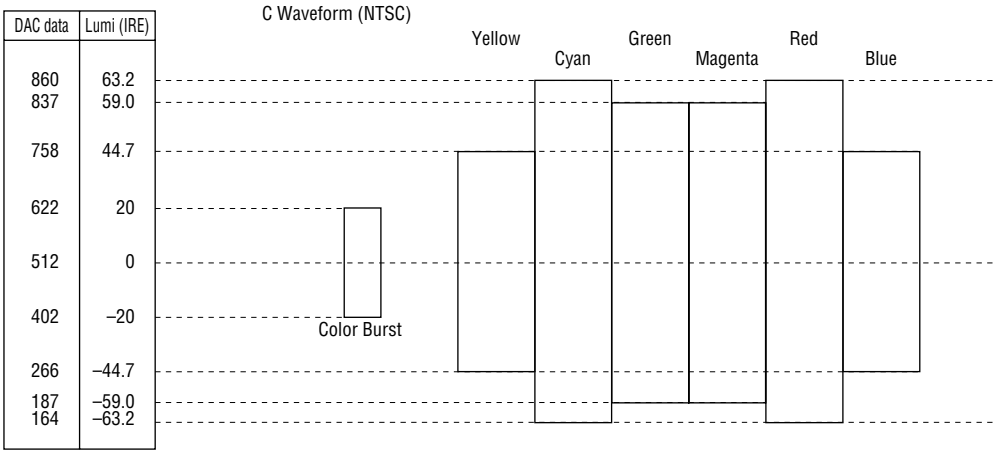
DAC data	Lumi (IRE)
775	100.0
713	88.6
611	70.1
548	58.7
452	41.3
389	29.9
287	11.4
224	0.0
4	–40.0



NTSC Y Signal Output (Setup 0)

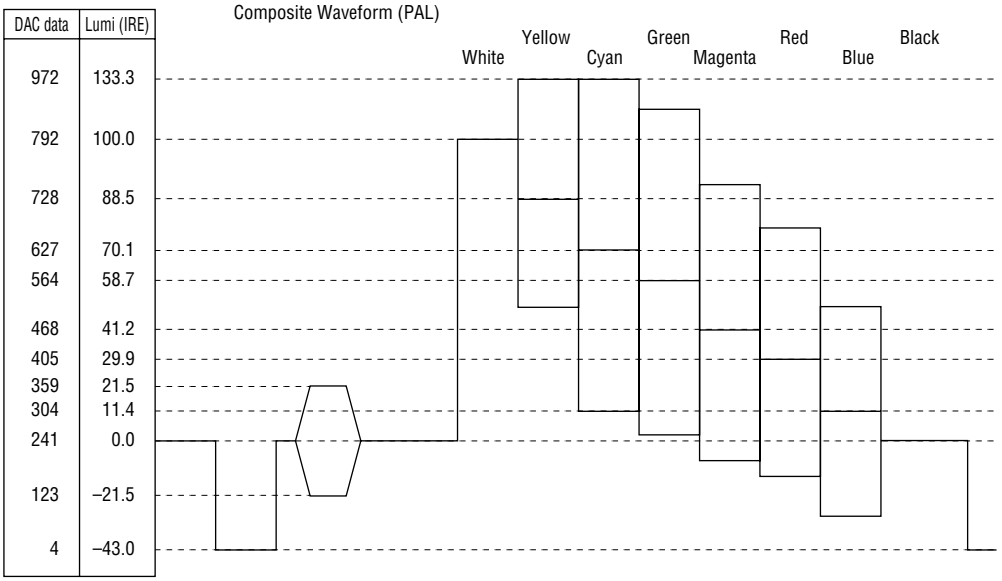
• NTSC chrominance (C) signal output

DAC data	Lumi (IRE)
860	63.2
837	59.0
758	44.7
622	20
512	0
402	–20
266	–44.7
187	–59.0
164	–63.2



NTSC C Signal Output (Setup 0)

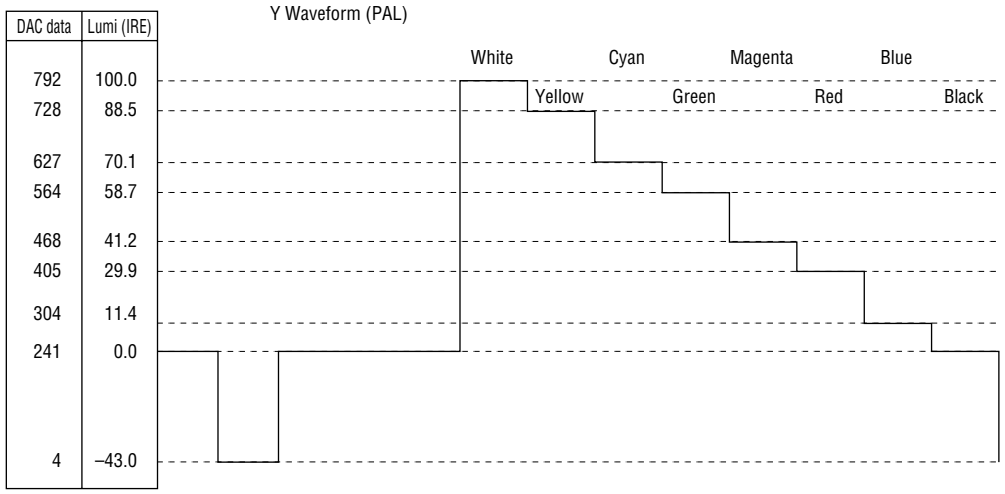
PAL Composite Signal



PAL Composite Signal

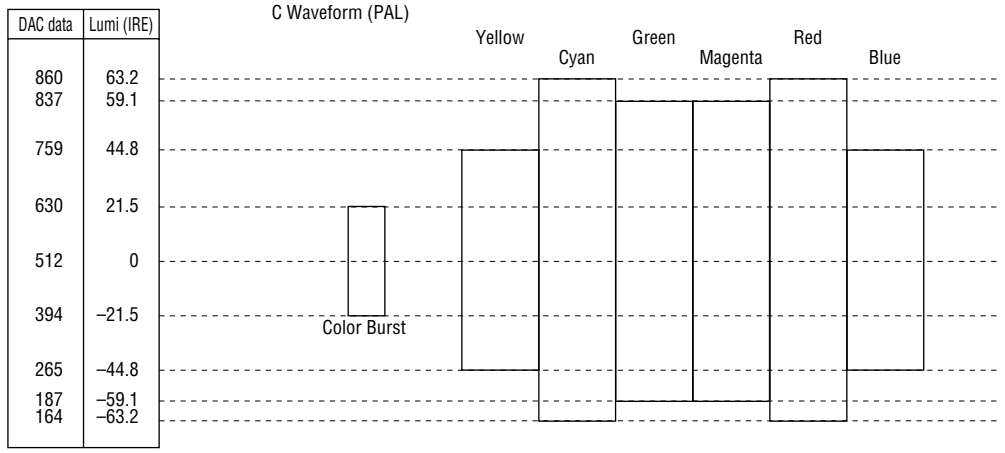
PAL S-Video Signal

• PAL luminance (Y) signal output



PAL Y Signal Output

• PAL chrominance (C) signal output

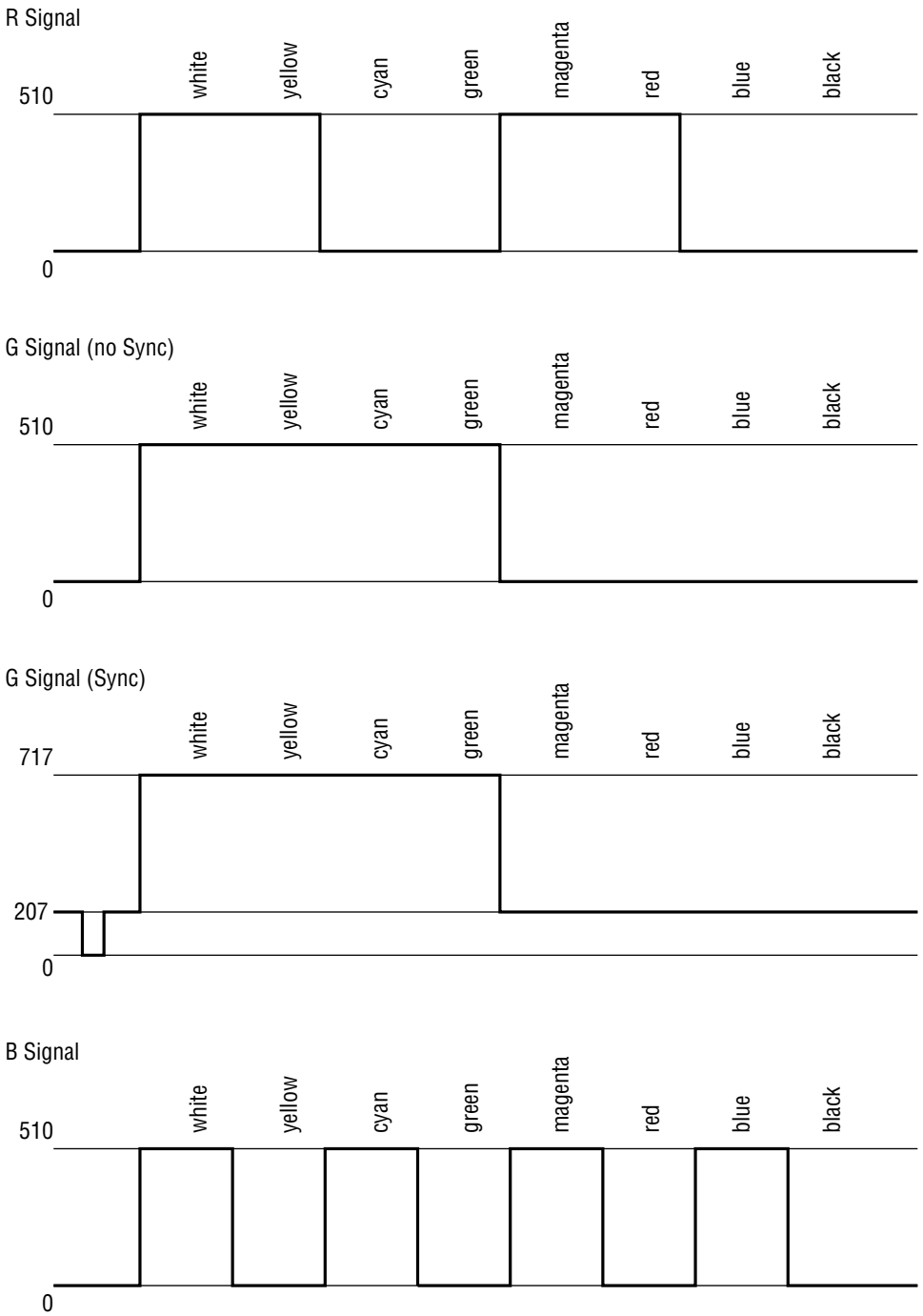


PAL C Signal Output

RGB Output Waveform

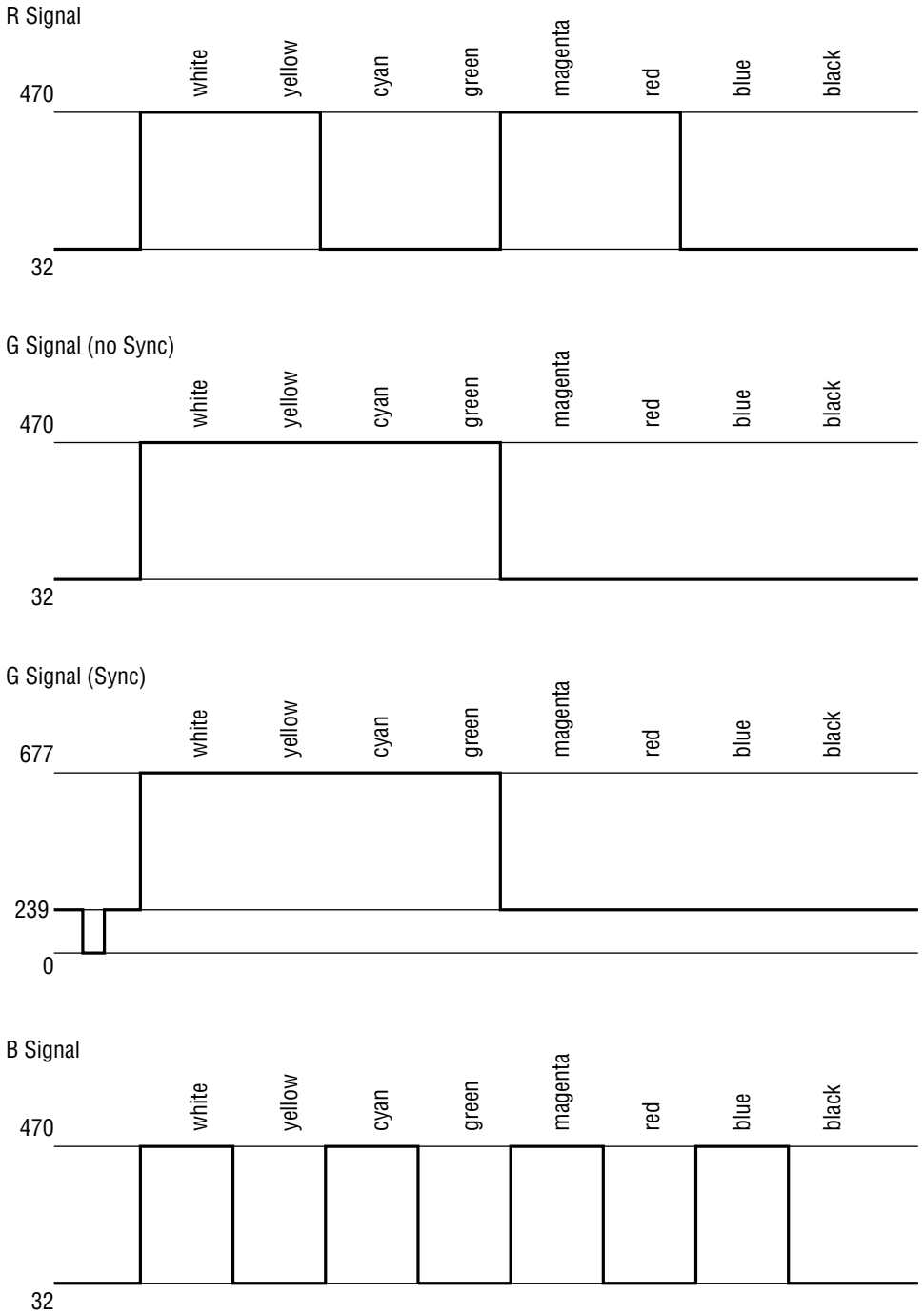
1) Output level setting: 0-510 (MR1[5] = 0)

Whether or not the Sync signal is added to the G signal is determined by setting of register CR0[6]. (CR0[6] = "0": No Sync is added, CR0[6] = "1": Sync is added)



RGB Signal (Output Level Setting: 0-510)

2) Output level setting: 32-470 (MR1[5] = 1)

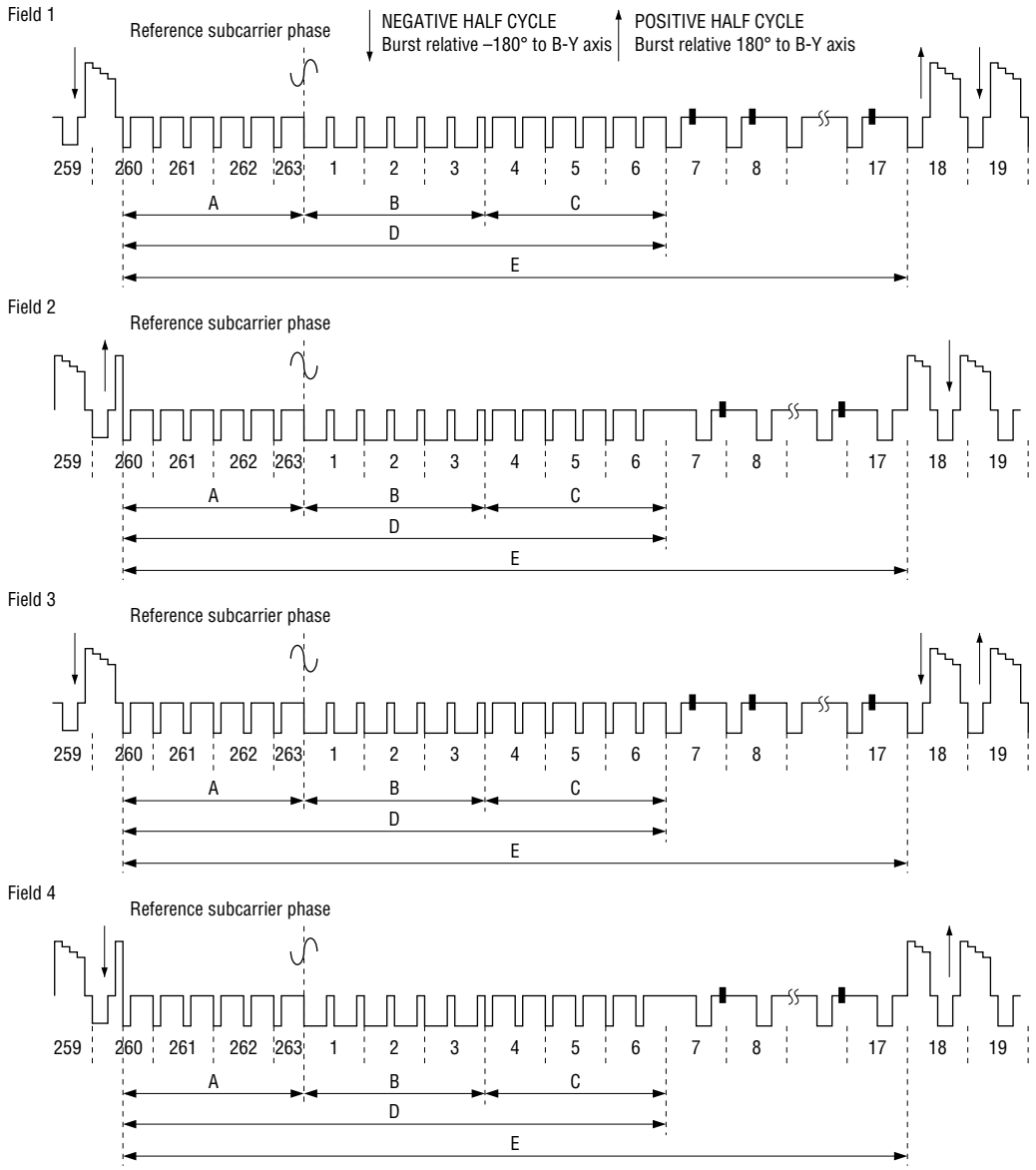


RGB Signal (Output Level Setting: 32-470)

NTSC/PAL OUTPUT TIMING

The output timing conforms to the ITU-R BT.624-4 standard.
Shown below are the output waveforms of composite signals with the interlaced or non-interlaced scanning method in the NTSC or PAL operation mode.

NTSC (Interlaced)

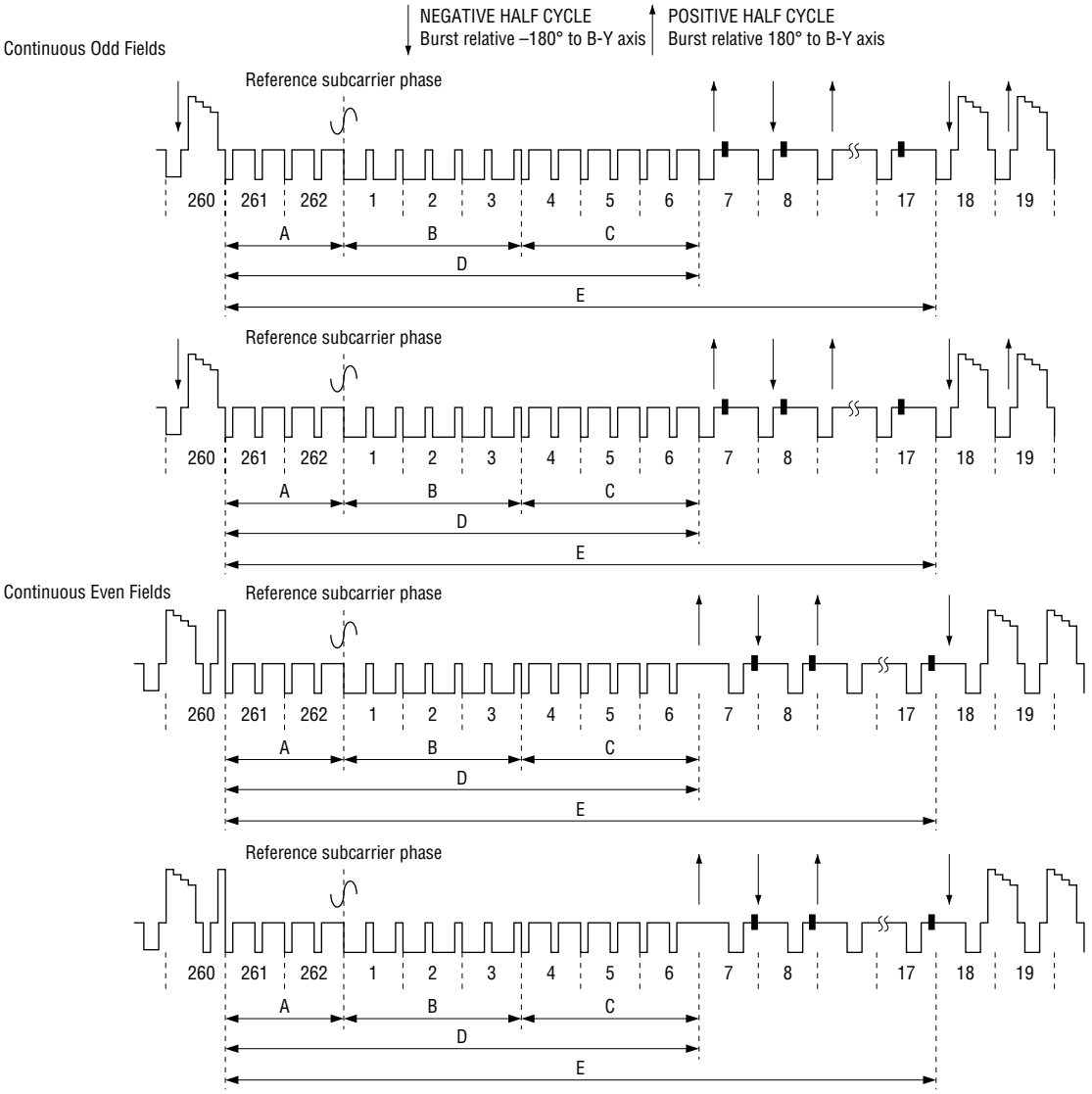


Output timing (Interlaced NTSC)

Symbol	Name	Period
		Odd field (Even field)
A	First equalizing pulse period (3H)	259.5 to 262.5H
B	Vertical synchronization period (3H)	1 to 3H
C	Second equalizing pulse period (3H)	4 to 6H
D	Burst pause period	1 to 6,259.5 to 262.5H
E	Vertical blanking period (20H)	1 to 17,259.5 to 262.5H

Output timing (Interlaced NTSC)

NTSC (Non-interlaced)

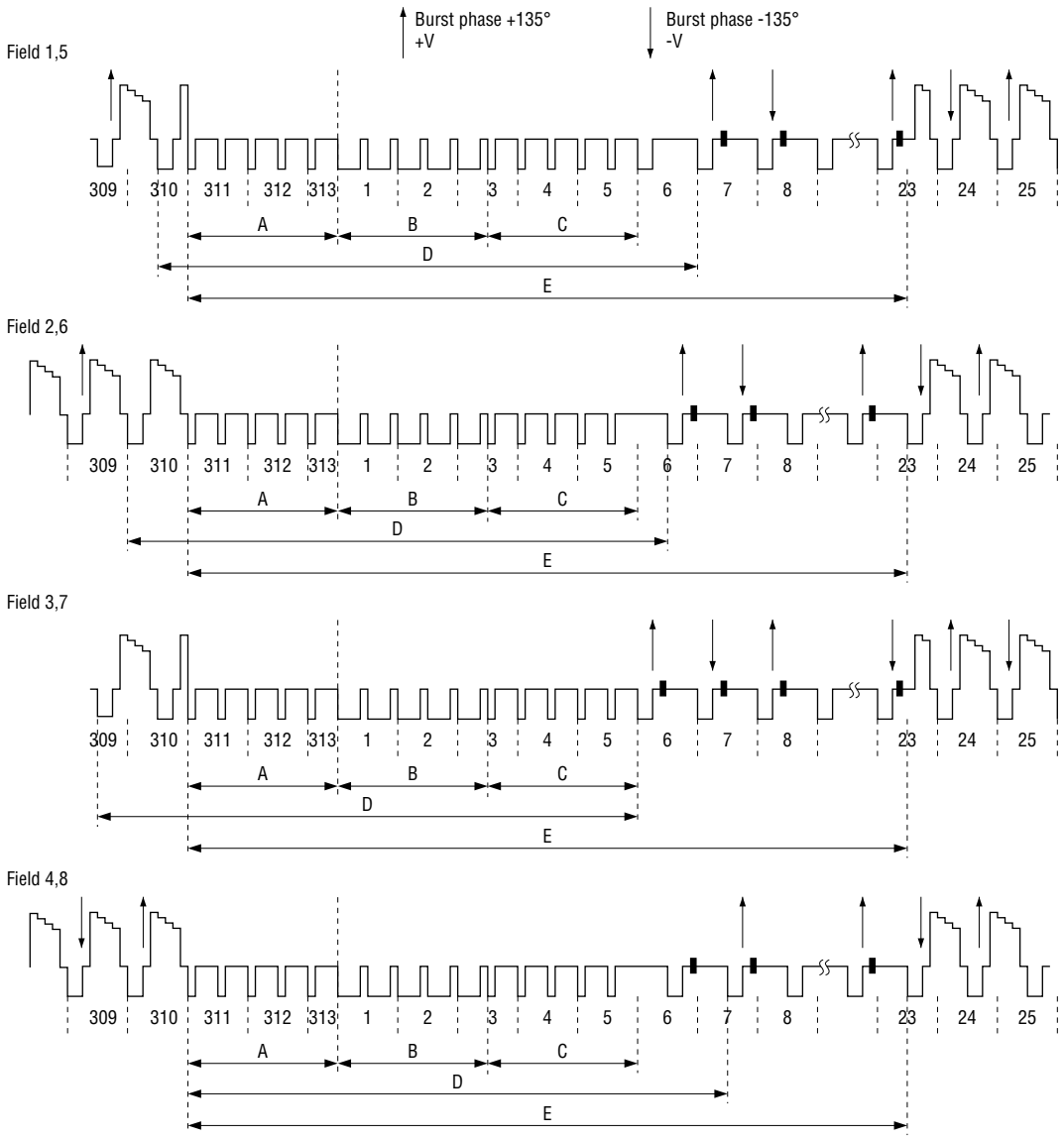


Output timing (Non-interlaced NTSC)

Symbol	Name	Period
		Continuous odd • even fields
A	First equalizing pulse period (2H)	261 to 262H
B	Vertical synchronization period (3H)	1 to 3H
C	Second equalizing pulse period (2H)	4 to 6H
D	Burst pause period	261 to 6H
E	Vertical blanking period (19H)	261 to 17H

Output timing (Non-interlaced NTSC)

PAL (Interlaced)

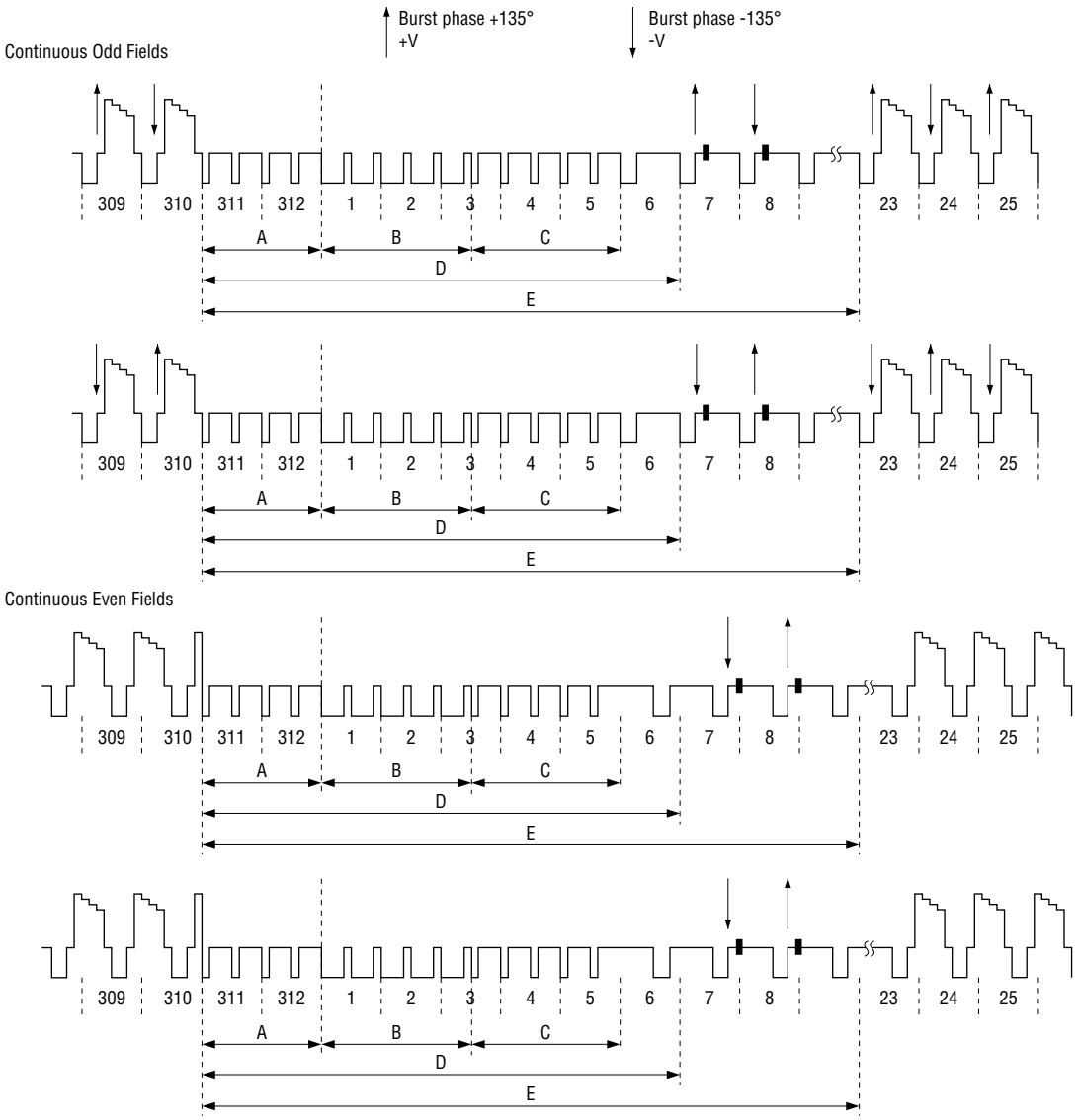


Output timing (Interlaced PAL)

Symbol	Name	Period			
		Field 1,5	Field 2,6	Field 3,7	Field 4,8
A	First equalizing pulse period (2.5H)	311 to 312.5H	311 to 312.5H	311 to 312.5H	311 to 312.5H
B	Vertical synchronization period (2.5H)	1 to 2.5H	1 to 2.5H	1 to 2.5H	1 to 2.5H
C	Second equalizing pulse period (2.5H)	2.5 to 5H	2.5 to 5H	2.5 to 5H	2.5 to 5H
D	Burst pause period	1 to 6,310 to 312.5H	1 to 5.5,308.5 to 312.5H	1 to 5,311 to 312.5H	1 to 6.5,309.5 to 312.5H
E	Vertical blanking period (25H)	1 to 22.5,311 to 312.5H	1 to 22.5,311 to 312.5H	1 to 22.5,311 to 312.5H	1 to 22.5,311 to 312.5H

Output timing (Interlaced PAL)

PAL (Non-interlaced)

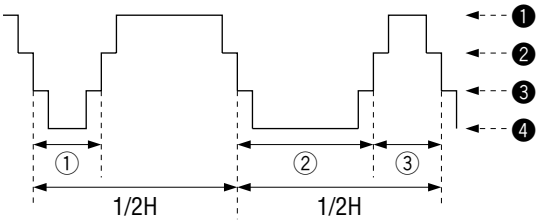


Output timing (Non-interlaced PAL)

Symbol	Name	Period
		Continuous odd • even fields
A	First equalizing pulse period (2H)	311 to 312H
B	Vertical synchronization period (2.5H)	1 to 2.5H
C	Second equalizing pulse period (2.5H)	2.5 to 5H
D	Burst pause period	311 to 6H
E	Vertical blanking period (24H)	311 to 22H

Output timing (Non-interlaced PAL)

Equalizing Pulse, Vertical Synchronization Period



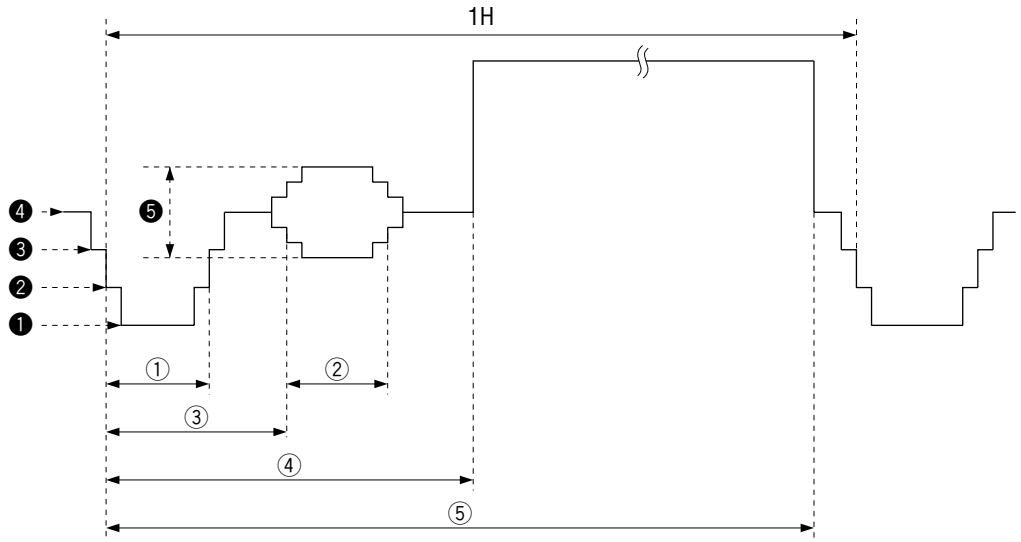
①Equalizing pulse width
②Vertical sync pulse width
③Serration

❶Blanking level
❷(synchronizing + blanking level) × (2/3)
❸(synchronizing + blanking level) × (1/3)
❹Synchronzing level

Setting content of equalizing pulse vertical synchronization period (T_{CLKX1} is sampling clock cycle in each mode)

	①	②	③	1/2H
ITU-R BT.601 NTSC	$31T_{CLKX1}$	$365T_{CLKX1}$	$64T_{CLKX1}$	$429T_{CLKX1}$
ITU-R BT.601 PAL	$32T_{CLKX1}$	$369T_{CLKX1}$	$63T_{CLKX1}$	$432T_{CLKX1}$
4Fsc NTSC	$33T_{CLKX1}$	$387T_{CLKX1}$	$68T_{CLKX1}$	$455T_{CLKX1}$
Square pixel NTSC	$28T_{CLKX1}$	$332T_{CLKX1}$	$58T_{CLKX1}$	$390T_{CLKX1}$
Square pixel PAL	$35T_{CLKX1}$	$403T_{CLKX1}$	$69T_{CLKX1}$	$472T_{CLKX1}$

Horizontal Blanking Period



①Horizontal sync pulse width
②Burst signal output period
③Burst signal start
④Horizontal blanking period (excluding front porch)
⑤Front porch start

❶Synchronzing level
❷(synchronizing + blanking level) × (1/3)
❸(synchronizing + blanking level) × (2/3)
❹Blanking level
❺Peak to peak value of burst

Horizontal blanking period

Setting content of horizontal blanking period (T_{CLKX1} is sampling clock cycle in each mode)

	①	②	③	④	⑤	Total dots/1H
ITU-R BT.601 NTSC	$63T_{CLKX1}$	$31T_{CLKX1}$	$71T_{CLKX1}$	$127T_{CLKX1}$	$838T_{CLKX1}$	858
ITU-R BT.601 PAL	$63T_{CLKX1}$	$31T_{CLKX1}$	$75T_{CLKX1}$	$142T_{CLKX1}$	$844T_{CLKX1}$	864
4Fsc NTSC	$67T_{CLKX1}$	$36T_{CLKX1}$	$75T_{CLKX1}$	$135T_{CLKX1}$	$889T_{CLKX1}$	910
Square pixel NTSC	$58T_{CLKX1}$	$31T_{CLKX1}$	$65T_{CLKX1}$	$116T_{CLKX1}$	$762T_{CLKX1}$	780
Square pixel PAL	$69T_{CLKX1}$	$34T_{CLKX1}$	$82T_{CLKX1}$	$155T_{CLKX1}$	$922T_{CLKX1}$	944

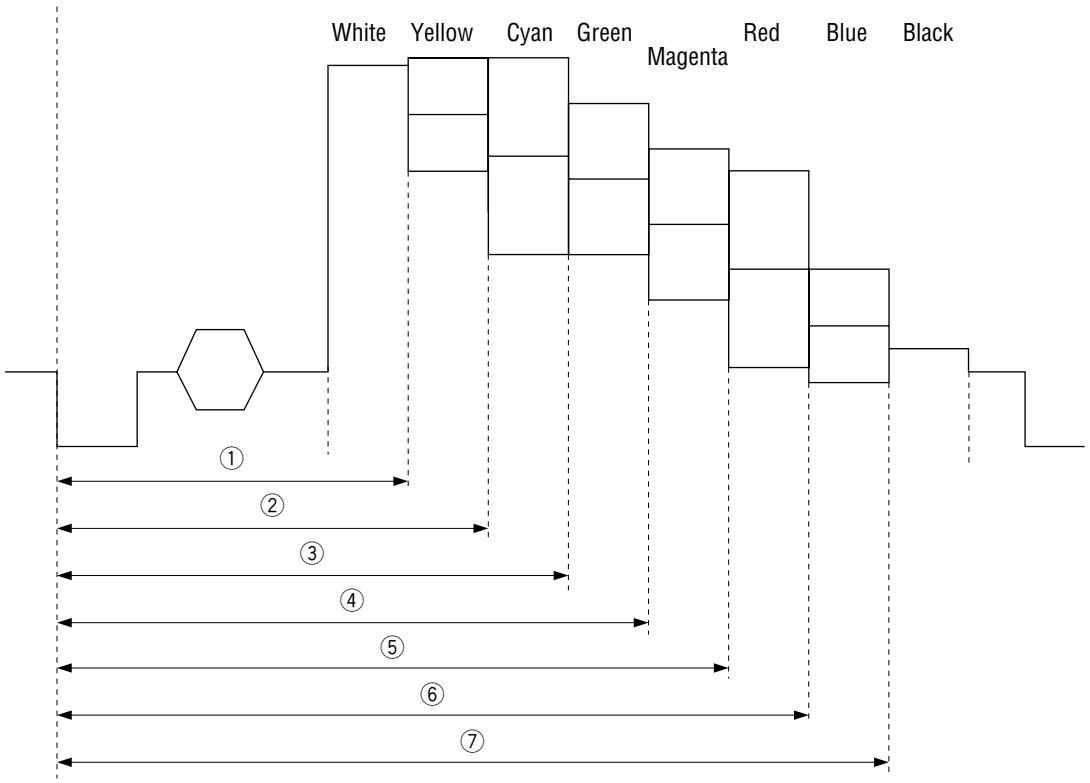
Setting content of horizontal blanking period

SETUP LEVEL SETTING

When the NTSC operation mode is selected, one of the two kinds of setup level can be selected by setting of internal register (MR1[7]).
When the setup level 0IRE (MR1[7] = "0") is selected, the Black-to-White is 100IRE.
When the setup level 7.5IRE (MR1[7] = "1") is selected, the Black-to-White is 92.5IRE.
However, this setup function is valid only for the NTSC mode and invalid for the PAL mode.

COLOR BAR GENERATION FUNCTION

The 25% luminance order color bar or 50% luminance order color bar or 75% luminance order color bar or 100% luminance order color bar is output by setting internal register CR0[2:1]. The output timings for each color bar color are as follows.



Output timing of each color bar color

Operation mode	hblank	①	②	③	④	⑤	⑥	⑦	1H
ITU-R BT.601 NTSC	$127T_{CLKX1}$	$216T_{CLKX1}$	$305T_{CLKX1}$	$394T_{CLKX1}$	$483T_{CLKX1}$	$572T_{CLKX1}$	$661T_{CLKX1}$	$750T_{CLKX1}$	$858T_{CLKX1}$
ITU-R BT.601 PAL	$142T_{CLKX1}$	$230T_{CLKX1}$	$318T_{CLKX1}$	$406T_{CLKX1}$	$494T_{CLKX1}$	$582T_{CLKX1}$	$670T_{CLKX1}$	$757T_{CLKX1}$	$864T_{CLKX1}$
4Fsc NTSC	$135T_{CLKX1}$	$230T_{CLKX1}$	$325T_{CLKX1}$	$419T_{CLKX1}$	$513T_{CLKX1}$	$607T_{CLKX1}$	$701T_{CLKX1}$	$795T_{CLKX1}$	$910T_{CLKX1}$
Square pixel NTSC	$116T_{CLKX1}$	$197T_{CLKX1}$	$278T_{CLKX1}$	$359T_{CLKX1}$	$440T_{CLKX1}$	$521T_{CLKX1}$	$602T_{CLKX1}$	$682T_{CLKX1}$	$780T_{CLKX1}$
Square pixel PAL	$155T_{CLKX1}$	$251T_{CLKX1}$	$347T_{CLKX1}$	$443T_{CLKX1}$	$539T_{CLKX1}$	$635T_{CLKX1}$	$731T_{CLKX1}$	$827T_{CLKX1}$	$944T_{CLKX1}$

(T_{CLKX1} : sampling clock period)

Contents of color bar output timing setting

SETTINGS OF EACH MODE

1) Switching Between Master Mode and Slave Mode

By setting the external terminals MS and MODE[3:0] or internal registers MR1[3] and MR0[3:0], the encoder can select either operation in the master mode in which sync signals are internally generated or operation in the slave mode in which the encoder operates through receiving external sync signals.
The switching between master mode and slave mode by settings the external terminals and internal registers are described below.
If the ITU-R BT.656 standard is selected when external terminal MODE[3:0] is "0000" or internal register MR0[3:0] is "0000", the slave mode is selected irrespective of settings of external terminals and internal registers.

Switching between master mode and slave mode

Control by external terminal

MR0[7]	MS	MODE[3:0]	Operation mode
0 (External terminal is valid)	0 (Slave)	"0000"	Slave mode (ITU-R BT.656)
		Other than "0000"	Slave mode (specified mode other than ITU-R BT.656)
	1 (Master)	"0000"	Slave mode (ITU-R BT.656)
		Other than "0000"	Master mode (specified mode other than ITU-R BT.656)

Control by internal register

MR0[7]	MR1[3]	MR0[3:0]	Operation mode
1 (Internal terminal is valid)	0 (Slave)	"0000"	Slave mode (ITU-R BT.656)
		Other than "0000"	Slave mode (specified mode other than ITU-R BT.656)
	1 (Master)	"0000"	Slave mode (ITU-R BT.656)
		Other than "0000"	Master mode (specified mode other than ITU-R BT.656)

2) Setting of Sleep Mode

When the external terminal RGBMODE is "0" (YCbCr mode), the sleep mode is selected when MODE[3:0] is "1111". The sleep mode cannot be selected by setting of internal registers. The sleep mode that is selected by setting of internal registers is valid only for a D/A converter through MR0[5].

3) Settings of Input Modes (RGB and YCbCr)

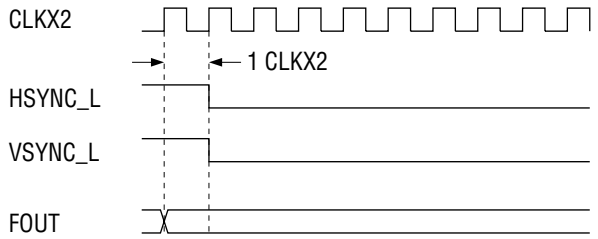
RGB Mode: The RGB mode is selected when the external terminal RGBMODE is "1", MODE[3:0] is a pixel frequency ("0101/01100/0111/1110"), and internal register MR0[4] is "1".

YCbCr Mode: The YCbCr mode is selected when the external terminal RGBMODE is "0", MODE[3:0] is a mode other than sleep mode, and internal register MR0[4] is "0".

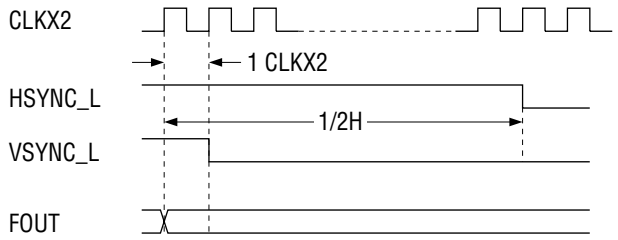
FOUT OUTPUT TIMING

(1) In Master Mode

• Odd Field

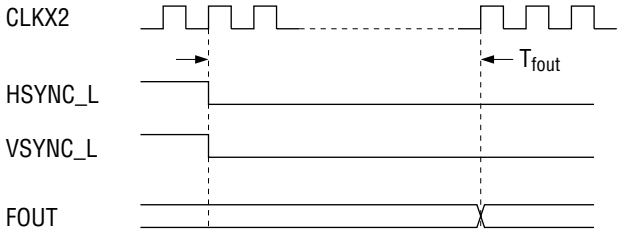


• Even Field

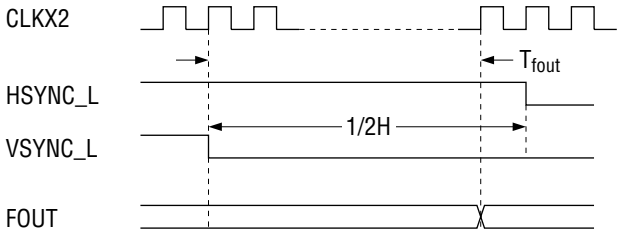


(2) In Slave Mode

• Odd Field



• Even Field



T_{fout} values in slave mode depend on pixel rates. The following table lists the T_{fout} values to each pixel rate.

Input interface	T_{fout}
ITU-R BT.656	5 CLKX2
YCbCr (8bit)	9 CLKX2
YCbCr (16bit)	9 CLKX2 or 10 CLKX2
RGB	9 CLKX2 or 10 CLKX2

GENLOCK FUNCTIONS

The functions of GENLOCK pin either in the master mode or in the slave mode are described below.

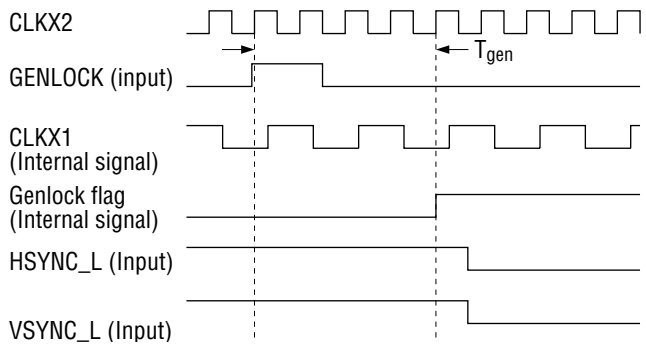
GENLOCK Functions in Master Mode or in Slave Mode

Operation mode	MR1[0]	MR1[1]	GENLOCK Function	
Slave mode	0 (External GENLOCK: valid)	0 (GENLOCK ON)	Input mode	A pulse that is input to the GENLOCK pin resets the subcarrier phase.
		1 (GENLOCK OFF)	Input mode	GENLOCK OFF invalidates pulses that are input to the GENLOCK pin.
	1 (Internal register: valid)	0 (GENLOCK ON)	Input mode	The internal register resets the subcarrier phase. External timing is ignored.
		1 (GENLOCK OFF)	Input mode	GENLOCK OFF does not reset the subcarrier phase. External timing is ignored.
Master mode	0 (External GENLOCK: valid)	0 (GENLOCK ON)	Output mode	An external pin can output pulses to reset the subcarrier phase. GENLOCK ON resets the subcarrier phase and its reset timing is output.
		1 (GENLOCK OFF)	Output mode	An external pin can output pulses to reset the subcarrier phase.GENLOCK OFF does not reset the subcarrier phase and its reset timing is not output.
	1 (Internal register: valid)	0 (GENLOCK ON)	Output mode	An external pin cannot output pulses. GENLOCK ON with MR1[1] resets the subcarrier phase but its reset timing is not output.
		1 (GENLOCK OFF)	Output mode	An external pin cannot output pulses. GENLOCK OFF does not reset the subcarrier phase and its reset timing is not output.

Slave Mode

When in the slave mode, the encoder can receive the subcarrier-phase reset signal from the external GENLOCK pin. The subcarrier-phase pulse should be input at the timing that meets the AC characteristics. If the GENLOCK pulse is input to the encoder in the NTSC mode, the subcarrier phase is reset when the pulse reaches the 4th field. And if the GENLOCK pulse is input to the encoder in the PAL mode, the subcarrier phase is reset when the pulse reaches the eighth field.
5 CLKX2 pulses (Genlock setup time: Tgen) are required for the time from when the reset signal is input to the GENLOCK pin to when the internal GENLOCK flag is set. Thus, if the GENLOCK pulse is input 5 CLKX2 pulses before the HSYNC_L and VSYNC_L signals at the first field are input, the subcarrier phase is reset at the first field after the first input even if the internal state of the encoder is any field. The subcarrier phase, however, cannot be reset if the GENLOCK pin is fixed high.

(1) Input Timing (Slave mode)

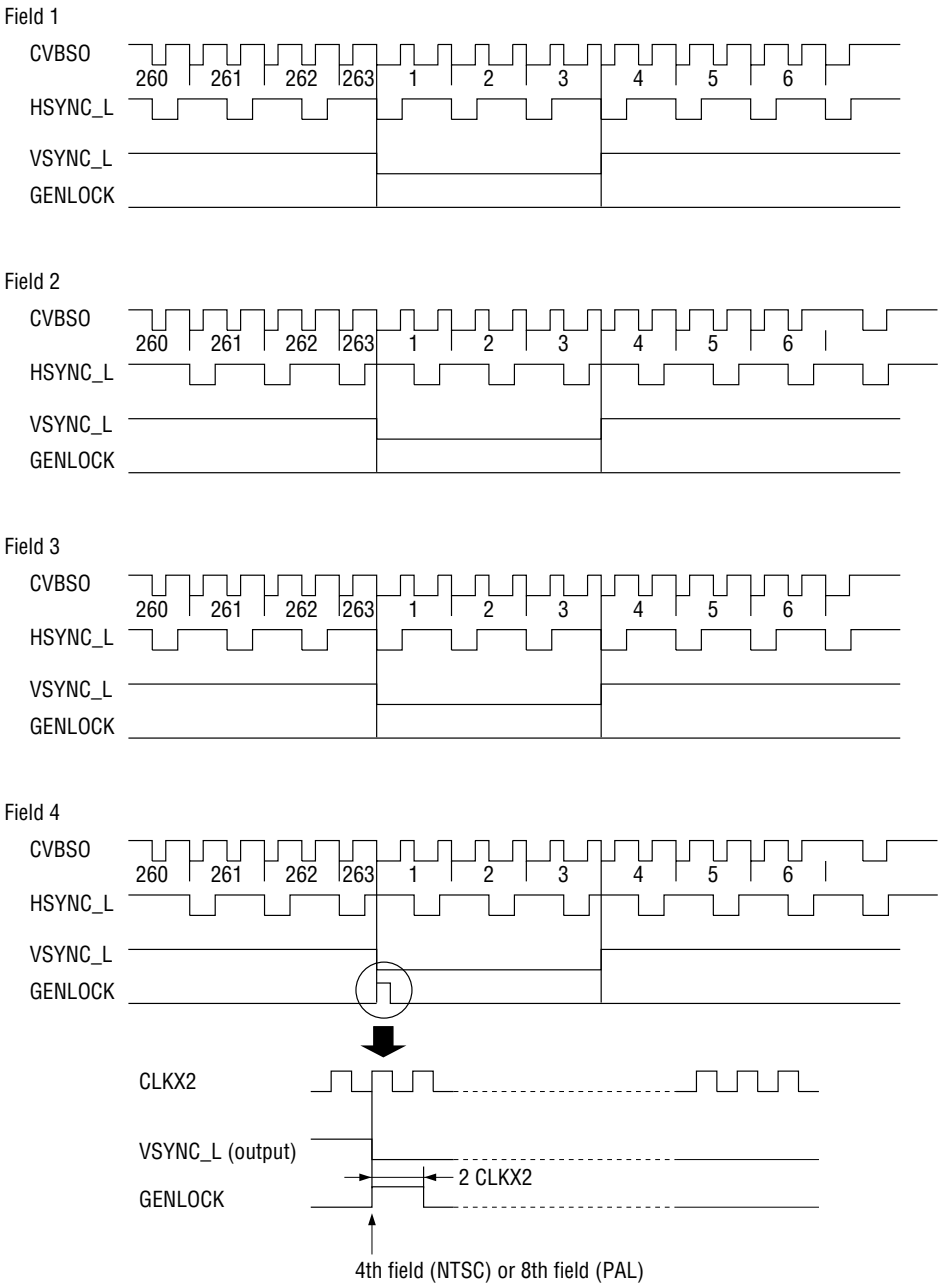


GENLOCK Input Timing

Master Mode

If the external GENLOCK pin is valid (MR1[0] = "0"), the subcarrier-phase reset signal is output from the GENLOCK pin. When the encoder is in the NTSC mode, the signal is output at the falling edge of a HSYNC_L or VSYNC_L signal at the 4th field. When in the PAL mode, the signal is output at the falling edge of a HSYNC_L or VSYNC_L signal at the 8th field. The pulse width of GENLOCK is equivalent to two cycles of CLKX2.

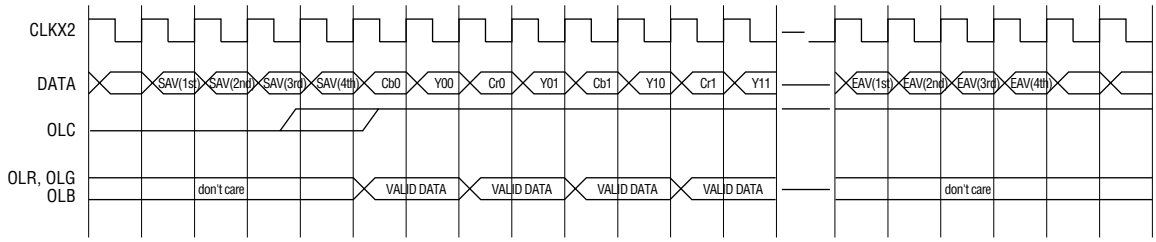
(2) Output Timing (Master mode) (NTSC)



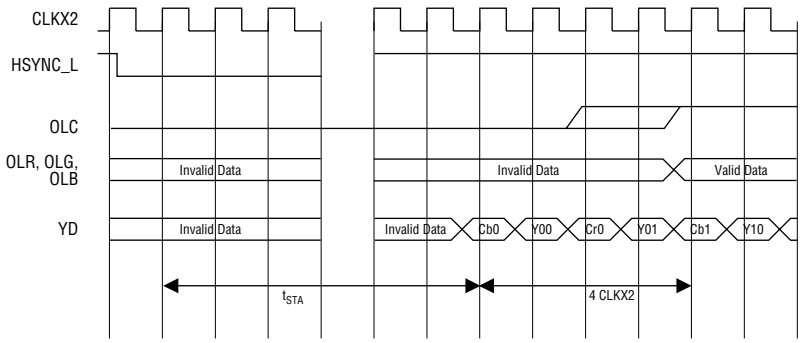
GENLOCK Output Timing

3-BIT TITLE/GRAPHICS MULTI-FUNCTION

When composite or S-video output is selected, it is possible to impose characters or graphics on the image by inputting the overlay color RGB signal from the external pins OLR, OLG, and OLB. Switching between overlay input and image data output is made by using the external pin OLC. When the RGB signal output is selected, the graphics multi-function is invalid. If the input image signal does not exist, the blue back display can be output by setting OLC and OLB to "1".
The overlay input timing in the ITU-R BT.656 input mode is different from that in the 8-bit YCbCr or RGB input mode. The overlay input data in the ITU-R BT.656 input mode becomes valid immediately after fetching the 4th EAV signal. The overlay input data in the 8-bit YCbCr or RGB input mode becomes valid after HSYNC_L becomes "L" and Tstart passes and 4 CLKX2 pulses are input. In the above two cases, the OLC input should be "H" when data becomes valid. However, "data becomes valid" means that data is internally processed, and does not means that data can be output.



Overlay input timing (ITU-R BT.656 input mode)



Overlay input timing (8-bit YCbCr or RGB input mode)

INTERNAL REGISTERS

All registers can be written.
Details of the internal registers are described below.

Register name	R/W	Sub-address		Item to be set	Description
MR0 (Mode register)	Write Only	00	MR0 [7]	Override	Switching between the external terminal and internal register settings(for the operation mode) *0 : External terminal setting enabled 1 : Internal register setting enabled
			MR0 [6]	Chroma format	Chrominance signal input format *0 : Offset binary 1 : 2's complement
			MR0 [5]	DAC sleep control	DAC sleep mode Control *0 : DAC active 1 : DAC sleep
			MR0 [4]	RGBMODE	Input signal switching *0 : YCbCr 1 : RGB Valid only in MODE [3:0] set as follows : (0101/0110/0111/1101/1110)
			MR0 [3:0]	Video mode select	Operation mode switching Corresponds to the external MODE [3:0] pin. Logic & DAC Sleep mode cannot be set. The sleep mode by the register is valid for only DAC through MR0[5]. *0000 : NTSC ITU-R BT.656 0001 : NTSC 27 MHz YCbCr 0010 : NTSC 24.52 MHz Square Pixel 0011 : NTSC 28.64 MHz 4Fsc 0101 : NTSC 13.5 MHz YCbCr 0110 : NTSC 12.27 MHz 0111 : NTSC 14.32 MHz 1000 : PAL ITU-R BT.656 1001 : PAL 27 MHz YcbCr 1010 : PAL 29.5 MHz Square Pixel 1101 : PAL 13.5 MHz 1110 : PAL 14.75 MHz 1111 : invalid

Register name	R/W	Sub-address		Item to be set	Description
MR1 (Mode register)	Write Only	01	MR1 [7]	Black level Control	Black level setup Note : Valid in NTSC mode only *0 : Black level 0IRE 1 : Black level 7.5IRE
			MR1 [6]	Counter Control	Non-standard signal input mode switching *0 : Corresonds to standard signal only 1 : Corresponds to standard and non-standard signals. (The field is normally judged when a signal, in which the number of lines per field is different, is input.)
			MR1 [5]	RGB input Level	RGB input level switching RGB input level *0 : 0 to 255 1 : 16 to 235 RGB output level *0 : 0 to 510 1 : 32 to 470
			MR1 [4]	OUTSEL	Output signal switching *0 : S-video/composite 1 : RGB
			MR1 [3]	Master/Slave	Master/Slave operation switching *0 : Slave 1 : Master
			MR1 [2]	INTERLANCE	Scanning *0 : Interlace 1 : Non-interlace
			MR1 [1]	Genlock Control	Genlock function On/Off control *0 : Genlock On 1 : Genlock Off
MR1 (Command Register)	Write Only	01	MR1 [0]	Genlock Select	External Genlock pin/internal register switching for subcarrier reset control *0 : Subcarrier phase reset signal is input or output to and from external Genlock pin. • When in master mode, the reset pulse is output one field before reset is performed. The reset pulse is output only when MR1[1] is "0". • When in slave mode, reset is performed by reset signal from external pin. 1 : Content of internal register MR1[1] is valid.

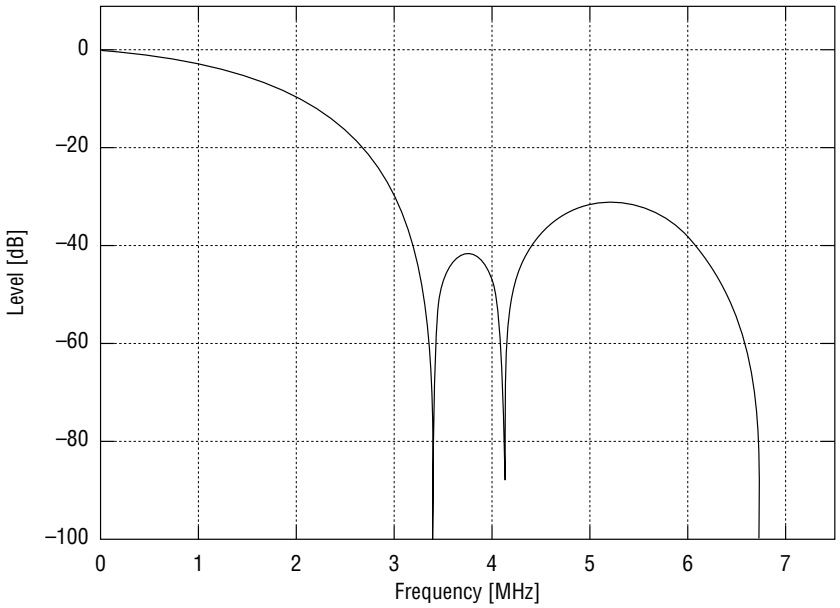
Register name	R/W	Sub-address		Item to be set	Description
CR0 (Command Register)	Write Only	02	CR0 [6]	CSYNC	Addition control of CSYNC_L at RGB output *0 : No addition of CSYNC to G signal 1 : Addition of CSYNC
			CR0 [5]	FOUT	FOUT polarity change *0 : Odd field "H", Even field "L" 1 : Odd field "L", Even field "H"
			CR0 [4]	Trap Filter	TRAP filter On/Off control *0 : Trap filter Off 1 : Trap filter On
			CR0 [3]	Color Bar	Adjusting luminance order color bar output control *0 : Input image data or overlay data 1 : Luminance order color bar
			CR0 [2:1]	Overlay level	Overlay signal/adjusting luminance order color bar output level control 11 : 25% 10 : 50% 01 : 75% *00 : 100%
			CR0 [0]	Sampling ratio	Sampling ratio control *0 : 4:2:2 1 : 4:1:1
CR1 (Command Register)	Write Only	03	CR1 [3:0]	Luminance Level	Adjusting luminance level of input image data *0000 : 100.00% 0001 : 96.875% 0010 : 93.750% 0011 : 90.675% 0100 : 87.500% 0101 : 84.375% 0110 : 81.250% 0111 : 78.125% 1000 : 75.000% 1001 : 71.875% 1010 : 68.750%

FILTER CHARACTERISTICS

The characteristics of LPF used for color signal processing and interpolation filters used for upsampling processing are shown below.

LPF for 422 Color Signals

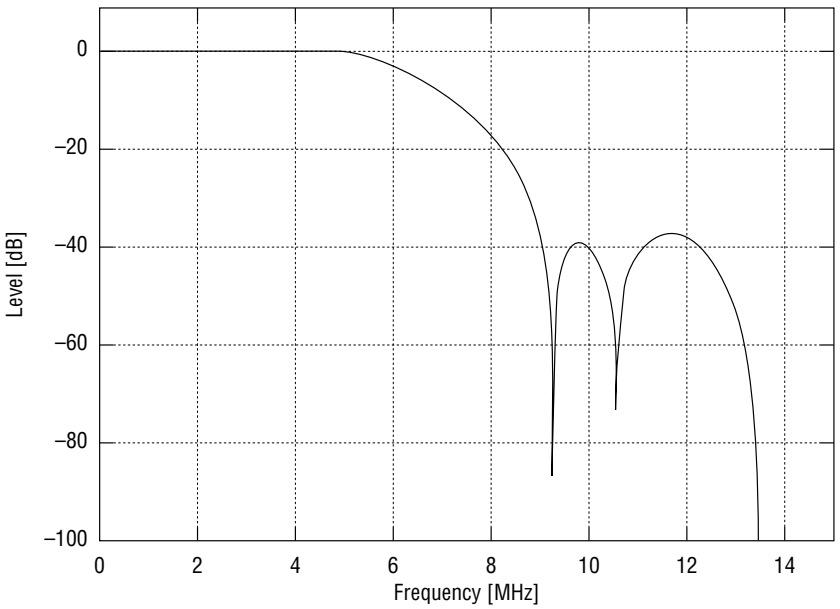
The following shows the characteristics when the clock frequency is 27 MHz.



422 Interpolation + LPF Frequency Characteristic

Interpolation Filter

The following shows the characteristics when the clock frequency is 27 MHz.

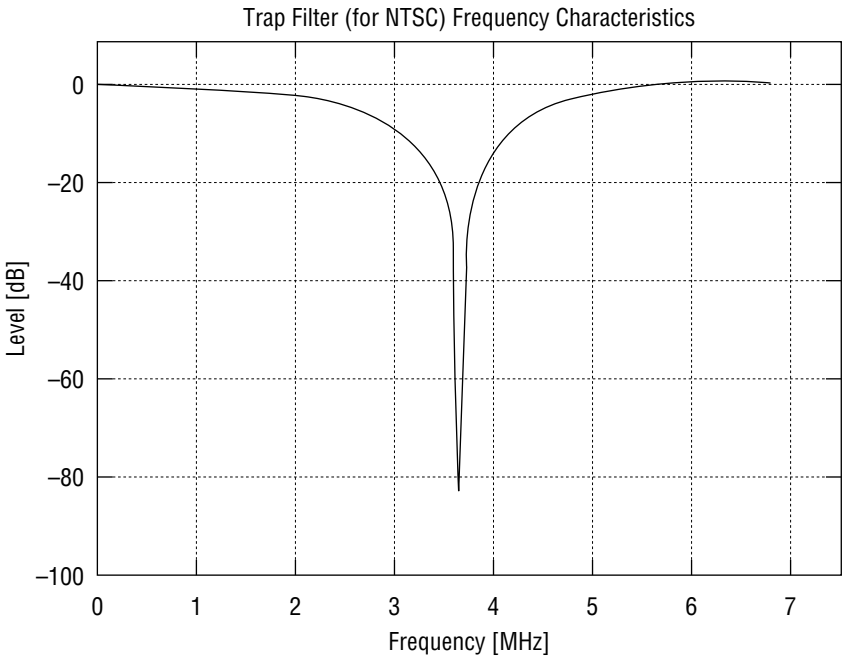


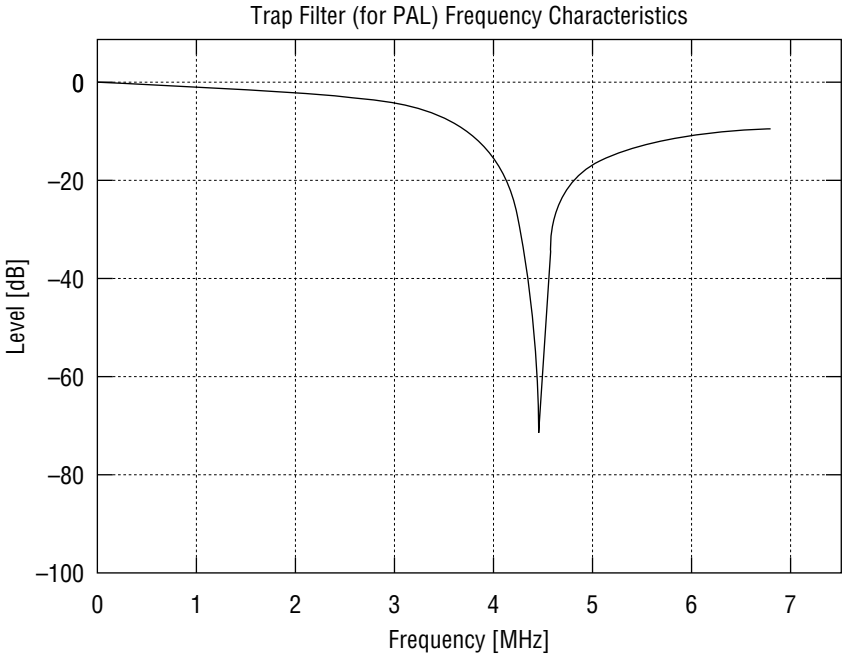
Up Sampling Filter Frequency Characteristic

(Note) The characteristics of these filters are based on design data.

Trap Filter

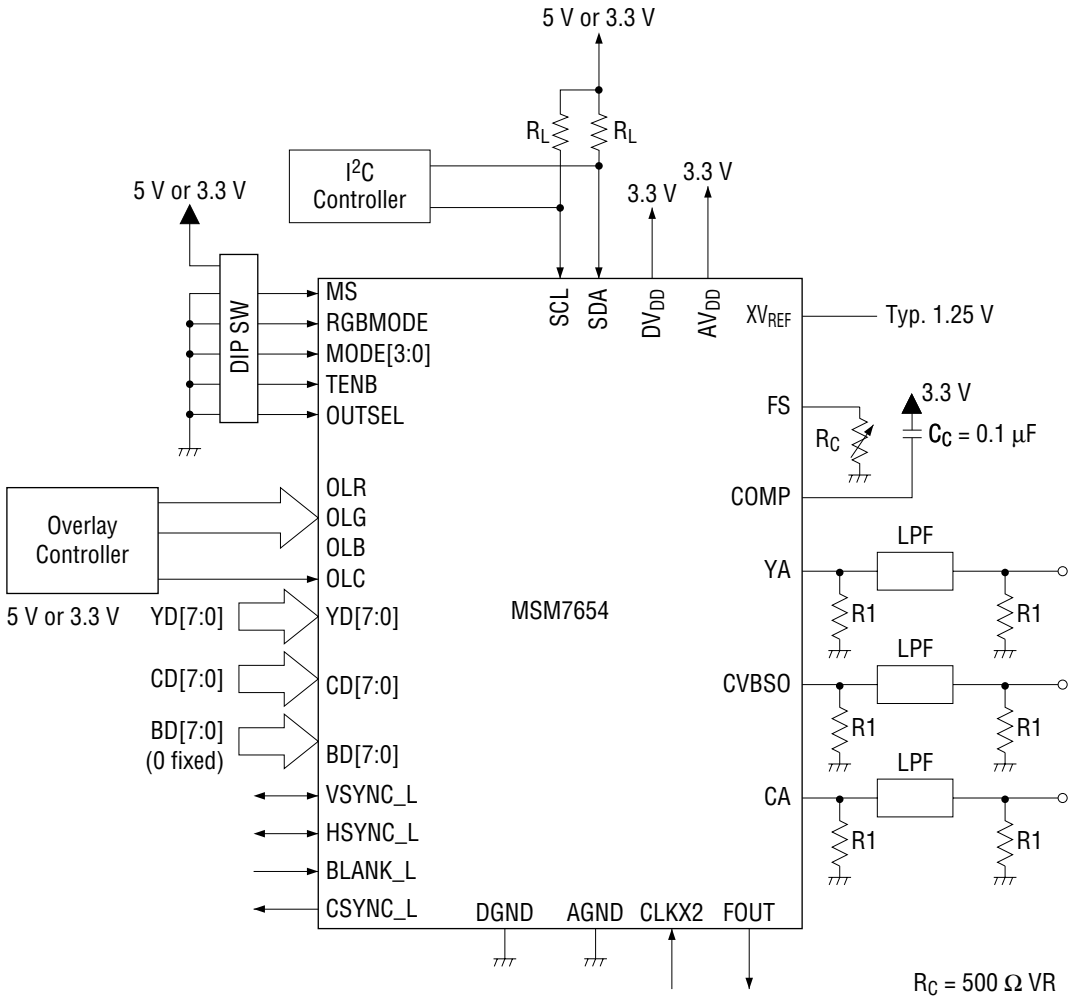
The following shows the characteristics when the clock frequency is 27 MHz.



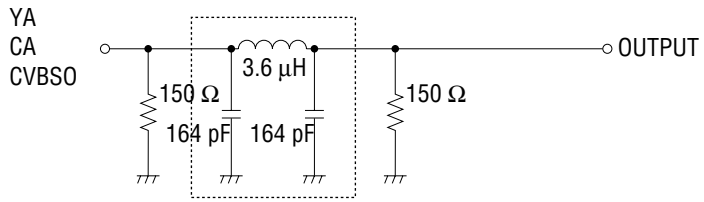


(Note) The characteristics of these filters are based on design data.

APPLICATION CIRCUIT EXAMPLE (YCbCr 16-bit input mode)



Sample of Analog Output Circuit

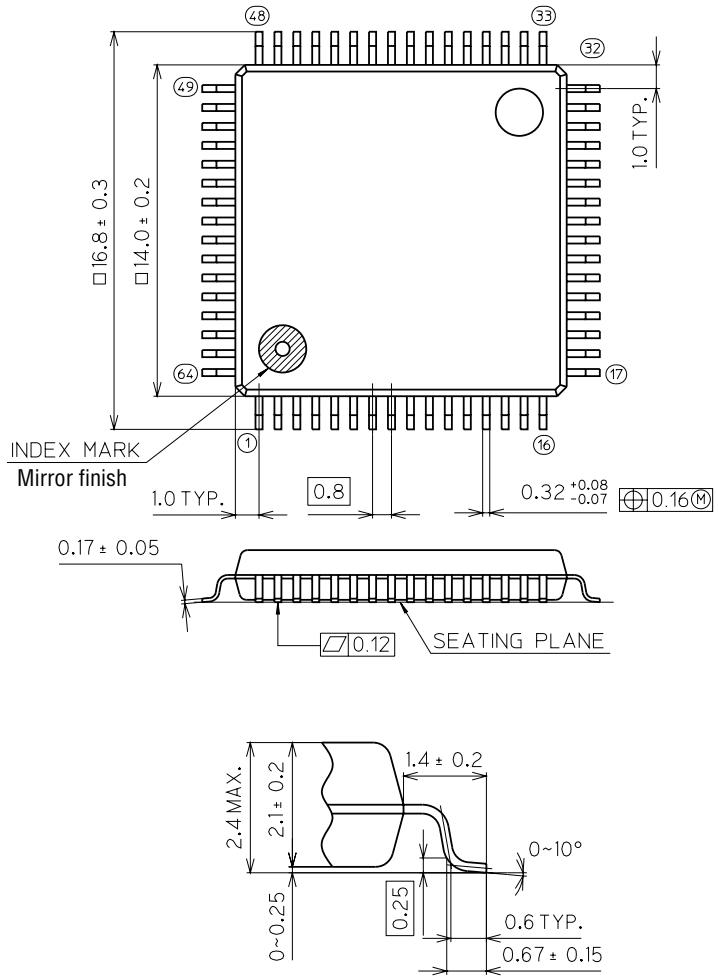


⬚ LPF (TOKO, INC-make 628LJN-1471 is recommended.)

Note: The filters shown above are samples to be referenced.
Filters to be used can be selected by the user.
The analog output circuit shown above is a sample when a destination connected to is terminated with 75 Ω load. If the connected destination is not terminated or is drived with 37.5 Ω load, the analog output circuit should use 75 Ω resistors.
If the YA, CA and CVBSO pins are terminated with 37.5 Ω load, an operational amplifier is not used.

PACKAGE DIMENSIONS

(Unit : mm)



64-Pin Plastic QFP

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