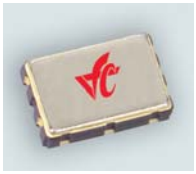
VFXO311
XO Ultra Low Jitter 2.5V, 3.3V
5x7mm SMD, LVPECL / LVDS / LVCMOS

Valpey Fisher Corporation
High Frequency, Low Phase Noise Timing Solutions

Features

- 60MHz to 800MHz Frequency Range
- Differential Output Levels (LVPECL/LVDS)
- Single Ended LVCMOS output available
- <0.2ps jitter RMS over 12KHz ~ 20MHz
- Selectable OE Logic



RoHS Status

RoHS 6/6

Applications

- Optical Networking, SONET / SDH
- 10 Gigabit Ethernet
- Broadband Access

Electrical Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Frequency Range	F		60 60		800 320	MHz	PECL / LVDS CMOS
Frequency Stability	ΔF/F	Vs. Operating Temperature			± 50 ± 25 ± 20	ppm	*Order Code B* *Order Code C* *Order Code D*
		Vs. Supply Voltage Vs. Aging / Year		± 3 ± 3 ±1		ppm/V ppm ppm	 First Year After first year
Operating Temperature	T		0° -40°		+70° +85°	°C	*Order Code B* *Order Code G*
Output		LVPECL LVDS LVCMOS					*Order Code L* *Order Code D* *Order Code C*
Supply Voltage	Vcc		3.15 2.25	3.3 2.5	3.45 2.75	V	*Order Code E* *Order Code G*
Period Jitter RMS		155.52 MHz 311.04 MHz 622.08 MHz		2.5 2.5 4	3 3 6	ps	
Integrated Jitter RMS **12KHz to 20MHz**		155.52MHz 311.04MHz 622.08MHz		0.25 0.18 0.09		ps	
Period Jitter Peak-to-Peak		155.52MHz 311.04MHz 622.08MHz		18 18 25	20 20 30	ps	

* NOTE: Certain frequencies above 500MHz ($3.3V_{DD}$) and above 300MHz (2.5VDD) are not available. Consult factory for availability.

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Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Supply Current	Icc	38 – 100MHz 100 – 300MHz 300 – 640MHz			65 80 90	mA	PECL
		38 – 100MHz 100 – 320MHz 320 – 640MHz			45 60 70	mA	LVDS
		At 100MHz, load = 15pF		16	20	mA	CMOS
Load	50 Ohm to V_{DD}-2V (PECL) 100 Ohm (LVDS)						
Output High Voltage	V_{OH}	R_L = 50 ohm to (V_{DD}-2V) I_{OH} = -8.5mA	2.4	V_{DD}-1.025 1.4	1.6	V	PECL LVDS CMOS
Output Low Voltage	V_{OL}	I_{OL} = -8.5mA	0.9	1.1	V_{DD}-1.620 0.4	V	PECL LVDS CMOS
Output Differential Voltage	V_{OD}		247	355	454	mV	LVDS
Output Drive Voltage	I_{OSD}	V_{OL} = 0.4V, V_{OH} = 2.4V		8.5		mA	CMOS
Offset Voltage	V_{OS}		1.125	1.2	1.375	V	LVDS
Rise / Fall Time	Tr/Tf	20% to 80%		0.25 0.3 1.2	0.45 0.7 1.6	ns	PECL LVDS CMOS
Duty Cycle		V_{DD} – 1.3V @ 1.25V 50% V_{DD}	45	50	55	%	PECL LVDS CMOS
Tristate	"1": Output Enable – Pin 2 may float 2.8V min (3.3V V_{DD}) or 2.25V min (2.5V V_{DD}) "0": Tristate – Pin 2 requires 0.4V max (3.3V or 2.5V V_{DD})						

Phase Noise Performance

Parameter	Output Type	Frequency Range (MHz)	Carrier Freq. (MHz)	10Hz	100Hz	1KHz	10 KHz	100 KHz	1 MHz	10 MHz
Phase Noise (dBc/Hz)	PECL LVDS	300 - 800	622.08	-55	-85	-110	-130	-137	-148	-150
	CMOS	120 – 320	155.52	-50	-82	-110	-128	-142	-148	-150
	PECL LVDS	120 – 320	155.52	-50	-82	-110	-128	-142	-148	-150
	CMOS	60 – 160	155.52	-65	-95	-122	-138	-142	-148	-149
	PECL LVDS	60 – 160	155.52	-65	-95	-122	-138	-142	-148	-149

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Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Lead Temperature		Soldering, 10s max			260	°C	
Storage Temperature	Ts		-55		+125°	°C	
Junction Temperature	Tj				+125°	°C	
ESD Protection		Input static discharge voltage protection			2	kV	
Supply Voltage	V_{DD}				4.6	V	
Output Voltage	Vo		V_{DD}-0.5		V_{DD}+0.5	V	

Environmental and Mechanical Conditions

Parameter	Specification
Shock	1000 Gs, 0.35ms, ½ sine wave, 3 shocks in each plane
Humidity	Resistant to 85 ºR.H. at 85 ºC
Vibration	10-2000 Hz of 0.06" d.a. or 20 Gs, whichever is less
Leak	MIL STD 883, Method 1014, Condition A1
Case	Ceramic with hermetic reistance-welded metal lid
Pads	Solderable gold over nickel
Marking	Epoxy ink or laser engraved
Resistance to Solvents	MIL STD 202, Method 215

How to Order

VFXO311 — □□□□ — **FREQUENCY, MHz**

Stability

Code	Specification
B	50 ppm
C	25 ppm
D	20 ppm

Temperature Range

Code	Specification
B	0°C to 70°C
G	-40°C to 85°C

Supply Voltage

Code	Output
E	3.3V
G	2.5V

Output

Code	Output
L	LVPECL
D	LVDS
C	CMOS

Note: DG combination not available at all frequencies. Consult factory.

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LVPECL, LVDS

Pin #	Connection
1	N/C
2	Tristate
3	Case, GND
4	Output
5	$\overline{\text{Output}}$
6	Supply Voltage

LVCMOS

Pin #	Connection
1	N/C
2	Tristate
3	Case, GND
4	Output
5*	N/C
6	Supply Voltage

*For LVCMOS, Dual single ended outputs available – consult factory