Definitions of Ultra-Stable and Stable

Multilayer Ceramic Capacitors are generally divided into classes which are defined by the capacitance temperature characteristics over specified temperature ranges.

These are designated by alpha numeric codes.
Code definitions are summarised below and are also available in the relevant national and international specifications.

1. C0G - Ultra Stable Class 1 Ceramic (EIA Class 1)

Spec.	Classification	Temperature range °C	Maximum capacitance change	Syfer dielectric code
CECC	1B/CG	-55 +125	0 ± 30ppm/°C	C
EIA	C0G (NP0)	-55 +125	0 ± 30ppm/°C	C
MIL	CG (BP)	-55 +125	0 ± 30ppm/°C	C

Capacitors within this class have a dielectric constant range from 10 to 100. They are used in applications which require ultra stable dielectric characteristics with negligible dependence of capacitance and dissipation factor with time, voltage and frequency. They exhibit the following characteristics:-

a) Time does not significantly affect capacitance and dissipation factor (Tan δ) – no ageing.
b) Capacitance and dissipation factor are not affected by voltage.
c) Linear temperature coefficient.

2. X7R – Stable Class II Ceramic (EIA Class II)

Spec.	Classification	Temperature range °C	Maximum capacitance change % over temperature range		Syfer dielectric code
			No DC volt applied	Rated DC Volt	
CECC	2C1	-55 +125	±20	+20 -30	R
	2R1	-55 +125	±15		X
	2X1	-55 +125	±15	+15 -25	B
EIA	X7R	-55 +125	±15	-	X
MIL	BX	-55 +125	±15	+15 -25	B
	BZ	-55 +125	±20	+20 -30	R

Capacitors of this type have a dielectric constant range of 1000-4000, and also have a non-linear temperature characteristic which exhibits a dielectric constant variation of less than ±15% (2R1) from its room temperature value, over the specified temperature range. Generally used for by-passing (decoupling), coupling, filtering, frequency discrimination, DC blocking and voltage transient suppression with greater volumetric efficiency than Class I units, whilst maintaining stability within defined limits.

Capacitance and dissipation factor are affected by:-
Time (Ageing)
Voltage (AC or DC)
Frequency

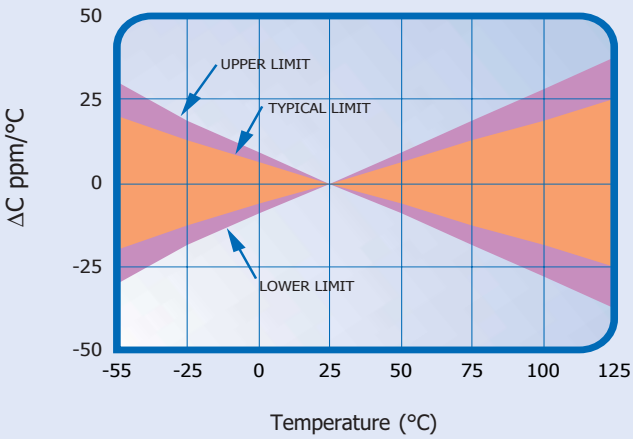
Technical Summary

Dielectric Characteristics

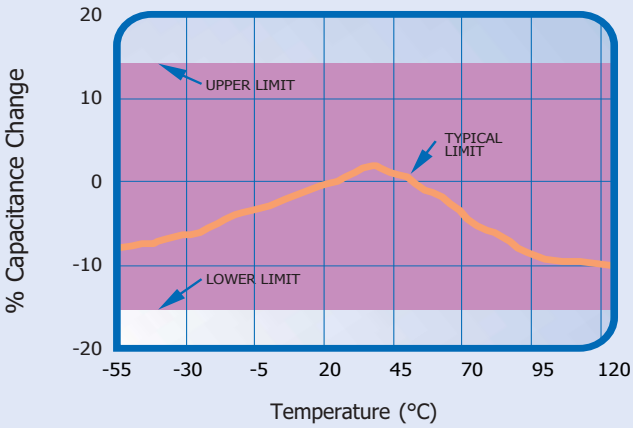
	C0G			X7R		
Dielectric classification	Ultra stable			Stable		
CECC	1B/CG			2C1	2R1	2X1
EIA		C0G(NPO)			X7R	
MIL			CG(BP)	BZ		BX
Rated temperature range	-55°C to +125°C			-55°C to +125°C		
Maximum capacitance change over temperature range						
No DC voltage applied	0 ± 30 ppm/°C			±20%	±15%	±15%
Rated DC voltage applied				+20-30%	-	+15-25%
Syfer dielectric ordering code	C			R	X	B
Tangent of loss angle (tan δ)	Cr > 50pF ≤ 0.0015 Cr ≤ 50pF = 0.0015 (15 +0.7 Cr)			≤ 0.025		
Insulation resistance (Ri) Time constant (Ri X Cr) (whichever is the less)	100G Ω or 1000s			100G Ω or 1000s		
Capacitance tolerance	Cr < 10pF ± 0.10pF (B) ± 0.25pF (C) ± 0.50pF (D) ± 1.0pF (F) Cr ≥ 10pF ± 1% (F) ± 2% (G) ± 5% (J) ± 10% (K)			± 5% (J) ± 10% (K) ± 20% (M)		
Dielectric strength	Voltage applied for 5 seconds. Charging current limited to 50 mA maximum.					
16-200V	2.5 times			2.5 times		
>200V <500V	Rated voltage + 250V			Rated voltage + 250V		
500V/630V	1.5 times			1.5 times		
≥1kV	1.25 times			1.25 times		
Climatic category (IEC)						
Chip	55/125/56			55/125/56		
Moulded	55/125/56			55/125/56		
Dipped	55/125/21			55/125/21		
Discoidal	55/125/56			55/125/56		
Ageing characteristic (Typical)	Zero			1% per time decade		
Approvals						
Chip	CECC 32 101 801			CECC 32 101 801		
Moulded radial	CECC 30 601 009			CECC 30 701 007		
Dipped radial	CECC 30 601 008			CECC 30 701 013		

Typical Dielectric Temperature Characteristics

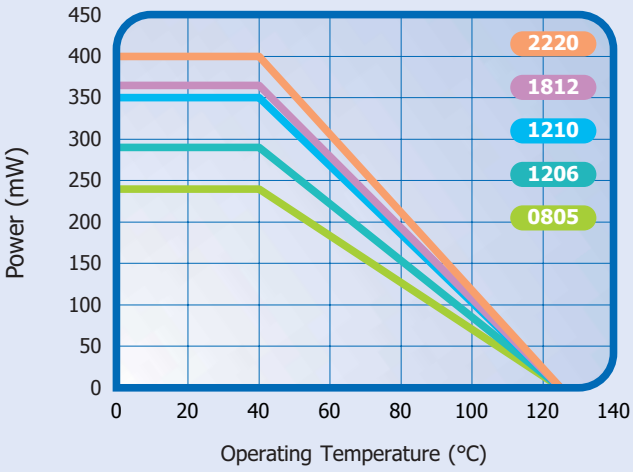
C0G Capacitance Vs Temperature



X7R Capacitance Vs Temperature



Power Ratings for COG and X7R



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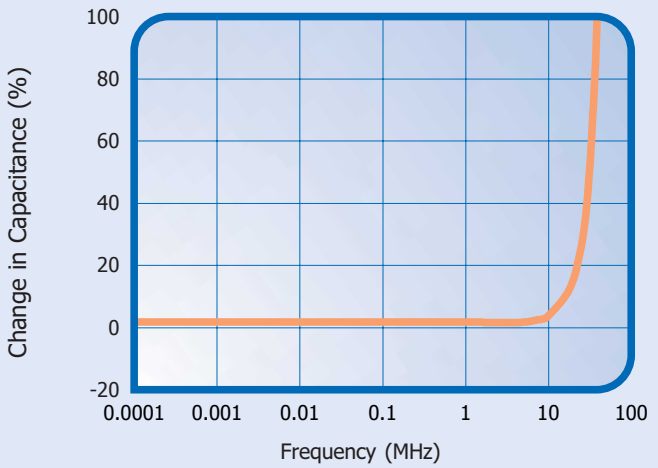
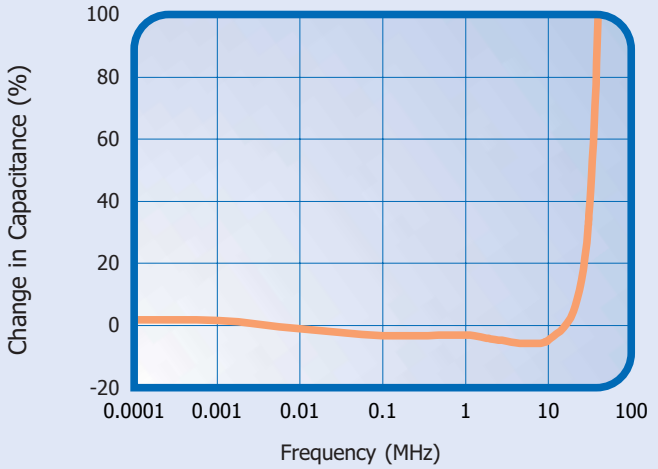
Technical Summary

Capacitance vs Frequency - 10nF chip

Ultra Stable C0G dielectric

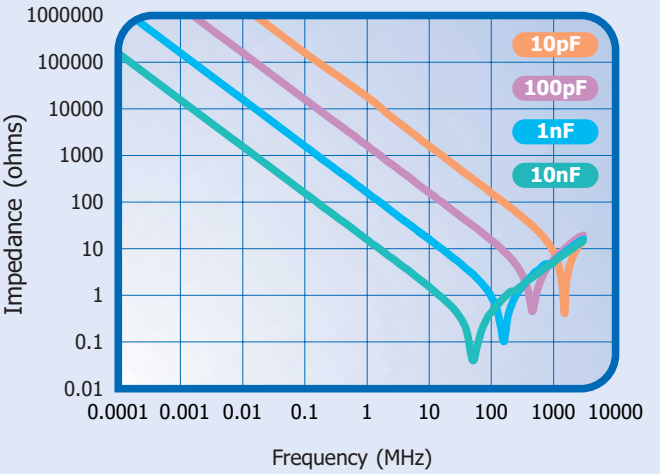


Stable X7R dielectric

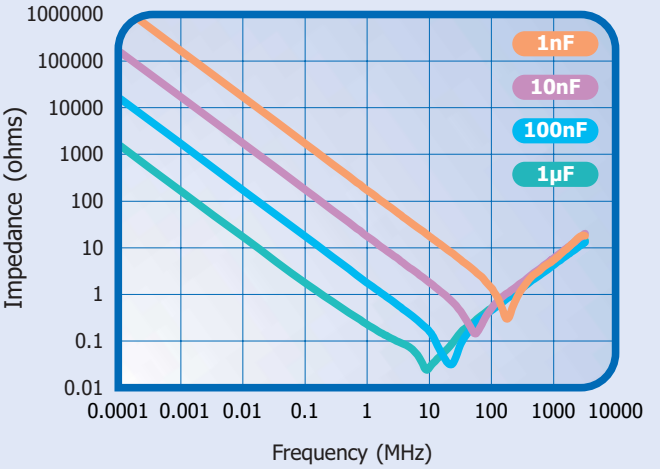


Impedance vs Frequency - chips

Ultra Stable C0G dielectric

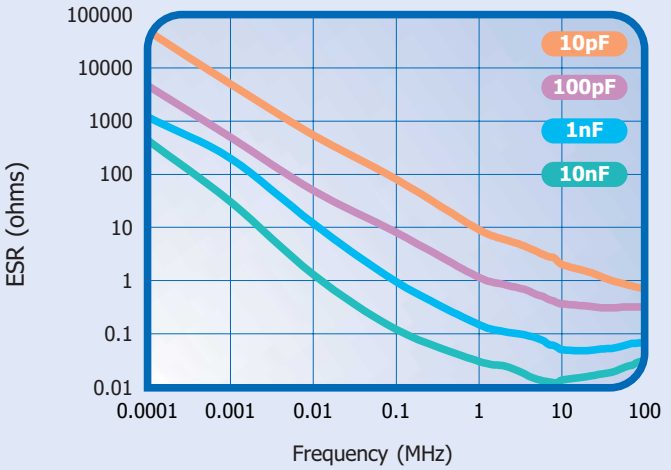


Stable X7R dielectric

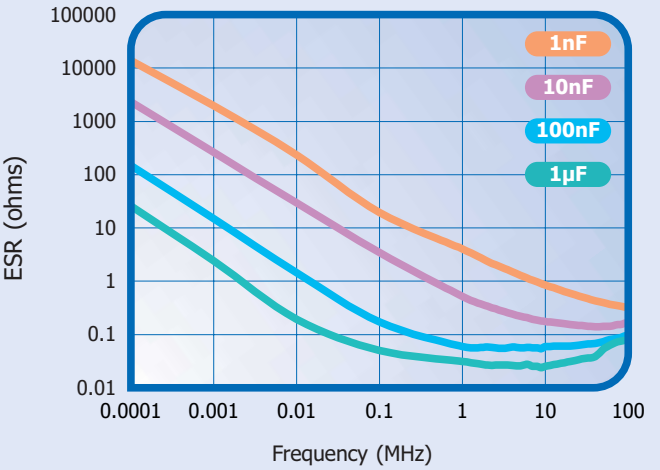


E.S.R. vs Frequency - chips

Ultra Stable C0G dielectric



Stable X7R dielectric



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Ageing of Ceramic Capacitors

Ageing

Capacitor ageing is a term used to describe the negative, logarithmic capacitance change which takes place in ceramic capacitors with time. The crystalline structure for barium titanate based ceramics changes on passing through its Curie temperature (known as the Curie Point) at about 125°C. This domain structure relaxes with time and in doing so, the dielectric constant reduces logarithmically; this is known as the ageing mechanism of the dielectric constant.

The more stable dielectrics have the lowest ageing rates.

The ageing process is reversible and repeatable.

Whenever the capacitor is heated to a temperature above the Curie Point the ageing process starts again from zero.

The ageing constant, or ageing rate, is defined as the percentage loss of capacitance due to the ageing process of the dielectric which occurs during a decade of time (a tenfold increase in age) and is expressed as percent per logarithmic decade of hours. As the law of decrease of capacitance is logarithmic, this means that in a capacitor with an ageing rate of 1% per decade of time, the capacitance will decrease at a rate of:

a) 1% between 1 and 10 hours
b) An additional 1% between the following 10 and 100 hours
c) An additional 1% between the following 100 and 1000 hours
d) An additional 1% between the following 1000 and 10000 hours etc
e) The ageing rate continues in this manner throughout the capacitor's life.

Typical values of the ageing constant for our Multilayer Ceramic Capacitors are:

Dielectric class	Typical agreed value
Ultra Stable C0G	Negligible capacitance loss through ageing
Stable X7R	1% per decade of time

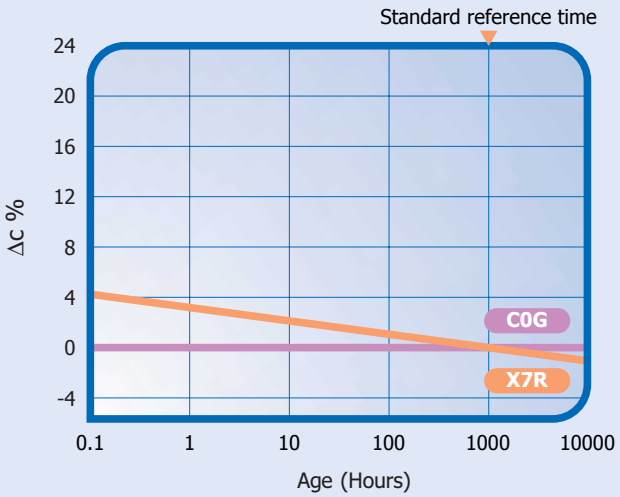
Capacitance Measurements

Because of ageing it is necessary to specify an age for referee measurements at which the capacitance shall be within the prescribed tolerance. This is fixed at 1000 hours, since for practical purposes there is not much further loss of capacitance after this time.

All capacitors shipped are within their specified tolerance at the standard reference age of 1000 hours after having cooled through their Curie temperature.

The ageing curve for any ceramic dielectric is a straight line when plotted on semi-log paper.

Capacitance vs Time - Ageing



Summary and Conclusions

1.0 The recommended sequence of testing Multilayer Ceramic Capacitors is as follows:

a) Capacitance. Applying factors based on the manufacturer's ageing rate and the time elapsed since the last Curie temperature excursion.

b) Dissipation factor

c) Voltage proof test

d) Insulation resistance

e) Other tests. If any limits are specified for change in capacitance during a long term test (life test, for example), the capacitor should be de-aged before both initial and final measurements. De-ageing is accomplished by exposure of the capacitors to 150°C for 1 hour (without voltage) and stabilised at room temperature for 24 hours before capacitance measurements are made.

2.0 The ageing process is completely repeatable and predictable for a given capacitor.

3.0 Capacitance change is negative and logarithmic in respect to time.

4.0 Class C0G dielectric has a negligible ageing rate.

5.0 Class 2 ceramic dielectrics have ageing rates which will vary from 0.8 to 8%, dependent upon particular ceramic composition employed. This wide capacitance change, as a result of 'shelf' ageing and temperature cycling, illustrates why close-tolerance (less than ±5%) high dielectric constant ceramics should not be specified.

6.0 Soldering both leaded and chip class 2 capacitors into a circuit will, because of the ageing phenomenon, give a temporary increase in capacitance value. The magnitude of this change will be dependent on the soldering temperature, time and dielectric class.

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Quality Requirements

Full details of the Qualification and Testing to Specification requirements are contained in the appropriate IEC/CECC specifications. Below are listed the major test parameters applicable to all our multilayer ceramic products. Under "Requirements Limits", where applicable, typical results of our products are listed.

Rating	Test procedures	Requirement Limits
Capacitance	At 20°C ± 1°C (Ref tests)	
Class 1B/CG	≦1000pF ≦1 volt rms at 1 MHz > 1000pF ≦1 volt rms at 1kHz	E24 Series of values available, see size and capacitance tables
Class 2C1 2R1 2X1	Preconditioning 1 hour at upper category temperature, followed by 24 hours at standard atmospheric conditions 1.0V rms at 1kHz for chip product. 0.5V rms at 1kHz for radial leaded product.	After correcting to allow for 1000 hour ageing E12 series of values available, see size and capacitance tables
Capacitance Tolerance		
Class 1B/CG	as for capacitance	Cr < 10pF ± 0.10pF (B) ± 0.25pF (C) ± 0.50pF (D) ± 1.00pF (F) Cr ≧ 10pF ± 1% (F) ± 2% (G) ± 5% (J) ± 10% (K)
Class 2C1 2R1 2X1	as for capacitance	± 5% (J) ± 10% (K) ± 20% (M)
Tangent of loss angle (Tan δ)		
Class 1B/C	as for capacitance	Cr > 50pF:tan δ ≦ 15×10^{-4} Cr ≦ 50pF: tan δ = 0.015(15/Cr+0.7) Typical results: 0.0005 to 0.0008
Class 2C1 2R1 2X1	as for capacitance	tan δ ≦ 250×10^{-4} Typical results 2C1 - 0.015 to 0.020

Rating	Test procedures	Requirement Limits
Climatic sequence test		
1. Dry heat	15 hours at upper category temperature	No visible damage
2. Damp heat cycle	1 cycle of 24 hours at 55°C ±2°C Relative humidity 95-100% no voltage applied	
3. Cold cycle	Lower category temperature for 2 hours	
4. Low air pressure	20m bar, 15° to 35°C for 5 minutes, during last minute rated voltage applied.	No visible damage No breakdown or flashover
5. Damp heat	Class 1B/CG and Class 2C1, 2R1, 2X1 4 cycles as 2 above: after a recovery period	No visible damage Markings remain legible Capacitance change Class 1B/CG ± 2% or 2pF whichever is greater. Typical results:- negligible change. Class 2C1, 2R1, 2X1 ± 10% Typical results:- chips <0.5%, leaded caps. 1-2% Tangent of loss angle (tan δ) Class 1B/CG - 2 times initial value Typical results:- no change Class 2C1, 2R1, 2X1 - 0.05 Typical results:- no change Insulation resistance Class 1B/CG - 2500MΩ or 25s whichever is less. Typical results:- >20GΩ Class 2C1, 2R1, 2X1, ≧1000MΩ or 25s whichever is less. Typical results:- >20GΩ
Endurance	1000 hours at 1.5 times rated voltage and at upper category temperatures 1B/CG and 2C1, 2R1, 2X1 at 125°C. Recovery (class 2 only) 24 hours at standard atmospheric conditions.	No visible damage. Markings remain legible Capacitance change Class 1B/CG ±2% or 1pF whichever is greater. Typical results:- negligible change. Class 2C1, 2R1, 2X1 ± 10% Typical results:- ±2 to 5% Tan δ change Less than 1.5 times initial value. Typical results:- No change IR change Less than 0.25 times initial value. Typical results:- >20GΩ

Technical Summary

Quality Requirements/Factory and Product Approvals

Rating	Test procedures	Requirement Limits
Robustness of Terminations (Tensile (pull) test) Radial units only	For 0.5mm (0.02 inches) dia leads 10N (1Kg (2.2lbs)). For 0.6mm (0.025) dia leads 10N (1Kg (2.2lbs)).	No visible damage
Bending test Radial units only	2 bends through 90° weight 5N (0.5Kg)	No visible damage
Adhesion Chips only	Chip capacitor mounted on a substrate. A force of 5N (0.5Kg) is applied normally to the line joining the terminations and in a line parallel to the substrate. The force is applied progressively without shock for 10 ± 1 second.	No visible damage
Solderability test Chips only	Flux Bath Temperature 20±2°C; solder bath temperature 230±10°C. immersed in flux bath for 5±1sec; immersed in solder bath for 2±0.5 sec. Recovery for 30-0+10 mins.	Termination area shall be at least 90% covered with smooth solder coating. No more than 10% termination to be leached or dewetted, with not more than 5% concentrated in one area.
Resistance to soldering heat Chips only	Immersed in flux bath for 2 sec; immersed in solder bath 260° +5°C for 10 ± 1 sec.	No capacitance change from initial value. Class 1B/CG - 0.5% or 0.5pF. Typical results:- negligible change. Class 2C1, 2R1, 2X1 - 5% +10% Typical results:- <1%
Solderability Leaded capacitors	No preliminary drying or preconditioning. Temperature as for chip capacitors. Solder bath method, immersion of leads up to 2 + 0.5 - 0mm from the body of the capacitor for 3 seconds using a heat shield.	Good tinning
Resistance to soldering heat Leaded capacitors	Temperature as for chip capacitors. Immersion of the capacitor leads to within 3.5 - 0 + 0.5mm from capacitor body.	No visible damage. Capacitance change from initial Class 1B/CG ≦ 0.5% or 0.5pF whichever is greater. Typical results:- negligible change Class 2C1, 2R1, 2X1 - ≦10% Typical results:- <1%
Destructive Physical Analysis All chips for all product ranges	Sample every batch. Metallographic examination in a suitable resin. Half sample in transverse plane, remainder longitudinal plane. Examination under suitable magnification of X 100 to X 300.	As detailed in the relevant specification
Accelerated Damp Heat Steady State Surface mount chip only	85°C, 85% RH, 500hrs Half - In series 100KΩR 1.5 Vdc Half - In series 6.8KΩR 50 Vdc	Recovery time 4-24 hours IR measurement including series R not less than 10% of initial measurement

Factory Approvals

Factory manufacturing approval	Certificate number
CECC	M/0039/CECC/UK
ISO 9001	FM 21663
SEMKO	0101155 / 0132054
TUV	R2110618
BSI	KM 54929

A number of requirements must be achieved to obtain factory manufacturing approval under the above schemes. They are specified in the appropriate Quality Assurance manuals and concern the following:

1. Appointment and supervision of the factory inspection staff and facilities.
2. Control of the manufacturing process.
3. Operation of the test and calibration facilities.
4. Control of changes in the design and manufacture.
5. Stores procedures.
6. Maintenance of accurate records to enable batch traceability.

After an initial factory audit, the supervision of approvals is continuously monitored by an independent inspection authority.

Product Approval

Standard products are approved to the appropriate CECC specification. A complete listing of our product approvals is available upon request. The approvals give the equipment manufacturer the opportunity to purchase multilayer ceramic capacitors to commonly agreed and widely accepted specifications. Qualification approval of a product involves:

1. Specification of the product in an approved specification meeting the defined rules.
2. Qualification testing, including electrical, mechanical, environmental and life testing.
3. Supervision of testing and authentication of results.

Under these systems where product approval is held a formal certificate of conformity will accompany the components when they are despatched.

Certificate Test Record (CTR)

A periodical summary of certified test records (CTR's) obtained from specified tests for approved components to CECC specifications are available upon request.
Copies of qualification approval certificates are available.
Products approved to CECC specification generally comply with the appropriate MIL specification.

Quality Assurance and Burn-in

The establishment and maintenance of our ongoing quality programme under the 'Factory and Product Approval' schemes, together with the following tests and inspections on all products ensures the conformance of our product to customers' requirements.

1. 100% capacitance and tan δ testing.
2. 100% voltage proof testing.

We can also provide a service to supply 'burn-in or stress screened' product where required on a sample or 100% basis, test conditions subject to negotiation.

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Application Notes

Notes intended to guide and assist our customers in using multilayer ceramic capacitors in surface mount technology are available from Syfer.
The information concentrates on the handling, mounting, connection, cleaning, test and re-work requirements particular to MLC's for SMD technology, to ensure a suitable match between component capability and user expectation. Some extracts are given below.

Handling

Ceramics are dense, hard, brittle and abrasive materials. They are liable to suffer mechanical damage, in the form of chips or cracks, if improperly handled.
Terminations will be abraded onto chip surfaces if loose chips are tumbled in bulk. Metallic tracks will be left on the chip surfaces which might pose a reliability hazard.
Surface mount MLC's should never be handled with fingers; perspiration and skin oils can inhibit solderability and will aggravate cleaning.
MLC's should never be handled with metallic instruments. Metal tweezers should never be used as these can chip the product and may leave abraded metal tracks on the product surface. Plastic or plastic coated metal type are readily available and recommended - these should be used with an absolute minimum of applied pressure.
Counting or visual inspection of MLC's is best performed on a clean glass or hard plastic surface.
If MLC's are dropped or subjected to rough handling, they should be visually inspected before use. Electrical inspection may also reveal gross damage via a change in capacitance, an increase in dissipation factor or a decrease either in insulation resistance or electrical strength.

Transportation

Where possible, any transportation should be carried out with the product in its unopened original packaging. If already opened, any environmental control agents supplied should be returned to packaging and the packaging re-sealed.
Avoid paper and card as a primary means of handling, packing, transportation and storage of loose chip capacitors. Many grades have a sulphur content which will adversely affect termination solderability.
Loose chips should always be packed with sulphur-free wadding to prevent impact or abrasion damage during transportation.

Storage

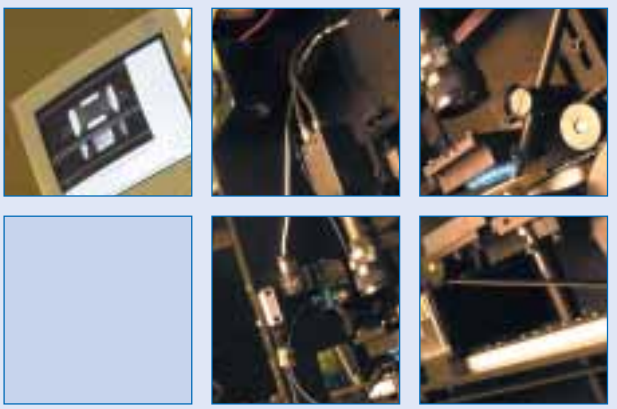
Incorrect storage of surface mount MLC's can lead to problems for the user.
Rapid tarnishing of the terminations, with an associated degradation of solderability, will occur if the product comes into contact with industrial gases such as sulphur dioxide and chlorine. Storage in free air, particularly moist air, can result in termination oxidation.
Packaging should not be opened until the MLC's are required for use. If opened, the pack should be re-sealed as soon as is practicable. Alternatively, the contents could be kept in a sealed container with an environmental control agent.
Long term storage conditions, ideally, should be temperature controlled between -5 and +40°C and humidity controlled between 40 and 60% R.H.
Taped product should be stored out of direct sunlight, which might promote a deterioration in tape or adhesive performance.
Product, stored under the conditions recommended above, in its "as received" packaging, has a minimum shelf life of 2 years.

Mechanical Considerations For Mounted Ceramic Chip Capacitors

Due to its brittle nature, ceramic chip capacitors are more prone to excesses of mechanical stress than other components used in surface mounting.
One of the most common causes of failure is directly attributable to bending the printed circuit board after solder attachment. The excessive or sudden movement of the flexible circuit board stresses the inflexible ceramic block causing a crack to appear at the weakest point, usually the ceramic/termination interface. The crack may initially be quite small and not penetrate into the inner electrodes; however, subsequent handling and rapid changes in temperature will cause the crack to enlarge.
This mode of failure is often invisible to normal inspection techniques as the resultant cracks usually lie under the capacitor terminations and if left, can lead to catastrophic failure. More importantly, mechanical cracks, unless they are severe will not be detected by normal electrical testing of the completed circuit, failure only occuring at some later stage after moisture ingression.
The degree of mechanical stress generated on the printed circuit board is dependent upon several factors including the board material and thickness, the amount of solder and land pattern. The amount of solder applied is important, as an excessive amount reduces the chip's resistance to cracking.
As to where board flexing occurs sufficiently to produce mechanical stress cracks, it is Syfer's experience that more than 90% are due to board depanelisation, a process where two or more circuit boards are separated after soldering is complete. Other manufacturing stages that should be reviewed include:-

1) Attaching rigid components such as connectors, relays, display panels, heat sinks etc.
2) Fitting conventional leaded components. Special care must be exercised when rigid terminals, as found on large can electrolytic capacitors, are inserted.
3) Storage of boards in such a manner which allows warping.
4) Automatic test equipment, particularly the type employing "bed of nails" and support pillars.
5) Positioning the circuit board in its enclosure especially where this is a "snap-fit".

Further information regarding the mechanical stressing of ceramic multilayer chip capacitors is available on request from our sales office.



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Application Notes

Recommended Process Temperature - Time

The various methods of attachment of chips onto substrates invariably involve thermal cycling and the components may be thermally sensitive. This is particularly true of MLC's. Any temperature steps employed must, in broad terms, be kept below 120°C (248°F) and steps of no more than 70°C (158°F) to 80°C (176°F) are preferred when MLC's, size 1812 and above, are used on the substrate. Ideally the pre-heat zone should elevate the substrate from room temperature to solder operations temperature - in practice, constraints are in place as a result of required process throughput, equipment capability and material properties.
The pre-heat temperature rise of the MLC's should be kept to around 2°C (3.6°F) per second and should be reduced below this when larger chip planforms are used. In practice, successful ranges tend to lie in the area 1.5 to 4°C (2.7 to 7.2°F) per second dependent upon substrate and components.

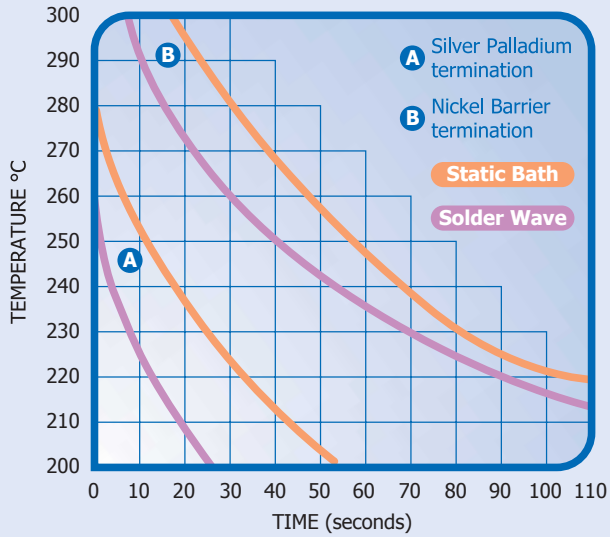
Actual component temperatures may be verified at various points on the board, by the attachment of fine thermocouples with a bead diameter of no more than 0.25mm. This may be effected using a thermally conductive adhesive. The attachment points should be the upper surface of a component termination for Wave soldering (for re-flow methods, attachment should be made to the component footprint). Use of thru' holes for fixing thermocouples should be avoided.
The introduction of a soak, at the end of the pre-heat, is useful, when larger components are used, as this allows temperature uniformity to be established across the substrate. Soldering a 'cool' substrate may induce substrate warpage. The magnitude or direction of the warpage may change on cooling imposing damaging stresses upon the SMD components.
Solder time should be minimised. The maximum permissible solder time that a surface mounted multilayer ceramic capacitor can be subjected to is dependent upon the termination material and the process temperature characteristics.
For chip sizes 1812 and above, cooling to ambient temperature should be allowed to occur naturally. Natural cooling allows a gradual relaxation of thermal mismatch stresses in the solder joints, very important for large chips. Draughts should be avoided. Forced air cooling can induce thermal breakage, and cleaning with cold fluids immediately after a soldering process may result in cracked MLC capacitors.

Solder Time (see Fig 1)

Solder melting time should be minimised. The maximum permissible solder time that a surface mounted multilayer ceramic capacitor can be subjected to is dependent upon the termination material and process temperature/time.
Fig 1 shows Comparative Temperature/Time data for silver palladium and nickel barrier terminations to meet the "Solderability Test" as specified for both a static solder bath and a solder wave. These curves should not be exceeded in terms of the maximum exposure time.

Fig 1. Solder Time Temperature Curves

Recommended maximum exposure time as a function of temperature.



Successive soldering cycles (including rework) are cumulative in terms of temperature and percentage of time in affecting the capacitor in terms of solderability and resistance to soldering heat.

Important Note:

All standard Chip Capacitors are compatible with lead-free soldering.

Capacitor Application Notes (Available direct from Syfer)

- Capacitance ageing of Multilayer Ceramic Capacitors
- Multilayer Ceramic Capacitors and Surface Mount Technology
- Mechanical Considerations for Ceramic Chip Capacitors
- Stacked Chip Capacitor assembly, handling & usage
- Advances in Surface Mount Filtering Technology - New Integrated Passive Components (IPC).
- Multilayer Ceramic EMI Filters
- Multilayer Varistor Filters - Truly multi-functional passive components
- Affordable Transient Protection - Filter connectors with multilayer planar varistor arrays
- Advances in EMI Filters
- Mechanical Cracking of Chip Capacitors

If you require further copies of this catalogue or any of the above mentioned publications, please contact our sales office.
(Tel: +44 (0)1603 723310)

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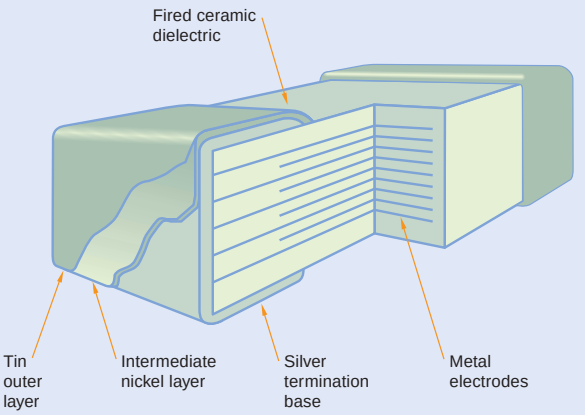
Leaching

Leaching is the term for the dissolution of silver into the solder during the soldering operation. This weakens the terminations leading to an increase in equivalent series resistance (ESR), tan δ and open circuit faults as well as the possibility of the chip becoming detached from the substrate.

To prevent leaching, the following should be observed:-

1. Prework should be kept to a minimum.
2. An adequate preheat period is essential.
3. Solder temperature should be held at the lower end of the normal range.
4. Dwell time should be kept to a minimum.
5. Use ceramic chip capacitors with an "anti-leaching layer". We incorporate a "barrier layer" of nickel in the end terminations to prevent leaching.

Multilayer Ceramic Chip - with Nickel Barrier Termination



Ordering information for Surface Mount Chip Capacitors

Example: .....0805 J 100 0101 J C T □□□

Type No/Size ref

Termination
- Y = Nickel Barrier with Polymeric Silver Termination base
- F = Silver Palladium
- J = Nickel Barrier with Silver Termination base

Voltage d.c.

016 =	16 Volts	1K0 =	1kV
025 =	25 Volts	2K0 =	2kV
050 =	50 Volts	3K0 =	3kV
063 =	63 Volts	4K0 =	4kV
100 =	100 Volts	5K0 =	5kV
200 =	200 Volts		
250 =	250 Volts		
500 =	500 Volts		
630 =	630 Volts		

Capacitance (pF)
- First digit - 0
- Second digit - First significant figure of capacitance value
- Third digit - Second significant figure of capacitance value
- Fourth digit - Number of zeros following. eg. 0102 = 1000pF.

For values that do not fit the model above, insert the capacitance code letter for the decimal point
e.g. 8P20 = 8.2pF
13N6 = 13.6nF

Suffix Code
The remaining alpha/numeric digits are used to denote variations from standard products to customer special requirements (electrical, packing, mechanical, environmental, coding etc.)

Taped and Reeled Chips (see applicable individual catalogue page for quantities)
- T = 178mm (7" reel)
- R = 330mm (13" reel)
- B = Bulk pack - tubs
- C = Bulk pack - cassette

Dielectric code

Dielectric		Classes		
Class	**Code**	**CECC**	**EIA**	**MIL**
Ultra stable	C	1B/CG	C0G(NP0)	CG/(BP)
Stable	X	2R1	X7R	
Ultra High Frequency	Q			
To special order				
Stable	B	2X1		BX
Stable	R	2C1		BZ

Capacitance Tolerance Code

Ultra stable class			Stable class	
Cr < 10pF	± 0.10 pF	B	± 5%	J
	± 0.25 pF	C	± 10%	K
	± 0.5 pF	D	± 20%	M
Cr ≥ 10pF	± 1%	F		
	± 2%	G		
	± 5%	J		
	± 10%	K		

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Chip availability quick reference guide

		0603	0805	1206	1210	1808	1812	2220	2225	3640	5550	8060
16V	C0G	0.47p - 1.2n	1.0p - 4.7n	1.0p - 12n	3.9p - 22n	n/a	10p - 47n	10p - 82n	10p - 100n	n/a	n/a	n/a
	X7R	100p - 100n	100p - 330n	100p - 1.0µ	1.0n - 1.5µ	n/a	3.9n - 3.3µ	10n - 5.6µ	18n - 6.8µ	n/a	n/a	n/a
25V	C0G	0.47p - 1.0n	1.0p - 3.9n	1.0p - 10n	3.9p - 18n	n/a	10p - 33n	10p - 68n	10p - 100n	n/a	n/a	n/a
	X7R	100p - 56n	100p - 220n	100p - 820n	1.0n - 1.2µ	n/a	3.9n - 2.2µ	10n - 4.7µ	18n - 5.6µ	n/a	n/a	n/a
50/63V	C0G	0.47p -470p	1.0p - 2.7n	1.0p - 8.2n	3.9p - 12n	n/a	10p - 27n	10p - 56n	10p - 82n	n/a	n/a	n/a
	X7R	100p - 47n	100p - 180n	100p - 470n	1.0n - 680n	n/a	3.9n - 1.5µ	10n - 2.2µ	18n - 3.3µ	n/a	n/a	n/a
100V	C0G	0.47p - 330p	1.0p - 1.5n	1.0p - 4.7n	3.9p - 8.2n	n/a	10p - 18n	10p - 39n	10p - 56n	n/a	n/a	n/a
	X7R	100p - 10n	100p - 47n	100p - 150n	1.0n - 330n	n/a	3.9n - 680n	10n - 1.0µ	18n - 1.5µ	n/a	n/a	n/a
200/ 250V	C0G	0.47p - 100p	1.0p - 680p	1.0p - 2.2n	3.9p - 3.9n	4.7p - 4.7n	10p - 8.2n	10p - 18n	10p - 22n	n/a	n/a	n/a
	X7R	100p - 5.6n	100p - 27n	100p - 100n	1.0n - 180n	15p - 180n	3.9n - 390n	10n - 680n	18n - 820n	n/a	n/a	n/a
500V	C0G	n/a	1.0p - 270p	1.0p -1.2n	3.9p - 2.7n	4.7p - 2.7n	10p - 6.8n	10p -15n	10 p -18n	10p - 56n	390p - 100n	680p - 180n
	X7R	n/a	10p - 8.2n	10p - 33n	15p - 100n	15p - 100n	22p -270n	180p - 560n	180p - 820n	390p - 1.0µ	560p - 1.8µ	10n - 3.3µ
630V	C0G	n/a	1.0p - 180p	1.0p - 1.0n	3.9p - 1.8n	4.7p - 2.2n	10p -5.6n	10p -10n	10p -15n	n/a	n/a	n/a
	X7R	n/a	n/a	10p - 10n	15p - 27n	15p - 33n	22n - 150n	180p - 330n	180p - 390n	390p - 680n	560p - 1.2µ	10n - 2.2µ
1kV	C0G	n/a	n/a	1.0p - 470p	3.9p - 1.0n	4.7p - 1.2n	10p - 3.3n	10p - 8.2n	10p - 10n	10p - 22n	390p - 39n	680p - 68n
	X7R	n/a	n/a	10p - 2.7n	15p - 6.8n	15p - 18n	22p - 56n	180p - 120n	180p - 150n	390p - 180n	560p - 390n	10n - 1.0µ
2kV	C0G	n/a	n/a	1.0p - 100p	3.9p - 220p	4.7p - 220p	10p - 820p	10p - 1.8n	10p - 2.2n	10p - 5.6n	390p - 10n	680p - 18n
	X7R	n/a	n/a	10p - 1.0n	15p - 2.2n	15p - 2.2n	22p - 4.7n	180p - 12n	180p - 15n	390p - 47n	560p - 82n	10n - 150n
3kV	C0G	n/a	n/a	n/a	n/a	4.7p - 100p	10p - 390p	10p - 820p	10p - 1.0n	10p - 2.2n	390p - 4.7n	680p - 8.2n
	X7R	n/a	n/a	n/a	n/a	15p -680p	22p - 1.8n	180p - 5.6n	180p - 6.8n	390p - 18n	560p - 39n	10n - 68n
4kV	C0G	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	10p - 1.0n	390p - 2.2n	680p - 4.7n
	X7R	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	390p - 6.8n	560p - 15n	10n - 33n
5kV	C0G	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	10p - 560p	390p - 1.5n	680p - 3.3n
	X7R	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	560p - 8.2n	10n - 18n

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CECC approved values by style/voltage - in capacitance code

Surface Mount

CECC Classification	Volts d.c.	0805	1206	1210	1812	2220	2225
1B/CG	50/63	100 - 102	100 - 332	100 - 682	221 - 183	471 - 333	561 - 473
1B/CG	100	100 - 271	100 - 102	100 - 222	221 - 472	471 - 103	561 - 153
1B/CG	200/250	100 - 390	100 - 181	100 - 391	221 - 821	471 - 182	561 - 272
BX/2X1	50/63	101 - 123	681 - 393	102 - 104	392 - 224	123 - 474	152 - 564
BX/2X1	100	101 - 332	681 - 123	102 - 273	392 - 563	123 - 124	152 - 154
BX/2X1	200/250	101 - 102	681 - 472	102 - 103	392 - 223	123 - 473	152 - 683
2C1	50/63	101 - 183	681 - 683	102 - 154	392 - 334	123 - 824	152 - 105
2C1	100	101 - 562	681 - 273	102 - 563	392 - 124	123 - 274	152 - 394
2C1	200/250	101 - 152	681 - 682	102 - 153	392 - 333	123 - 683	152 - 104
X7R/2R1	50/63	101 - 473	681 - 104	102 - 224	393 - 474	123 - 105	152 - 155
X7R/2R1	100	101 - 123	681 - 333	102 - 104	392 - 184	123 - 394	152 - 474
X7R/2R1	200/250	101 - 152	681 - 682	102 - 153	392 - 333	123 - 823	152 - 104

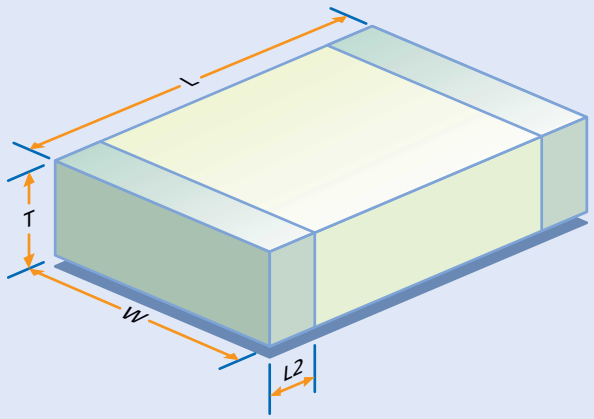
Dipped and Moulded

CECC Classification	Volts d.c.	8111M	8121M	8131M	8123Z	8133Z
1B/CG	50/63	3p9 - 273	3p9 - 273	3p9 - 273	3p9 - 273	3p9 - 273
1B/CG	100	3p9 - 273	3p9 - 273	3p9 - 273	3p9 - 273	3p9 - 273
1B/CG	200/250	3p9 - 273	3p9 - 273	3p9 - 273	3p9 - 273	3p9 - 273
X7R/2R1	50/63	101 - 105	101 - 105	101 - 105	101 - 105	101 - 105
X7R/2R1	100	101 - 105	101 - 105	101 - 105	101 - 105	101 - 105
X7R/2R1	200/250	101 - 105	101 - 105	101 - 105	101 - 105	101 - 105

Dimensions

Dimensions

Size	Length (L) mm inches	Width (W) mm inches	Thickness (T) mm inches max	Termination Band L2 mm inches min	Termination Band L2 mm inches max
0603	1.6 ± 0.2	0.8 ± 0.2	0.8	0.1	0.4
	0.063 ± 0.008	0.031 ± 0.008	0.031	0.004	0.015
0805	2.0 ± 0.3	1.25 ± 0.2	1.3	0.13	0.75
	0.08 ± 0.012	0.05 ± 0.008	0.051	0.005	0.03
1206	3.2 ± 0.3	1.6 ± 0.2	1.6	0.25	0.75
	0.126 ± 0.012	0.063 ± 0.008	0.063	0.01	0.03
1210	3.2 ± 0.3	2.5 ± 0.3	1.8	0.25	0.75
	0.126 ± 0.012	0.10 ± 0.012	0.07	0.01	0.03
1410	3.6 ± 0.3	2.5 ± 0.3	2.0	0.25	0.75
	0.14 ± 0.012	0.1 ± 0.012	0.08	0.01	0.03
1806	4.5 ± 0.35	1.6 ± 0.2	1.3	0.25	0.75
	0.177 ± 0.012	0.063 ± 0.008	0.051	0.01	0.03
1808	4.5 ± 0.35	2.0 ± 0.3	2.0	0.25	1.0
	0.18 ± 0.014	0.08 ± 0.012	0.08	0.01	0.04
1812	4.5 ± 0.35	3.2 ± 0.3	1.8	0.25	1.0
	0.18 ± 0.014	0.126 ± 0.012	0.07	0.01	0.04
2211	5.70 ± 0.4	2.79 ± 0.3	2.54	0.25	0.8
	0.225 ± 0.016	0.110 ± 0.012	0.1	0.01	0.03
2215	5.70 ± 0.4	3.31 ± 0.35	2.54	0.25	0.8
	0.225 ± 0.016	0.15 ± 0.014	0.1	0.01	0.03
2220	5.7 ± 0.4	5.0 ± 0.4	1.8	0.25	1.0
	0.225 ± 0.016	0.197 ± 0.016	0.07	0.01	0.04
2225	5.7 ± 0.4	6.3 ± 0.4	1.8	0.25	1.0
	0.225 ± 0.016	0.25 ± 0.016	0.07	0.01	0.04
3640	9.2 ± 0.5	10.16 ± 0.5	2.5	0.5	1.5
	0.36 ± 0.02	0.40 ± 0.02	0.08	0.02	0.06
5550	14.0 ± 0.5	12.7 ± 0.5	2.5	0.5	1.5
	0.55 ± 0.02	0.50 ± 0.02	0.1	0.02	0.06
8060	20.3 ± 0.5	15.24 ± 0.5	2.5	0.5	1.5
	0.80 ± 0.02	0.60 ± 0.02	0.1	0.02	0.06



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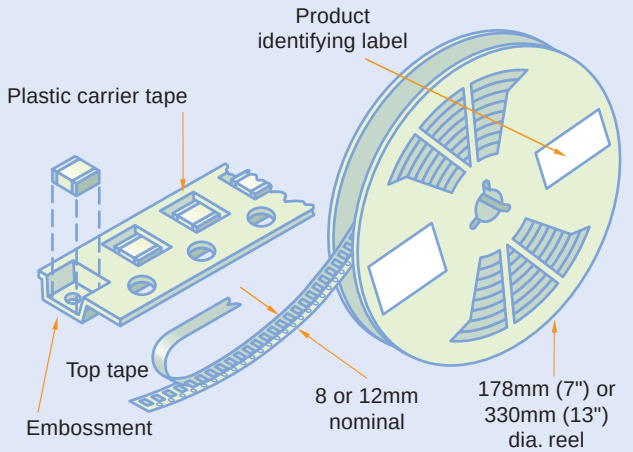
Packaging information

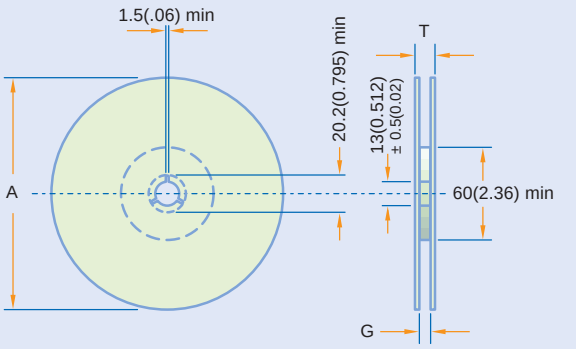
Tape and reel packing of surface mounting chip capacitors for automatic placement are in accordance with IEC60286-3.



Peel force

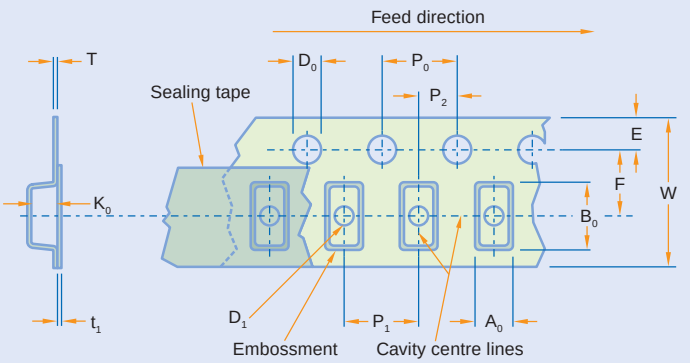
The peel force of the top sealing tape is between 0.2 and 1.0 Newton at 180°. The breaking force of the carrier and sealing tape in the direction of unreeling is greater than 10 Newtons.

Reel dimensions mm (inches)



Symbol	Description	178mm reel	330mm reel
A	Reel diameter	178 (7)	330 (13)
G	Reel inside width	8.4 (0.33)	12.4 (0.49)
T	Reel outside width	14.4 (0.56) max	18.4 (0.72) max

Tape dimensions



Dimensions mm (inches)

Symbol	Description	8mm tape	12mm tape
A_0 B_0 K_0	Width of cavity Length of cavity Depth of cavity	Dependent on chip size to minimize rotation	
W	Width of tape	8.0 (0.315)	12.0 (0.472)
F	Distance between drive hole centres and cavity centres	3.5 (0.138)	5.5 (0.213)
E	Distance between drive hole centres and tape edge	1.75 (0.069)	
P_1	Distance between cavity centres	4.0 (0.156)	8.0 (0.315)
P_2	Axial distance between drive hole centres and cavity centres	2.0 (0.079)	
P_0	Axial distance between drive hole centres	4.0 (0.156)	
D_0	Drive hole diameter	1.5 (0.059)	
D_1	Diameter of cavity piercing	1.0 (0.039)	1.5 (0.059)
XT	Carrier tape thickness	0.3 (0.012) ±0.1 (0.004)	0.4 (0.016) ±0.1 (0.004)
Xt_1	Top tape thickness	0.1 (0.004) max	

Packaging information

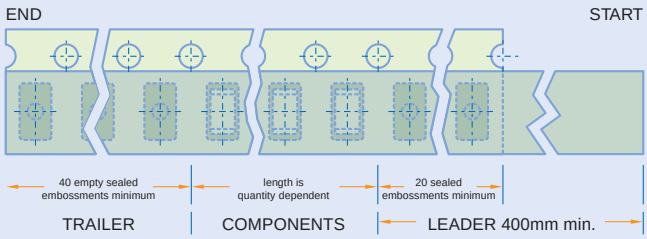
Leader and Trailer

Missing Components

The number of missing components in the tape may not exceed 0.25% of the total quantity with not more than three consecutive components missing. This must be followed by at least six properly placed components.

Identification

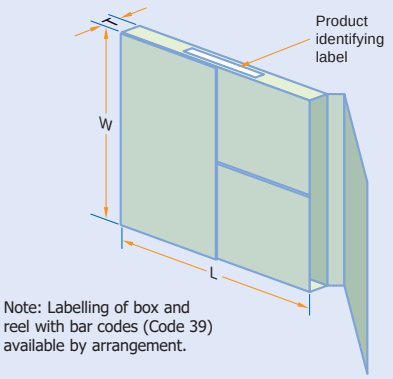
Each reel is labelled with the following information: manufacturer, chip size, capacitance, tolerance, rated voltage, dielectric type, batch number, date code and quantity of components.



Outer Packaging

Outer Carton Dimensions mm (inches) max.

Reel Size	No. of reels	L	W	T
178 (7.0)	1	185 (7.28)	185 (7.28)	25 (0.98)
178 (7.0)	4	190 (7.48)	195 (7.76)	75 (2.95)
330 (13.0)	1	335 (13.19)	335 (13.19)	25 (0.98)



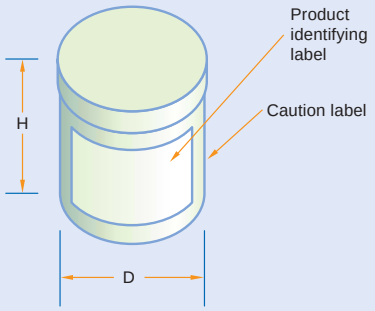
Note: Labelling of box and reel with bar codes (Code 39) available by arrangement.

Bulk Packing - Tubs

Chips are supplied in rigid re-sealable plastic tubs together with impact cushioning wadding. Tubs are labelled with the details: chip size, capacitance, tolerance, rated voltage, dielectric type, batch number, date code and quantity of components.

Dimensions mm (inches)

H	60 (2.36)
D	50 (1.97)



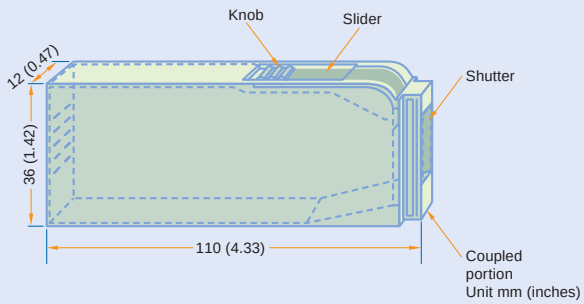
Bulk Packaging-Cassette

Chips can be supplied in a cassette designed for attachment to a surface mount placement machine. The case is made from an anti-static transparent plastic material and can store chips in sizes up to 1206. Labelling is the same as for the bulk tubs.

Capacity

Dimensions mm (inches)

Chip Size	Thickness	Capacity
0603	0.8 (0.031)	15,000
0805	0.6 (0.024)	10,000
1206	0.6 (0.024)	5,000



SYFER TECHNOLOGY LIMITED
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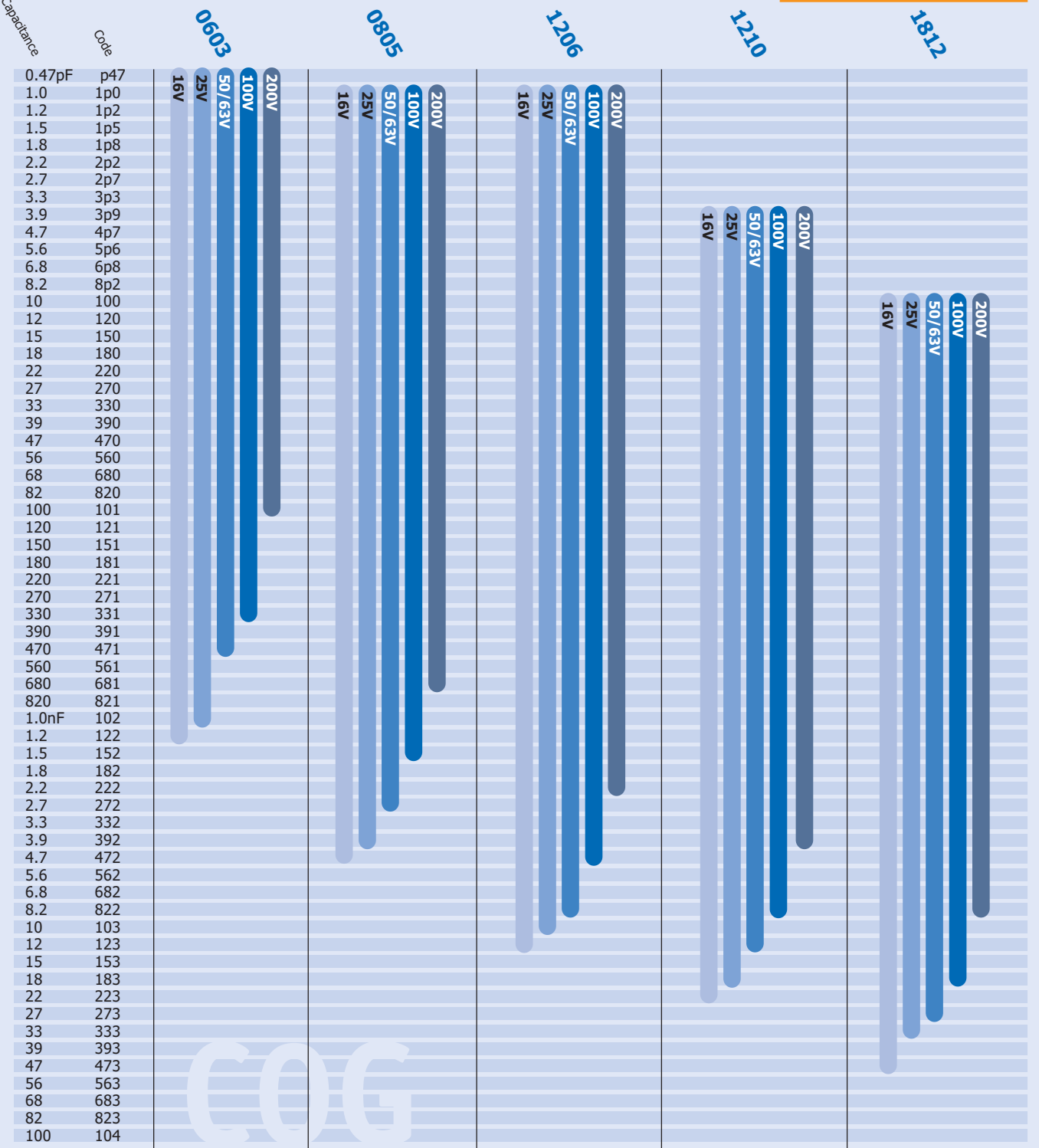
Standard Voltage 16Vdc - 200Vdc

Ultra-stable Dielectric

C0G



	0603	0805	1206	1210	1812
Max. Chip Thickness	0.8mm 0.031″	1.3mm 0.051″	1.6mm 0.063″	1.8mm 0.07″	1.8mm 0.07″
Reel 178mm (7″)	4000	3000	2500	2000	1000
Qty. 330mm (13″)	16000	12000	10000	8000	4000

notes

1. For details of ordering see page 12.
2. We reserve the right to supply reeled quantities commensurate with Chip thickness. Refer to Sales Office.

www.syfer.com

Standard Voltage 16Vdc - 200Vdc

Ultra-stable Dielectric

C0G

Capacitance	Code	2220					2225				
		16V	25V	50/63V	100V	200V	16V	25V	50/63V	100V	200V
0.47pF	p47										
1.0	1p0										
1.2	1p2										
1.5	1p5										
1.8	1p8										
2.2	2p2										
2.7	2p7										
3.3	3p3										
3.9	3p9										
4.7	4p7										
5.6	5p6										
6.8	6p8										
8.2	8p2										
10	100										
12	120										
15	150										
18	180										
22	220										
27	270										
33	330										
39	390										
47	470										
56	560										
68	680										
82	820										
100	101										
120	121										
150	151										
180	181										
220	221										
270	271										
330	331										
390	391										
470	471										
560	561										
680	681										
820	821										
1.0nF	102										
1.2	122										
1.5	152										
1.8	182										
2.2	222										
2.7	272										
3.3	332										
3.9	392										
4.7	472										
5.6	562										
6.8	682										
8.2	822										
10	103										
12	123										
15	153										
18	183										
22	223										
27	273										
33	333										
39	393										
47	473										
56	563										
68	683										
82	823										
100	104										

Max. Chip Thickness	1.8mm 0.07″	1.8mm 0.07″
Reel 178mm (7″)	1000	1000
Qty. 330mm (13″)	4000	4000

notes

1. For details of ordering see page 12.
2. We reserve the right to supply reeled quantities commensurate with Chip thickness. Refer to Sales Office.

SYFER TECHNOLOGY LIMITED
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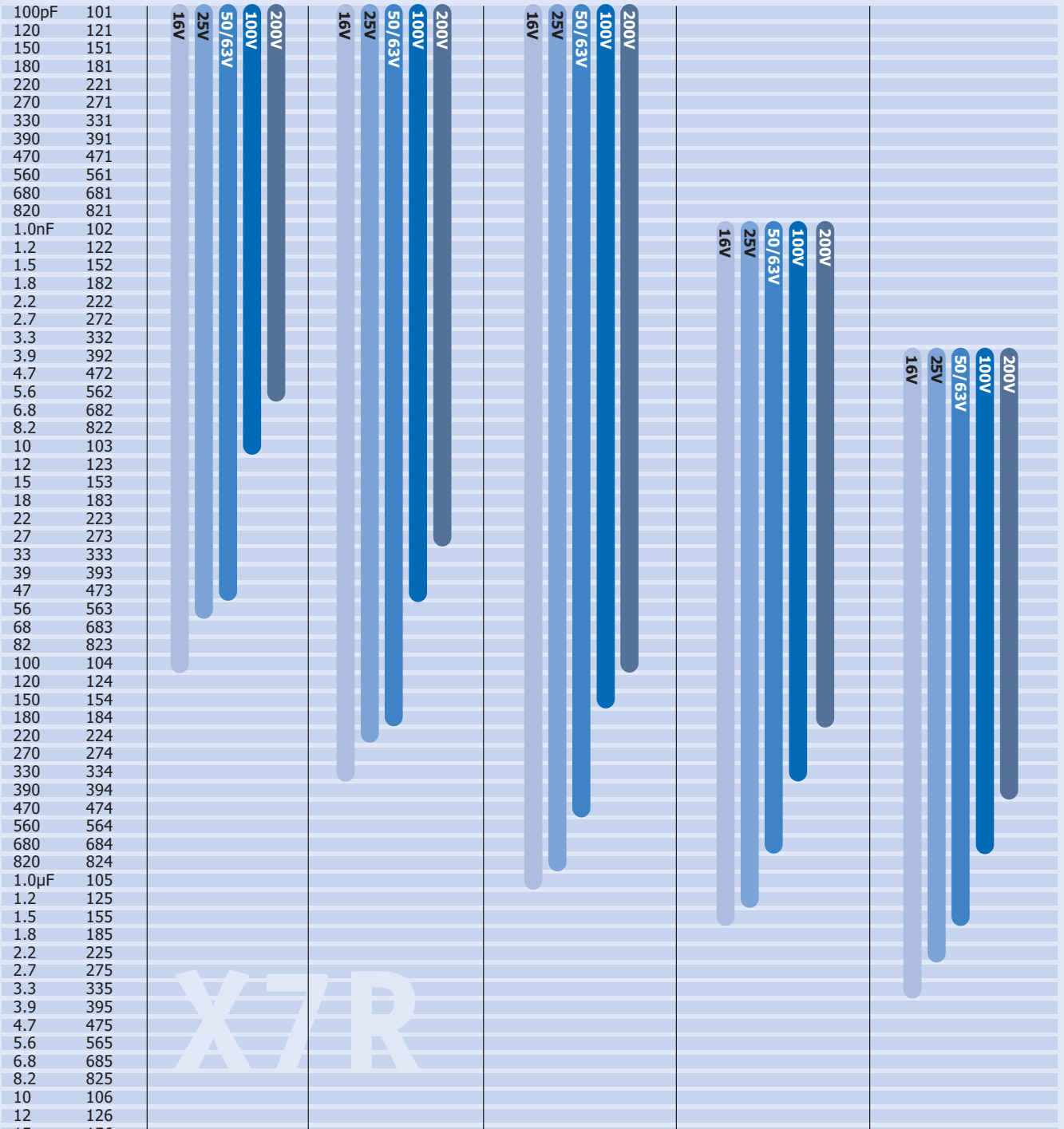
Standard Voltage 16Vdc - 200Vdc

Stable Dielectric

X7R



Capacitance	Code
100pF	101
120	121
150	151
180	181
220	221
270	271
330	331
390	391
470	471
560	561
680	681
820	821
1.0nF	102
1.2	122
1.5	152
1.8	182
2.2	222
2.7	272
3.3	332
3.9	392
4.7	472
5.6	562
6.8	682
8.2	822
10	103
12	123
15	153
18	183
22	223
27	273
33	333
39	393
47	473
56	563
68	683
82	823
100	104
120	124
150	154
180	184
220	224
270	274
330	334
390	394
470	474
560	564
680	684
820	824
1.0µF	105
1.2	125
1.5	155
1.8	185
2.2	225
2.7	275
3.3	335
3.9	395
4.7	475
5.6	565
6.8	685
8.2	825
10	106
12	126
15	156

	0603	0805	1206	1210	1812
Max. Chip Thickness	0.8mm 0.031″	1.3mm 0.051″	1.6mm 0.063″	1.8mm 0.07″	1.8mm 0.07″
Reel 178mm (7″)	4000	3000	2500	2000	1000
Qty. 330mm (13″)	16000	12000	10000	8000	4000

notes

1. For details of ordering see page 12.
2. We reserve the right to supply reeled quantities commensurate with Chip thickness. Refer to Sales Office.

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Surface Mount Chip Capacitors

Standard Voltage 16Vdc - 200Vdc

Stable Dielectric

X7R

Capacitance	Code	2220	2225
100pF	101		
120	121		
150	151		
180	181		
220	221		
270	271		
330	331		
390	391		
470	471		
560	561		
680	681		
820	821		
1.0nF	102		
1.2	122		
1.5	152		
1.8	182		
2.2	222		
2.7	272		
3.3	332		
3.9	392		
4.7	472		
5.6	562		
6.8	682		
8.2	822		
10	103	16V 25V 50/63V 100V 200V	16V 25V 50/63V 100V 200V
12	123		
15	153		
18	183		
22	223		
27	273		
33	333		
39	393		
47	473		
56	563		
68	683		
82	823		
100	104		
120	124		
150	154		
180	184		
220	224		
270	274		
330	334		
390	394		
470	474		
560	564		
680	684		
820	824		
1.0µF	105		
1.2	125		
1.5	155		
1.8	185		
2.2	225		
2.7	275		
3.3	335		
3.9	395		
4.7	475		
5.6	565		
6.8	685		
8.2	825		
10	106		
12	126		
15	156		
Max. Chip Thickness		1.8mm 0.070"	1.8mm 0.070"
Reel 178mm (7")		1000	1000
Qty. 330mm (13")		4000	4000

notes

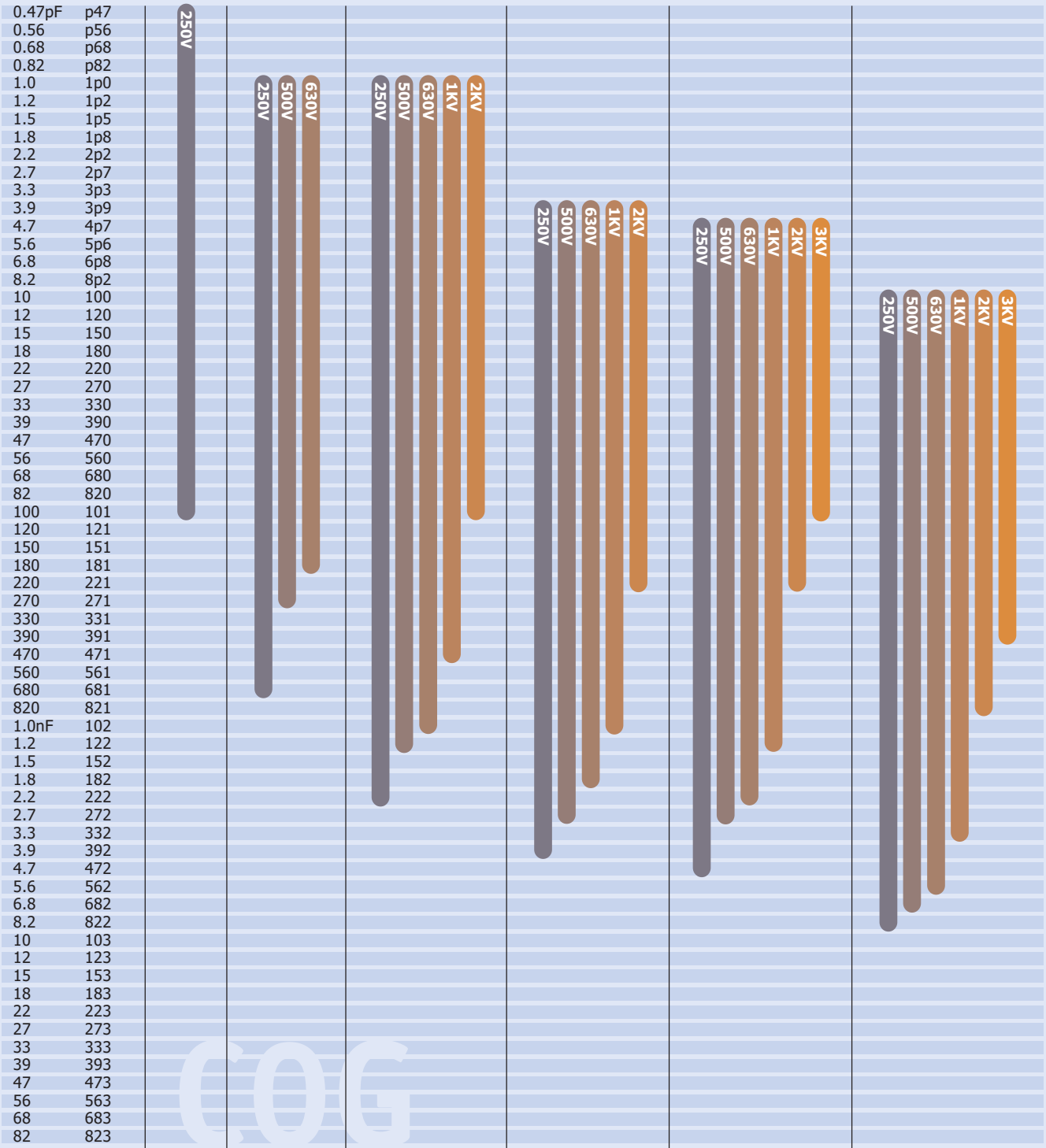
1. For details of ordering see page 12.
2. We reserve the right to supply reeled quantities commensurate with Chip thickness. Refer to Sales Office.

SYFER TECHNOLOGY LIMITED
A DOVER Company

High Voltage 250Vdc - 5kVdc

Ultra-stable Dielectric

C0G



							250V	> 250V
Max. Chip Thickness	0.8mm 0.031″	1.3mm 0.051″	1.6mm 0.063″	2.0mm 0.07″	2.0mm 0.08″	1.8mm 0.07″	2.5mm 0.1″	
Reel 178mm (7″)	4000	3000	2500	2000	1500	1000		
Qty. 330mm (13″)	16000	12000	10000	8000	8000	4000		

notes

1. For details of ordering see page 12.
2. We reserve the right to supply reeled quantities commensurate with Chip thickness. Refer to Sales Office.

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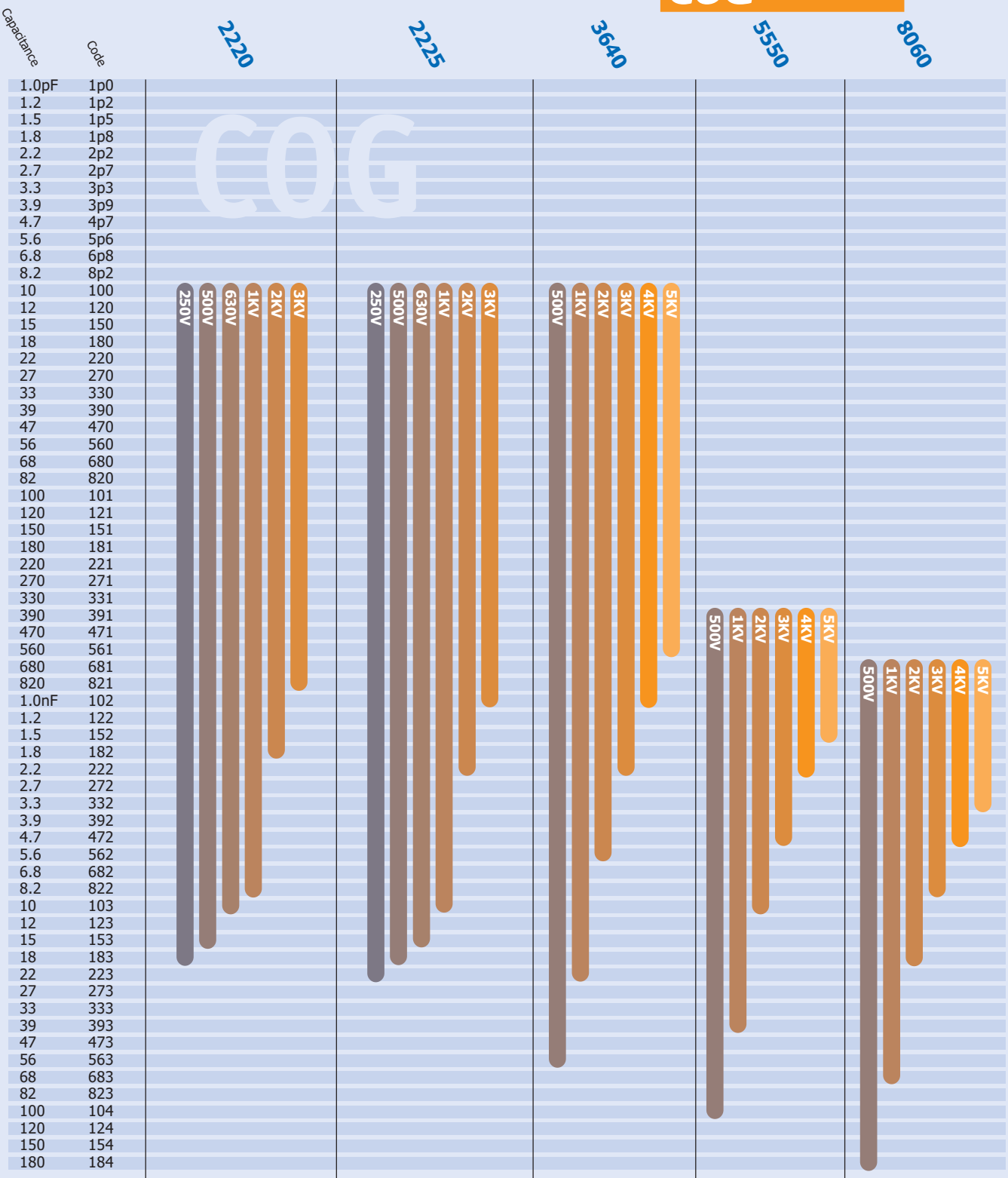
High Voltage 250Vdc - 5kVdc

Ultra-stable Dielectric

C0G



Capacitance	Code
1.0pF	1p0
1.2	1p2
1.5	1p5
1.8	1p8
2.2	2p2
2.7	2p7
3.3	3p3
3.9	3p9
4.7	4p7
5.6	5p6
6.8	6p8
8.2	8p2
10	100
12	120
15	150
18	180
22	220
27	270
33	330
39	390
47	470
56	560
68	680
82	820
100	101
120	121
150	151
180	181
220	221
270	271
330	331
390	391
470	471
560	561
680	681
820	821
1.0nF	102
1.2	122
1.5	152
1.8	182
2.2	222
2.7	272
3.3	332
3.9	392
4.7	472
5.6	562
6.8	682
8.2	822
10	103
12	123
15	153
18	183
22	223
27	273
33	333
39	393
47	473
56	563
68	683
82	823
100	104
120	124
150	154
180	184

	2220		2225		3640	5550	8060
	250V	>250V	250V	>250V			
Max. Chip Thickness	1.8mm 0.07″	2.5mm 0.1″	1.8mm 0.07″	2.5mm 0.1″	2.5mm 0.1″	2.5mm 0.1″	2.5mm 0.1″
Reel 178mm (7″)	1000		1000		n/a	n/a	n/a
Qty. 330mm (13″)	4000		4000		n/a	n/a	n/a

notes

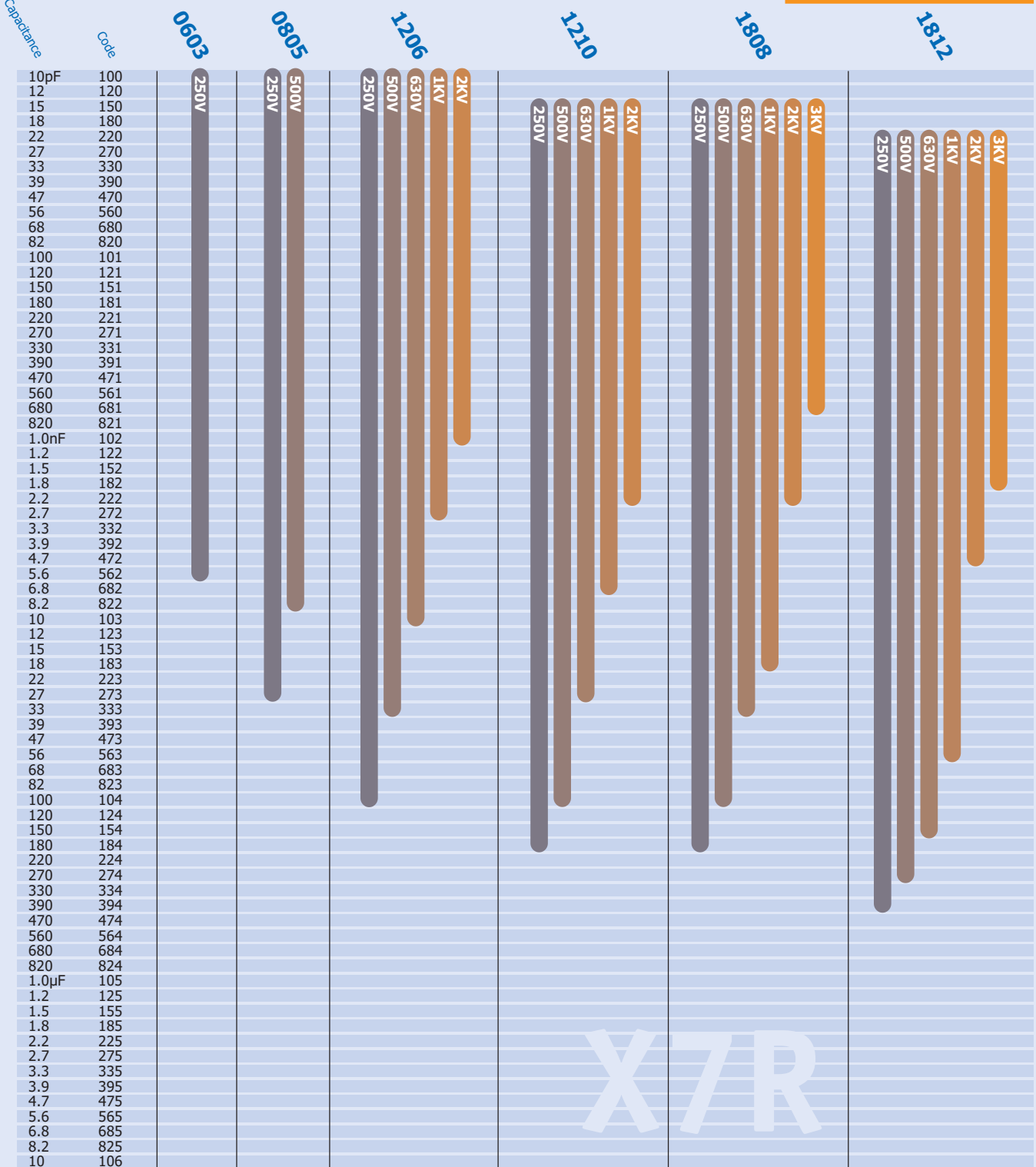
1. For details of ordering see page 12.
2. We reserve the right to supply reeled quantities commensurate with Chip thickness. Refer to Sales Office.

SYFER TECHNOLOGY LIMITED
A DOVER Company

High Voltage 250Vdc - 5kVdc

Stable Dielectric

X7R



Capacitance	Code
10pF	100
12	120
15	150
18	180
22	220
27	270
33	330
39	390
47	470
56	560
68	680
82	820
100	101
120	121
150	151
180	181
220	221
270	271
330	331
390	391
470	471
560	561
680	681
820	821
1.0nF	102
1.2	122
1.5	152
1.8	182
2.2	222
2.7	272
3.3	332
3.9	392
4.7	472
5.6	562
6.8	682
8.2	822
10	103
12	123
15	153
18	183
22	223
27	273
33	333
39	393
47	473
56	563
68	683
82	823
100	104
120	124
150	154
180	184
220	224
270	274
330	334
390	394
470	474
560	564
680	684
820	824
1.0µF	105
1.2	125
1.5	155
1.8	185
2.2	225
2.7	275
3.3	335
3.9	395
4.7	475
5.6	565
6.8	685
8.2	825
10	106

	0603	0805	1206	1210 250V	1210 >250V	1808	1812 250V	1812 >250V
Max. Chip Thickness	0.8mm 0.031″	1.3mm 0.051″	1.6mm 0.063″	1.8mm 0.07″	2.0mm 0.08″	2.0mm 0.08″	1.8mm 0.07″	2.5mm 0.1″
Reel 178mm (7″)	4000	3000	2500	2000		1500	1000	
Qty. 330mm (13″)	16000	12000	10000	8000		8000	4000	

notes

1. For details of ordering see page 12.
2. We reserve the right to supply reeled quantities commensurate with Chip thickness. Refer to Sales Office.

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High Voltage 250Vdc - 5kVdc

Stable Dielectric

X7R

Capacitance	Code	2220	2225	3640	5550	8060
10pF	100					
12	120					
15	150					
18	180					
22	220					
27	270					
33	330					
39	390					
47	470					
56	560					
68	680					
82	820					
100	101					
120	121					
150	151					
180	181	250V 500V 630V 1KV 2KV 3KV	250V 500V 630V 1KV 2KV 3KV			
220	221					
270	271					
330	331					
390	391					
470	471			500V 1KV 2KV 3KV 4KV		
560	561					
680	681					
820	821					
1.0nF	102					
1.2	122					
1.5	152					
1.8	182					
2.2	222					
2.7	272					
3.3	332					
3.9	392					
4.7	472				500V 1KV 2KV 3KV 4KV 5KV	
5.6	562					
6.8	682					
8.2	822					
10	103					500V 1KV 2KV 3KV 4KV 5KV
12	123					
15	153					
18	183					
22	223					
27	273					
33	333					
39	393					
47	473					
56	563					
68	683					
82	823					
100	104					
120	124					
150	154					
180	184					
220	224					
270	274					
330	334					
390	394					
470	474					
560	564					
680	684					
820	824					
1.0µF	105					
1.2	125					
1.5	155					
1.8	185					
2.2	225					
2.7	275					
3.3	335					
3.9	395					
4.7	475					
5.6	565					
6.8	685					
8.2	825					
10	106					

	250V	>250V	250V	>250V			
Max. Chip Thickness	1.8mm 0.07″	2.5mm 0.1″	1.8mm 0.07″	2.5mm 0.1″	2.5mm 0.1″	2.5mm 0.1″	2.5mm 0.1″
Reel 178mm (7″)	1000		1000		n/a	n/a	n/a
Qty. 330mm (13″)	4000		4000		n/a	n/a	n/a

notes

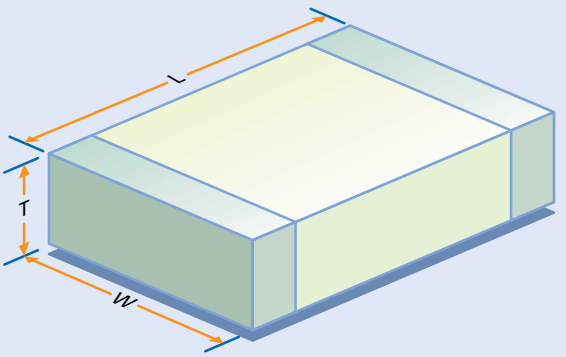
1. For details of ordering see page 12.
2. We reserve the right to supply reeled quantities commensurate with Chip thickness. Refer to Sales Office.

SYFER TECHNOLOGY LIMITED
A DOVER Company

Tip and Ring

X7R

Syfer's range of 250V d.c. chip capacitors is ideal for telephone line filtering (Tip'N Ring) applications.
These parts are rated for telephone voltages and block the DC line voltage whilst passing the subscriber's AC signal pulse. They are designed as replacements for high voltage leaded film capacitors thereby saving PC board space and reducing weight.
This range has a wide band operation, low ESR, excellent high frequency filtering and improved temperature performance compared to film capacitors.



Capacitance Range	100nF to 1.0µF
Chip Sizes	1812, 2220, 2225 (1825 available to special order)
Temperature Range	-55°C to +125°C
Dielectric Withstand Voltage	Minimum 500V (5 seconds)
Dielectric	X7R
Voltage	250V d.c.
Life Test	1000hrs, 300V d.c. at 85°C
Taped and Reeled	1812 1K pieces on 178mm (7") reels 4K pieces on 330mm (13") reels 2220/2225 500 pieces on 178mm (7") reels 2K pieces on 330mm (13") reels

Type	**1812**	**2220**	**2225**
Dimensions mm (inches)			
Length (L)	4.5±0.35 (0.18±0.014)	5.7±0.4 (0.22±0.016)	5.7±0.4 (0.22±0.016)
Width (W)	3.2±0.3 (0.13±0.012)	5.0±0.4 (0.2±0.016)	6.3±0.4 (0.25±0.016)
Thickness (T) Max	2.0 (0.08)	2.5 (0.1)	2.5 (0.1)
Rated voltage d.c.	250V	250V	250V

Cap. range	**Code**	Minimum and Maximum capacitance values available
100nF	104	
120nF	124	
150nF	154	
180nF	184	
220nF	224	
270nF	274	
330nF	334	
390nF	394	
470nF	474	
560nF	564	
680nF	684	
820nF	824	
1.0µF	105	

Ordering Information

1812	J	250	0474	K	X	T
Chip Size	**Termination** J = Nickel Barrier	**Voltage** 250 = 250Vdc	**Capacitance** Expressed in picofarads (pF). First digit is 0. Second and third digits are significant figures of capacitance code. The fourth digit is number of zeros following. eg: 0474 = 470,000pF = 470nF	**Tolerance** J = ± 5% K = ±10% M = ±20%	**Dielectric** X = X7R	**Packaging** T = 178mm (7") reel R = 330mm (13") reel B = Bulk

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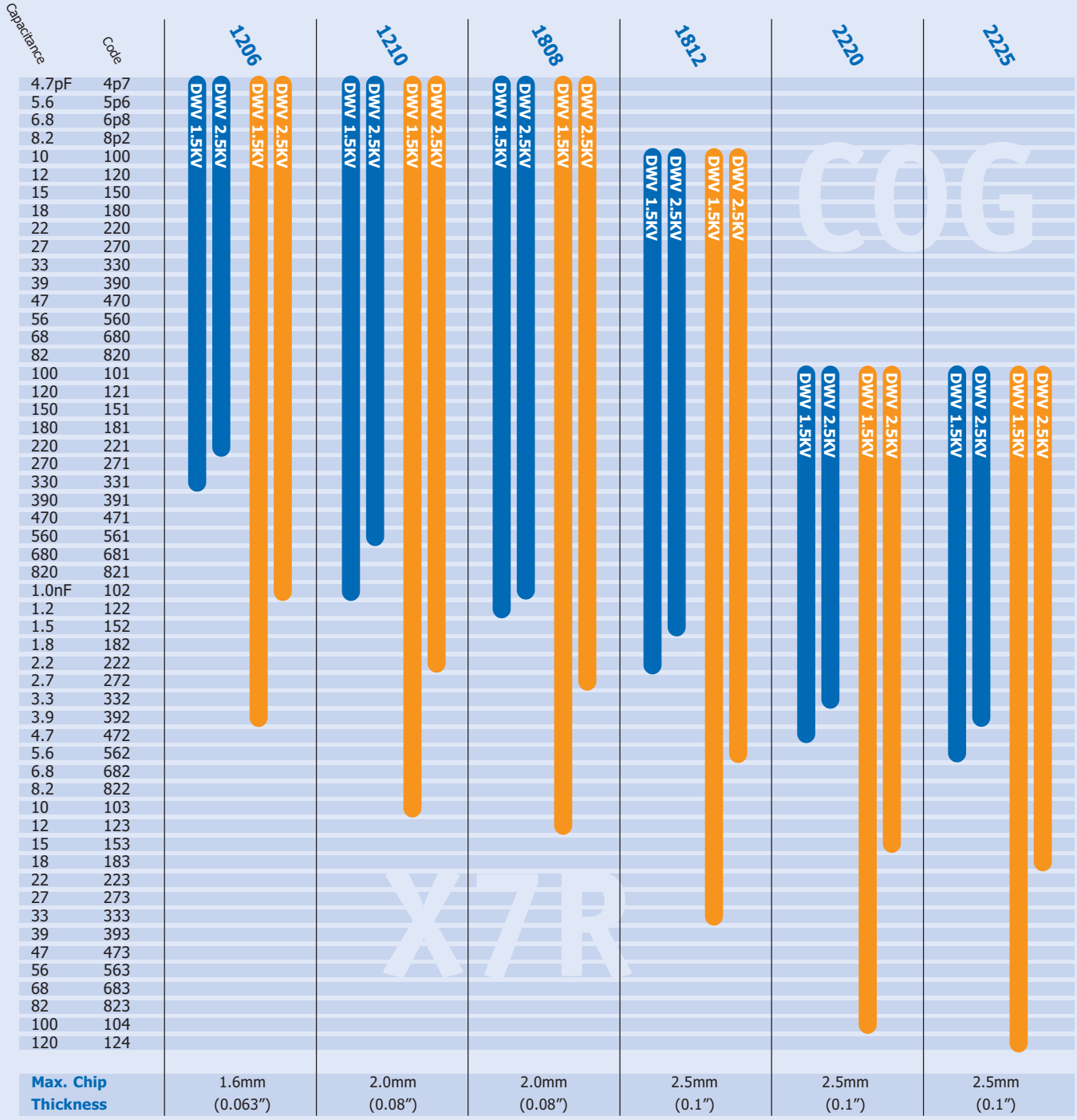
High Dielectric Withstand Voltage

C0G/X7R

High Dielectric Withstand Voltage Range

The Syfer DWV range is specifically designed for use in applications where a high Dielectric Withstand Voltage (DWV) is required. DWV ratings of 1500Vdc and 2500Vdc are available in chip sizes from 1206 to 2225, in both C0G and X7R dielectrics. These ratings are based on an application of the DWV voltage for a period of up to 60 seconds (where the charging current is limited to 50mA). These parts have a continuous rated voltage of 500Vdc/250Vac. This product is 100% DWV tested at the specified voltages to ensure Flashover (arcing) across the surface does not occur. For other rated voltages or DWV voltages, consult the Syfer sales department.

C0G X7R



	1206	1210	1808	1812	2220	2225
Max. Chip Thickness	1.6mm (0.063")	2.0mm (0.08")	2.0mm (0.08")	2.5mm (0.1")	2.5mm (0.1")	2.5mm (0.1")

notes

1. For specific ordering information refer to Sales Office.

SYFER TECHNOLOGY LIMITED
A DOVER Company

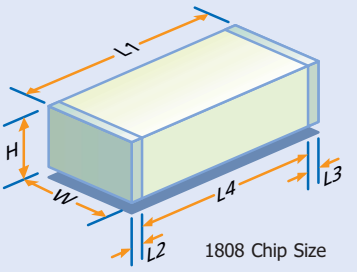
Safety Certified Surge Protection Chip

C0G

Syfer Technology's Surge Protection (SP) range of ceramic chip capacitors are Class Y3/X2 compliant and designed specifically for use in equipment certified to IEC 60950 including modems, faxes, telephones and other electronic equipment where over voltage surges can occur - i.e. a lightning strike.

This range of capacitors is approved and certified by SEMKO (certificate number 0101155/01 for X2 : 0101155/02 for Y3) and TUV (certificate number R2110618).

An application guide is available on request.



1808 Chip Size

Marked parts can be released to both SEMKO and TUV approval. Unmarked parts can be supplied tested in accordance with, but not certified by, SEMKO and TUV.

SEMKO

TÜV Rheinland Product Safety — BAUART GEPRÜFT TYPE APPROVED

Specification	Details
EN132400: 1994 A2: 1998 + A3: 1998 + A4: 1999 IEC 60384-14 second edition 1993 + A1: 1995	Meets the electrical requirements of these specifications for class Y3 and X2 devices. These capacitors do not meet the creepage distance and marking requirements of these specifications.
EN 61000-4-5 IEC 1000-4-5 IEC 801-4-5	Meets the requirements within these specifications for impulse testing, for 1.2/50µS (2Ω source) and 10/700µS (15Ω source) waveforms. Peak value for both waveforms = 2.5kV.
IEC 60950: 1992	Certified for use in equipment intending to be certified to IEC 60950. Units meet the creepage limitations set out within this specification. Impulse requirements for this specification are met or exceeded by those specified in EN 132400 and EN 61000-4-5.
IEEE 802.3	Meets the 1500Vrms isolation requirements of section 12.10.1 of this specification.

Capacitance Specification

Nominal Cap value (E12 range)	Tolerance	DF Limit Calculate max. as follows:-
4.7pF - 8.2pF	±0.25pF, ±0.5pF	0.1 x ((15/Cr) +0.7)
10pF - 47pF	±1%, ±2%, ±5%, ±10%	0.1 x ((15/Cr) +0.7)
56pF - 1000pF	±1%, ±2%, ±5%, ±10%	0.1% Max.

Electrical Specification

Operating Temperature	-55°C to +125°C
Temperature Coefficient	C0G = 0 ± 30 ppm/°C, Ultra Stable Class 1 Ceramic (EIA Class 1)
Insulation resistance at +25°C	>100GΩ
Insulation resistance at +125°C	>10GΩ
Dielectric Strength (DWV)	1500VAC/3000VDC
Rated voltage	250VAC
Climatic Category (IEC)	55/125/56
Ageing rate	Zero
Test parameters for capacitance	1Vrms @ 1MHz @ 20°C
Test parameters for DF	1Vrms @ 1MHz @ 20°C

Mechanical Specification

Chip Size	1808
Length (L1)	4.5mm ± 0.35mm (0.18" ± 0.014")
Width (W)	2.0mm ± 0.3mm (0.08" ± 0.012")
Thickness (H)	2.0mm (0.08") Max.
Termination Bands (L2, L3)	0.25 - 0.80mm (0.01" - 0.03")
Creepage Distance (L4)	2.5mm (0.1") Min.
Termination Material	Nickel Barrier (Tin over Nickel)
Solderability	IEC 68-2-20

Reeled Quantities	178mm (7")	1500
	330mm (13")	8000

Ordering Information

1808	J	A25	0102	J	C	T	SP	U
Chip Size	**Termination** J= Nickel Barrier	**Voltage** A25=250VAC	**Capacitance** Expressed in picofarads (pF). First digit is 0. Second and third digits are significant figures of capacitance code. The fourth digit is number of zeros following. Example: 0102=1000pF. For values below 10pF insert a P for the decimal point. eg: 8P20=8.2pF	**Tolerance** <10pF C = ±0.25pF D = ±0.5pF ⩾10pF F = ±1% G = ±2% J = ±5% K = ±10%	**Dielectric** C=C0G	**Packaging** T = 178mm (7") reel R = 330mm (13") reel B = Bulk	SP=1808 Safety tested surge protection capacitors (marked)	U=Unmarked

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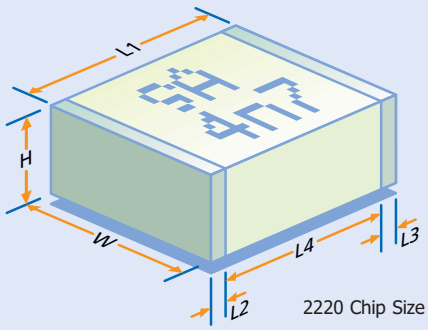
250Vac Safety Standard Approved Chip

X7R

Syfer Technology's range of Safety Standard Approved Capacitors are approved and certified by BSI to IEC 60384-14 2nd Edition: 1993 and EN 132400: 1995.
Class X1/Y2 (Syfer Type A) covers capacitance values from 150pF to 4.7nF.
Class X2 (Syfer Type B) covers capacitance values from 150pF to 10nF.
These surface mount capacitors offer high capacitance values in a small low cost package size, ideal for automatic placement.
Ideal for use in modems, faxes, telephones, the AC line of the switching power supply of battery chargers, AC adaptors and many other applications.



2220 Chip Size

IEC 60384-14: 1993+A1

All product will be marked with the Syfer Logo, type code and capacitance value, as per IEC384-14 / EN132400

Capacitance Specification

Chip Size	Nominal Cap value (E12 range)	Tolerance	Class	Syfer Type
2220	150pF - 4.7nF	±10%, ±20%	X1/Y2	A
2220	150pF - 10nF	±10%, ±20%	X2	B

Ranges

Capacitance	Syfer part Number	Syfer Type	Class
150pF	2220JA250151*XTB16	Type A	X1/Y2
180pF	2220JA250181*XTB16		
220pF	2220JA250221*XTB16		
270pF	2220JA250271*XTB16		
330pF	2220JA250331*XTB16		
390pF	2220JA250391*XTB16		
470pF	2220JA250471*XTB16		
560pF	2220JA250561*XTB16		
680pF	2220JA250681*XTB16		
820pF	2220JA250821*XTB16		
1nF	2220JA250102*XTB16		
1.2nF	2220JA250122*XTB16		
1.5nF	2220JA250152*XTB16		
1.8nF	2220JA250182*XTB16		
2.2nF	2220JA250222*XTB16		
2.7nF	2220JA250272*XTB16		
3.3nF	2220JA250332*XTB16		
3.9nF	2220JA250392*XTB16		
4.7nF	2220JA250472*XTB16		
5.6nF	2220JA250562*XTB17	Type B	X2
6.8nF	2220JA250682*XTB17		
8.2nF	2220JA250822*XTB17		
10nF	2220JA250103*XTB17		

Electrical Specification

Rated voltage	250Vac
Dielectric Type	X7R (2R1, CECC ±15%, no D.C. Bias)
Temperature Range	-55°C to +125°C
Climatic Category	55/125/56/C
Insulation resistance	100GΩ
Ageing rate	1% per decade of time
Voltage Proof	3000Vdc/2000Vac

Mechanical Specification

Chip Size	2220
Length (L1)	5.7mm ± 0.4mm (0.225" ± 0.016")
Width (W)	5.0mm ± 0.4mm (0.197" ± 0.016")
Thickness (H)	2.5mm Max. (0.1" Max.)
Termination Bands (L2, L3)	0.25 - 0.65mm (0.01" - 0.026")
Creepage Distance (L4)	4.0mm Min. (0.16" Min.)

Reeled Quantities	178mm (7")	1000
	330mm (13")	4000

Ordering Information

2220	J	A25	0471	K	X	T	B16
Chip Size	**Termination** J= Nickel Barrier	**Voltage** A25=250VAC	**Capacitance** Expressed in picofarads (pF). First digit is 0. Second and third digits are significant figures of capacitance code. The fourth digit is number of zeros following. Example: 0471=470pF.	**Tolerance** K = ±10% M= ±20%	**Dielectric** X = X7R	**Packaging** T = 178mm (7") reel R = 330mm (13") reel B = Bulk	B16 = Type A: X1/Y2 B17 = Type B: X2

notes

1. For X2 (Type B) values below 5.6nF, X1 (Type A) parts will be substituted.
2. The normal failure mode of Multilayer Ceramic Capacitors is short circuit and as such due consideration should be made to the requirements of IEC384-14 / EN132400 for class X1/X2 and Y2 capacitors, and their connection to mains voltages.

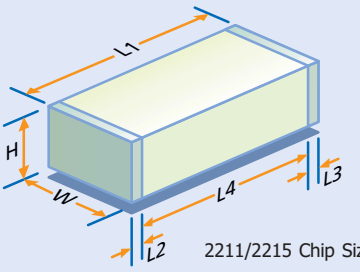
SYFER TECHNOLOGY LIMITED
A DOVER Company

Safety Surge Protection Chip

C0G

Syfer Technology has approval for a range of ceramic chip capacitors to Class Y2/X1 designed specifically for use in equipment certified to IEC 60950 (2000 edition) including modems, faxes, telephones and other electronic equipment where over voltage surges can occur - i.e. a lightning strike.

This range of capacitors is approved and certified by SEMKO (certificate number 0132054 / 01-02) and TUV.



2211/2215 Chip Sizes

Marked parts can be released to both SEMKO and TUV approval. Unmarked parts can be supplied tested in accordance with, but not certified by, SEMKO and TUV.

SEMKO

TÜV Rheinland Product Safety — BAUART GEPRÜFT — TYPE APPROVED

Specification	Details
EN132400: 1994 A2: 1998 + A3: 1998 + A4: 1999 IEC 60384-14 second edition 1993 + A1: 1995	Meets the electrical requirements of these specifications for class Y2 and X1 devices.
IEC 60950: 2000	Certified for use in equipment intending to be certified to IEC 60950.
IEEE 802.3	Meets the 1500Vrms isolation requirements of section 12.10.1 of this specification.

Capacitance Specification

Syfer Chip Size	Nominal value (E12 range)	Cap Tolerance	DF Limit Calculate max. as follows:-
2211	4.7pF - 8.2pF	±0.25pF, ±0.5pF	0.1 x ((15/Cr) +0.7)
2211	10pF - 47pF	±1%, ±2%, ±5%, ±10%	0.1 x ((15/Cr) +0.7)
2211	56pF - 680pF	±1%, ±2%, ±5%, ±10%	0.1% Max.
2215	820pF - 1000pF	±1%, ±2%, ±5%, ±10%	0.1% Max.

Electrical Specification

Operating Temperature	-55°C to +125°C
Temperature Coefficient	C0G = 0 ± 30 ppm/°C, Ultra Stable Class 1 Ceramic (EIA Class 1)
Insulation resistance at +25°C	>100GΩ
Insulation resistance at +125°C	>10GΩ
Dielectric Strength (DWV)	1500VAC/3000VDC
Rated voltage	250VAC
Climatic Category (IEC)	55/125/56
Ageing rate	Zero
Test parameters for capacitance	1Vrms @ 1MHz @ 20°C
Test parameters for DF	1Vrms @ 1MHz @ 20°C

Mechanical Specification

Length (L1)		5.7mm ± 0.4mm (0.225" ± 0.016")
Width (W)	**2211 size**	2.79mm ± 0.3mm (0.110" ± 0.012")
	2215 size	3.81mm ± 0.35mm (0.150" ± 0.014")
Thickness (H)		2.54 (0.1) Max.
Termination Bands (L2, L3)		0.25 - 0.80mm (0.01" - 0.03")
Creepage Distance (L4)		4.0mm (0.16") Min.
Termination Material		Nickel Barrier (Tin over Nickel)
Solderability		IEC 68-2-20

Reeled Quantities	178mm (7")	750
	330mm (13")	3000

Ordering Information

2211	J	A25	0681	J	C	T	-	U
Chip Size	**Termination** J= Nickel Barrier	**Voltage** A25=250VAC	**Capacitance** Expressed in picofarads (pF). First digit is 0. Second and third digits are significant figures of capacitance code. The fourth digit is number of zeros following. Example: 0681=680pF. For values below 10pF insert a P for the decimal point. eg: 8P20=8.2pF	**Tolerance** <10pF C = ±0.25pF D = ±0.5pF ⩾10pF F = ±1% G = ±2% J = ±5% K = ±10%	**Dielectric** C=C0G	**Packaging** T = 178mm (7") reel R = 330mm (13") reel B = Bulk	Safety tested surge protection capacitors (marked) Code to be agreed	U=Unmarked

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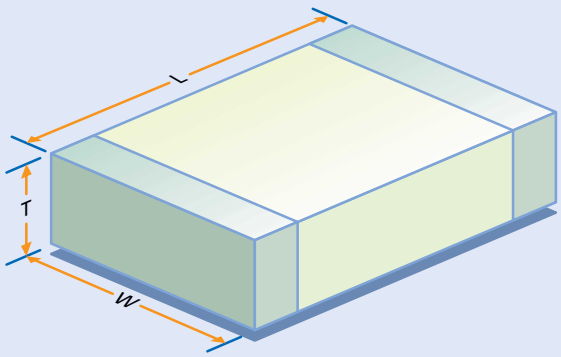
High Temperature Chip

X8R

Description

The X8R dielectric will operate from -55°C to +150°C, with a maximum capacitance change ±15% (without applied voltage).
The devices are available in sizes 0805 to 2225, with voltage ranges from 25V to 200V and capacitance values from 1nF to 1.8µF.
The capacitors have been developed by Syfer to meet demand from various applications in the automotive and industrial markets and in other electronic equipment exposed to high temperatures. The increased use of electronics in automotive "under the hood" applications has created demand for this product range.
The X8R range incorporates a specially formulated termination with a nickel barrier finish that has been designed to enhance the mechanical performance of these SMD chip capacitors in harsh environments typically present in automotive applications.



Capacitance Range
1.0nF to 1.8µF

Temperature Coefficient of Capacitance (TCC)
± 15% from -55°C to +150°C

Dissipation Factor (DF)
≤ 0.025

Insulation Resistance (IR)
100G Ω or 1000secs (whichever is the less).

Dielectric Withstanding Voltage (DWV)
2.5 x rated voltage for 5±1 seconds,
50 mAmps charging current maximum.

Ageing Rate
1% per decade (typical)

Size		0805	1206	1210	1812	2220	2225
Length (L).mm		2.0±0.3	3.2±0.3	3.2±0.3	4.5±0.35	5.7±0.4	5.7±0.4
Width (W).mm		1.25±0.2	1.6±0.2	2.5±0.3	3.2±0.3	5.0±0.4	6.3±0.4
Thickness (H). max		1.3	1.6	1.8	1.8	1.8	1.8
Min. Cap. Value		1.0nF	2.2nF	4.7nF	6.8nF	10nF	10nF
Max. Cap. Value according to the rated d.c. voltage	*25V*	56nF	180nF	330nF	680nF	1.5µF	1.8µF
	50V	33nF	120nF	220nF	470nF	680nF	1.0µF
	100V	15nF	56nF	120nF	220nF	470nF	560nF
	200V	10nF	33nF	68nF	120nF	220nF	330nF
ReeledQuantity	*178mm (7" reel)*	3000	2500	2000	1000	1000	1000
	330mm (13" reel)	12000	10000	8000	4000	4000	4000

Available in E12 values: 10, 12, 15, 18, 22, 27, 33, 39, 47, 56, 68, 82

Ordering Information

1206	Y	100	0473	K	N	T
Chip Size 0805 1206 1210 1812 2220 2225	**Termination** Y = Nickel Barrier with polymeric silver termination	**Voltage dc** 025 = 25V 050 = 50V 100 = 100V 200 = 200V	**Capacitance** Expressed in picofarads (pF). First digit is 0. Second and third digits are significant figures of capacitance code. The fourth digit is number of zeros following. eg: 0473=47000pF =47nF.	**Tolerance** J = ±5% K = ±10% M = ±20%	**Dielectric** N = X8R	**Packaging** T = 178mm (7") reel R = 330mm (13") reel B = Bulk

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Low Profile - 25/50V

C0G/X7R

Capacitance	Code	C0G 0805	C0G 1206	C0G 1210	X7R 0805	X7R 1206	X7R 1210
0.47pF	0p47	0.45 / 0.45	0.45 / 0.45	0.45 / 0.45			
0.56	0p56	0.45 / 0.45	0.45 / 0.45	0.45 / 0.45			
0.68	0p68	0.45 / 0.45	0.45 / 0.45	0.45 / 0.45			
0.82	0p82	0.45 / 0.45	0.45 / 0.45	0.45 / 0.45			
1.0	1p0	0.45 / 0.45	0.45 / 0.45	0.45 / 0.45			
1.2	1p2	0.45 / 0.45	0.45 / 0.45	0.45 / 0.45			
1.5	1p5	0.45 / 0.45	0.45 / 0.45	0.45 / 0.45			
1.8	1p8	0.45 / 0.45	0.45 / 0.45	0.45 / 0.45			
2.2	2p2	0.45 / 0.45	0.45 / 0.45	0.45 / 0.45			
2.7	2p7	0.45 / 0.45	0.45 / 0.45	0.45 / 0.45			
3.3	3p3	0.45 / 0.45	0.45 / 0.45	0.45 / 0.45			
3.9	3p9	0.45 / 0.45	0.45 / 0.45	0.45 / 0.45			
4.7	4p7	0.45 / 0.45	0.45 / 0.45	0.45 / 0.45			
5.6	5p6	0.45 / 0.45	0.45 / 0.45	0.45 / 0.45			
6.8	6p8	0.45 / 0.45	0.45 / 0.45	0.45 / 0.45			
8.2	8p2	0.45 / 0.45	0.45 / 0.45	0.45 / 0.45			
10	100	0.45 / 0.45	0.45 / 0.45	0.45 / 0.45			
12	120	0.45 / 0.45	0.45 / 0.45	0.45 / 0.45			
15	150	0.45 / 0.45	0.45 / 0.45	0.45 / 0.45			
18	180	0.45 / 0.45	0.45 / 0.45	0.45 / 0.45			
22	220	0.45 / 0.45	0.45 / 0.45	0.45 / 0.45			
27	270	0.45 / 0.45	0.45 / 0.45	0.45 / 0.45			
33	330	0.45 / 0.45	0.45 / 0.45	0.45 / 0.45			
39	390	0.45 / 0.45	0.45 / 0.45	0.45 / 0.45			
47	470	0.45 / 0.45	0.45 / 0.45	0.45 / 0.45			
56	560	0.45 / 0.45	0.45 / 0.45	0.45 / 0.45			
68	680	0.45 / 0.45	0.45 / 0.45	0.45 / 0.45			
82	820	0.45 / 0.45	0.45 / 0.45	0.45 / 0.45			
100	101	0.45 / 0.45	0.45 / 0.45	0.45 / 0.45			
120	121	0.45 / 0.45	0.45 / 0.45	0.45 / 0.45			
150	151	0.45 / 0.45	0.45 / 0.45	0.45 / 0.45			
180	181	0.45 / 0.45	0.45 / 0.45	0.45 / 0.45			
220	221	0.45 / 0.45	0.45 / 0.45	0.45 / 0.45			
270	271	0.45 / 0.45	0.45 / 0.45	0.45 / 0.45			
330	331	0.45 / 0.45	0.45 / 0.45	0.45 / 0.45			
390	391	0.45 / 0.45	0.45 / 0.45	0.45 / 0.45			
470	471	0.45 / 0.50	0.45 / 0.45	0.45 / 0.45			
560	561	0.45 / 0.50	0.45 / 0.45	0.45 / 0.45			
680	681	0.45 / 0.60	0.45 / 0.45	0.45 / 0.45			
820	821	0.45 / 0.65	0.45 / 0.45	0.45 / 0.45			
1.0nF	102	0.50	0.45 / 0.45	0.45 / 0.45			
1.2	122	0.60	0.45 / 0.45	0.45 / 0.45			
1.5	152	0.65	0.45 / 0.45	0.45 / 0.45			
1.8	182		0.45 / 0.45	0.45 / 0.45			
2.2	222		0.45 / 0.45	0.45 / 0.45			
2.7	272		0.45 / 0.45	0.45 / 0.45			
3.3	332		0.45 / 0.45	0.45 / 0.45			
3.9	392		0.45 / 0.45	0.45 / 0.45			
4.7	472		0.45 / 0.45	0.45 / 0.45			
5.6	562		0.45 / 0.45	0.45 / 0.45			
6.8	682		0.45 / 0.45	0.45 / 0.45			
8.2	822		0.45 / 0.45	0.45 / 0.45			
10	103		0.45 / 0.45	0.45 / 0.45			
12	123		0.45 / 0.45	0.45 / 0.45			
15	153		0.45 / 0.45	0.45 / 0.45			
18	183		0.45 / 0.45	0.45 / 0.45			
22	223		0.45 / 0.45	0.45 / 0.45			
27	273		0.45 / 0.45	0.45 / 0.45			
33	333		0.45 / 0.45	0.45 / 0.45			
39	393		0.45 / 0.45	0.45 / 0.45			
47	473		0.45 / 0.45	0.45 / 0.45			
56	563		0.45 / 0.45	0.45 / 0.45			
68	683		0.45 / 0.45	0.45 / 0.45			
82	823		0.45 / 0.45	0.45 / 0.45			
100	104		0.45 / 0.45	0.45 / 0.45			
120	124		0.45 / 0.45	0.45 / 0.45			
150	154		0.45 / 0.45	0.45 / 0.45			
180	184		0.45 / 0.45	0.45 / 0.45			
220	224		0.45 / 0.45	0.45 / 0.45			

Application

Available in four maximum thicknesses of 0.45mm, 0.50mm, 0.60mm and 0.65mm. The 0.45mm type is ideal for use in smart cards and sensors, where an extremely low thickness is required.
The 0.65mm capacitors are designed to be surface mounted beneath a plastic leaded chip carrier. This method minimises circuit inductance and allows higher packaging densities to be achieved. They are ideal for decoupling logic circuits and memories up to 1 megabyte.
All types are available with either silver/ palladium or nickel barrier terminations.

25V 50V

Reeled Quantities	178mm (7")	330mm (13")
0805	3000	12000
1206	2500	10000
1210	2000	8000

Ordering Information

0805	J	025	0102	J	C	B
Chip Size	**Termination** J = Nickel Barrier F = Palladium/ Silver	**Voltage** 025 = 25V 050 = 50V	**Capacitance** Expressed in picofarads (pF). First digit is 0. Second and third digits are significant figures of capacitance code. The fourth digit is number of zeros following. eg: 0102=1000pF. For values below 10pF insert a P for the decimal point. eg: 8P20=8.2pF	**Tolerance** IEC Code	**Dielectric** C = C0G X = X7R	**Packaging** B = Bulk T = Taped

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Ultra High Frequency

HIGH Q

Features

- High 'Q' Factor at high frequencies
- High RF power capabilities
- Low ESR
- High self resonant frequencies
- Excellent stability across temperature range
- Small size

Capacitance	Code	0603	0805	1206	1210
0.47pF	0p47	100V	100V	100V	
0.56	0p56				
0.68	0p68				
0.82	0p82				
1.0	1p0				
1.2	1p2				
1.5	1p5				
1.8	1p8				
2.2	2p2				
2.7	2p7				
3.3	3p3				
3.9	3p9				
4.7	4p7				
5.6	5p6				
6.8	6p8				
8.2	8p2				
10	100				100V
12	120				
15	150				
18	180				
22	220				
27	270				
33	330				
39	390				
47	470				
56	560				
68	680				
82	820				
100	101				
120	121				
150	151				
180	181				
220	221				
270	271				
330	331				
390	391				
470	471				
560	561				
680	681				
820	821				
1.0nF	102				

			200V	200V	200V
				500V	500V

High Frequency Measurement and Performance of High 'Q' Multilayer Ceramic Capacitors

Introduction

Capacitors used in high frequency applications are generally used in two particular circuit applications:

- As a DC block providing an AC coupling path between other components.
- As a shunt path to ground for AC voltages thus providing a decoupling path.

At very high frequencies much more capacitor design data is needed by a circuit designer. As well as the normal data relating to Capacitance and Tan δ, 'Q' and E.S.R. are required. If RF/microwave circuit simulation aids are being used, then the designer will require information relating to the 1 Port and 2 Port parameters, the 'S' parameters denoted by S11, S21, S12, S22.
The measurement problem becomes complex because the resultant measurements should properly describe the parameters of the multilayer capacitor but be totally uninfluenced by any test jigs used in the measurement.
The first and extensive part of this measurement sequence involves the calibration (otherwise known as 'de-embedding') of all the test jigs.
The information on Syfer Technology High 'Q' Capacitors contained in this catalogue has been produced utilising a Hewlett Packard Network Analyser - HP8753A, together with the Hewlett Packard 'S' Parameter Test Set - HP 85046A.

Measurement Theory

At frequencies above 30MHz, the measurements from conventional capacitor bridges become invalid because it is not possible to maintain a true four-terminal connection to the capacitor under test, hence phase errors occur and this prohibits the separation of the resistive and reactive components which need to be measured.
In addition the 'open' circuits and 'short' circuits used to calibrate the bridge become degraded. The 'open' circuits become capacitive and the 'short' circuits become inductive, hence measurement accuracy is destroyed.
However, other measurement techniques can be used to solve these problems. These techniques use the behaviour of electric 'waves' travelling along a transmission line, e.g. a co-axial cable or a micro-strip line.
If the transmission line is terminated by an unknown impedance, e.g. the capacitor under test, then a reflected wave is created which is sent back towards the test signal generator and has a magnitude and phase angle dependent on the unknown impedance. We now have two waves, travelling in opposite directions, giving, in effect, the required four terminal connections to the capacitor, provided only that these waves can be separated out and independently measured.
This separation is easily possible using variations on standard Wheatstone Bridge principles. Hence by the measurement of the magnitudes and phases of these travelling waves, which are called Scattering or 'S' waves, the capacitor parameters can be calculated.
It should be noted that since these measurements rely on reflected waves, any changes in physical size, or changes in characteristic impedance between the measurement system and the points to which the capacitor is connected, will create additional and unwanted reflected waves, which will degrade the measurement accuracy.
Accuracy of capacitor placement relative to the calibration plane is also critical. For instance, measurements of a capacitor having a 'Q' of approximately 3000 and thus a Tan δ of 0.00035 will mean the phase loss angle will be of the order of 0.02 or restated -89.98 of phase or further restated, real and imaginary ratios approaching 1:3000. To achieve measurement accuracy, the connections to the capacitor under test should operate to at least one order better than this phase angle value. In jigging or mechanical terms 1.00mm of displacement from the correct or calibration plane, represents 0.1 of phase angle, thus the phase angle errors due to the jigging etc., should be less than 0.02mm (0.0008"). These calculations assume a dielectric constant of 1 and a frequency of 100MHz.

notes

1. For details of ordering see page 37.
2. Additional sizes and values available on request.
3. Available only with Nickel Barrier terminations.

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Measurement Techniques

Three different measurement jig methods have been used:

- The H.P. 16091A co-axial test jig was used to determine:
  - Capacitance
  - Tan δ
  - 'Q'
  - E.S.R.
- To simulate the DC block mode and shunt or decoupling mode, special micro-strip line test jigs were designed and made.

Equipment

The measurement system used comprises a HP 8753A Vector Network Analyser, HP 85046A 'S' parameter test set and HP 16091A test jig together with the relevant specialist cables, connectors and micro-strip line test jigs.

Notes

a) The swept frequency range over which all measurements were taken was 1MHz to 3GHz with measurements at 10MHz increments below 1GHz, increments of 50MHz above 1GHz.
b) For the very low capacitance values, the lowest frequencies at which sensible data was obtained appeared to be greater than 50MHz, the data is thus presented.
c) The curves showing the resonant points for the capacitors have been left in as a guide to these points of resonance. However, due to the rapid changes in all aspects of the capacitors' parameters near to the resonant point, such measurements should be treated with caution. Above resonance the capacitance curves are dominated by the self-inductance of the capacitor.
d) For specific design work it may be possible to provide full 'S' Parameter data. If this is required please contact our Sales Office.

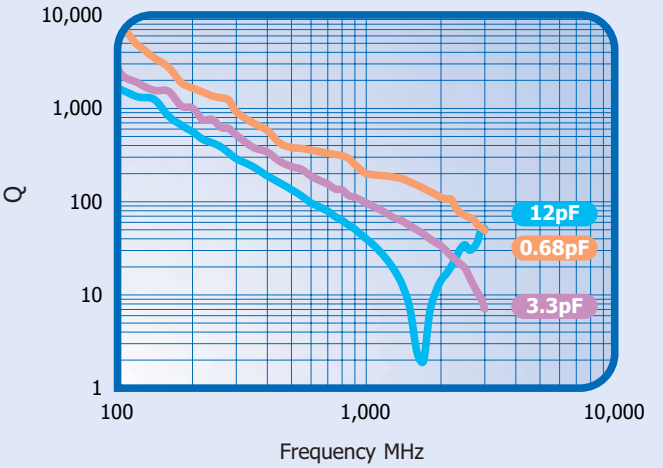




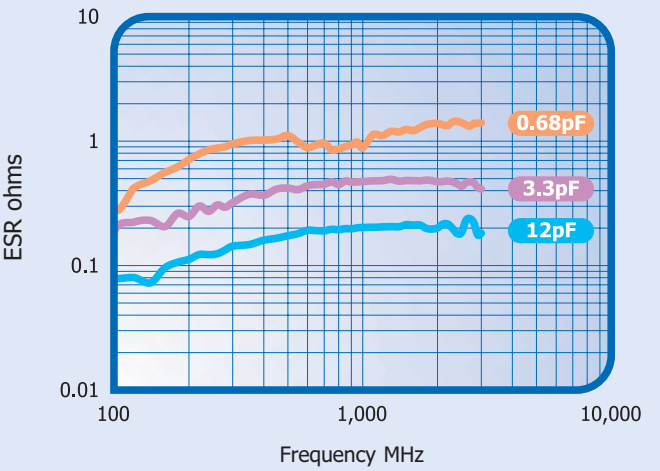


All values - 0603 chip size

Q



ESR



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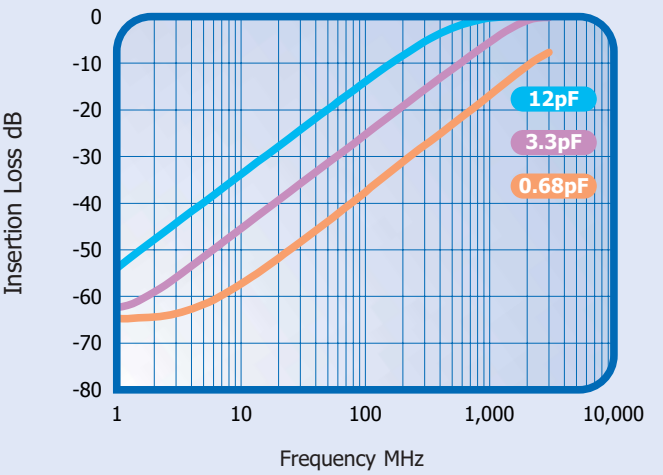

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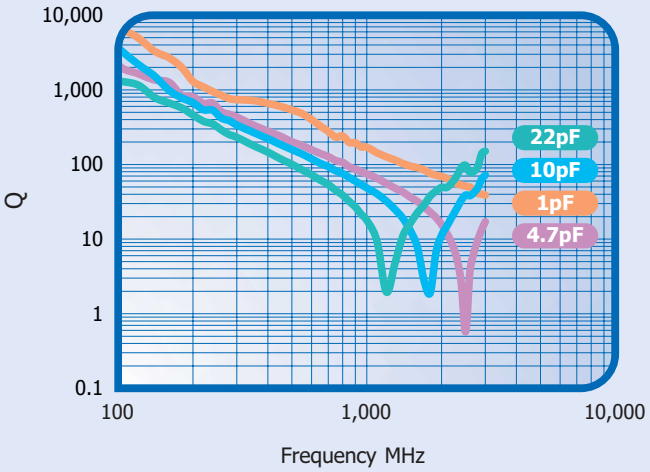
Ultra High Frequency

HIGH Q

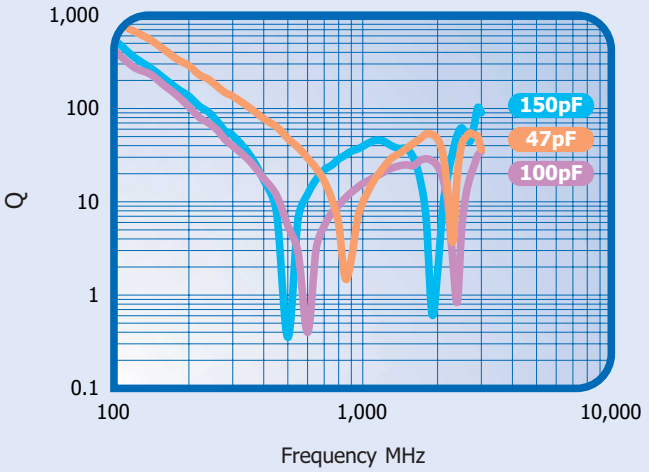
Low values - 0805 chip size

Q



High values - 0805 chip size

Q



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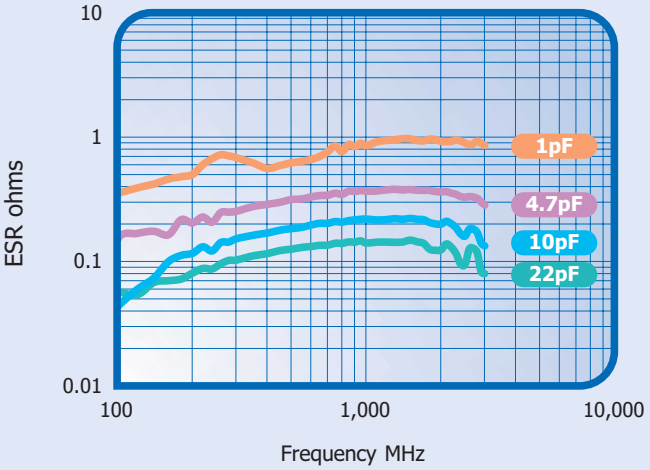
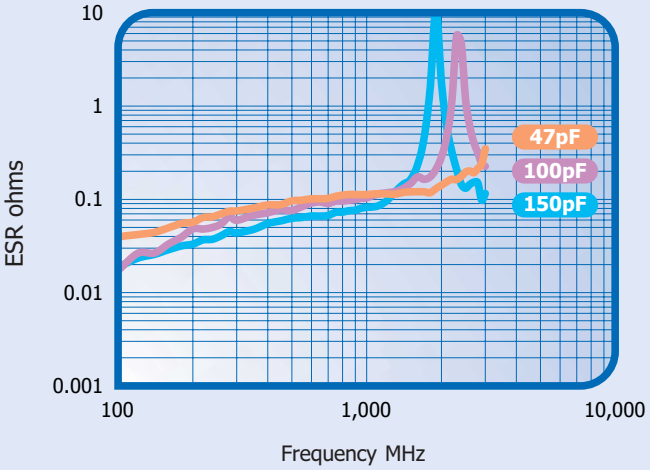


ESR



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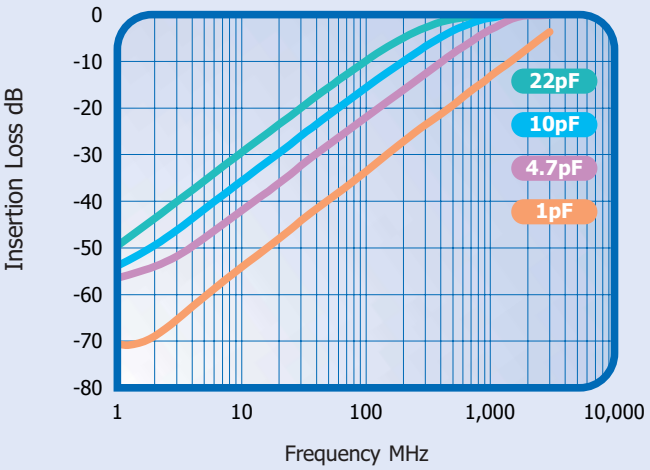

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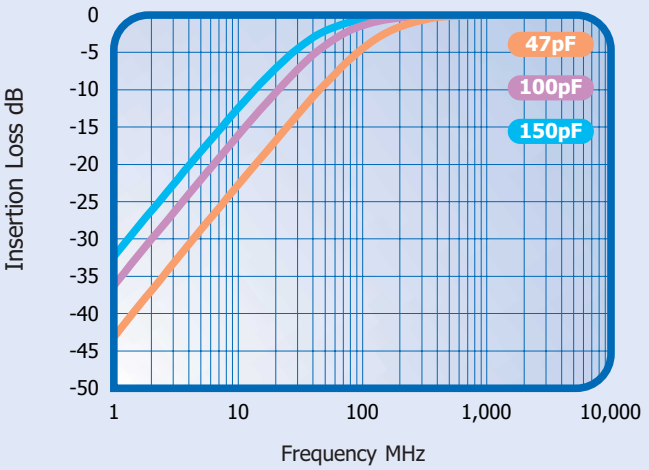

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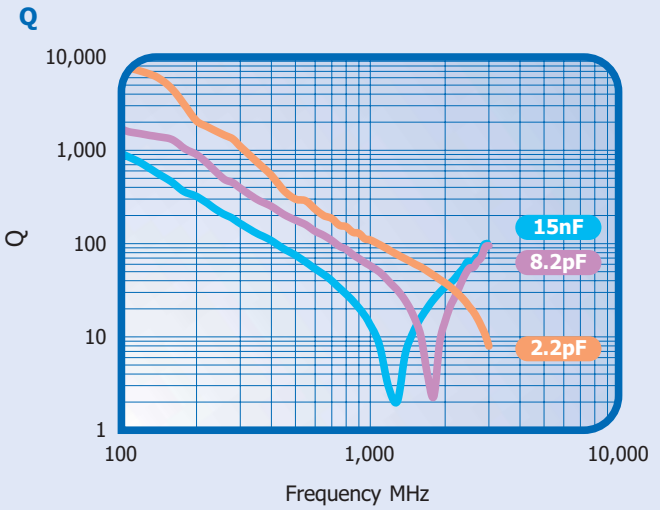
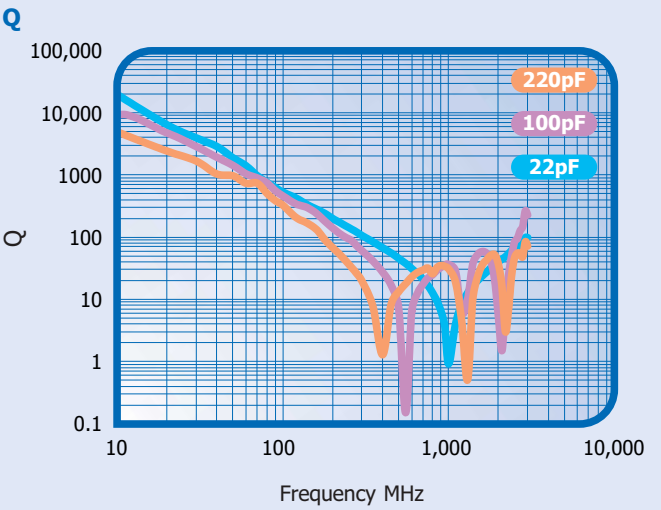
HIGH Q

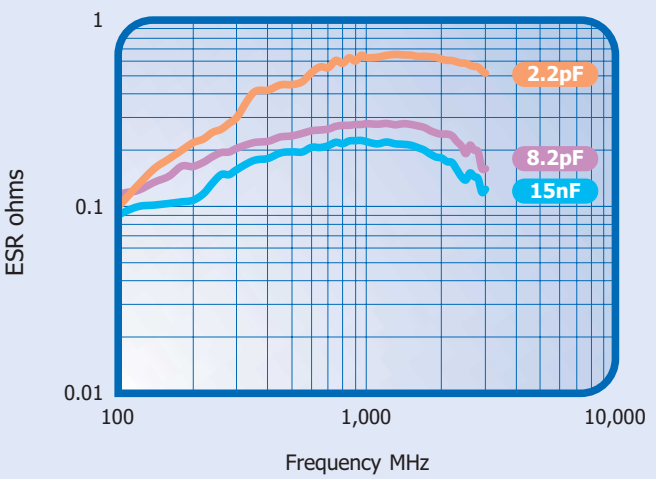
Low values - 1206 chip size



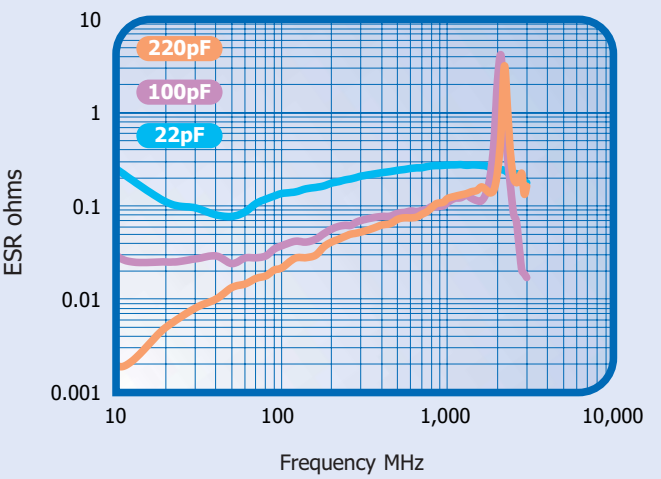
High values - 1206 chip size



ESR



ESR



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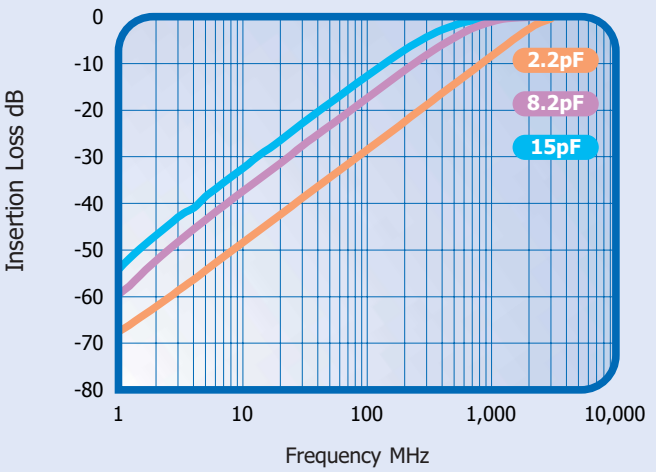

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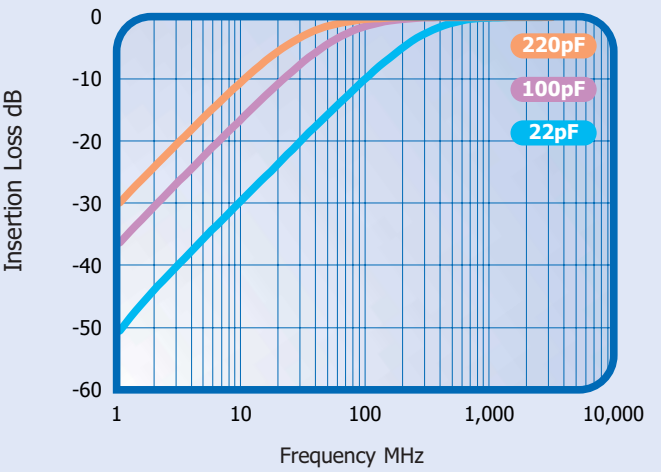

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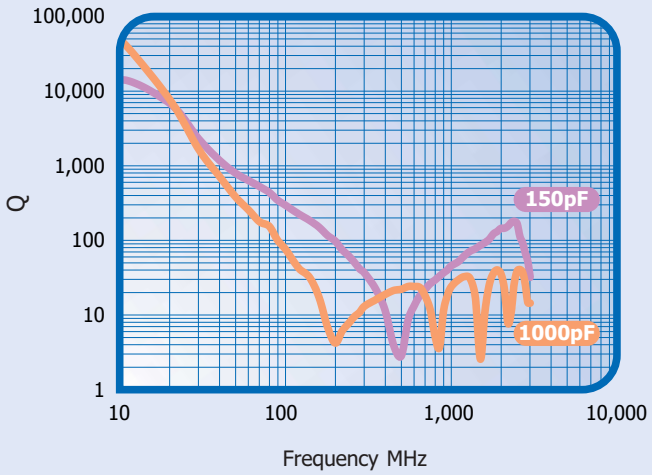
HIGH Q

All values - 1210 chip size

Q



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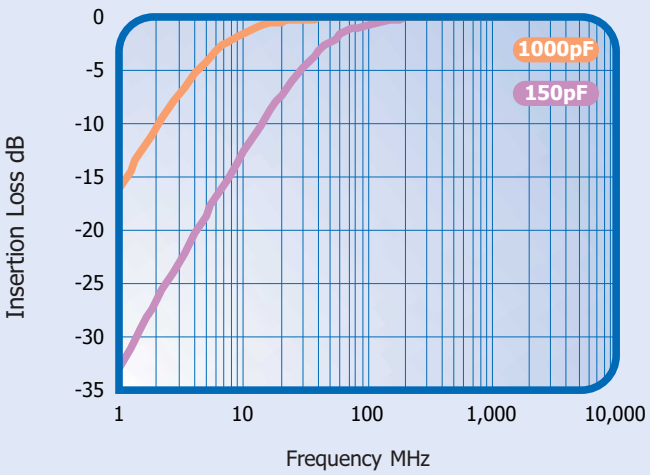
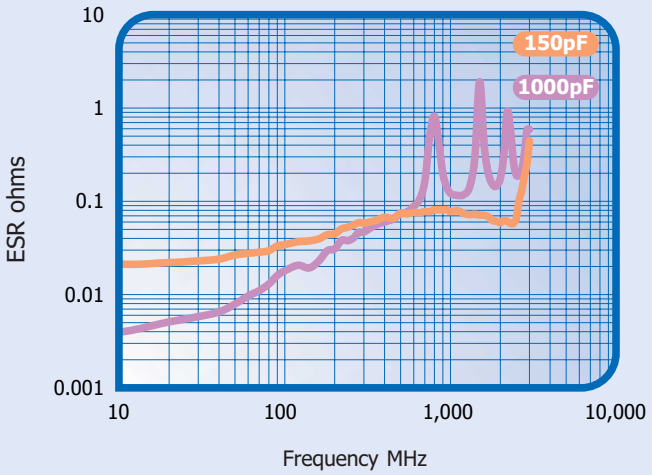


ESR



General Technical Specifications

Syfer Reference	Q = High Q Ceramic
Capacitance Range	0.47pF to 1nF
Operating Temperature Range	-55°C to +125°C
Voltage Rating	100V, 200V, 500V
Environmental Classification	55/125/56
Typical Capacitance change over Temperature Range	0 ±30ppm/°C
Measuring Frequency for measurement of Capacitance and Dissipation Factor	1MHz
Measuring Voltage	1Vrms
Test Voltage	2.5 x nominal voltage/5secs

Reeled Quantities	0805	1206	1210
178mm (7")	3000	2500	2000
330mm (13")	12000	10000	8000

Ordering Information

0805	J	100	0101	K	Q	T
Chip Size	**Termination** J = Nickel Barrier	**Voltage** 100 = 100V 200 = 200V 500 = 500V	**Capacitance** Expressed in picofarads (pF). First digit is 0. Second and third digits are significant figures of capacitance code. The fourth digit is number of zeros following. Example: 0101=100pF. For values below 10pF insert a P for the decimal point. eg: 8P20=8.2pF	**Tolerance** <10pF B= ±0.1pF C=±0.25pF D=±0.5pF ≥10pF F=±1% G=±2% J=±5% K=±10%	**Dielectric** Q = High Q Ceramic	**Packaging** T=178mm (7") reel B=Bulk

SYFER TECHNOLOGY LIMITED
A DOVER Company

Stacked Chip Capacitors

C0G/X7R

Introduction

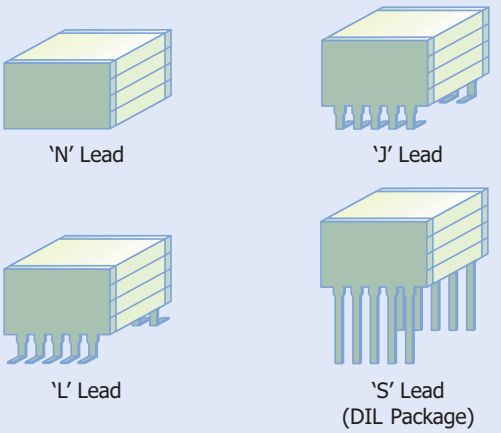
These ranges of both High Capacitance and High Voltage Multilayer ceramic capacitor assemblies are designed for use in high frequency switched mode power supplies, DC-DC converters and similar applications.
Low ESR and low ESL are inherent in the design giving the assemblies a high current capability up to 1MHz and offer far superior performance than either aluminium or tantalum electrolytic capacitors.Various lead options are available, making them suitable for mounting on ceramic substrate or epoxy printed circuit boards.

Summary of Standard Range

Chip sizes covered	1812; 2220; 2225; 3640; 5550; 8060.
Working Voltages	50V to 2kV as standard.
Capacitance Range	39pF to 1.8µF in Ultra Stable COG Dielectric 820pF to 68µF in Stable X7R Dielectric.

Special chip sizes, working voltages, capacitance values and specific custom requirements will be considered. Please refer all enquiries to the Sales Office.

Available Lead Options



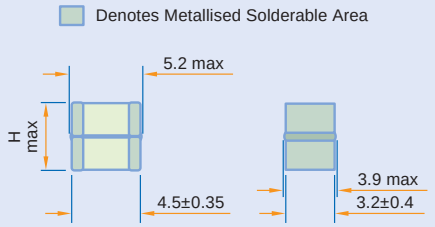
'N' Lead | 'J' Lead | 'L' Lead | 'S' Lead (DIL Package)

Note: 1. Not all lead options are available with all chip sizes. Check specific assembly drawings for available options.

Available Options and Dimensions (mm)

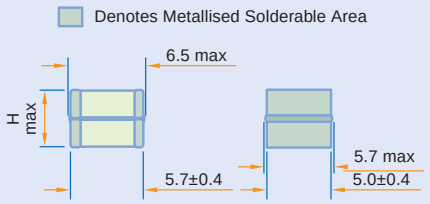
Chip Size 1812

Unleaded assembly only ('N' lead option)

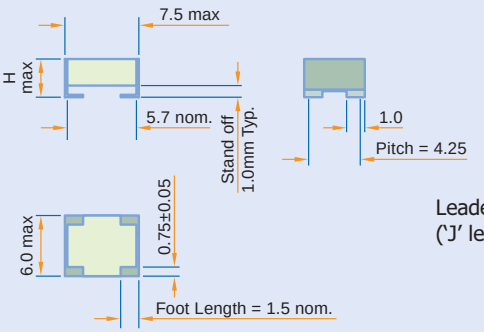


Chip Size 2220

'J' & 'L' Leaded or Unleaded ('N') assemblies



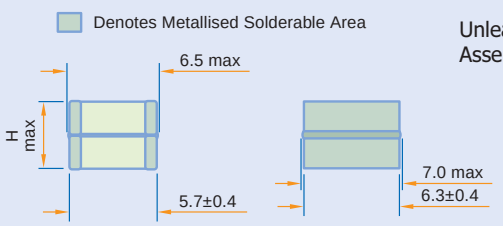
Unleaded Assembly



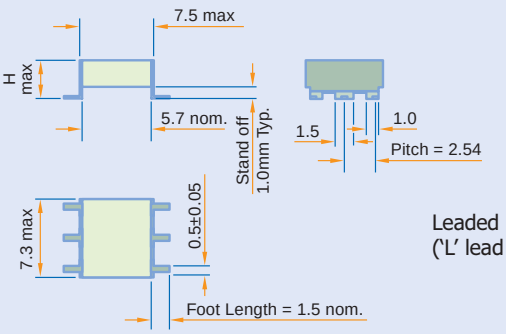
Leaded Assembly ('J' lead shown.)

Chip Size 2225

'J' & 'L' Leaded or Unleaded ('N') assemblies



Unleaded Assembly



Leaded Assembly ('L' lead shown.)

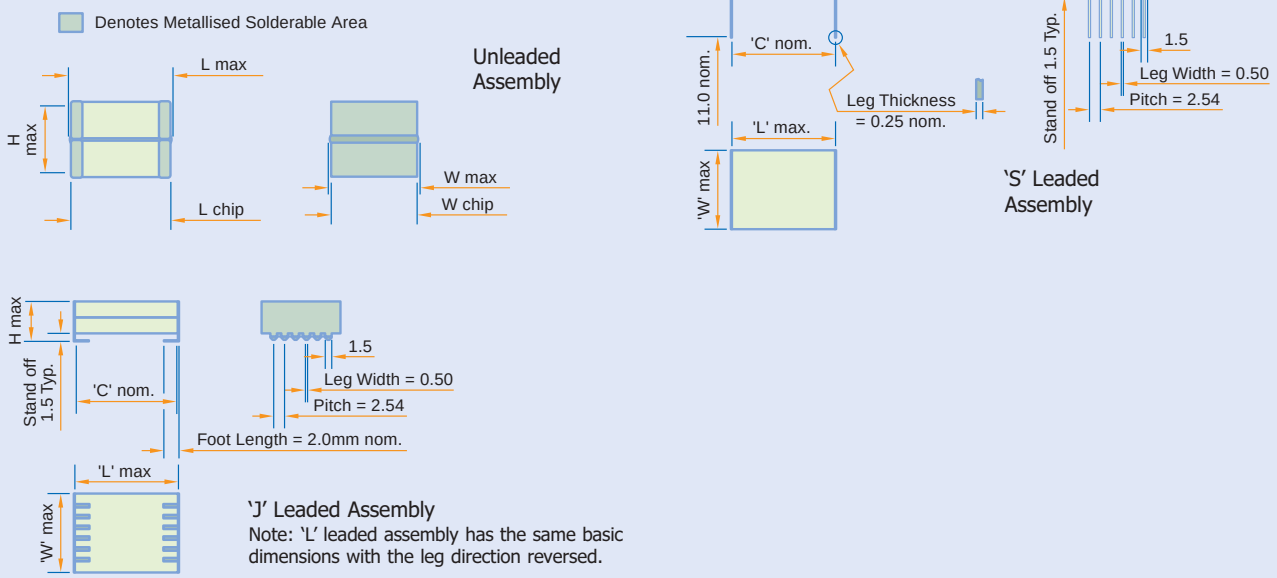
Stacked Chip Capacitors

COG/X7R

Available Options and Dimensions (mm)

Chip Size 3640, 5550, 8060

'J', 'L' & 'S' Leaded or Unleaded ('N') assemblies



'J' Leaded Assembly

Note: 'L' leaded assembly has the same basic dimensions with the leg direction reversed.

Dimensions (mm)

Leaded assembly dimensions

	3640	5550	8060
W max	11.5	14.0	16.5
C nom	9.2	14.0	20.3
L max	11.7	16.5	22.8
No. of leads per side	4	5	6

Un-leaded assembly dimensions

	3640	5550	8060
L max	10.7	15.5	21.8
L chip	9.2	14.0	20.3
W max	11.2	13.7	16.2
W chip	10.16	12.7	15.24

Max Stack Height (H)

No. of Chips	Range (size)	Unleaded Assemblies	'J' & 'L' leaded Assemblies	'S' leaded Assemblies
1	≤ 2225	N/A	4.5	N/A
	≥ 3640	N/A	5.5	3.25
2	≤ 2225	5.25	7.0	N/A
	≥ 3640	6.75	8.75	6.75
3	≤ 2225	7.75	9.5	N/A
	≥ 3640	10.0	12.0	10.0
4	≤ 2225	10.25	12.0	N/A
	≥ 3640	13.25	15.25	13.25
5	≤ 2225	12.75	14.5	N/A
	≥ 3640	16.5	18.5	16.5

SYFER TECHNOLOGY LIMITED

Stacked Chip Capacitors

COG

Capacitance	Code	1812 ('N' Lead only)						2220 ('N', 'J' & 'L' Lead)						2225 ('N', 'J' & 'L' Lead)					
Rated Voltage d.c.		50	100	200	500	1K	2K	50	100	200	500	1K	2K	50	100	200	500	1K	2K
39pF	390						1						1						1
47	470						1						1						1
56	560						1						1						1
68	680						1						1						1
82	820						1						1						1
100	101						1						1						1
120	121						1						1						1
150	151						1						1						1
180	181						1						1						1
220	221						1						1						1
270	271						1						1						1
330	331						1						1						1
390	391						1						1						1
470	471						1						1						1
560	561						1						1						1
680	681						1						1						1
820	821					1	2						1						1
1.0nF	102					1	2						1						1
1.2	122					1	2						1						1
1.5	152					1	3						1						1
1.8	182					1	3					1	2						1
2.2	222					1	3					1	2						1
2.7	272					1	4					1	2					1	2
3.3	332			1	1	2	5					1	2					1	2
3.9	392			1	1	2	5					1	3					1	2
4.7	472			1	1	2						1	3					1	3
5.6	562			1	1	3						1	4					1	3
6.8	682			1	1	3				1	1	2	4					1	4
8.2	822			2	2	3				1	1	2	5					1	4
10	103		1	2	2	4				1	1	2					1	2	5
12	123		1	2	2	5				1	1	2					1	2	
15	153		1	3	3					1	1	3					1	2	
18	183		1	3	3				1	2	2	3					1	3	
22	223	1	2	3	4				1	2	2	4				1	2	3	
27	273	1	2	4	4				1	2	2	5			1	2	2	4	
33	333	2	2	5	5				1	3	3				1	2	2	4	
39	393	2	2	5					1	3	3				1	2	2	5	
47	473	2	3					1	2	3	3				1	3	3		
56	563	2	3					1	2	4	4				1	3	3		
68	683	3	4					2	2	5	5			1	2	4	4		
82	823	3	4					2	2	5				1	2	4	4		
100	104	4	5					2	3					2	2	5	5		
120	124	4						3	3					2	2				
150	154	5						3	4					2	3				
180	184							4	5					3	3				
220	224							4						3	4				
270	274							5						4	5				
330	334													4					
390	394													5					
470	474																		
560	564																		
680	684																		
820	824																		
1.0µF	105																		
1.2	125																		
1.5	155																		
1.8	185																		

COG

notes

1. For details of ordering see page 44.
2. The table above indicates the number of chips required to achieve the capacitance value.
3. Higher voltages (To 5kV max) may be available on request

Stacked Chip Capacitors

COG

Capacitance	Code	3640 ('J', 'L' & 'S' Lead)						5550 ('J', 'L' & 'S' Lead)						8060 ('J', 'L' & 'S' Lead)					
Rated Voltage d.c.		50	100	200	500	1K	2K	50	100	200	500	1K	2K	50	100	200	500	1K	2K
39pF	390																		
47	470																		
56	560																		
68	680																		
82	820																		
100	101						11111111111111												
120	121																		
150	151																		
180	181																		
220	221																		
270	271																		
330	331																		
390	391																		
470	471																		
560	561																		
680	681																		
820	821																		
1.0nF	102						1122233445						111111111122233455						1111111111122233445
1.2	122																		
1.5	152																		
1.8	182																		
2.2	222																		
2.7	272																		
3.3	332																		
3.9	392																		
4.7	472																		
5.6	562																		
6.8	682					1111122233455													
8.2	822																		
10	103																		
12	123																		
15	153																		
18	183																		
22	223				1122233445													1111122233445	
27	273																		
33	333																		
39	393			1122233445													1122233445		
47	473																		
56	563																		
68	683		1122223345 5								1122233455					1122233455			
82	823																		
100	104																		
120	124	1122233445							1122223455						1122223455				
150	154																		
180	184																		
220	224																		
270	274																		
330	334																		
390	394																		
470	474																		
560	564																		
680	684																		
820	824																		
1.0µF	105																		
1.2	125																		
1.5	155																		
1.8	185																		

notes

1. For details of ordering see page 44.
2. The table above indicates the number of chips required to achieve the capacitance value.
3. Higher voltages (To 5kV max) may be available on request

SYFER TECHNOLOGY LIMITED
A DOVER Company

Stacked Chip Capacitors

X7R

Capacitance	Code	1812 ('N' Lead only)						2220 ('N', 'J' & 'L' Lead)						2225 ('N', 'J' & 'L' Lead)					
Rated Voltage d.c.		50	100	200	500	1K	2K	50	100	200	500	1K	2K	50	100	200	500	1K	2K
820pF	821						11111111111111122233445						1111111111111222334455						1111111111111222334455
1.0nF	102																		
1.2	122																		
1.5	152																		
1.8	182																		
2.2	222																		
2.7	272																		
3.3	332																		
3.9	392																		
4.7	472																		
5.6	562						1111111111122233445						1111111111122233445						1111111111122233445
6.8	682																		
8.2	822																		
10	103																		
12	123																		
15	153																		
18	183																		
22	223																		
27	273				1111111111122233445														
33	333																		
39	393																		
47	473																		
56	563												1111111111122233445						
68	683																		
82	823																		
100	104																		
120	124																		
150	154			1111111122233445															
180	184																		
220	224																		
270	274																		
330	334																		
390	394																		
470	474		1111222334455																
560	564																		
680	684																		
820	824	1111222334455																	
1.0µF	105																		
1.2	125																		
1.5	155																		
1.8	185																		
2.2	225																		
2.7	275																		
3.3	335																		
3.9	395																		
4.7	475																		
5.6	565																		
6.8	685																		
8.2	825																		
10	106																		
12	126																		
15	156																		
18	186																		
22	226																		
27	276																		
33	336																		
39	396																		
47	476																		
56	566																		
68	686																		

notes

1. For details of ordering see page 44.
2. The table above indicates the number of chips required to achieve the capacitance value.
3. Higher voltages (To 5kV max) may be available on request

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Stacked Chip Capacitors

X7R

Capacitance	Code	3640 ('J', 'L' & 'S' Lead)						5550 ('J', 'L' & 'S' Lead)						8060 ('J', 'L' & 'S' Lead)					
Rated Voltage d.c.		50	100	200	500	1K	2K	50	100	200	500	1K	2K	50	100	200	500	1K	2K
820pF	821																		
1.0nF	102																		
1.2	122																		
1.5	152																		
1.8	182																		
2.2	222																		
2.7	272																		
3.3	332																		
3.9	392																		
4.7	472																		
5.6	562																		
6.8	682						11111111112223345												
8.2	822																		
10	103																		
12	123												11111111112223345						
15	153																		
18	183																		
22	223																		11111111112223345
27	273																		
33	333																		
39	393																		
47	473					11111111112223345													
56	563																		
68	683																		
82	823																		
100	104												11111111112223345						
120	124																		
150	154																		
180	184				11111111112223345														
220	224																		
270	274																		
330	334																		
390	394																		
470	474																		
560	564																		
680	684																		
820	824			1112223345															
1.0µF	105																		
1.2	125																		
1.5	155		1122233455																
1.8	185																		
2.2	225																		
2.7	275	1112223455																	
3.3	335																		
3.9	395																		
4.7	475																		
5.6	565																		
6.8	685																		
8.2	825																		
10	106																		
12	126																		
15	156																		
18	186																		
22	226																		
27	276																		
33	336																		
39	396																		
47	476																		
56	566																		
68	686																		

notes

1. For details of ordering see page 44.
2. The table above indicates the number of chips required to achieve the capacitance value.
3. Higher voltages (To 5kV max) may be available on request

SYFER TECHNOLOGY LIMITED
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Stacked Chip Capacitors

C0G/X7R

Ordering Information

8060	B	500	0126	K	X	B	J	W00	5
Chip Size	**Finish** B = Bare Chip Assembly V = Lacquer Coated	**Voltage** 050 = 50V 100 = 100V 200 = 200V 500 = 500V 1K0 = 1000V 2K0 = 2000V	**Capacitance** Expressed in picofarads (pF). First digit is 0. Second and third digits are significant figures of capacitance code. The fourth digit is number of zeros following. eg: 0126=12µF.	**Tolerance** M = ±20% Standard K = ±10% Optional	**Dielectric** C = C0G X = X7R	**Packaging** R = 330mm (13") reel B = Bulk	**Mounting Style** N = Bare Chip SM Assembly J = J leaded SM Assembly L = L leaded SM Assembly S = Straight leaded DIL Assembly	**Customer Special Requirements**	**No. of Chips**

Notes

1. Other capacitance tolerances may also be available.
2. Lacquer coating is optional on chip sizes ≥ 3640. See design notes below.
3. Tape and reel packing is available on 2220 & 2225 single chip 'J' and 'L' leaded products and 1812, 2220, 2225 2-stack unleaded ('N' leaded) products. All other products will be supplied bulk packed in protective foam. Special waffle packing requirements can be considered.
4. Higher working voltages and alternative chip sizes are also available by special request.

Materials

In all cases, leadframes, where fitted, will be silver plated phospher bronze.

Chip to chip attachment, and chip to leadframe attachment will be by either high melting point solder (M.Pt. 300ºC typ.) or high conductivity silver loaded epoxy adhesive depending on product.

Lacquer coating, where specified, is a mineral filled modified silicone.

Design Notes

When specifying these components, consideration must be given to their physical size, aspect ratio and mass with particular reference to thermal mismatch, mechanical shock and vibration characteristics.

It is not recommended that chip sizes greater than 3640 are mounted directly to the board, but are lifted clear using stand off leads ('J' or 'L') to prevent mechanical cracking.

Where possible, using a larger size chip with less chips in the stack will result in a more stable product when placed on the board, as the result of an improved aspect ratio.

A general handling recommendations sheet covering these, and other points, is available upon request from our Sales Office.

Lacquer coating is available as an option to improve the flash over resistance of high voltage packages. Refer to ordering details (above) to specify this option.

A data sheet covering recommended pad designs is available on request from our Sales Office.

Please refer all specific enquiries to the Sales Office.

Capacitor Arrays

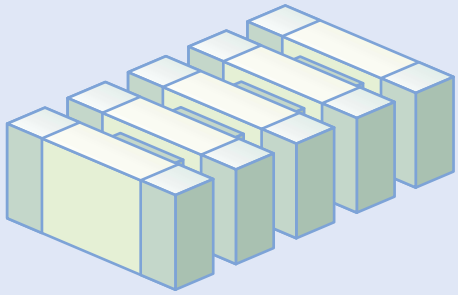
C0G/X7R

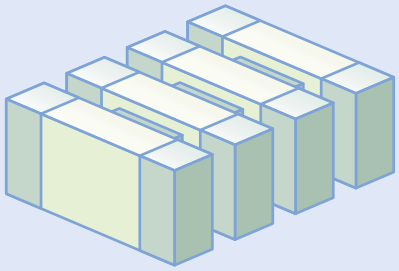
The Cap-Rack (US Patent 6,058,004) is an assembly of individual chip capacitors, bonded with high temperature epoxy. This construction permits the assembly of dissimilar capacitance values or dielectrics into one single component, providing extended freedom for board space utilization. The design reduces harmful thermal stress during assembly, behaving as individual components, not as a single large ceramic mass. The Cap-Rack also reduces "cross talk" to insignificant levels by elimination of capacitance coupling between adjacent capacitors. Cap-Racks are available as groupings of chip sizes 0603, 0805, 1206, 1210, 1808 and 1812, from pairs to as many as eight chips. See separate data sheets for capacitance ranges of the various sizes. Custom sizes, particularly for high voltage applications, are also available. Footprint dimensions can vary to optimize board space usage.

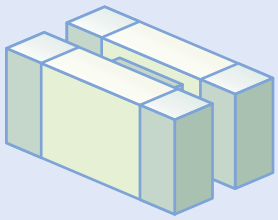
This is an application specific product that may be designed to meet your technical requirements in partnership with Syfer Technology engineers.

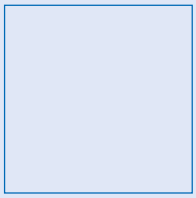
Please contact our Sales office for further assistance.

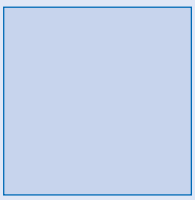
Typical Construction











SYFER TECHNOLOGY LIMITED
A DOVER Company

Planar Array Capability

Introduction

Syfer Technology Limited has been manufacturing and supplying Planar Capacitor Arrays since 1990. The multilayer Planar Array is an application specific component designed for use in multi-line EMI filter circuits, typically found in filtered connectors. Planar Array technology affords the user weight and volumetric efficiency as well as performance and reliability advantages compared to other capacitor technologies.
Syfer's position as the world's leading supplier has been achieved through utilisation of the advantages inherent in our "Wet-Stack" process. A stress-free component is produced with mechanical precision, enabling a filter assembly to withstand the most rigorous of electrical specifications.

Capability

The Planar Array is a unitary block of ceramic containing capacitors or a combination of capacitors, feedthrus and ground lines. Our current capability extends from a simple 2 hole unit to a complex 155-way device. Individual line connection is made to each capacitor through a terminated hole, whilst the ground connection is made at the device perimeter. Very low impedances are encountered as signals are presented with multi-directional paths to ground.

Mechanical

Working with customers in the EMC field has enabled Syfer to develop a comprehensive range of planforms. These include the following:-

- Circular (MIL-C-38999 and similar)
- ARINC 404 and 600
- "D" SUB (Rectangular and Trapezoidal)
- High Density "D" SUB
- Micro-D (MIL - C - 83513)
- Nano-D

Special custom shapes are also available. Component thicknesses are produced from a minimum of 1.40 mm (0.055 inches) to a maximum 3.18mm (0.125 inches).

Electrical

The holes within the planar array are required to perform differing electrical functions. This could embrace the following:-

- Multiple capacitance values (to a wide ratio)
- Hole to hole insertion loss specification
- Hole grounding to a specified maximum resistance
- Functionless holes (Feedthru's)

Maximum capacitance values obtainable are determined by a number of parameters. These include :-

- Dielectric material (C0G & X7R)
- Product dimensions
- Voltage ratings

Typical capacitance ranges for C0G and X7R dielectric are 47pF to 4nF and 250pF to 600nF respectively.

Product dimensions. Hole pitch, hole diameter and product thickness are the major mechanical influences on maximum capacitance value. Preferred dimensions for standard layouts are available on request.

Voltage rating. The more common voltage ratings are 100, 200 and 300 volts DC but parts are available to a dielectric withstand voltage (DWV) capability of 3,000 volts DC. Transient voltage capability may be specified.

Quality Assurance

Syfer's Planar Array manufacture is an integral part of its overall facility for the high-volume fabrication of Multilayer Ceramic Capacitors. It is afforded the benefit of sophisticated and highly automated material, manufacturing, test and quality assurance procedures commensurate with Syfer's ISO9001 approval and its reputation as a leading supplier in this field.
Statistical Process Control techniques are employed throughout and all Planar lots built are subject to both external visual inspection and internal examination by micro-section.
Our final test facility is fully automated. All parts are 100% tested for the following parameters:-

- Capacitance value
- Dissipation factor
- Insulation resistance
- Dielectric withstand voltage up to 1500V DC

General Information

Termination Material

Periphery. Two termination materials are offered as standard. These are either gold plating over nickel or silver-palladium, both of which are suitable for use with a ground spring connection. For applications where a solder joint is required, silver-platinum may be substituted. Generally, Planar Arrays are large devices and direct attachment to connector shell or printed circuit board is not recommended as a result of mismatch between coefficients of thermal expansion.

Holes. Gold over nickel or a silver-platinum material is used for both the hole termination and the surrounding pads. These materials offer good solder wetting and a high level of resistance to solder leaching.

High Voltage Parts

Syfer's maximum 100% DWV test capability is 1,500 Volts DC. Lots requiring DWV specification at higher voltages are subject to A.Q.L. testing at the specified DWV level after being fully tested at 1,500V DC. A similar A.Q.L. test is conducted on the dielectric breakdown voltage of the lot.
All parts requiring a DWV test at voltages above 750 V DC are lacquer coated to prevent surface flashover under conditions of high humidity.

Orientation

Identifying notches are provided in the device periphery to facilitate recognition of orientation during manufacture and use. Rectangular planforms have a single notch close to the hole (pin) 1 position. Circular planforms have a notch as near to the 12 o'clock position as the layout permits. For multi-function circular planforms, normally, an additional pair of notches is provided in the right hand quadrant of the pin engaging face.

Compliant spring clips

An option for the planar arrays is to supply them with compliant spring clips. The clips are soldered to each hole in the array, allowing the user to push the connector contact through the clip without soldering.
This enables a quicker assembly procedure and an improved yield, both factors contributing to a reduction in overall cost of assembly. An additional benefit is that any movement or stress on the contact does not transfer stress to the ceramic array. Four sizes of clip are available

Planar Arrays

Planar Array Outlines

The following outlines represent a small selection from Syfer's Planar Array manufacturing capability.

Rectangular Planar Arrays

Syfer's manufacturing capability allows the production of a wide range of outlines from 150 hole DOD-STD 1842 down to the 9 way microminiature NANO style.
Multi-capacitance values, grounded holes and feedthroughs can be accommodated in most outlines.

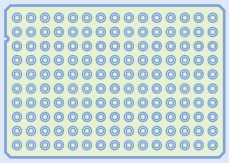
50 WAY 'D' MIL STD 18277

37 WAY 'D' MIL STD 18276

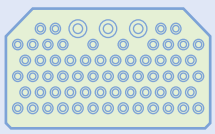
9 WAY 'D' MIL STD 18273

25 WAY SUB MINIATURE MIL STD 83513

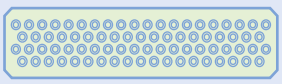
150 WAY DOD STD 1842



67 WAY MS 3157



78 WAY HIGH DENSITY MIL STD 18277

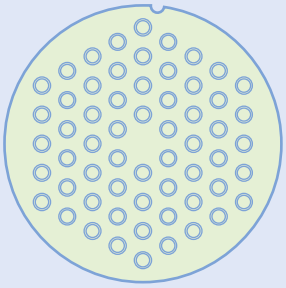


9 WAY NANO

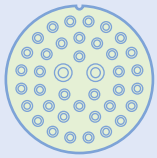
Circular Planar Arrays

Various MIL-STD designs can be supplied with diameters ranging from 8.1 mm (0.32 ins) to 50.8 mm (2.0 ins). The Planar Arrays can contain multi - capacitance values, grounded holes and feedthroughs.

40-62 MIL STD 1651



20-39 MIL STD 1669



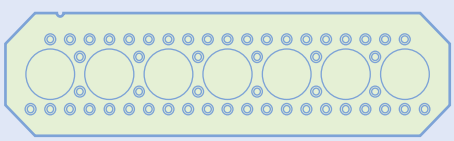
14-35 MIL STD 1560A

8-35 MIL STD 1560A

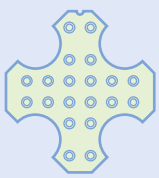
Special Designs

Syfer is always pleased to consider the manufacture of custom arrays, two examples of which are shown below. We will be pleased to offer design guidance to engineers if required.

59 WAY SPECIAL



20T4 DOD STD 1842 (SPECIAL)



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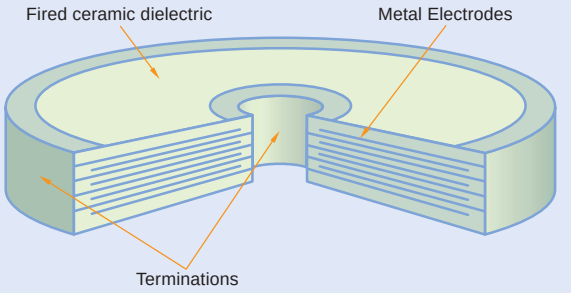
Discoidal Chip Capacitors

C0G/X7R

Introduction/Technical Summary

The Discoidal Chip Multilayer Ceramic Capacitor is the natural complement to the single plate and tube ceramic capacitors which are the key elements of many EMI filters. The single layer designs are limited in capacitance values available, whilst the Multilayer Discoidal Chip process has increased the range to 4.7uF.
Discoidal Chip Multilayer Ceramic Capacitors are of a configuration suitable for direct mounting into filters, onto bulkheads and hybrid circuits. Due to their geometry, they have excellent RF performance characteristics as well as very high Self Resonant Frequencies. They are offered with a choice of C0G or X7R ceramic.



General Specification

Sizes:
From 2.5mm to 25mm outside diameter

Dielectrics:
C0G, X7R

Capacitance Range:
10pF to 4.7µF

Capacitance Tolerance:
±2%, ±5%, ±10%, ±20%, -20%+80%, -0%+100%

Voltage:
50V to 3kV

Operating Temperature Range:
C0G/X7R, -55°C to +125°C

Termination Options:
Silver-Palladium, Silver-Platinum, Gold over Nickel

The above parameters are indicative, please contact our Sales Office with your specific enquiry.

For a product to meet your individual requirement please specify:

Capacitance
Test conditions as listed under 'Quality Requirements' page 8.

Tolerance
Test conditions as listed under 'Quality Requirements' page 8.

DC Voltage

Temperature range

Dielectric

Dimensions

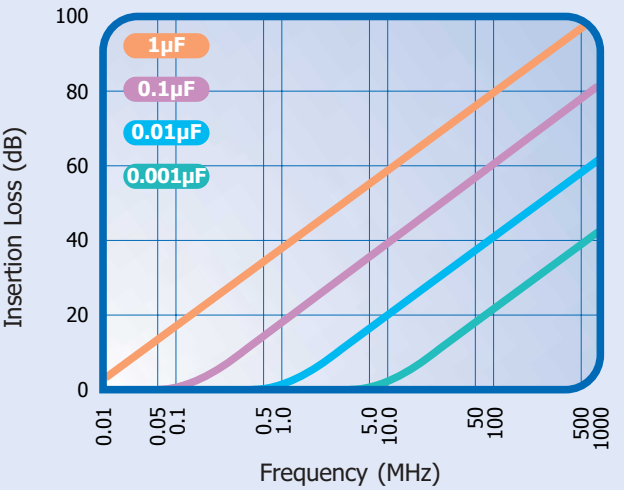
Outside Diameter	MIN	MAX
Inside Diameter	MIN	MAX
Thickness		MAX

Application Notes

Discoidal Chip Multilayer Ceramic Capacitors are manufactured using the same material as the SMT Chips, they therefore have the same general characteristics as already listed in this catalogue. Handling, transportation, storage, cleaning and recommended soldering process apply equally to both Surface Mount Rectangular and Discoidal Chips.

Insertion Loss

At a given frequency, the insertion loss of a filter connected into a given transmission system is defined as the ratio of voltages appearing across the line immediately beyond the point of insertion, before and after insertion of the filter under test.
The discoidal chip MLC capacitors are capable of providing almost theoretical insertion loss performance when installed in metal cases or onto a metal chassis.



Theoretical Insertion Loss of Ideal Capacitors

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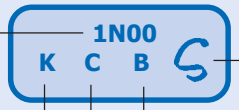
Marking and Ordering information

Marking information

All encapsulated capacitors are marked with:- Capacitance value, tolerance, rated d.c. voltage, dielectric, and where size permits Syfer logo. All moulded units are marked additionally with year and week of manufacture, and capacitance value on top of the unit.

Example: 1000pF ±10% 50V 2X1 dielectric



Capacitance:

Code	Capacitance
3P00	3pF
10P0	10pF
100P	100pF
1N00	1000pF
10N0	10nF
1U00	1µF

Tolerance:

Code	Tolerance
C	±0.25pF
D	±0.5pF
F	±1.0pF or ±1%
G	±2%
J	±5%
K	±10%
M	±20%

Dielectric code

Dielectric		Classes		
Class	**Code**	**CECC**	**EIA**	**MIL**
Ultra stable	C	1B/CG	COG(NPO)	CG/(BP)
Stable	X	2R1	X7R	
To special order				
Stable	B	2X1		BX
Stable	R	2C1		BZ

Rated voltage d.c.

Code	Voltage
C	50
D	63
E	100
F	200
Q	500
Z	1KV
M	2KV
P	3KV
S	4KV
U	5KV

Ordering information for Radial Lead Capacitors

Example: ..... 8111M 100 0102 J C □□□

Type No/Size ref

Voltage d.c.

050 = 50 Volts	1K0 = 1KV
063 = 63 Volts	2K0 = 2KV
100 = 100 Volts	3K0 = 3KV
200 = 200 Volts	4K0 = 4KV
500 = 500 Volts	5K0 = 5KV

Capacitance (pF)

- First digit - 0
- Second digit - First significant figure of capacitance value
- Third digit - Second significant figure of capacitance value
- Fourth digit - Number of zeros following. eg. 0102 = 1000pF. For values below 10pF insert a P for the decimal point. eg. 8P20 = 8.2pF

Suffix code. The remaining alpha/numeric digits are used to denote variation from the standard products of customer special requirements (electrical, packing, mechanical, environmental, coding etc.)

Dielectric code

Dielectric		Classes		
Class	**Code**	**CECC**	**EIA**	**MIL**
Ultra stable	C	1B/CG	COG(NPO)	CG/(BP)
Stable	X	2R1	X7R	
To special order				
Stable	B	2X1		BX
Stable	R	2C1		BZ

Capacitance tolerance code

Ultra stable class			Stable class	
Cr < 10pF	± 0.25 pF	C	± 5%	J
	± 0.5 pF	D	± 10%	K
Cr ≥ 10pF	± 1%	F	± 20%	M
	± 2%	G		
	± 5%	J		
	± 10%	K		

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Dipped and Moulded

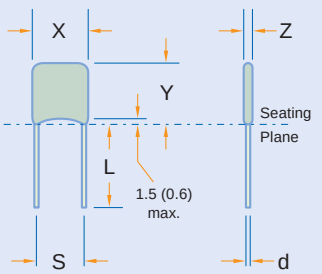
C0G/X7R

Dimensions

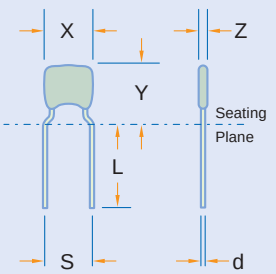
	Size	CECC	Width (X) max mm inches	Height (Y) max mm inches	Thickness (Z) max mm inches	Lead Space (S) mm inches	Lead Length (L) min mm inches	Lead Diameter (d) mm inches
	Case	Pattern						
Dipped Radial								
8111M	A	A	3.81 0.15	5.31 0.21	2.54 0.10	2.54±0.4 0.1±.0.016	5.0 0.2	0.5±0.05 0.02±0.002
8111N	F	B	3.81 0.15	5.31 0.21	2.54 0.10	5.08±0.4 0.2±0.016	5.0 0.2	0.5±0.05 0.02±0.002
8121M	B	A	5.08 0.20	6.58 0.26	3.18 0.125	2.54±0.4 0.1±0.016	5.0 0.2	0.5±0.05 0.02±0.002
8121N	C	B	5.08 0.20	6.58 0.26	3.18 0.125	5.08±0.4 0.2±0.016	5.0 0.2	0.5±0.05 0.02±0.002
8131M	D	A	7.62 0.30	9.12 0.36	3.81 0.15	5.08±0.4 0.2±0.016	5.0 0.2	0.5±0.05 0.02±0.002
8141M	H	A	10.16 0.40	11.66 0.46	3.81 0.15	5.08±0.4 0.2±0.016	5.0 0.2	0.5±0.05 0.02±0.002
8151M	J	A	12.70 0.50	14.20 0.56	5.08 0.20	10.1±0.4 0.4±0.016	5.0 0.2	0.6±0.05 0.025±0.002
8161M			18.50 0.73	16.50 0.65	6.00 0.24	14.5±0.5 0.57±0.02	5.0 0.2	0.6±0.05 0.025±0.002
8171M			25.00 0.98	20.00 0.79	6.00 0.24	20.5±0.5 0.81±0.02	5.0 0.2	0.6±0.05 0.025±0.002
Moulded Radial								
8123Z (CK05)	B	B	5.08 0.20	5.08 0.20	2.54 0.10	5.08±0.4 0.2±.0.016	30 1.2	0.6±0.05 0.025±0.002
8133Z (CK06)	C	A	7.62 0.30	7.62 0.30	2.54 0.10	5.08±0.4 0.2±0.016	30 1.2	0.6±0.05 0.025±0.002

Dipped Radial

Pattern A

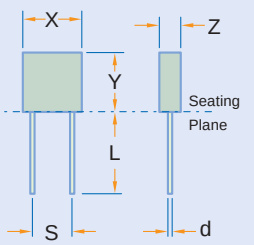


Pattern B

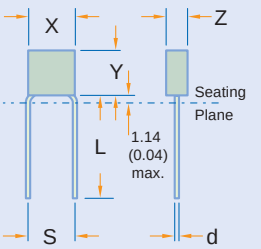


Moulded Radial

Pattern A



Pattern B



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Loose capacitors cropped and snap-in leads

Cropped Leads

Cropped leads between 4.0 (0.157) and 30.0 (1.18) are available to special order. Some of the preferred codes are listed below, together with the appropriate suffix code.
Dimensions as for standard product except as specified.

Dimensions mm (inches)

Suffix code - AE3
All radial ranges

Lead length (L)
6 ± 1 (0.236 ± 0.04)
from seating plane

Suffix code - AE4
All radial ranges

Lead length (L)
4 ± 1 (0.162 ± 0.04)
from seating plane

Suffix code - AD7
All radial ranges

Lead length (L)
5 ± 1 (0.2 ± 0.04)
from seating plane

Suffix code - AD5
All radial ranges

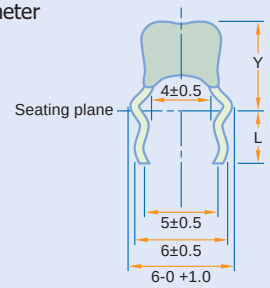
Lead length (L)
10 ± 1 (0.4 ± 0.04)
from seating plane

Snap in leads

Various forms of snap in leads (preformed) are available to special order, some of the preferred suffix codes are listed below.
Dimensions as for standard product except as specified.

Suffix code - AD1

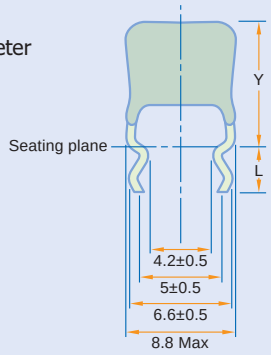
For PCB holes 0.9mm diameter
Types 8121N and 8131M



Dimensions
Y = 8121N 8 (0.315) Max
8131M 10 (0.394) Max
L = Min: 2.75 (0.108)
Max: 3.50 (0.138)

Suffix code - AD2

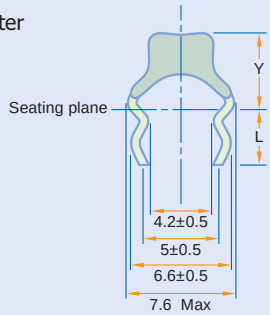
For PCB holes 1.2mm diameter
Types 8131M



Dimensions
Y = 10 (0.294) Max
L = Min: 2.75 (0.108)
Max: 3.50 (0.138)

Suffix code - AD3

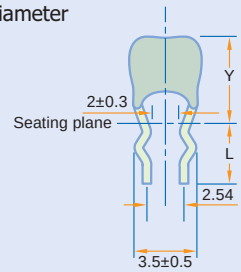
For PCB holes 1.2mm diameter
Types 8121N



Dimensions
Y = 8 (0.315) Max
L = Min: 2.75 (0.108)
Max: 3.50 (0.138)

Suffix code - AO7

For PCB holes 0.8 to 0.97mm diameter
Types 8121M



Dimensions
Y =6.58 (0.259) Max
L = Min: 2.75 (0.108)
Max: 3.50 (0.138)

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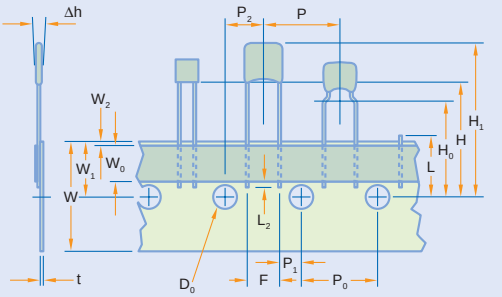
Bandoliered Packaging Information

A maximum of 3 consecutive components may be missing from the bandolier, followed by at least 6 filled positions.
Components missing from the bandolier are included in the total quantity, whereby the number of missing components may not exceed 0.25% of this total per packing module.
At the beginning and end of a reel the bandolier will exhibit at least 10 blank positions.

Minimum pull strength of product from tape = 5N.

Each reel/carton is provided with a label showing the:
Manufacturer, product style, batch identification, quantity and date code.
Labelling with bar codes (code 39) is available on request.

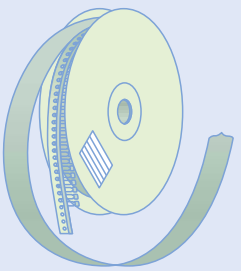


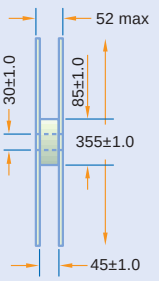
In accordance with IEC 60286 part 2

Dimensions mm (inches)

Description	Symbol	2.5mm lead space	5mm lead space	Tolerance
Lead wire diameter	d	0.5 (0.02), 0.6 (0.025)	0.5 (0.02), 0.6 (0.025)	±0.05 (0.002)
Component pitch	P	12.7 (0.5)	12.7 (0.5)	1.00 (0.04)
Feed hole pitch	P_0	12.7 (0.5)	12.7 (0.5)	±0.30 (0.01)
Feed hole centre to lead	P_1	5.08 (0.2)	3.81 (0.15)	±0.70 (0.03)
Feed hole centre to component	P_2	6.35 (0.25)	6.35 (0.25)	±0.70 (0.03)
Lead spacing	F	2.54 (0.10)	5.08 (0.20)	+0.6 (0.02) –0.1 (0.004)
Component alignment	Dh	0	0	±2.00(0.08)
Tape width	W	18.0 (0.70)	18.0 (0.70)	+1.00 (0.04) –0.50 (0.02)
Hold down tape width	W_0	6.0 (0.23)	6.0 (0.23)	±0.30 (0.01)
Hole position	W_1	9.0 (0.35)	9.0 (0.35)	±0.50 (0.02)
Hold down tape position	W_2	0.50 (0.02)	0.50 (0.02)	Max
Height to seating plane from tape centre (straight leads) (2)	H	16 (0.63) to 20 (0.79)	16 (0.63) to 20 (0.79)	As required
Height to seating plane from tape centre (formed leads) (2)	H_0	16 (0.63) to 20 (0.79)	16 (0.63) to 20 (0.79)	As required
Height to top of component from tape centre	H_1	32.2 (1.26)	32.2 (1.26)	Max
Feed hole diameter	D_0	4.0 (0.16)	4.0 (0.16)	±0.20 (0.008)
Carrier tape plus adhesive tape thickness	t	0.7 (0.03)	0.7 (0.03)	±0.20 (0.008)
Carrier tape thickness	-	0.5 (0.02)	0.5 (0.02)	±0.10 (0.004)
Cut out component snipped lead length from tape centre	L	11.0 (0.43)	11.0 (0.43)	Max
Lead wire protusion from hold down	L_2	2.0 (0.08)	2.0 (0.08)	Max

Bandoliered reels

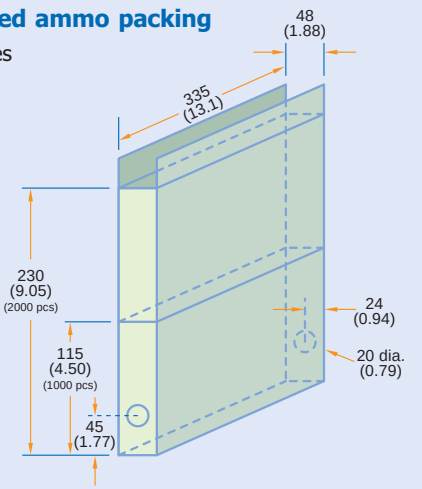




The adhesive tape faces outwards. The dispensing direction is as shown. For the protection of the components a paper inlay is inserted between the windings of the bandolier. At the end of the bandolier this paper inlay continues for at least a further two rotations.

Bandoliered ammo packing

2 carton sizes



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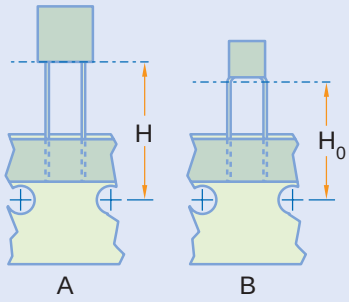
Bandoliered suffix codes

Moulded or dipped radial leaded types with 2.54 and 5.08mm lead spacing can be supplied bandoliered on reels or in ammo boxes to special order. Some of the preferred suffix codes for bandoliered products are given below.

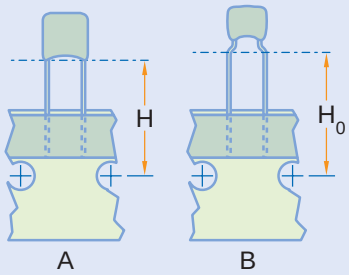
For bandoliered products the minimum order quantity, pieces, is specified in the tables below, larger orders must be in multiples of this quantity.

Moulded – straight and formed leads



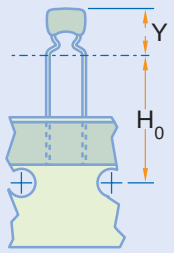
		Dimensions mm			Suffix code		
					Reel	AMMO pack	
Product code	Lead style	Diagram	H	H_0	2500pcs	1000pcs	2000pcs
8123Z	Formed 5.08 crs	B	–	16±0.5	C01	C02	C11
8133Z	Straight 5.08 crs	A	19±1	–	C01	C02	C11
8133Z	Straight 5.08 crs	A	16±0.5	–	C30	C31	C32

Dipped – straight and formed leads



					Suffix code		
					Reel	AMMO pack	
Product code	Lead style	Diagram	H	H_0	2500pcs	1000pcs	2000pcs
8111M	Straight 2.54 crs	A	19±1	–	C01	C02	C11
8111M	Straight 2.54 crs	A	16±0.5	–	C30	C31	C32
8111N	Formed 5.08 crs	B	–	16±0.5	C01	C02	C11
8121M	Straight 2.54 crs	A	19±1	–	C01	C02	C11
8121M	Straight 2.54 crs	A	16±0.5	–	C30	C31	C32
8121N	Formed 5.08 crs	B	–	16±0.5	C01	C02	C11
8131M	Straight 5.08 crs	A	19±1	–	C01	C02	C11
8131M	Straight 5.08 crs	A	16±0.5	–	C30	C31	C32

Dipped – stand-off lead form



				Suffix code		
				Reel	AMMO pack	
Product code	Lead style	Y max	H_0	2500pcs	1000pcs	2000pcs
8111N	Formed 5.08 crs	7.5	16±0.5	C12	C23	C22
8111N	Formed 5.08 crs	7.5	19±1	C13	C25	C24
8121N	Formed 5.08 crs	8.5	16±0.5	C12	C23	C22
8121N	Formed 5.08 crs	8.5	19±1	C13	C25	C24

This style has been developed to provide a meniscus-free seating plane with a stress relieving form for auto-insertion.

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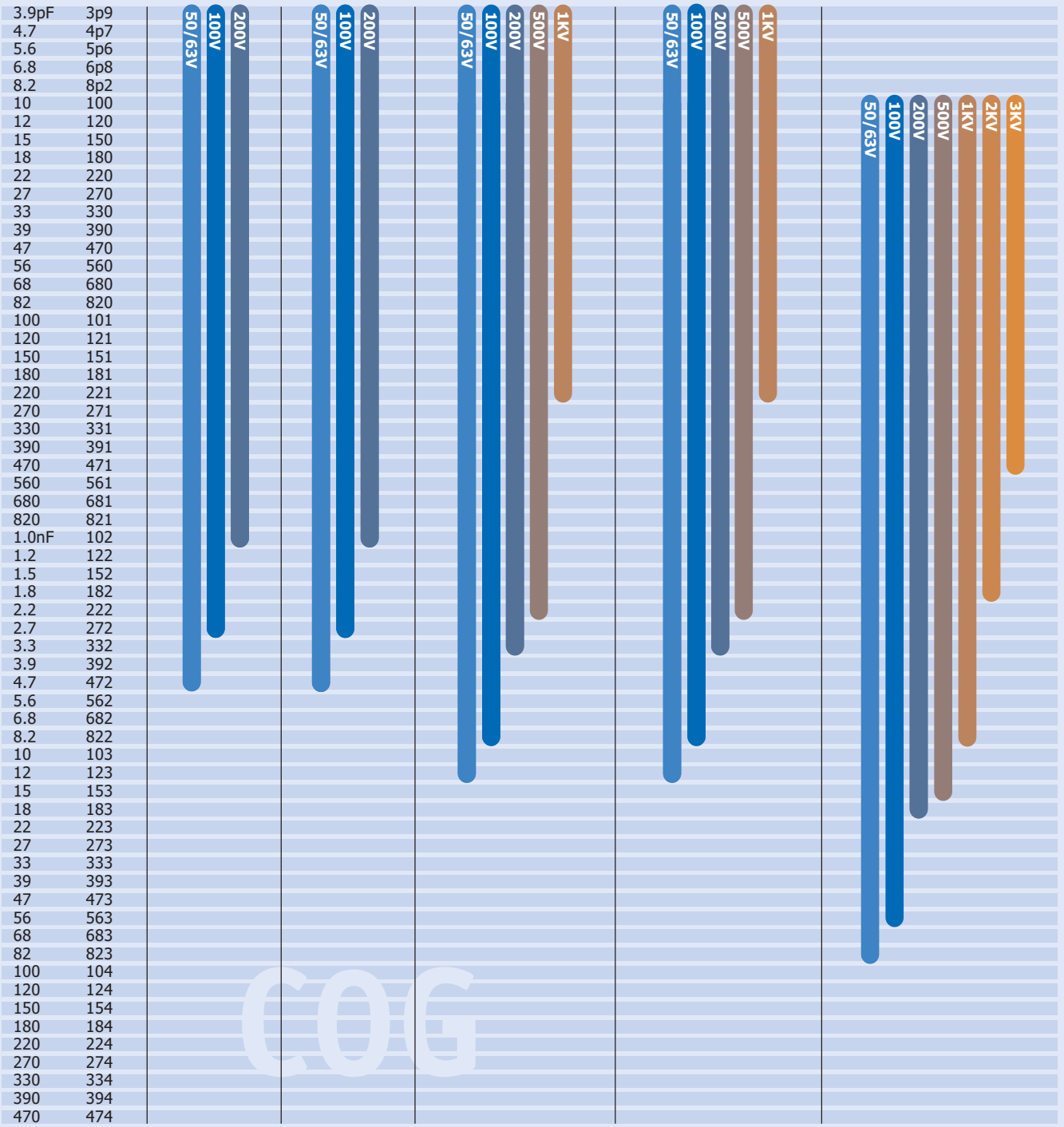
C0G



notes

1. Either pattern A or B may be supplied with the stated lead space (S) and wire diameter (d) and within the maximum dimesion of the specified type.
2. For sizes 8111, 8121 and 8131 at 50/63, 100 and 200V the capacitance values 3.9pF to 27nF can be supplied CECC Approved.

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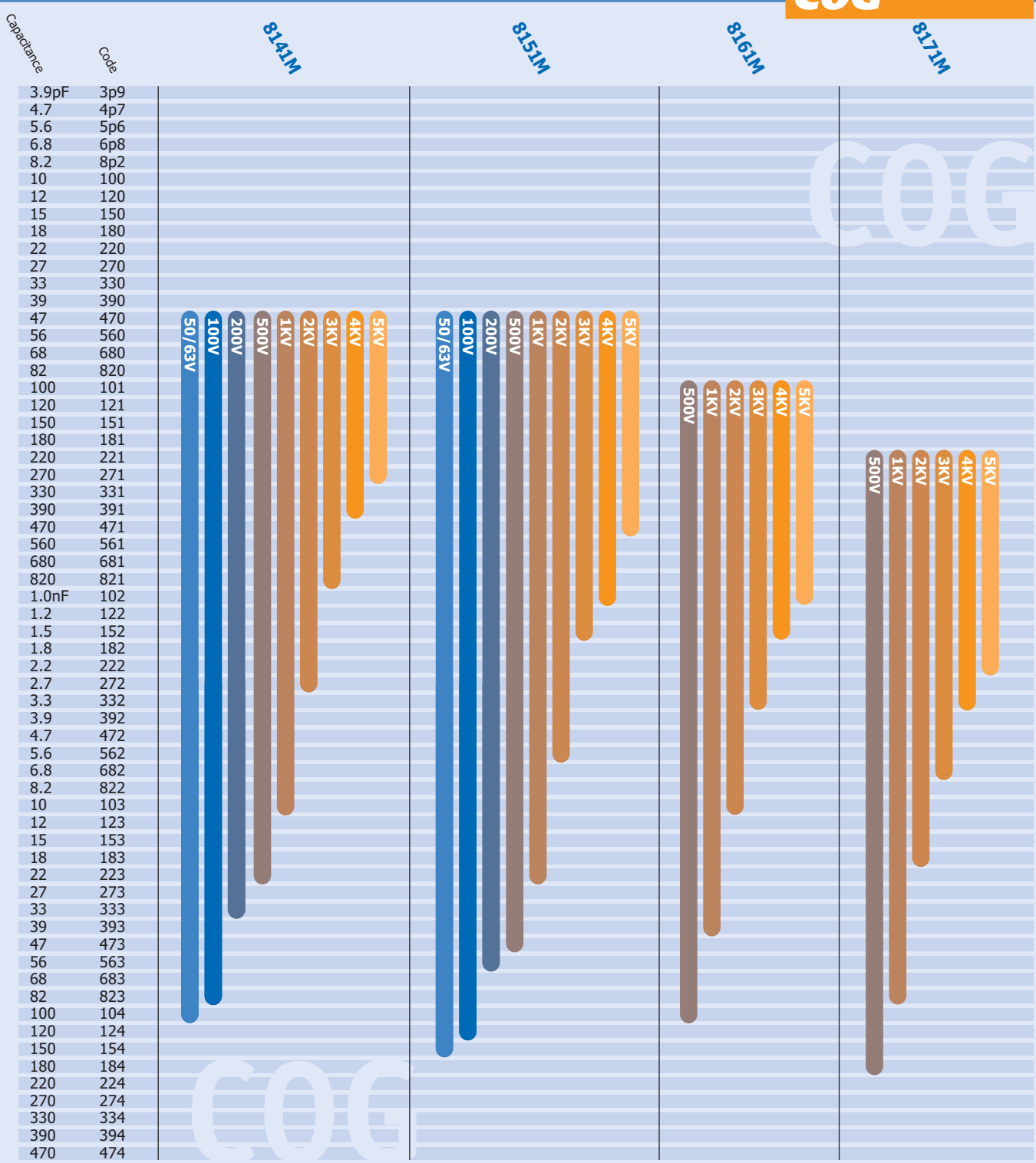

Capacitance	Code
3.9pF	3p9
4.7	4p7
5.6	5p6
6.8	6p8
8.2	8p2
10	100
12	120
15	150
18	180
22	220
27	270
33	330
39	390
47	470
56	560
68	680
82	820
100	101
120	121
150	151
180	181
220	221
270	271
330	331
390	391
470	471
560	561
680	681
820	821
1.0nF	102
1.2	122
1.5	152
1.8	182
2.2	222
2.7	272
3.3	332
3.9	392
4.7	472
5.6	562
6.8	682
8.2	822
10	103
12	123
15	153
18	183
22	223
27	273
33	333
39	393
47	473
56	563
68	683
82	823
100	104
120	124
150	154
180	184
220	224
270	274
330	334
390	394
470	474

notes

1. Either pattern A or B may be supplied with the stated lead space (S) and wire diameter (d) and within the maximum dimesion of the specified type.
2. For sizes 8111, 8121 and 8131 at 50/63, 100 and 200V the capacitance values 3.9pF to 27nF can be supplied CECC Approved.

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Stable Dielectric

X7R

Capacitance	Code	8111M	8111N	8121M	8121N	8131M
100pF	101	50/63V, 100V, 200V	50/63V, 100V, 200V	50/63V, 100V, 200V, 500V, 1KV	50/63V, 100V, 200V, 500V, 1KV	50/63V, 100V, 200V, 500V, 1KV, 2KV, 3KV
120	121					
150	151					
180	181					
220	221					
270	271					
330	331					
390	391					
470	471					
560	561					
680	681					
820	821					
1.0nF	102					
1.2	122					
1.5	152					
1.8	182					
2.2	222					
2.7	272					
3.3	332					
3.9	392					
4.7	472					
5.6	562					
6.8	682					
8.2	822					
10	103					
12	123					
15	153					
18	183					
22	223					
27	273					
33	333					
39	393					
47	473					
56	563					
68	683					
82	823					
100	104					
120	124					
150	154					
180	184					
220	224					
270	274					
330	334					
390	394					
470	474					
560	564					
680	684					
820	824					
1.0µF	105					
1.2	125					
1.5	155					
1.8	185					
2.2	225					
2.7	275					
3.3	335					
3.9	395					
4.7	475					
5.6	565					
6.8	685					
5.6	565					
6.8	685					
8.2	825					

X7R

notes

1. Either pattern A or B may be supplied with the stated lead space (S) and wire diameter (d) and within the maximum dimesion of the specified type.
2. For sizes 8111, 8121 and 8131 at 50/63, 100 and 200V the capacitance values 100pF to 1.0µF can be supplied CECC Approved (see Capacitance Table for available values).

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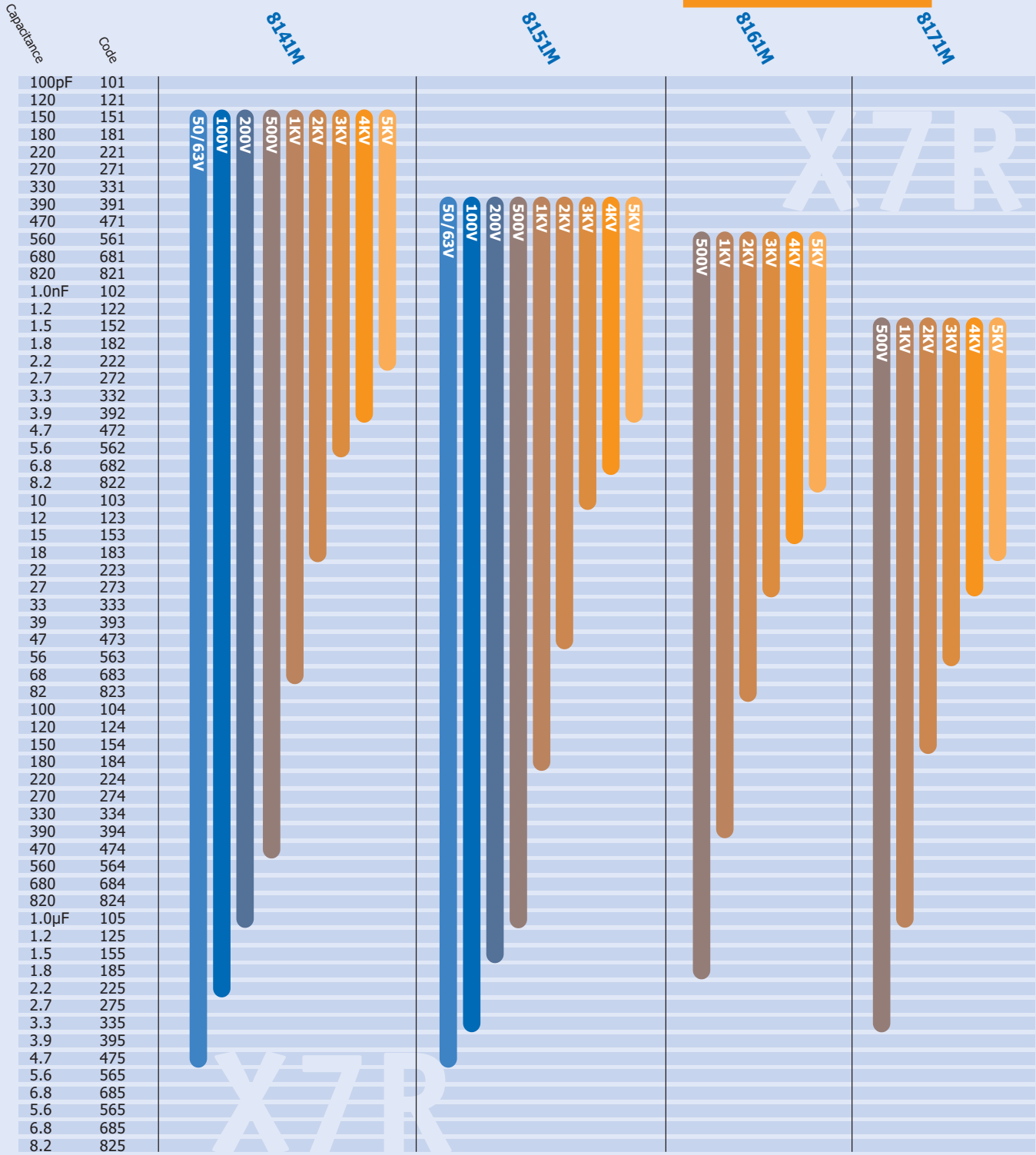
Stable Dielectric

X7R



Capacitance	Code
100pF	101
120	121
150	151
180	181
220	221
270	271
330	331
390	391
470	471
560	561
680	681
820	821
1.0nF	102
1.2	122
1.5	152
1.8	182
2.2	222
2.7	272
3.3	332
3.9	392
4.7	472
5.6	562
6.8	682
8.2	822
10	103
12	123
15	153
18	183
22	223
27	273
33	333
39	393
47	473
56	563
68	683
82	823
100	104
120	124
150	154
180	184
220	224
270	274
330	334
390	394
470	474
560	564
680	684
820	824
1.0µF	105
1.2	125
1.5	155
1.8	185
2.2	225
2.7	275
3.3	335
3.9	395
4.7	475
5.6	565
6.8	685
5.6	565
6.8	685
8.2	825

notes

1. Either pattern A or B may be supplied with the stated lead space (S) and wire diameter (d) and within the maximum dimesion of the specified type.
2. For sizes 8111, 8121 and 8131 at 50/63, 100 and 200V the capacitance values 100pF to 1.0µF can be supplied CECC Approved (see Capacitance Table for available values).

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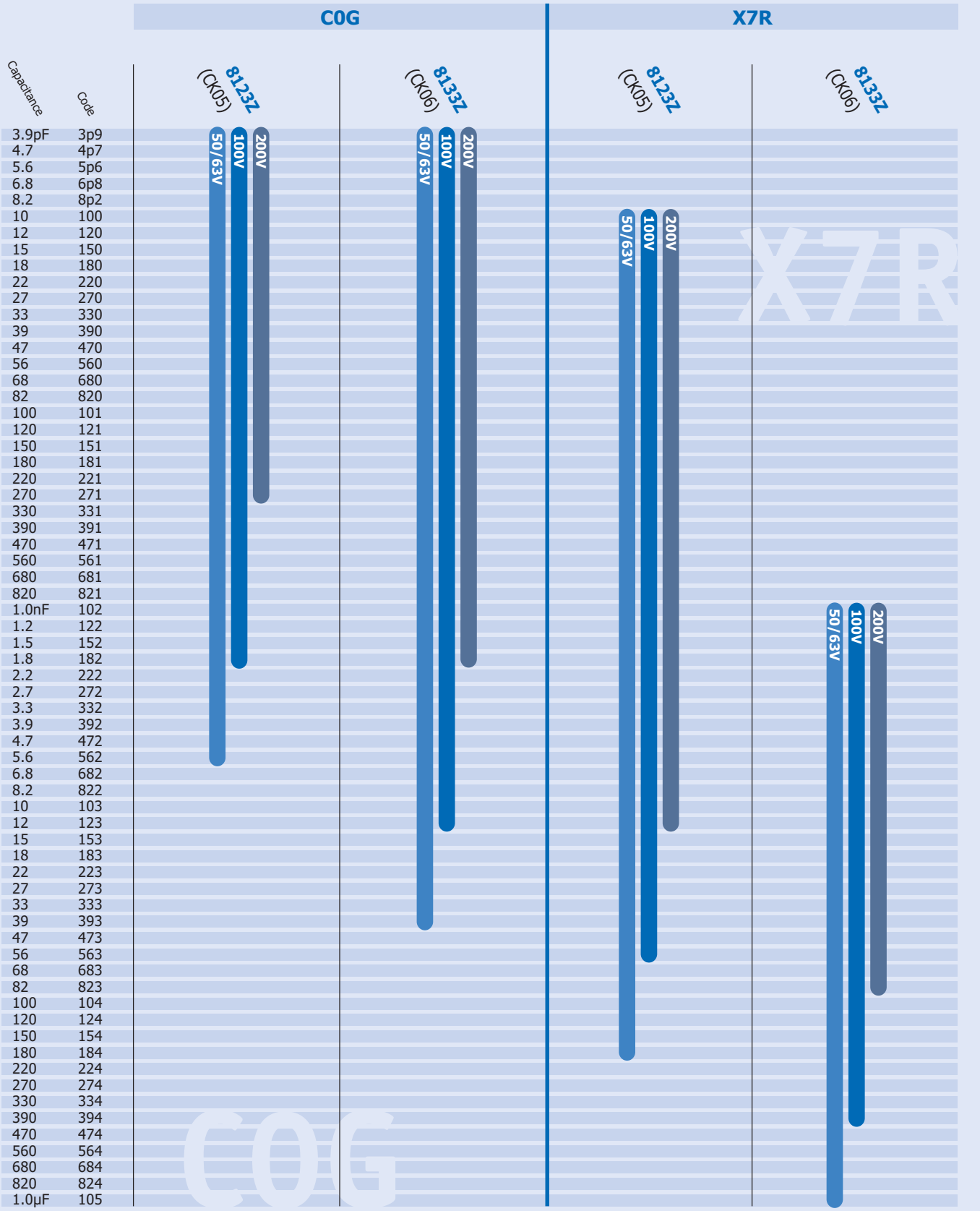
Ultra-stable and Stable Dielectric

C0G/X7R



notes

1. Capacitance values 3.9pF to 1.0µF can be supplied CECC Approved (see Capacitance Table for available values).

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