OKI Semiconductor

This version: Jan. 1998
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MSM82C51A-2RS/GS/JS

UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER

GENERAL DESCRIPTION

The MSM82C51A-2 is a USART (Universal Synchronous Asynchronous Receiver Transmitter) for serial data communication.
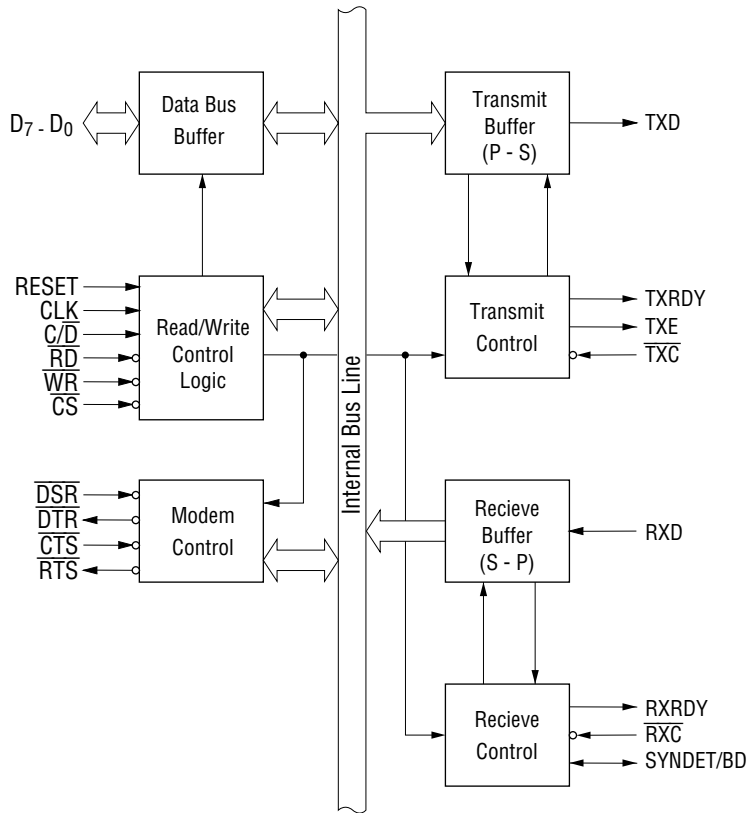
As a peripheral device of a microcomputer system, the MSM82C51A-2 receives parallel data from the CPU and transmits serial data after conversion. This device also receives serial data from the outside and transmits parallel data to the CPU after conversion.

The MSM82C51A-2 configures a fully static circuit using silicon gate CMOS technology. Therefore, it operates on extremely low power at 100 µA (max) of standby current by suspending all operations.
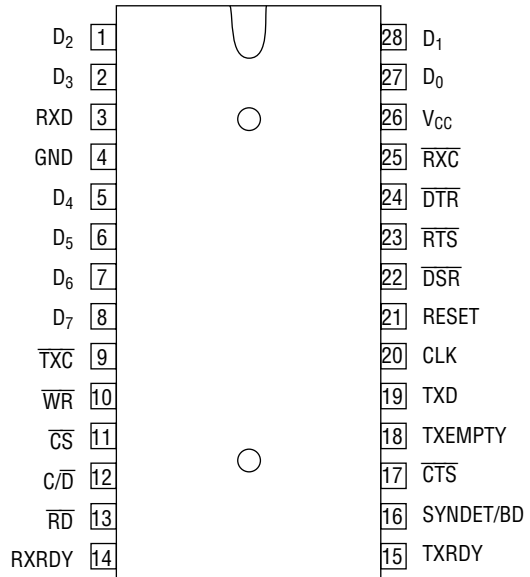
FEATURES

- Wide power supply voltage range from 3 V to 6 V
- Wide temperature range from –40°C to 85°C
- Synchronous communication upto 64 Kbaud
- Asynchronous communication upto 38.4 Kbaud
- Transmitting/receiving operations under double buffered configuration.
- Error detection (parity, overrun and framing)
- 28-pin Plastic DIP (DIP28-P-600-2.54): (Product name: MSM82C51A-2RS)
- 28-pin Plastic QFJ (QFJ28-P-S450-1.27): (Product name: MSM82C51A-2JS)
- 32-pin Plastic SSOP(SSOP32-P-430-1.00-K): (Product name: MSM82C51A-2GS-K)
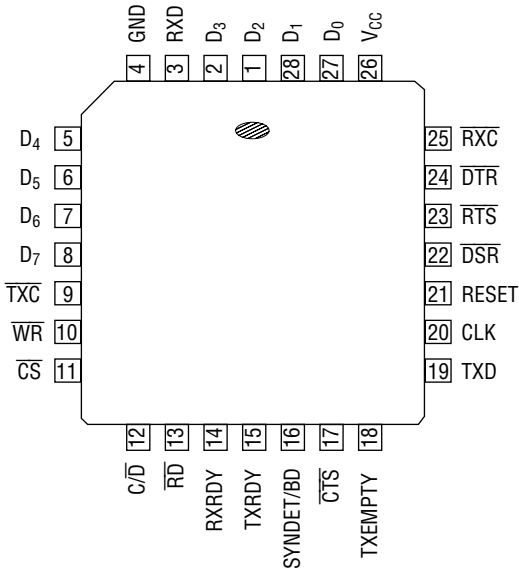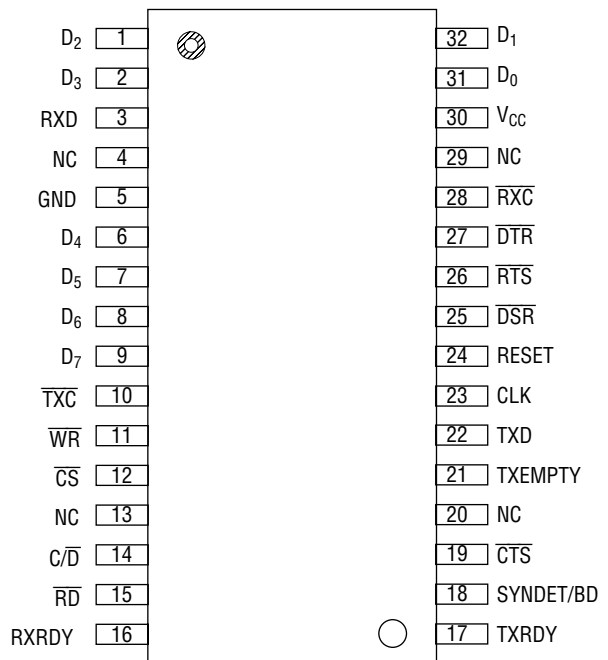
FUNCTIONAL BLOCK DIAGRAM

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PIN CONFIGURATION (TOP VIEW)

28 pin Plastic DIP

D_2	1		28	D_1
D_3	2		27	D_0
RXD	3		26	V_{CC}
GND	4		25	$\overline{RXC}$
D_4	5		24	$\overline{DTR}$
D_5	6		23	$\overline{RTS}$
D_6	7		22	$\overline{DSR}$
D_7	8		21	RESET
$\overline{TXC}$	9		20	CLK
$\overline{WR}$	10		19	TXD
$\overline{CS}$	11		18	TXEMPTY
$C/\overline{D}$	12		17	$\overline{CTS}$
$\overline{RD}$	13		16	SYNDET/BD
RXRDY	14		15	TXRDY

28 pin Plastic QFJ

Top pins (left to right): GND(4), RXD(3), D_3(2), D_2(1), D_1(28), D_0(27), V_{CC}(26)

Left pins (top to bottom):
D_4	5	25	$\overline{RXC}$
D_5	6	24	$\overline{DTR}$
D_6	7	23	$\overline{RTS}$
D_7	8	22	$\overline{DSR}$
$\overline{TXC}$	9	21	RESET
$\overline{WR}$	10	20	CLK
$\overline{CS}$	11	19	TXD

Bottom pins (left to right): $C/\overline{D}$(12), $\overline{RD}$(13), RXRDY(14), TXRDY(15), SYNDET/BD(16), $\overline{CTS}$(17), TXEMPTY(18)

32 pin Plastic SSOP

D_2	1		32	D_1
D_3	2		31	D_0
RXD	3		30	V_{CC}
NC	4		29	NC
GND	5		28	$\overline{RXC}$
D_4	6		27	$\overline{DTR}$
D_5	7		26	$\overline{RTS}$
D_6	8		25	$\overline{DSR}$
D_7	9		24	RESET
$\overline{TXC}$	10		23	CLK
$\overline{WR}$	11		22	TXD
$\overline{CS}$	12		21	TXEMPTY
NC	13		20	NC
$C/\overline{D}$	14		19	$\overline{CTS}$
$\overline{RD}$	15		18	SYNDET/BD
RXRDY	16		17	TXRDY

FUNCTION

Outline

The MSM82C51A-2's functional configuration is programed by software.
Operation between the MSM82C51A-2 and a CPU is executed by program control. Table 1 shows the operation between a CPU and the device.

Table 1 Operation between MSM82C51A and CPU

$\overline{CS}$	C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	
1	×	×	×	Data Bus 3-State
0	×	1	1	Data Bus 3-State
0	1	0	1	Status → CPU
0	1	1	0	Control Word ← CPU
0	0	0	1	Data → CPU
0	0	1	0	Data ← CPU

It is necessary to execute a function-setting sequence after resetting the MSM82C51A-2. Fig. 1 shows the function-setting sequence.
If the function was set, the device is ready to receive a command, thus enabling the transfer of data by setting a necessary command, reading a status and reading/writing data.
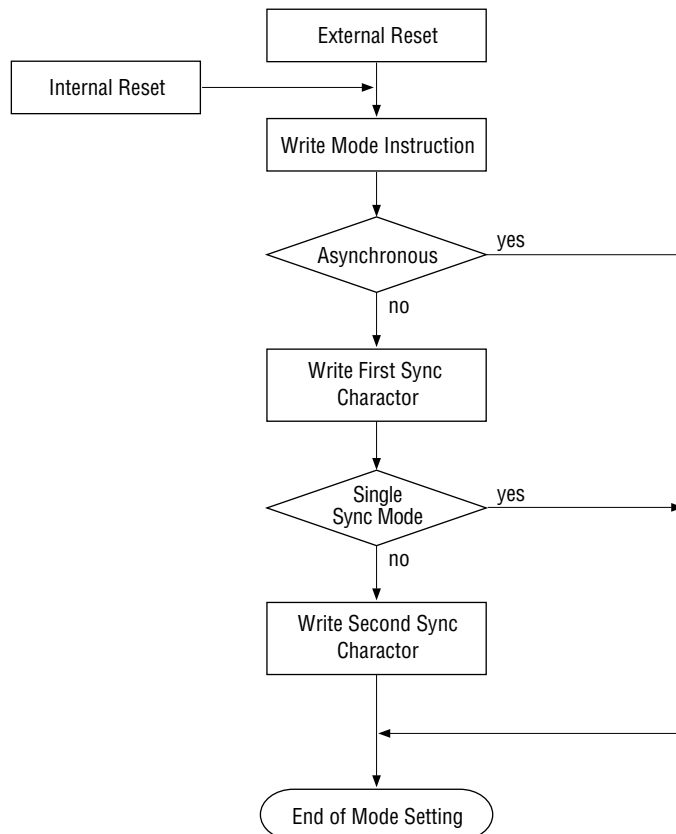

Fig. 1 Function-setting Sequence (Mode Instruction Sequence)

Control Words

There are two types of control word.
1. Mode instruction (setting of function)
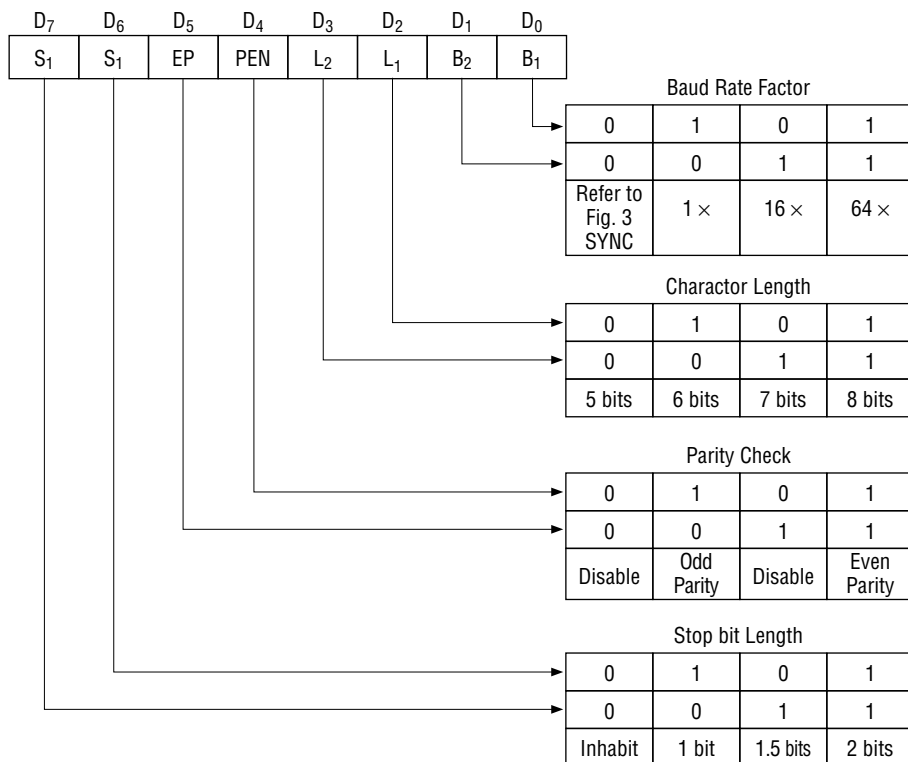2. Command (setting of operation)

1) Mode Instruction

Mode instruction is used for setting the function of the MSM82C51A-2. Mode instruction will be in "wait for write" at either internal reset or external reset. That is, the writing of a control word after resetting will be recognized as a "mode instruction."
Items set by mode instruction are as follows:

- Synchronous/asynchronous mode
- Stop bit length (asynchronous mode)
- Character length
- Parity bit
- Baud rate factor (asynchronous mode)
- Internal/external synchronization (synchronous mode)
- Number of synchronous characters (Synchronous mode)

The bit configuration of mode instruction is shown in Figures 2 and 3. In the case of synchronous mode, it is necessary to write one-or two byte sync characters.
If sync characters were written, a function will be set because the writing of sync characters constitutes part of mode instruction.
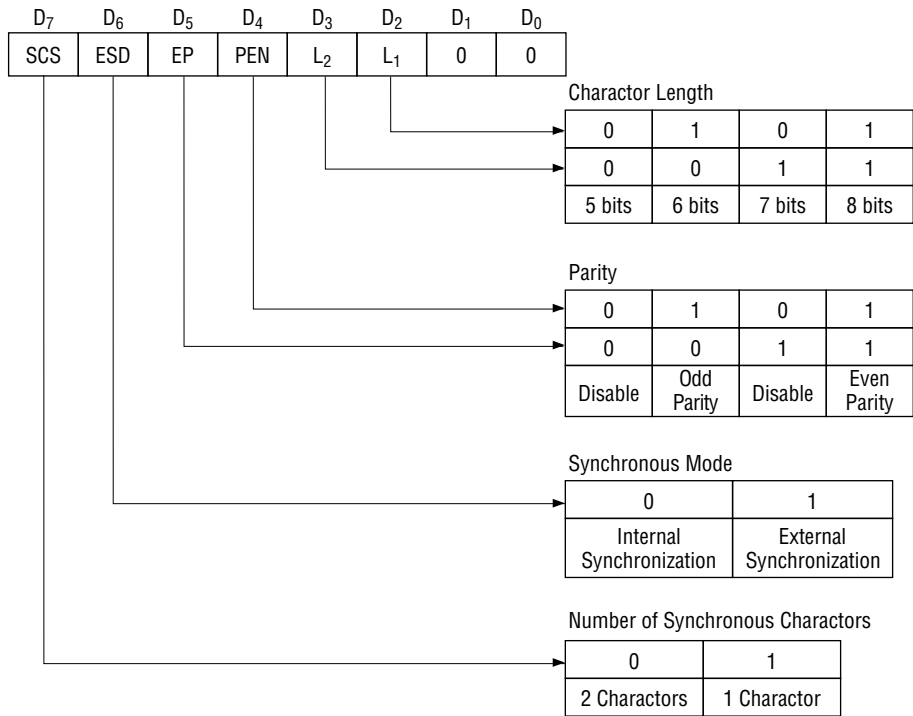
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
S_1	S_1	EP	PEN	L_2	L_1	B_2	B_1

Baud Rate Factor

0	1	0	1
0	0	1	1
Refer to Fig. 3 SYNC	$1\times$	$16\times$	$64\times$

Charactor Length

0	1	0	1
0	0	1	1
5 bits	6 bits	7 bits	8 bits

Parity Check

0	1	0	1
0	0	1	1
Disable	Odd Parity	Disable	Even Parity

Stop bit Length

0	1	0	1
0	0	1	1
Inhabit	1 bit	1.5 bits	2 bits

Fig. 2 Bit Configuration of Mode Instruction (Asynchronous)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SCS	ESD	EP	PEN	L_2	L_1	0	0

Charactor Length

0	1	0	1
0	0	1	1
5 bits	6 bits	7 bits	8 bits

Parity

0	1	0	1
0	0	1	1
Disable	Odd Parity	Disable	Even Parity

Synchronous Mode

0	1
Internal Synchronization	External Synchronization

Number of Synchronous Charactors

0	1
2 Charactors	1 Charactor

Fig. 3 Bit Configuration of Mode Instruction (Synchronous)

2) Command

Command is used for setting the operation of the MSM82C51A-2.
It is possible to write a command whenever necessary after writing a mode instruction and sync characters.
Items to be set by command are as follows:

- Transmit   Enable/Disable
- Receive Enable/Disable
- $\overline{DTR}$, $\overline{RTS}$ Output of data.
- Resetting of error flag.
- Sending to break characters
- Internal resetting
- Hunt mode (synchronous mode)

The bit configuration of a command is shown in Fig. 4.

D$_7$	D$_6$	D$_5$	D$_4$	D$_3$	D$_2$	D$_1$	D$_0$
EH	IR	RTS	ER	SBRK	RXE	DTR	TXEN

1…Transmit Enable
0…Disable

$\overline{DTR}$
$1 \rightarrow \overline{DTR} = 0$
$0 \rightarrow \overline{DTR} = 1$

1…Recieve Enable
0…Disable

1…Sent Break Charactor
0…Normal Operation

1…Reset Error Flag
0…Normal Operation

$\overline{RTS}$
$1 \rightarrow \overline{RTS} = 0$
$0 \rightarrow \overline{RTS} = 1$

1…Internal Reset
0…Normal Operation

1…Hunt Mode (Note)
0…Normal Operation
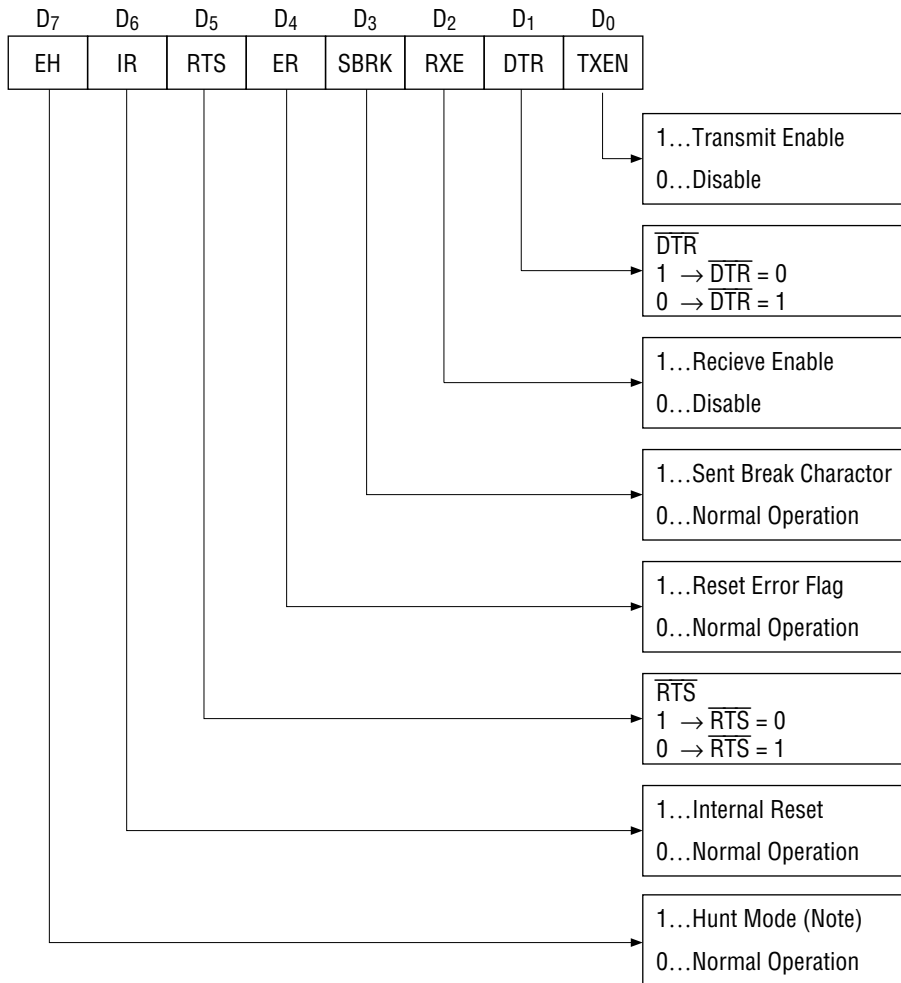
Note: Seach mode for synchronous charactors in synchronous mode.

Fig. 4 Bit Configuration of Command

Status Word

It is possible to see the internal status of MSM82C51A-2 by reading a status word.
The bit configuration of status word is shown in Fig. 5.
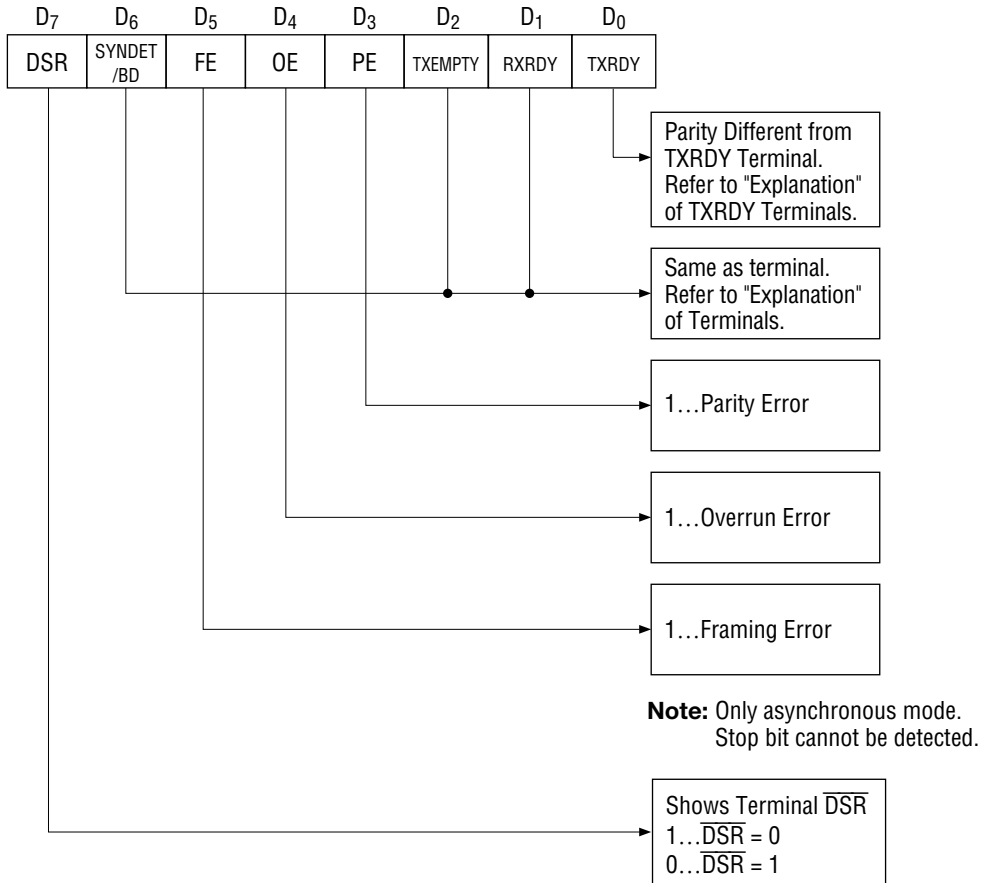
Fig. 5 Bit Configuration of Status Word

Standby Status

It is possible to put the MSM82C51A-2 in "standby status"
When the following conditions have been satisfied the MSM82C51A-2 is in "standby status."

(1) $\overline{CS}$ terminal is fixed at Vcc level.
(2) Input pins other $\overline{CS}$, D_0 to D_7, $\overline{RD}$, $\overline{WR}$ and C/$\overline{D}$ are fixed at Vcc or GND level (including SYNDET in external synchronous mode).

　　　Note:　When all output currents are 0, ICCS specification is applied.

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Pin Description

D₀ to D₇ (I/O terminal)

This is bidirectional data bus which receive control words and transmits data from the CPU and sends status words and received data to CPU.

RESET (Input terminal)

A "High" on this input forces the MSM82C51A-2 into "reset status."
The device waits for the writing of "mode instruction."
The min. reset width is six clock inputs during the operating status of CLK.

CLK (Input terminal)

CLK signal is used to generate internal device timing.
CLK signal is independent of $\overline{RXC}$ or $\overline{TXC}$.
However, the frequency of CLK must be greater than 30 times the $\overline{RXC}$ and $\overline{TXC}$ at Synchronous mode and Asynchronous "x1" mode, and must be greater than 5 times at Asynchronous "x16" and "x64" mode.

$\overline{WR}$ (Input terminal)

This is the "active low" input terminal which receives a signal for writing transmit data and control words from the CPU into the MSM82C51A-2.

$\overline{RD}$ (Input terminal)

This is the "active low" input terminal which receives a signal for reading receive data and status words from the MSM82C51A-2.

C/$\overline{D}$ (Input terminal)

This is an input terminal which receives a signal for selecting data or command words and status words when the MSM82C51A-2 is accessed by the CPU.
If C/$\overline{D}$ = low, data will be accessed.
If C/$\overline{D}$ = high, command word or status word will be accessed.

$\overline{CS}$ (Input terminal)

This is the "active low" input terminal which selects the MSM82C51A-2 at low level when the CPU accesses.

> Note: The device won't be in "standby status"; only setting $\overline{CS}$ = High.
> Refer to "Explanation of Standby Status."

TXD (output terminal)

This is an output terminal for transmitting data from which serial-converted data is sent out. The device is in "mark status" (high level) after resetting or during a status when transmit is disabled. It is also possible to set the device in "break status" (low level) by a command.

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TXRDY (output terminal)

This is an output terminal which indicates that the MSM82C51A-2 is ready to accept a transmitted data character. But the terminal is always at low level if $\overline{CTS}$ = high or the device was set in "TX disable status" by a command.

Note: TXRDY status word indicates that transmit data character is receivable, regardless
of $\overline{CTS}$ or command.
If the CPU writes a data character, TXRDY will be reset by the leading edge or $\overline{WR}$ signal.

TXEMPTY (Output terminal)

This is an output terminal which indicates that the MSM82C51A-2 has transmitted all the characters and had no data character.
In "synchronous mode," the terminal is at high level, if transmit data characters are no longer remaining and sync characters are automatically transmitted. If the CPU writes a data character, TXEMPTY will be reset by the leading edge of $\overline{WR}$ signal.

Note : As the transmitter is disabled by setting $\overline{CTS}$ "High" or command, data written
before disable will be sent out. Then TXD and TXEMPTY will be "High".
Even if a data is written after disable, that data is not sent out and TXE will be "High".After   the transmitter is enabled, it sent out. (Refer to Timing Chart of Transmitter Control and Flag   Timing)

$\overline{TXC}$ (Input terminal)

This is a clock input signal which determines the transfer speed of transmitted data.
In "synchronous mode," the baud rate will be the same as the frequency of $\overline{TXC}$.
In "asynchronous mode", it is possible to select the baud rate factor by mode instruction.
It can be 1, 1/16 or 1/64 the $\overline{TXC}$.
The falling edge of $\overline{TXC}$ sifts the serial data out of the MSM82C51A-2.

RXD (input terminal)

This is a terminal which receives serial data.

RXRDY (Output terminal)

This is a terminal which indicates that the MSM82C51A-2 contains a character that is ready to READ.
If the CPU reads a data character, RXRDY will be reset by the leading edge of $\overline{RD}$ signal.
Unless the CPU reads a data character before the next one is received completely, the preceding data will be lost. In such a case, an overrun error flag status word will be set.

$\overline{RXC}$ (Input terminal)

This is a clock input signal which determines the transfer speed of received data.
In "synchronous mode," the baud rate is the same as the frequency of $\overline{RXC}$.
In "asynchronous mode," it is possible to select the baud rate factor by mode instruction.
It can be 1, 1/16, 1/64 the $\overline{RXC}$.

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SYNDET/BD (Input or output terminal)

This is a terminal whose function changes according to mode.

In "internal synchronous mode." this terminal is at high level, if sync characters are received and synchronized. If a status word is read, the terminal will be reset.

In "external synchronous mode, "this is an input terminal.

A "High" on this input forces the MSM82C51A-2 to start receiving data characters.

In "asynchronous mode," this is an output terminal which generates "high level"output upon the detection of a "break" character if receiver data contains a "low-level" space between the stop bits of two continuous characters. The terminal will be reset, if RXD is at high level.

After Reset is active, the terminal will be output at low level.

$\overline{\text{DSR}}$ (Input terminal)

This is an input port for MODEM interface. The input status of the terminal can be recognized by the CPU reading status words.

$\overline{\text{DTR}}$ (Output terminal)

This is an output port for MODEM interface. It is possible to set the status of $\overline{\text{DTR}}$ by a command.

$\overline{\text{CTS}}$ (Input terminal)

This is an input terminal for MODEM interface which is used for controlling a transmit circuit. The terminal controls data transmission if the device is set in "TX Enable" status by a command. Data is transmitable if the terminal is at low level.

$\overline{\text{RTS}}$ (Output terminal)

This is an output port for MODEM interface. It is possible to set the status $\overline{\text{RTS}}$ by a command.

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ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Rating			Unit	Conditions
		MSM82C51A-2RS	MSM82C51A-2GS	MSM82C51A-2JS		
Power Supply Voltage	V_{CC}	−0.5 to +7			V	With respect to GND
Input Voltage	V_{IN}	−0.5 to V_{CC} +0.5			V	
Output Voltage	V_{OUT}	−0.5 to V_{CC} +0.5			V	
Storage Temperature	T_{STG}	−55 to +150			°C	—
Power Dissipation	P_D	0.9	0.7	0.9	W	Ta = 25°C

OPERATING RANGE

Parameter	Symbol	Range	Unit
Power Supply Voltage	V_{CC}	3 - 6	V
Operating Temperature	T_{op}	−40 to 85	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5	5.5	V
Operating Temperature	T_{op}	−40	+25	+85	°C
"L" Input Voltage	V_{IL}	−0.3	—	+0.8	V
"H" Input Voltage	V_{IH}	2.2	—	V_{CC} +0.3	V

DC CHARACTERISTICS

(V_{CC} = 4.5 to 5.5 V Ta = −40°C to +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Measurement Conditions
"L" Output Voltage	V_{OL}	—	—	0.45	V	I_{OL} = 2.5 mA
"H" Output Voltage	V_{OH}	3.7	—	—	V	I_{OH} = −2.5 mA
Input Leak Current	I_{LI}	−10	—	10	µA	$0 \le V_{IN} \le V_{CC}$
Output Leak Current	I_{LO}	−10	—	10	µA	$0 \le V_{OUT} \le V_{CC}$
Operating Supply Current	I_{CCO}	—	—	5	mA	Asynchronous X64 during Transmitting/ Receiving
Standby Supply Current	I_{CCS}	—	—	100	µA	All Input voltage shall be fixed at V_{CC} or GND level.

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AC CHARACTERISTICS

CPU Bus Interface Part

(V_{CC} = 4.5 to 5.5 V, Ta = −40 to 85°C)

Parameter	Symbol	Min.	Max.	Unit	Remarks
Address Stable before $\overline{RD}$	t_{AR}	20	—	ns	Note 2
Address Hold Time for $\overline{RD}$	t_{RA}	20	—	ns	Note 2
$\overline{RD}$ Pulse Width	t_{RR}	130	—	ns	—
Data Delay from $\overline{RD}$	t_{RD}	—	100	ns	—
$\overline{RD}$ to Data Float	t_{DF}	10	75	ns	—
Recovery Time between $\overline{RD}$	t_{RVR}	6	—	t_{CY}	Note 5
Address Stable before $\overline{WR}$	t_{AW}	20	—	ns	Note 2
Address Hold Time for $\overline{WR}$	t_{WA}	20	—	ns	Note 2
$\overline{WR}$ Pulse Width	t_{WW}	100	—	ns	—
Data Set-up Time for $\overline{WR}$	t_{DW}	100	—	ns	—
Data Hold Time for $\overline{WR}$	t_{WD}	0	—	ns	—
Recovery Time between $\overline{WR}$	t_{RVW}	6	—	t_{CY}	Note 4
RESET Pulse Width	t_{RESW}	6	—	t_{CY}	—

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Serial Interface Part

<div align="right">(V_{CC} = 4.5 to 5.5 V, Ta = −40 to 85°C)</div>

$(V_{CC} = 4.5 \text{ to } 5.5 \text{ V},\ Ta = -40 \text{ to } 85°C)$

Parameter		Symbol	Min.	Max.	Unit	Remarks
Main Clock Period		t_{CY}	160	—	ns	Note 3
Clock Low Tme		$t_{\bar{\phi}}$	50	—	ns	—
Clock High Time		t_{ϕ}	70	$t_{CY} -50$	ns	—
Clock Rise/Fall Time		t_r, t_f	—	20	ns	—
TXD Delay from Falling Edge of $\overline{TXC}$		t_{DTX}	—	1	μS	—
Transmitter Clock Frequency	$1 \times$ Baud	f_{TX}	DC	64	kHz	Note 3
	$16 \times$ Baud	f_{TX}	DC	615	kHz	
	$64 \times$ Baud	f_{TX}	DC	615	kHz	
Transmitter Clock Low Time	$1 \times$ Baud	t_{TPW}	13	—	t_{CY}	—
	$16 \times, 64 \times$ Baud	t_{TPW}	2	—	t_{CY}	—
Transmitter Clock High Time	$1 \times$ Baud	t_{TPD}	15	—	t_{CY}	—
	$16 \times, 64 \times$ Baud	t_{TPD}	3	—	t_{CY}	—
Receiver Clock Frequency	$1 \times$ Baud	f_{RX}	DC	64	kHz	Note 3
	$16 \times$ Baud	f_{RX}	DC	615	kHz	
	$64 \times$ Baud	f_{RX}	DC	615	kHz	
Receiver Clock Low Time	$1 \times$ Baud	t_{RPW}	13	—	t_{CY}	—
	$16 \times, 64 \times$ Baud	t_{RPW}	2	—	t_{CY}	—
Receiver Clock High Time	$1 \times$ Baud	t_{RPD}	15	—	t_{CY}	—
	$16 \times, 64 \times$ Baud	t_{RPD}	3	—	t_{CY}	—
Time from the Center of Last Bit to the Rise of TXRDY		t_{TXRDY}	—	8	t_{CY}	—
Time from the Leading Edge of $\overline{WR}$ to the Fall of TXRDY		$t_{TXRDY\ CLEAR}$	—	400	ns	—
Time From the Center of Last Bit to the Rise of RXRDY		t_{RXRDY}	—	26	t_{CY}	—
Time from the Leading Edge of $\overline{RD}$ to the Fall of RXRDY		$t_{RXRDY\ CLEAR}$	—	400	ns	—
Internal SYNDET Delay Time from Rising Edge of $\overline{RXC}$		t_{IS}	—	26	t_{CY}	—
SYNDET Setup Time for $\overline{RXC}$		t_{ES}	18	—	t_{CY}	—
TXE Delay Time from the Center of Last Bit		$t_{TXEMPTY}$	20	—	t_{CY}	—
MODEM Control Signal Delay Time from Rising Edge of $\overline{WR}$		t_{WC}	8	—	t_{CY}	—
MODEM Control Signal Setup Time for Falling Edge of $\overline{RD}$		t_{CR}	20	—	t_{CY}	—
RXD Setup Time for Rising Edge of $\overline{RXC}$ (1X Baud)		t_{RXDS}	11	—	t_{CY}	—
RXD Hold Time for Falling Edge of $\overline{RXC}$ (1X Baud)		t_{RXDH}	17	—	t_{CY}	—

Notes: 1. AC characteristics are measured at 150 pF capacity load as an output load based on 0.8 V at low level and 2.2 V at high level for output and 1.5 V for input.
  2. Addresses are $\overline{CS}$ and $C/\overline{D}$.
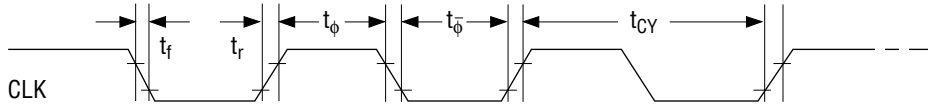 3. f_{TX} or $f_{RX} \leq 1/(30\ Tcy)$ $1\times$ Baud
     f_{TX} or $f_{RX} \leq 1/(5\ Tcy)$ $16\times, 64\times$ Baud
  4. This recovery time is mode Initialization only. Recovery time between command writes for Asynchronous Mode is 8 t_{CY} and for Synchronous Mode is 18 t_{CY}.
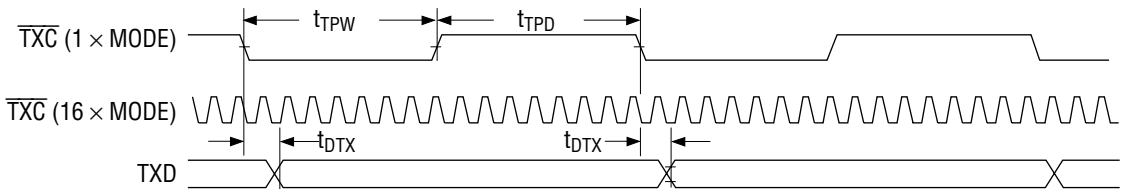   Write Data is allowed only when TXRDY = 1.
  5. This recovery time is Status read only.
     Read Data is allowed only when RXRDY = 1.
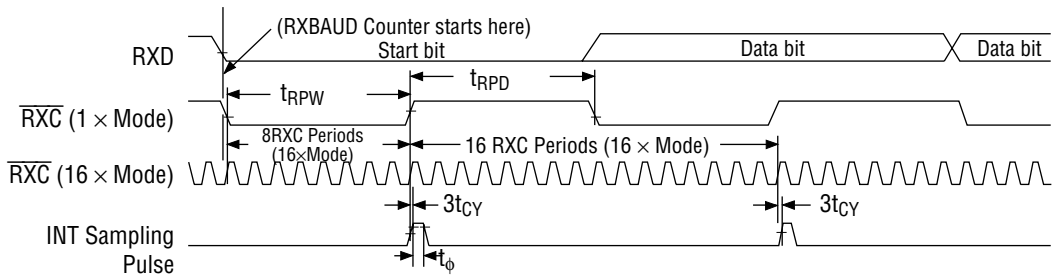
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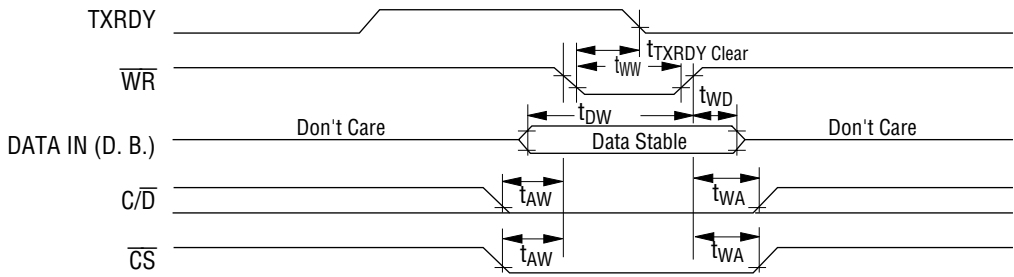**OKI** Semiconductor   **MSM82C51A-2RS/GS/JS**

TIMING CHART

Sytem Clock Input

CLK

t_f t_r t_ϕ t_ϕ t_{CY}

Transmitter Clock and Data

$\overline{TXC}$ (1 × MODE)

t_{TPW} t_{TPD}

$\overline{TXC}$ (16 × MODE)

TXD

t_{DTX} t_{DTX}

Receiver Clock and Data

RXD

(RXBAUD Counter starts here)
Start bit   Data bit   Data bit

$\overline{RXC}$ (1 × Mode)

t_{RPW} t_{RPD}

8RXC Periods
(16×Mode)   16 RXC Periods (16 × Mode)

$\overline{RXC}$ (16 × Mode)

INT Sampling
Pulse

$3t_{CY}$ $3t_{CY}$

t_ϕ

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Write Data Cycle (CPU → USART)

TXRDY

$t_{TXRDY\ Clear}$

$\overline{WR}$　　t_{WW}　　t_{WD}

t_{DW}

DATA IN (D. B.)　　Don't Care　　Data Stable　　Don't Care

C/$\overline{D}$　　t_{AW}　　t_{WA}

$\overline{CS}$　　t_{AW}　　t_{WA}

Read Data Cycle (CPU ← USART)

RXRDY

$t_{RXRDY\ Clear}$

$\overline{RD}$　　t_{RR}

t_{RD}　　t_{DF}

DATA OUT (D. B.)　　Data Float　　Data Out Active　　Data Float

C/$\overline{D}$　　t_{AR}　　t_{RA}

$\overline{CS}$　　t_{AR}　　t_{RA}
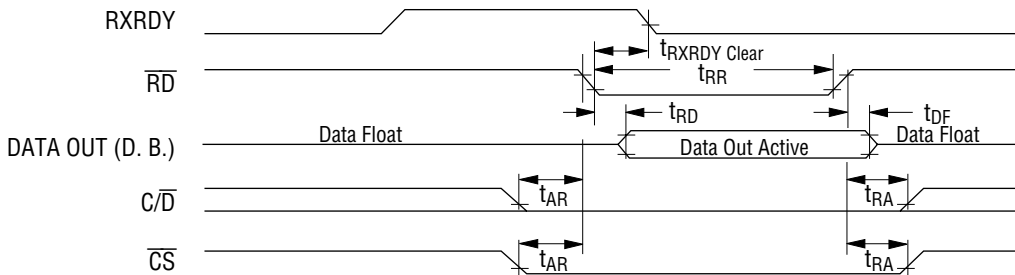
Write Control or Output Port Cycle (CPU → USART)

$\overline{DTR}.\overline{RTS}$

t_{WC}

$\overline{WR}$　　t_{WW}　　t_{WD}

t_{DW}

DATA IN (D. B.)　　Don't Care　　Data Stable　　Don't Care

C/$\overline{D}$　　t_{AW}　　t_{WA}

$\overline{CS}$　　t_{AW}　　t_{WA}
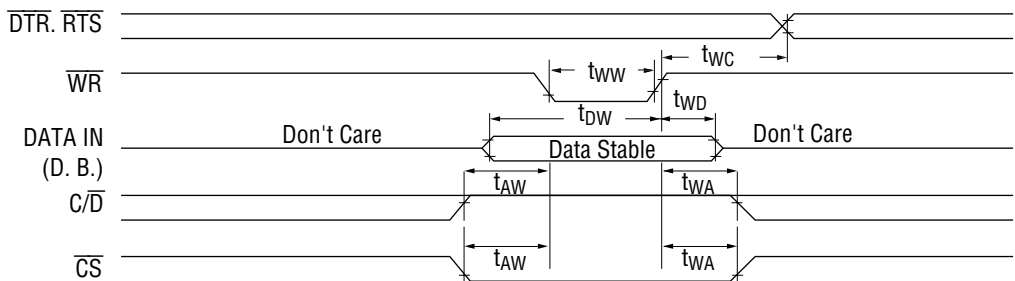
Read Control or Input Port Cycle (CPU ← USART)
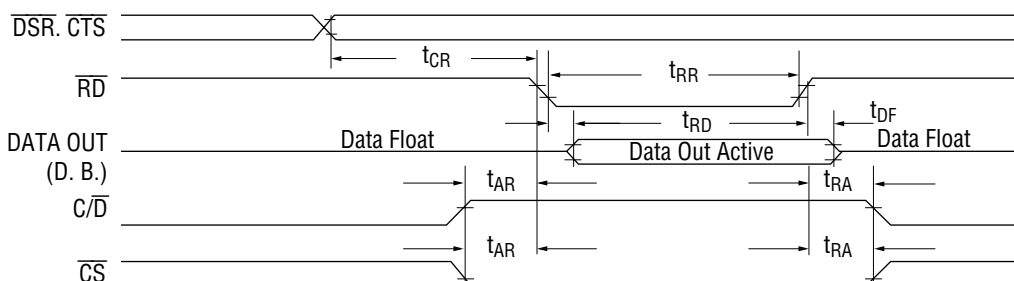
$\overline{DSR}.\overline{CTS}$

t_{CR}　　t_{RR}

$\overline{RD}$

t_{RD}　　t_{DF}

DATA OUT (D. B.)　　Data Float　　Data Out Active　　Data Float

C/$\overline{D}$　　t_{AR}　　t_{RA}
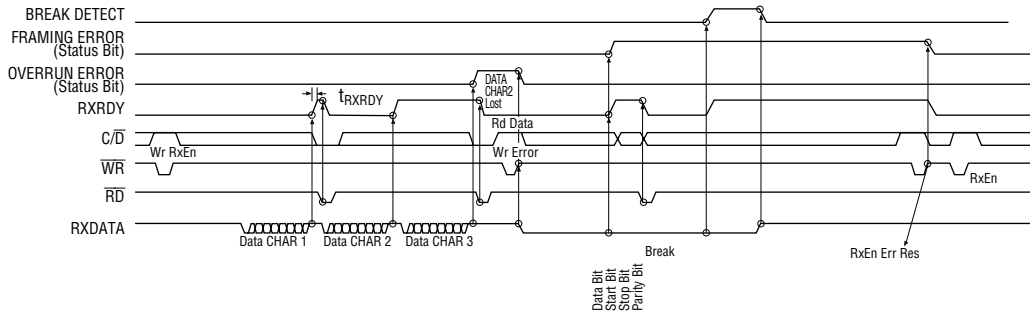
$\overline{CS}$　　t_{AR}　　t_{RA}

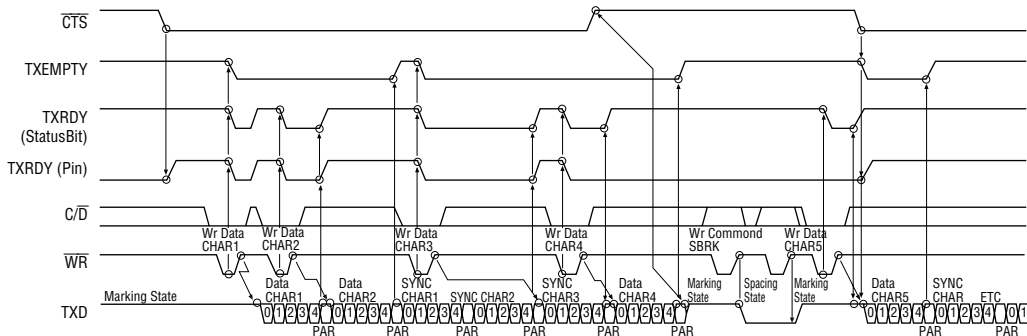## Transmitter Control and Flag Timing (ASYNC Mode)
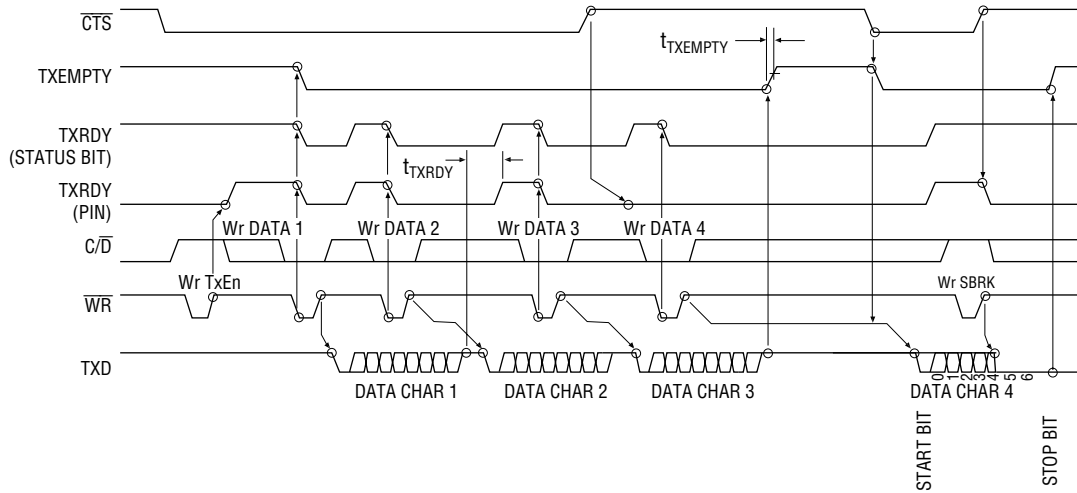
Note: The wave-form chart is based on the case of 7-bit data length + parity bit + 2 stop bit.

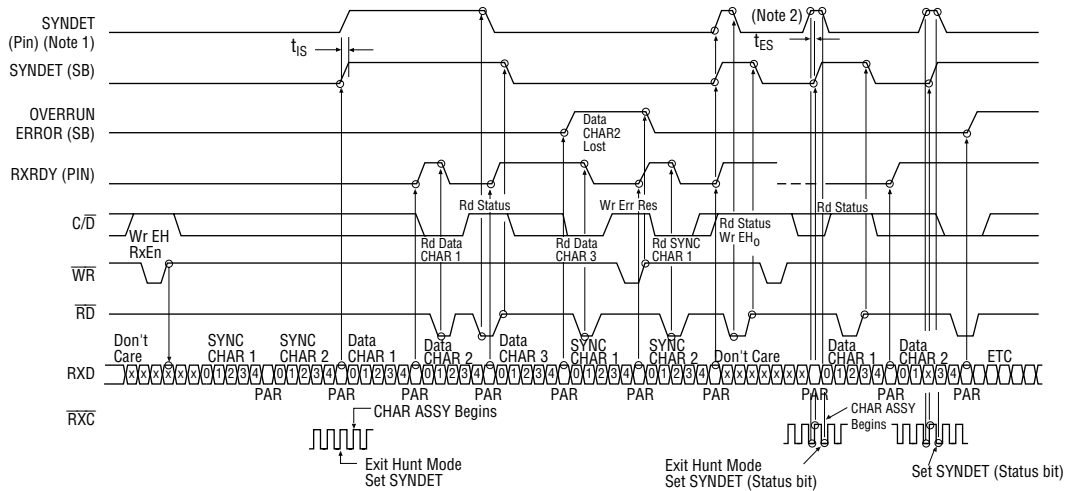## Receiver Control and Flag Timing (ASYNC Mode)

Note: The wave-form chart is based on the case of 7 data bit length + parity bit + 2 stop bit.

Transmitter Control and Flag Timing (SYNC Mode)

Note: The wave-form chart is based on the case of 5 data bit length + parity bit and 2 synchronous charactors.

Receiver Control and Flag Timing (SYNC Mode)

SYNDET (Pin) (Note 1)
SYNDET (SB)
OVERRUN ERROR (SB)
RXRDY (PIN)
C/D̄
W̄R̄
R̄D̄
RXD
R̄X̄C̄

t_{IS} t_{ES} (Note 2)

Rd Status   Wr Err Res   Rd Status   Rd Status Wr EH$_O$

Wr EH RxEn   Rd Data CHAR 1   Rd Data CHAR 3   Rd SYNC CHAR 1

Data CHAR2 Lost

Don't Care   SYNC CHAR 1   SYNC CHAR 2   Data CHAR 1   Data CHAR 2   Data CHAR 3   SYNC CHAR 1   SYNC CHAR 1   Don't Care   Data CHAR 1   Data CHAR 2   ETC

PAR   PAR   PAR   PAR   PAR   PAR   PAR   PAR   PAR

CHAR ASSY Begins   CHAR ASSY Begins

Exit Hunt Mode Set SYNDET   Exit Hunt Mode Set SYNDET (Status bit)   Set SYNDET (Status bit)

Note: 1. Internal Synchronization is based on the case of 5 data bit length + parity bit and 2 synchronous charactor.
2. External Synchronization is based on the case of 5 data bit length + parity bit.

Note: 1. Half-bit processing for the start bit
When the MSM82C51A-2 is used in the asynchronous mode, some problems are caused in the processing for the start bit whose length is smaller than the 1-data bit length. (See Fig. 1.)

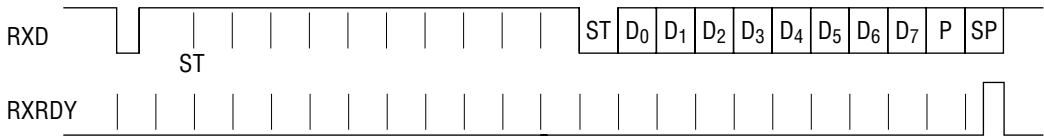| Start bit Length	Mode	Operation
Smaller than 7-Receiver Clock Length	×16	The short start bit is ignored. (Normal)
Smaller than 31-Receiver Clock Length	×64	The short start bit is ignored. (Normal)
8-Receiver Clock Length	×16	Data cannot be received correctly due to a malfunction.
32-Receiver Clock Length	×64	Data cannot be received correctly due to a malfunction.
9 to 16-Receiver Clock Length	×16	The bit is regarded as a start bit. (normal)
33 to 64-Receiver Clock Length	×64	The bit is regarded as a start bit. (normal)

2. Parity flag after a break signal is received (See Fig. 2.)
When the MSM82C51A-2 is used in the asynchrous mode, a parity flag may be set when the next normal data is read after a break signal is received.
A parity flag is set when the rising edge of the break signal (end of the break signal) is changed between the final data bit and the parity bit, through a RXRDY signal may not be outputted.
If this occurs, the parity flag is left set when the next normal dats is received, and the received data seems to be a parity error.

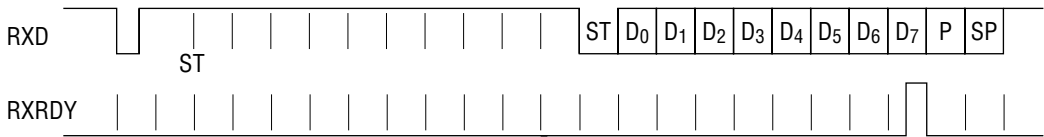**Half-bit Processing Timing Chart for the Start bit (Fig. 1)**

Normal Operation

RXD | ST | D_0 | D_1 | D_2 | D_3 | D_4 | D_5 | D_6 | D_7 | P | SP | ST | D_0 | D_1 | D_2 | D_3 | D_4 | D_5 | D_6 | D_7 | P | SP
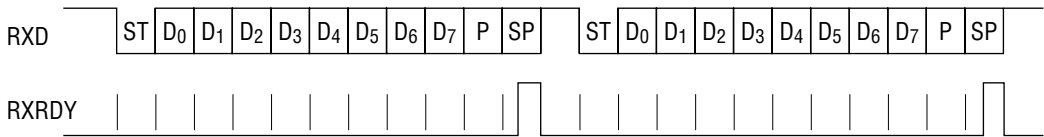
RXRDY

The Start bit Is Shorter Than a 1/2 Data bit

RXD

ST

ST | D_0 | D_1 | D_2 | D_3 | D_4 | D_5 | D_6 | D_7 | P | SP

RXRDY

The Start bit Is a 1/2 Data bit (A problem of MSM82C51A-2)

RXD

ST

ST | D_0 | D_1 | D_2 | D_3 | D_4 | D_5 | D_6 | D_7 | P | SP

RXRDY

A RXRDY signal is outputted during data reception due to a malfunction.

The Start bit Is Longer Than a 1/2 Data bit

RXD

ST

ST | D_0 | D_1 | D_2 | D_3 | D_4 | D_5 | D_6 | D_7 | P | SP

RXRDY
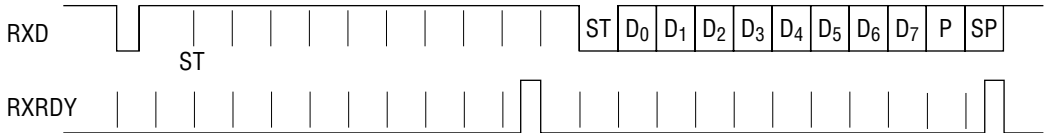
ST: Start bit
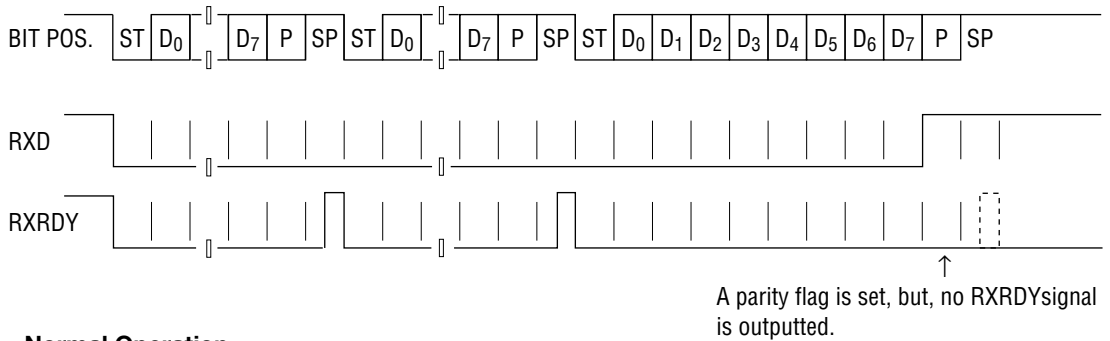SP: Stop bit
P: Parity bit
D_0 - D_7: Data bits

OKI Semiconductor   **MSM82C51A-2RS/GS/JS**

Break Signal Reception Timing and Parity Flag (Fig. 2)

Normal Operation

BIT POS. | ST | D$_0$ | | D$_7$ | P | SP | ST | D$_0$ | | D$_7$ | P | SP | ST | D$_0$ | D$_1$ | D$_2$ | D$_3$ | D$_4$ | D$_5$ | D$_6$ | D$_7$ | P | SP

RXD

RXRDY

No parity flag is set. and no RXRDY signal is outputted.

Bug Timing

BIT POS. | ST | D$_0$ | | D$_7$ | P | SP | ST | D$_0$ | | D$_7$ | P | SP | ST | D$_0$ | D$_1$ | D$_2$ | D$_3$ | D$_4$ | D$_5$ | D$_6$ | D$_7$ | P | SP

RXD

RXRDY

A parity flag is set, but, no RXRDYsignal is outputted.

Normal Operation

BIT POS. | ST | D$_0$ | | D$_7$ | P | SP | ST | D$_0$ | | D$_7$ | P | SP | ST | D$_0$ | D$_1$ | D$_2$ | D$_3$ | D$_4$ | D$_5$ | D$_6$ | D$_7$ | P | SP

RXD

RXRDY

A parity flag is set. and a RXRDY signal is outputted.
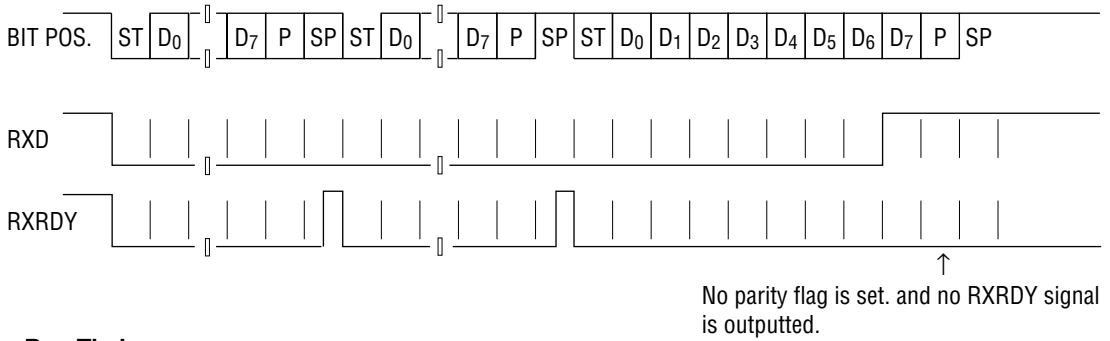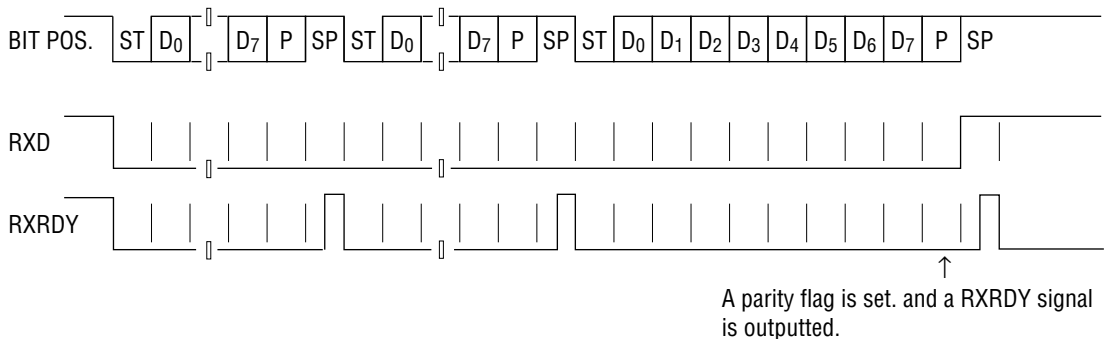
NOTICE ON REPLACING LOW-SPEED DEVICES WITH HIGH-SPEED DEVICES

The conventional low speed devices are replaced by high-speed devices as shown below.
When you want to replace your low speed devices with high-speed devices, read the replacement
notice given on the next pages.

High-speed device (New)	Low-speed device (Old)	Remarks
M80C85AH	M80C85A/M80C85A-2	8bit MPU
M80C86A-10	M80C86A/M80C86A-2	16bit MPU
M80C88A-10	M80C88A/M80C88A-2	8bit MPU
M82C84A-2	M82C84A/M82C84A-5	Clock generator
M81C55-5	M81C55	RAM.I/O, timer
M82C37B-5	M82C37A/M82C37A-5	DMA controller
M82C51A-2	M82C51A	USART
M82C53-2	M82C53-5	Timer
M82C55A-2	M82C55A-5	PPI

Differences between MSM82C51A and MSM82C51A-2

1) Manufacturing Process
These devices use a 3 μ Si-Gate CMOS process technology and have the same chip size.

2) Function
These devices have the same logics except for changes in AC characteristics listed in (3-2).

3) Electrical Characteristics
3-1) DC Characteristics

Parameter	Symbol	MSM82C51A	MSM82C51A-2
V_{OL} measurement conditions	I_{OL}	+2.0 mA	+2.5 mA
V_{OH} measurement conditions	I_{OH}	-400 μA	-2.5 mA

Although the output voltage characteristics of these devices are identical, but the measurement conditions of the MSM82C51A-2 are more restricted than the MSM82C51A.
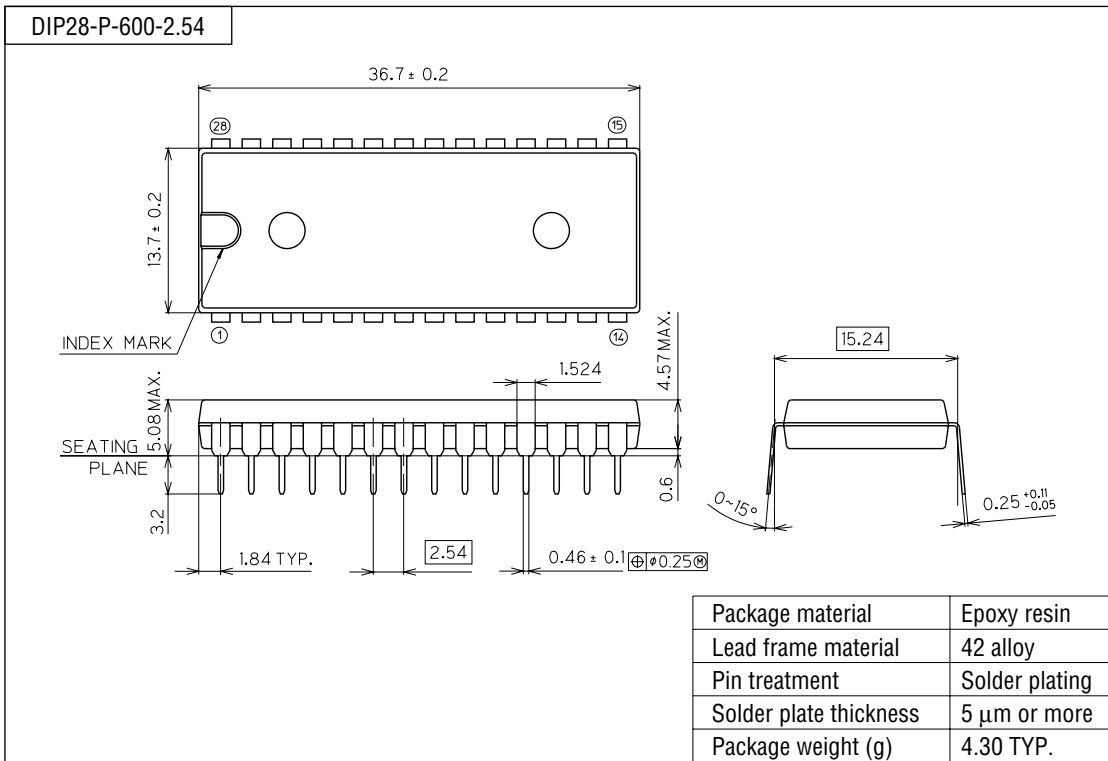
3-2) AC Characteristics

Parameter	Symbol	MSM82C51A	MSM82C51A-2
$\overline{RD}$ Pulse Width	t_{RR}	250 ns minimum	130 ns minimum
$\overline{RD}$ Rising to Data Difinition	t_{RD}	200 ns maximum	100 ns maximum
$\overline{RD}$ Rising to Data Float	t_{RF}	100 ns maximum	75 ns minimum
$\overline{WR}$ Pulse Width	t_{WW}	250 ns minimum	100 ns minimum
Data Setup Time for $\overline{WR}$ Rising	t_{DW}	150 ns minimum	100 ns minimum
Data Hold Time for $\overline{WR}$ Rising	t_{WD}	20 ns minimum	0 ns minimum
Master Clock Period	t_{CY}	250 ns minimum	160 ns minimum
Clock Low Time	$t_{\bar{\phi}}$	90 ns minimum	50 ns minimum
Clock High Time	t_{ϕ}	120 ns minimum t_{CY}-90 ns maximum	70 ns minimum t_{CY}-50 ns maximum

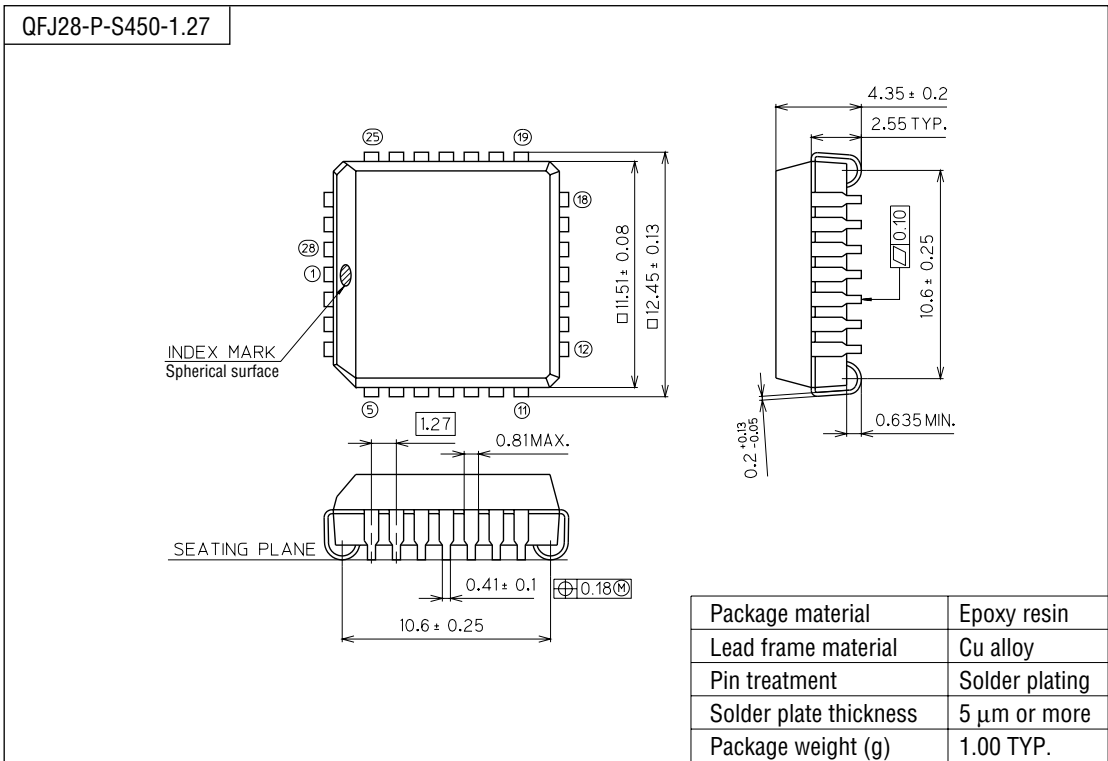As shown above, the MSM82C51A-2 satisfies the characteristics of the MSM82C51A.

OKI Semiconductor   **MSM82C51A-2RS/GS/JS**

PACKAGE DIMENSIONS

(Unit : mm)

DIP28-P-600-2.54

36.7 ± 0.2

13.7 ± 0.2

INDEX MARK

4.57MAX.

15.24

1.524

5.08 MAX.

SEATING PLANE

3.2

0~15°

0.25 +0.11 -0.05

0.6

1.84 TYP.

2.54

0.46 ± 0.1 ⊕ φ0.25 Ⓜ

Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	4.30 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).
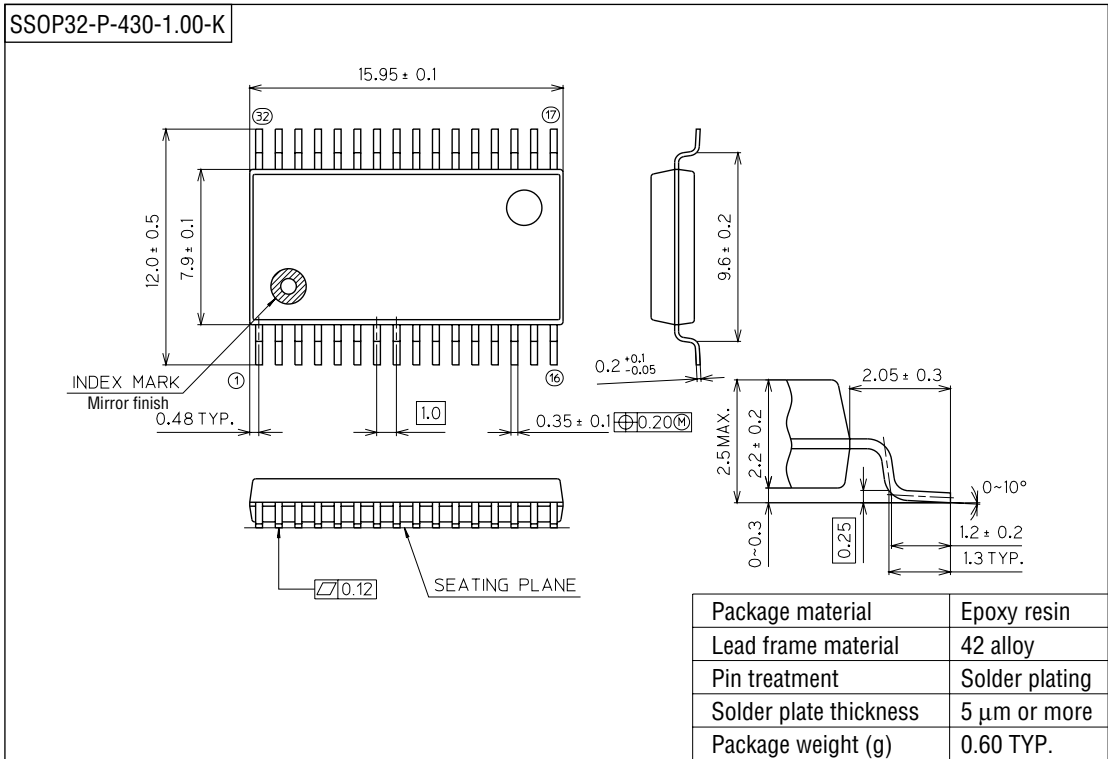
(Unit : mm)

QFJ28-P-S450-1.27

Package material	Epoxy resin
Lead frame material	Cu alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	1.00 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

SSOP32-P-430-1.00-K

Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.60 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

4) Notices on use

Note the following when replacing devices as the ASYNC pin is differently treated between the MSM82C84A and the MSM82C84A-5/MSM82C84A-2:

Case 1: When only a pullup resistor is externally connected to.
The MSM82C84A can be replaced by the MSM82C84A-2.

Case 2: When only pulldown resistor is externally connected to.
When the pulldown resistor is 8 kiloohms or less, the MSM82C84A can be replaced by the MSM82C84A-2.
When the pulldown resistor is greater than 8 kiloohms, use a pulldown resistor of 8 kiloohms or less.

Case 3: When an output of the other IC device is connected to the device.
The MSM82C84A can be replaced by the MSM82C84A-2 when the I_{OL} pin of the device to drive the $\overline{ASYNC}$ pin of the MSM82C84A-2 has an allowance of 100 μA or more.

HTTP //WWW.SENSOR-IC.COM/
HTTP //WWW.PC-PS.NET/
HTTP://WWW.SUNSTARE.COM/

E-MAIL   xjr5@163.com szss20@163.com
MSN: suns8888@hotmail.com
QQ: 195847376

1602
0755-83376549 83376489   83387030 83387016
0755-83376182 83338339   518033   (0)13902971329
2583   TEL/FAX
0755-83665529 25059422
132   3097
TEL 010-81159046 82615020 13501189838 FAX 010-82613476
668   2B35
TEL 021-28311762 56703037 13701955389 FAX 021-56703037
20   (   )
88   D23
TEL 029-81022619 13072977981 FAX:029-88789382
TEL: (0)13717066236
0755-83394033 13501568376