FEBL7048-01

OKI

Operation Manual for ML7048 Evaluation Board

3-Channel Single Rail Codec

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1. ML7048 EVALUATION BOARD

- This board evaluates the ML7048 (3-channel codec LSI).
- This board has a peripheral unit required to evaluate the ML7048 chip and facilitates evaluation of the device.
- See the ML7048 data sheet for more information on specifications and functions of the ML7048.

2. BOARD COMPONENTS

This evaluation board consists of the following:
- Evaluation board:..... 1 board
- Power cable:..... 1 cable
- Female connectors: ..... 1 set

3. EVALUATION CIRCUIT DIAGRAMS

Circuit diagrams of the evaluation board are on Pages 8 and 9. See them for jumper and external connections.

4. USING THE EVALUATION BOARD

4.1. Power Supplies

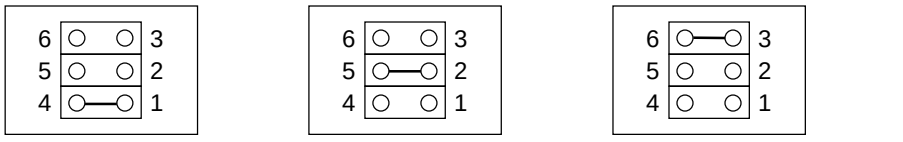
Connect the attached power cable to the evaluation board and supply the powers listed below to the board.
VDD1 (Red): +5 V power supply for the ML7048 device only
VDD2 (Red): +5 V power supply for operational amplifiers, etc.
VDD3 (Red): +5 V power supply for FPGA, ROM, crystal oscillator, etc.
GND1 (Black): Ground for the ML7048 device, operational amplifiers, etc.
GND2 (Black): Ground for FPGA, ROM, crystal oscillator, etc.
VSS (Blue): –5 V power supply for operational amplifiers

4.2. Jumpers

The evaluation board has ten jumpers — JP1 to JP10 — on it. Use them to connect the input and output signals to and from the ML7048 to one of the following: the BNC connector, the FPGA, or the flat cable connector.

- Jumping pins 1 and 4 (See Figure 1 (a).)
  This enables ML7048 signals to be directly input to and output from the BNC connector.
- Jumping pins 2 and 5 (See Figure 1 (b).)
  This enables transfer of ML7048 signals to be directly input to and output from the BNC connector through the FPGA.
  This setting enables the PCM codec tester (e.g. Anritu MS369B) to be used for evaluation of the ML7048.
- Jumping pins 3 and 6 (See Figure 1 (c).)
  This enables this evaluation board to be connected to an external evaluation board through the flat cable connector, which permits signal communications between these boards.

For relationship between ML7048 signals and jumpers, see Figure 4 (Evaluation Board Circuit Diagram 1).



(a) To connect ML7048 signals to the BNC

(b) To connect ML7048 signals to the FPGA

(c) To connect ML7048 signals to the flat cable connector

Figure 1 Jumper settings

4.3. Switches on the Evaluation Board

Table 1 Board switch functions

Switch		Function
SW1 to SW3	BCLK1 to BCLK3	**Transfer clock selection.** Selects a transfer clock by combining BCLK3, BCLK2, and BCLK1 states (see Table 2).
SW4 , SW5	CHSEL1, CHSEL2	**Channel 1/channel 2/channel 3 selection.** Selects a channel signal (CH1, CH2, or CH3) to be processed in the FPGA by combining CHSEL1 and CHSEL2 states (see Table 3).
SW6, SW9 SW10	TEST4, TEST2, TEST3	**LSI test control.** Controls the LSI test. For normal evaluation. Set TEST 2, TEST 3, and TEST 4 to the “L” level.
SW8	TEST1(PS)	**Parallel/serial control.** Selects either parallel or serial mode. Set TEST 1 to the “L” level to select parallel mode or to the “H” level to select serial mode.
SW7	MCKSEL	**Master clock selection.** Selects the master clock. Set this switch to the “L” level to select 12.288 MHz as the master clock or to the “H” level to select 15.360 MHz as the master clock.
SW11	PDN	**Power-down control.** Controls the power-down status. Set PDN to the “L” level to power down all circuits in the ML7048.
SW12 to SW14	PDN1, PDN2, PDN3	**Channel 1/channel 2/channel 3 power-down control.** Controls the Channel 1, Channel 2, and Channel 3 power-down. PDN1, PDN2, and PDN3 power-down control switches are for channel 1, channel 2, and channel 3, respectively. Set the PDN to the “H” level and the PDN1, PDN2, and PDN3 to the “L” level to go in power saving mode. (All analog circuits except the reference voltage generation circuit are being powered down.)

Table 2 Settings of transfer clocks

BCLK3	BCLK2	BCLK1	BCLK	
			MCKSEL “L”	MCKSEL “H”
0	0	0	2.048 MHz	1.536 MHz
0	0	1	1.024 MHz	768 kHz
0	1	0	512 kHz	384 kHz
0	1	1	256 kHz	192 kHz
1	0	0	128 kHz	96 kHz
1	0	1	64 kHz	—

Table 3 Selection of a channel

CHSEL1	CHSEL2	Channel
0	0	—
1	0	CH1
0	1	CH2
1	1	CH3

4.4. Flat Cable Connector

Use the flat cable connector to input the control signals from the outside or to output ML7048 signals to the outside. For signal assignment to the connector pins, see Figure 4 (Evaluation Board Circuit Diagram 1).

4.4.1. FPGA Interface

The evaluation board uses the ALTERA FLFX8000 programmable logic device to generate signals for controlling the ML7048. The FLFX8000 is an SRAM process and requires EPROMs to store configuration data. The FPGA generates transfer clocks and synchronous signals on the board and further has a FIFO function.

4.4.2. Signal assignment to FPGA pins

Table 4 Signal assignment to FPGA pins

Pin name	I/O	Description
MCK0	I	Master clock (12.288 MHz)
MCK1	I	Master clock (15.360 MHz)
BCLK1	I	Shift Clock Select signal
BCLK2	I	Shift Clock Select signal
BCLK3	I	Shift Clock Select signal
CHSEL1	I	Channel Select signal
CHSEL2	I	Channel Select signal
PDN	I	Power-Down Control signal
TEST1	I	Parallel/Serial Control signal
TEST2	I	Test Control signal 2
TEST4	I	Test Control signal 3
DOUT1	I	PCM signal input from the ML7048 on channel 1
DOUT2	I	PCM signal input from the ML7048 on channel 2
DOUT3	I	PCM signal input from the ML7048 on channel 3
DIN1	O	PCM signal output to the ML7048 on channel 1
DIN2	O	PCM signal output to the ML7048 on channel 2
DIN3	O	PCM signal output to the ML7048 on channel 3
RSYNC	O	Receive SYNC signal
XSYNC	O	Transmit SYNC signal
MCKSEL	I	Master Clock Select signal
MCK	O	Master clock (12.288 MHz or 15.360 MHz)
BCLK	O	PCM signal shift clock
PCMIN	I	PCM signal input
PCMOUT	O	PCM signal output
LMFRM	O	Level meter frame
OSCFRM	O	Oscillator frame

4.4.3. Timing diagrams

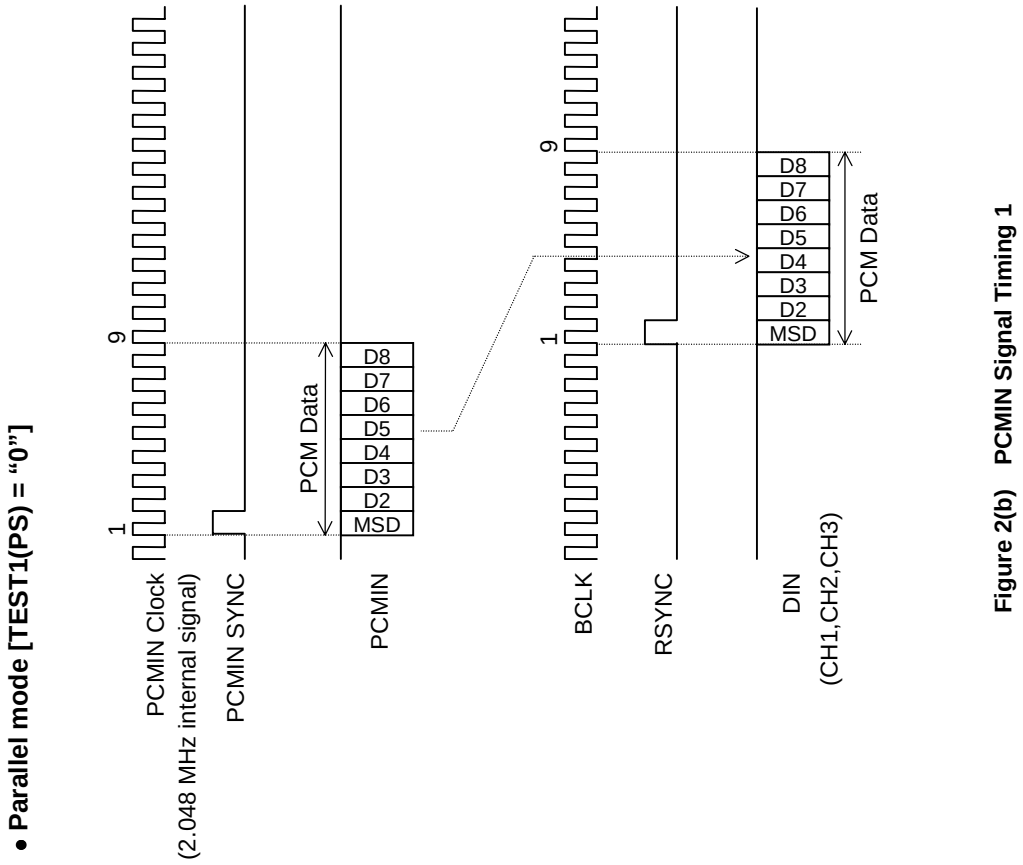


Figure 2(b) PCMIN Signal Timing 1

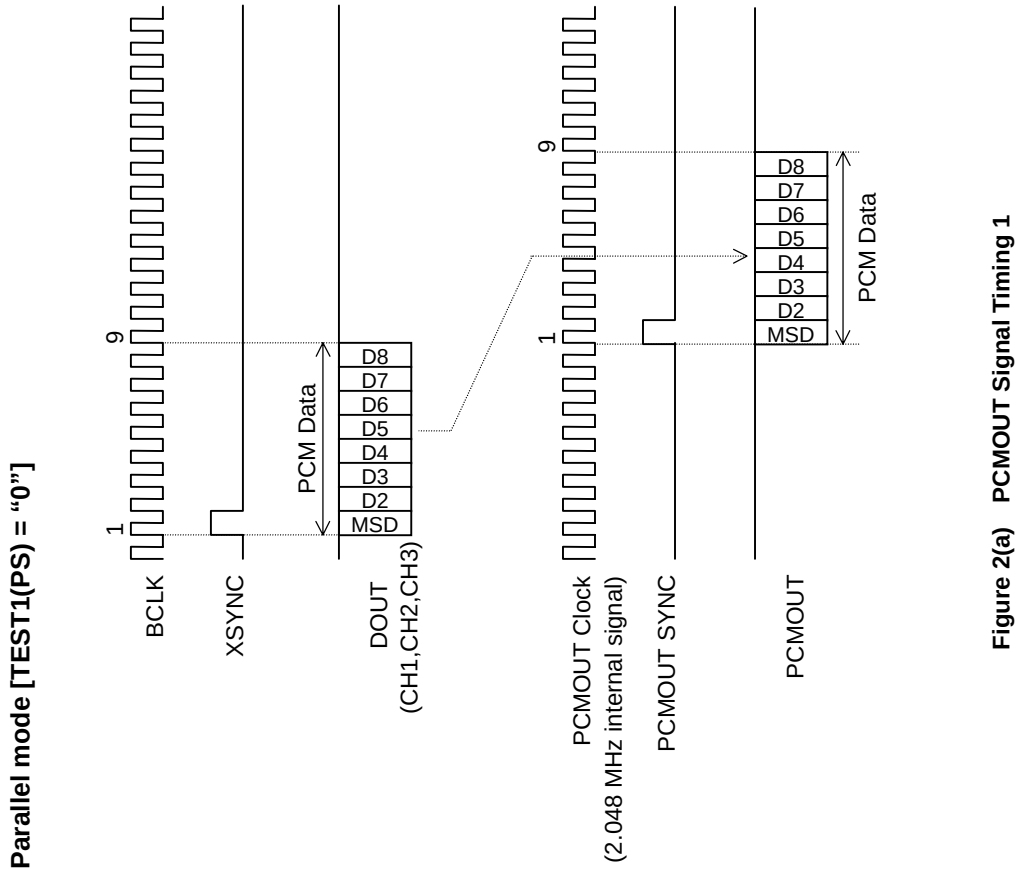


Figure 2(a) PCMOUT Signal Timing 1

● **Serial mode [TEST1(PS) = "1"]**

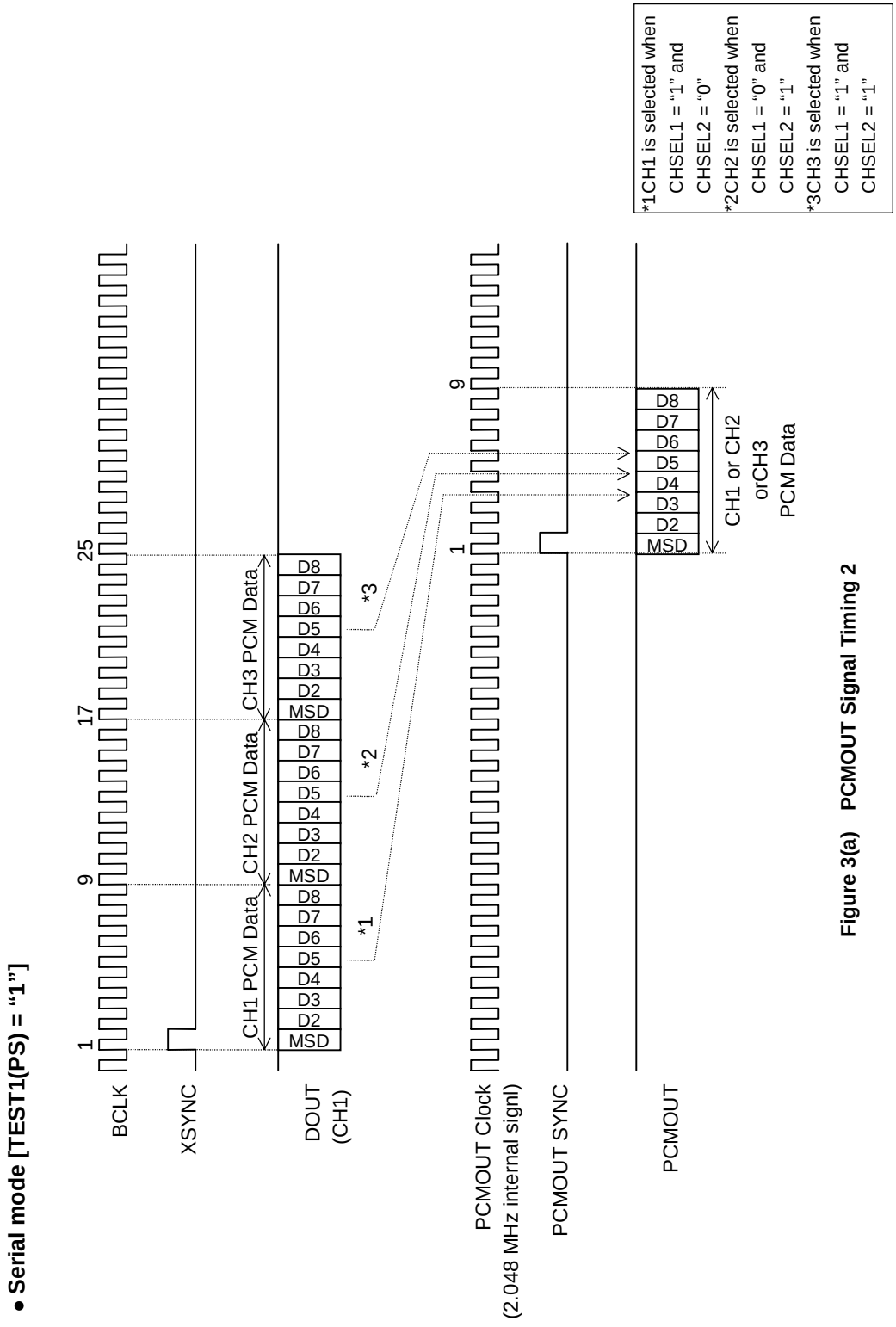


Figure 3(a) PCMOUT Signal Timing 2

• **Serial mode [TEST1(PS) = “1”]**

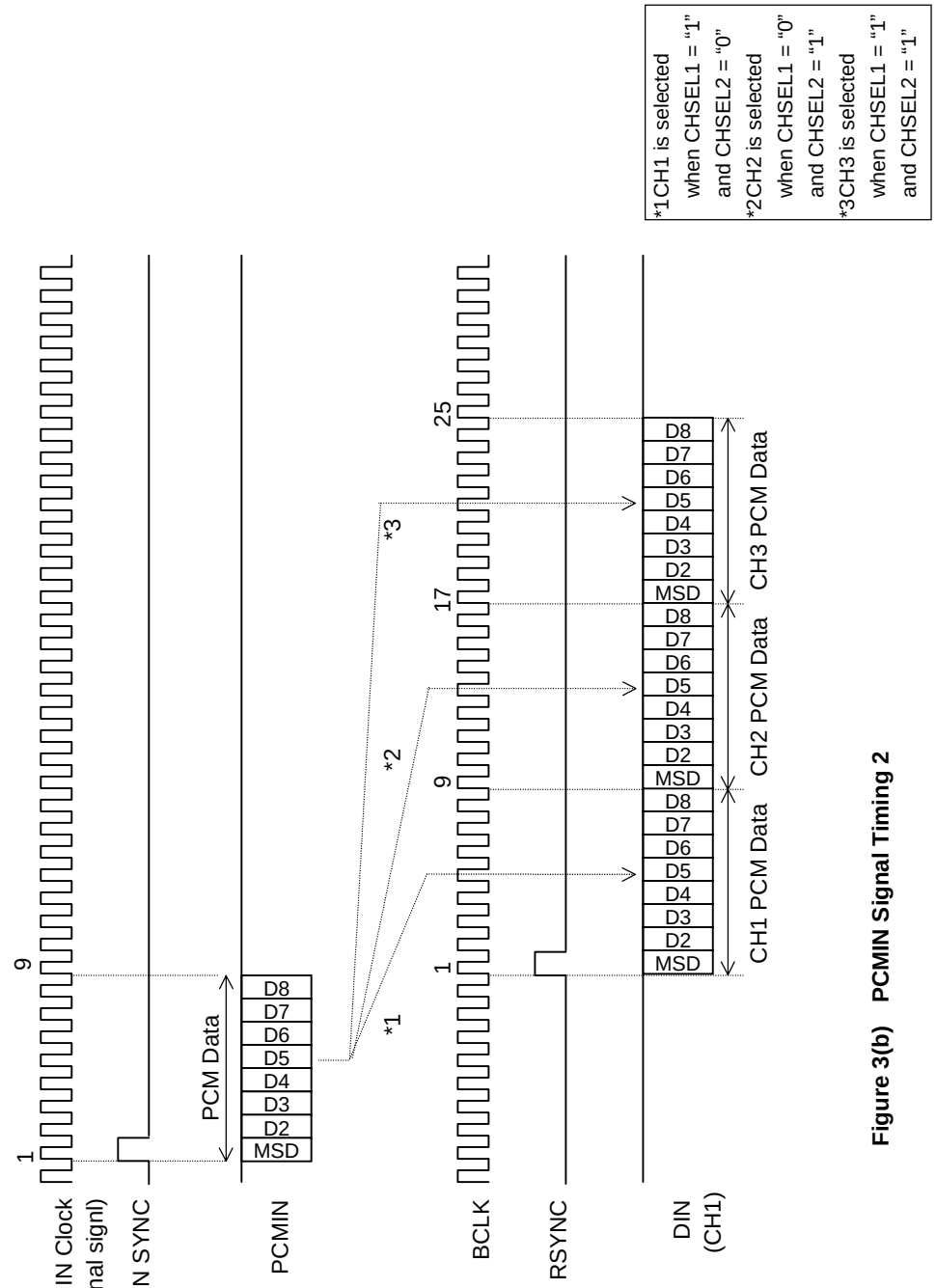


Figure 3(b) PCMIN Signal Timing 2

5. EVALUATION BOARD CIRCUIT DIAGRAM

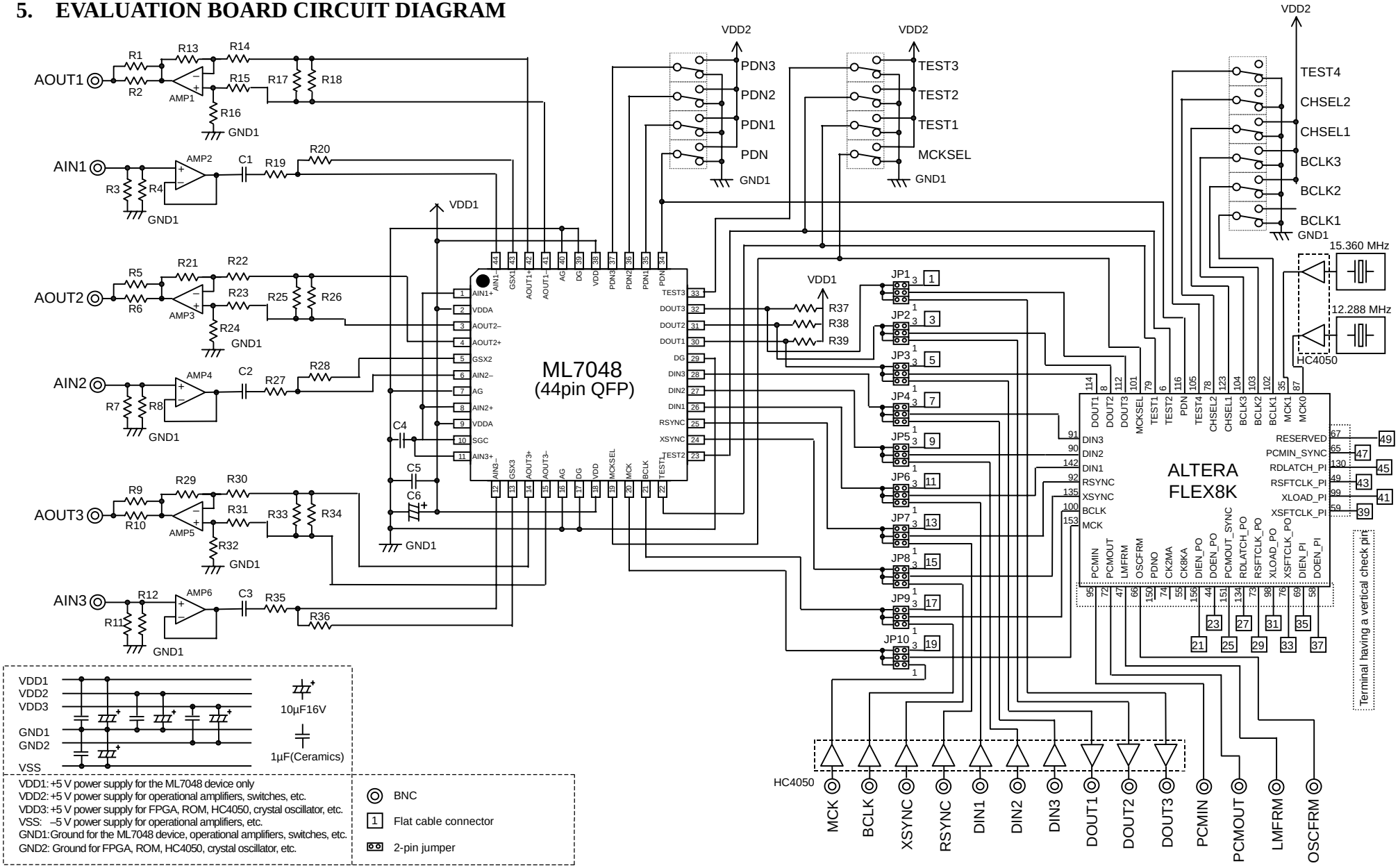
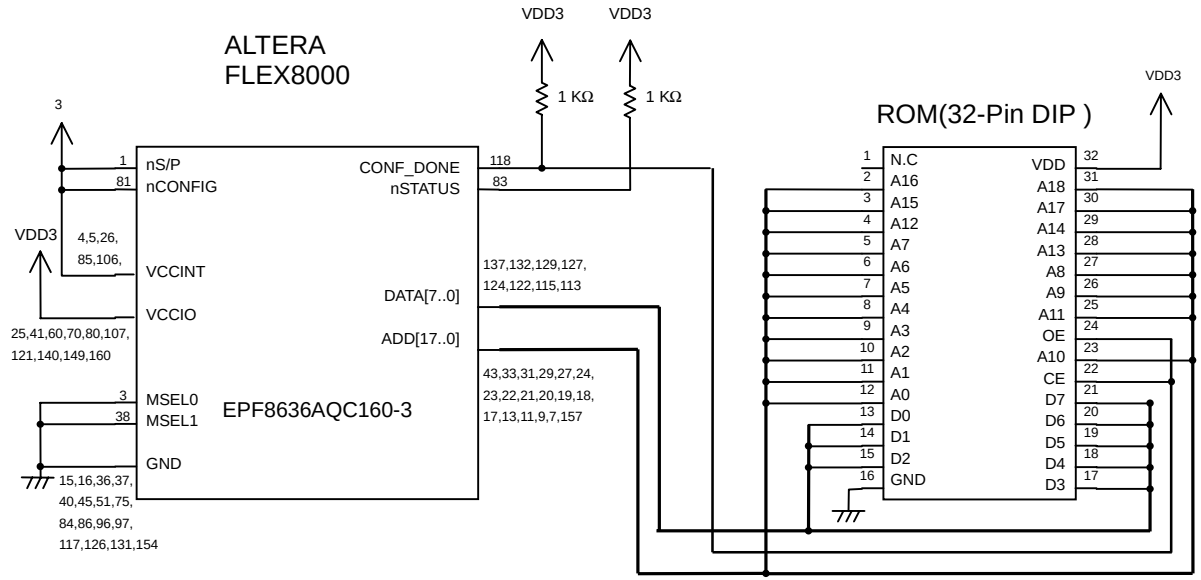


Figure 4 Evaluation Board Circuit Diagram 1



Parts table

Resistor		Capacitor		Amplifier	
Symbol	Value (Ω)	Symbol	Value (F)	Symbol	Part number
R1,R2,R3,R4	1.2k	C1	1µ	AMP1	HA17458
R5,R6,R7,R8	1.2k	C2	1µ	AMP2	HA17458
R9,R10,R11,R12	1.2k	C3	1µ	AMP3	HA17458
R13,R16	10k	C4	1µ	AMP4	HA17458
R17,R18	1.2k	C5	1µ	AMP5	HA17458
R14,R15,R19,R20	20k	C6	10µ(T)	AMP6	HA17458
R21,R24	10k				
R25,R26	1.2k				
R22,R23,R27,R28	20k				
R29,R32	10k				
R33,R34	1.2k				
R30,R31,R35,R36	20k				
R37,R38,R39	500				

(T) indicates a tantalum electrolytic capacitor.
The other capacitors are laminated ceramic capacitors.

Figure 5 Evaluation Board Circuit Diagram 2

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