FEUL63182A-02

OKI

MSM63182A/184A/188A
User's Manual

CMOS 4-bit microcontroller

SECOND EDITION

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Preface

This manual describes the hardware of Oki-original CMOS 4-bit microcontrollers MSM63182A, MSM63184A, and MSM63188A (hereinafter called MSM63180 family).

Refer to the “nX-4/250, 300 Core Instruction Manual” for details of the 4-bit CPU core nX-4/250 which is built in MSM63180 family devices.

The MSM63180 family-related manuals are shown below.

- nX-4/250, 300 Core Instruction Manual:
  Describes the base architecture and instruction set of nX-4/250 core and nX-4/300 core.

- SASM63K User’s Manual:
  Describes the structured assembler operation manual and assembler language specification.

- EASE63180 User's Manual:
  Describes the hardware of the emulator.

- DT63K Debugger/DTS63K Simulator User’s Manual:
  Describes the debugger commands and the hardware of the simulator.

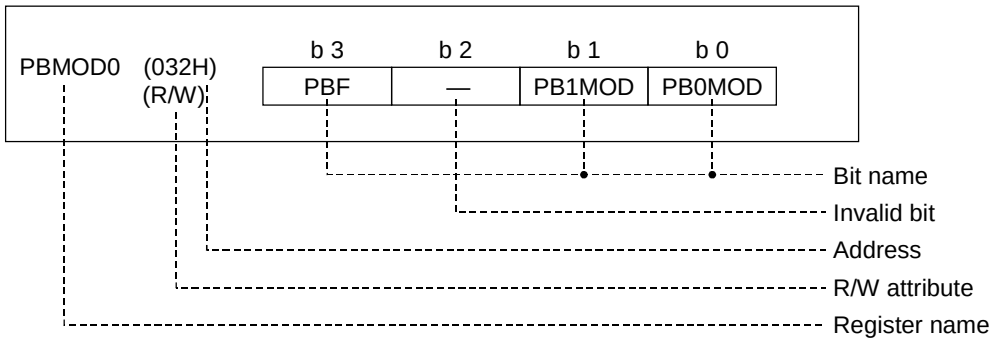
This document is subject to change without notice.

Notation

Classification	Notation	Description
■ Numeric value	xxh, xxH	Represents a hexadecimal number.
	xxb	Represents a binary number.
■ Unit	word, W	1 word = 16 bits
	byte, B	1 byte = 2 nibbles = 8 bits
	nibble, N	1 nibble = 4 bits
	maga-, M	10^6
	kilo-, K	$2^{10} = 1024$
	kilo-, k	$10^3 = 1000$
	milli-, m	10^{-3}
	micro-, µ	10^{-6}
	nano-, n	10^{-9}
	second, s (lower case)	second
	KB	1 KB = 1 kilobyte = 1024 bytes
	MB	1 MB = 1 megabyte = 2^{20} bytes = 1,048,576 bytes
■ Symbol	⚠ Note:	Gives more information about mistakable items.
	M182A	A chapter or page with this symbol describes the MSM63182A.
	M184A	A chapter or page with this symbol describes the MSM63184A.
	M188A	A chapter or page with this symbol describes the MSM63188A.
■ Terminology	"H" level	Indicates high side voltage signal levels V_{IH} and V_{OH} as specified by the electrical characteristics.
	"L" level	Indicates low side voltage signal levels V_{IL} and V_{OL} as specified by the electrical characteristics.

■ Register description

Invalid bit : When read, a value of "1" is always obtained. Write operations are invalid.
R/W attribute : "R" indicates data can be read and "W" indicates data can be written.



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Chapter 7 Clock Generator Circuit (OSC)

Chapter 8 Time Base Counter (TBC)

Chapter 9 Timers (TIMER)

Chapter 20 Battery Low Detect Circuit (BLD)

Chapter 21 Backup Circuit (BACKUP)

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Chapter 1

Overview

Chapter 1 Overview

1.1 Overview

The MSM63182A, MSM63184A, and MSM63188A are CMOS 4-bit microcontrollers, which ensure 0.9 V operation.

With the internal dot-matrix LCD drivers, these devices are best suited to such applications as game machines, toys, and watches that have a liquid crystal display.

The MSM63182A, MSM63184A, and MSM63188A are M63182A series mask ROM-version products of OLMS-63K family, which employs Oki's original CPU core nX-4/250.

1.2 Features

The MSM63182A, MSM63184A, and MSM63188A have the following features.

a. Extensive instruction set
- 439 instructions
  Transfer, rotate, increment/decrement, arithmetic operations, compare, logic operations, mask operations, bit operations, ROM table reference, external memory transfer, stack operations, flag operations, jump, conditional branch, call/return, control

b. Wide variety of addressing modes
- 4 types of data memory indirect addressing modes with current bank register, extra bank register, HL register and XY register
- Data memory bank internal direct addressing mode

c. Processing speed
- 2 clocks per machine cycle, with most instructions executed in 1 machine cycle
- Minimum instruction execution time: 61 μs (@ 32.768 kHz system clock)
  1 μs (@ 2 MHz system clock)

d. Clock generation circuit
- Low-speed clock:
  Crystal oscillation (32.768 kHz)
- High-speed clock:
  Ceramic oscillation (2 MHz max. when not using backup) or RC oscillation (1 MHz max. when not using backup) selected with software

e. Program memory space
- MSM63182A: 4K words
- MSM63184A: 8K words
- MSM63188A: 16K words
- Basic instruction length 16 bits/1 word

f. Data memory space
- MSM63182A: 384 nibbles
- MSM63184A: 640 nibbles
- MSM63188A: 3584 nibbles

g. External data memory space
- 64 Kbytes (expandable by the use of I/O ports)

h. Stack level

	Call stack level	Register stack level
MSM63182A	8	16
MSM63184A	8	16
MSM63188A	16	16

i. Ports

- Input ports
  Selectable as input with pull-up resistance/input with pull-down resistance/high-impedance input
- Output ports
  Selectable as P-channel open drain output/N-channel open drain output/CMOS output/high-impedance output
- Input/output ports
  Selectable as input with pull-up resistance/input with pull-down resistance/high-impedance input
  Selectable as P-channel open drain output/N-channel open drain output/CMOS output/high-impedance output
- Can be interfaced with external peripherals that use a different power supply than this device uses.
- Number of ports:

	Input ports	Output ports	I/O ports
MSM63182A	2 ports × 4 bits	4 ports × 4 bits	3 ports × 4 bits
MSM63184A	2 ports × 4 bits	4 ports × 4 bits	5 ports × 4 bits
MSM63188A	2 ports × 4 bits	6 ports × 4 bits	6 ports × 4 bits

j. Buzzer function (MSM63182A/MSM63184A only)

- Buzzer output: 0.946 kHz to 5.461 kHz (15 steps)
- Buzzer output modes: Intermittent tone 1/tone 2, single tone, continuous tone

k. Melody output function (MSM63188A only)

- Melody sound frequency: 529 to 2979 Hz
- Tone length: 63 varieties
- Tempo: 15 varieties
- Melody data: Stored in the program memory
- Buzzer driver signal output: 4 kHz

l. LCD driver

- Number of segments:
  MSM63182A: 512 segments max. (32 seg. × 16 com.)
  MSM63184A: 640 segments max. (40 seg. × 16 com.)
  MSM63188A: 1024 segments max. (64 seg. × 16 com.)
- 1/1 to 1/16 duty
- 1/4 or 1/5 bias
- Selectable as all-on mode/all-off mode/power down mode/normal display mode
- Adjustable contrast

m. Multiplier/divider circuits (MSM63188A only)
- Multiplier 8 bit × 8 bit = 16 bit
- Divider 16 bit/8 bit = 16 bit... 8 bit

n. Reset function
- Reset through RESET pin
- Power-on reset
- Reset to low-speed oscillation halt

o. Battery check
- Low-voltage supply check
- Judgment voltage
  Selectable as 1.05 ±0.10 V, 1.30 ±0.15 V, 2.20 ±0.20 V, or 2.80 ±0.30 V

p. Power supply backup
- Backup circuit (voltage multiplier) enables operation at 0.9 V minimum

q. Timers, counters
- 8-bit timer × 4 (MSM63188A only)
  Selectable as auto-reload mode/capture mode/clock frequency measurement mode
- Watchdog timer × 1
  Has an overflow cycle of 2 seconds.
- 100 Hz timer × 1
  1/100 sec. measurement possible
- 15-bit time base counter × 1
  1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, 64 Hz, 128 Hz signals can be read

r. Serial port (MSM63188A only)
- Mode: Selectable as UART mode/synchronous mode
- UART communication speed: 1200 bps, 2400 bps, 4800 bps, 9600 bps
- Clock frequency in synchronous mode: 32.768 kHz (internal clock mode), external clock frequency
- Data length: 5 to 8 bits

s. Shift register (MSM63184A only)
- Shift clock: 1 CLK (system clock) or 1/2 CLK, external clock
- Data length: 8 bits

t. Interrupt causes

	External causes	Internal causes
MSM63182A	2	6
MSM63184A	3	7
MSM63188A	4	13

u. Shipping products

	Package	Product name
MSM63182A	• 128-pin flat package (128QFP) QFP128-P-1420-0.50-K	MSM63182A-xxxGS-K
	• Chip (107 pads)	MSM63182A-xxx
MSM63184A	• 128-pin flat package (128QFP) QFP128-P-1420-0.50-K	MSM63184A-xxxGS-K
	• Chip (123 pads)	MSM63184A-xxx
MSM63188A	• 176-pin flat package (176LQFP) LQFP176-P-2424-0.50-BK	MSM63188A-xxxGS-BK
	• Chip (159 pads)	MSM63188A-xxx (xxx denotes the code number.)

v. Power supply voltage

- When backup used: 0.9 to 2.7 V (when the low-speed clock is operating)
  1.2 to 2.7 V (operating frequency: 300 to 500 kHz)
  1.5 to 2.7 V (operating frequency: 200 kHz to 1 MHz)
- When backup not used: 1.8 to 5.5 V (operating frequency: 300 to 500 kHz)
  2.2 to 5.5 V (operating frequency: 300 kHz to 1 MHz)
  2.7 to 5.5 V (operating frequency: 200 kHz to 2 MHz)

Table 1-1 Functions List

Function		Symbol	Interrupt	MSM63182A	MSM63184A	MSM63188A	Page
ROM (16 bits)		ROM	—	4064	8160	16352	2-9
RAM (4 bits)		RAM	—	384	640	3584	2-10
STACK RAM	Call	STACK	—	8	8	16	2-6
	Register			16	16	16	2-7
System reset generation circuit		RST	—	●	●	●	3-2
MSM63182A interrupt		lNT182	—	●	—	—	4-1
MSM63184A interrupt		NT184	—	—	●	—	5-1
MSM63188A interrupt		lNT188	—	—	—	●	6-1
Clock generation circuit		OSC	—	●	●	●	7-1
Time base counter		TBC	4	●	●	●	8-1
Timer		TIMER	4	—	—	●	9-1
100 Hz timer counter		100HzTC	1	●	●	●	10-1
Watchdog timer		WDT	1	●	●	●	11-1
Port 0 (I)		P0	1	●	●	●	12-2
Port 1 (I)		P1		●	●	●	
Port 2 (O)		P2	—	—	—	●	12-10
Port 3 (O)		P3	—	—	—	●	
Port 4 (O)		P4	—	●	●	●	12-14
Port 5 (O)		P5	—	●	●	●	
Port 6 (O)		P6	—	●	●	●	
Port 7 (O)		P7	—	●	●	●	
Port 8 (I/O)		P8	1	●	●	●	12-22
Port 9 (I/O)		P9	—	●	●	●	
Port A (I/O)		PA	—	●	●	●	
Port B (I/O)		PB	1	—	—	●	12-31
Port C (I/O)		PC	1	—	—	●	12-38
Port D (I/O)		PD	—	—	●	●	12-46
Port E (I/O)		PE	1	—	●	—	12-50
External memory interface		EXTMEM	—	●	●	●	13-1
Melody driver		MELODY	1	—	—	●	14-1
Buzzer driver		BUZZER	—	●	●	—	15-1
Serial port		SIO	2	—	—	●	16-1
Shift register		SFT	1	—	●	—	17-1
LCD driver	COM	LCD	—	16	16	16	18-1
	SEG			32	40	64	
Display register		DSPR	—	128	160	256	18-8
Multiplication/Division		MULDIV	—	—	—	●	19-1
Bias generation circuit		BIAS	—	●	●	●	18-3
Battery low detection circuit		BLD	—	●	●	●	20-1
Backup circuit		BACKUP	—	●	●	●	21-1

1.3 Block Diagram

The Figures 1-1, 1-2, and 1-3 show the block diagrams of MSM63182A, MSM63184A, MSM63188A, respectively.

Asterisks (*) indicate the port secondary functions. Signal names enclosed by chain lines (-·-·-) indicate interface signals of the V_{DDI} power supply system.

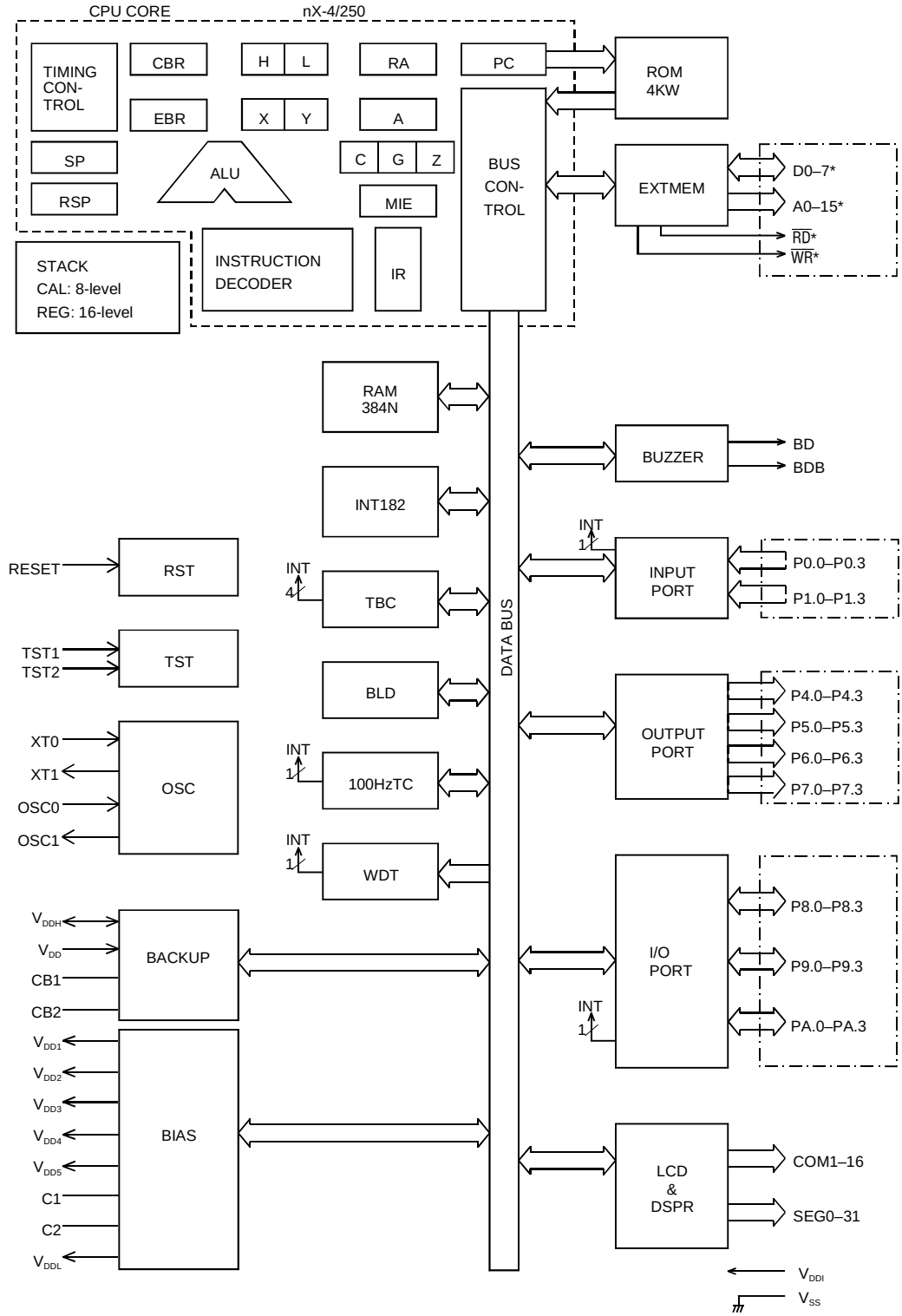


Figure 1-1 MSM63182A Block Diagram

Asterisks (*) indicate the port secondary functions. Signal names enclosed by chain lines (----) indicate interface signals of the V_{DDI} power supply system.

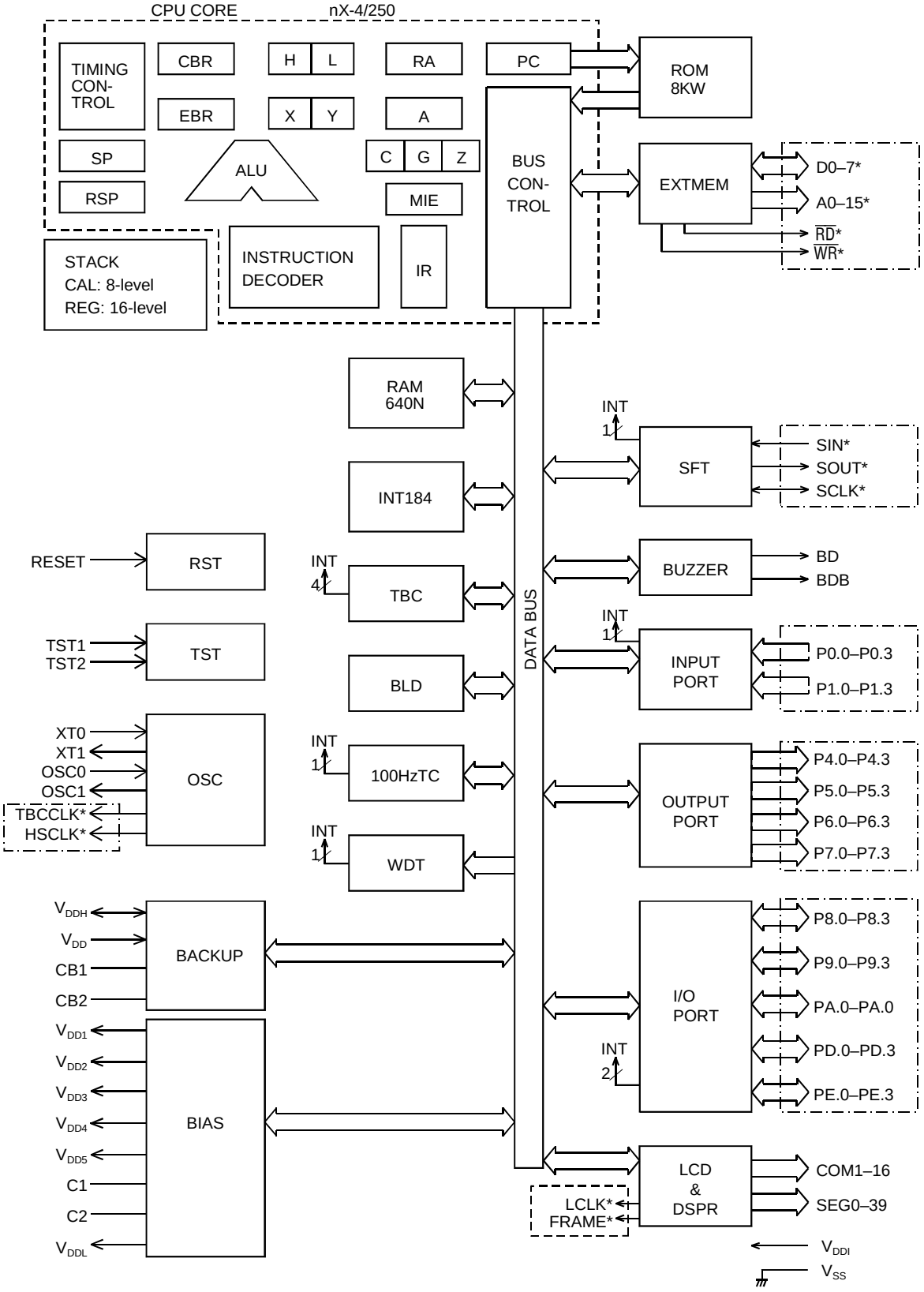


Figure 1-2 MSM63184A Block Diagram

Asterisks (*) indicate the port secondary functions. Signal names enclosed by chain lines (┈┈) indicate interface signals of the V_{DDI} power supply system.

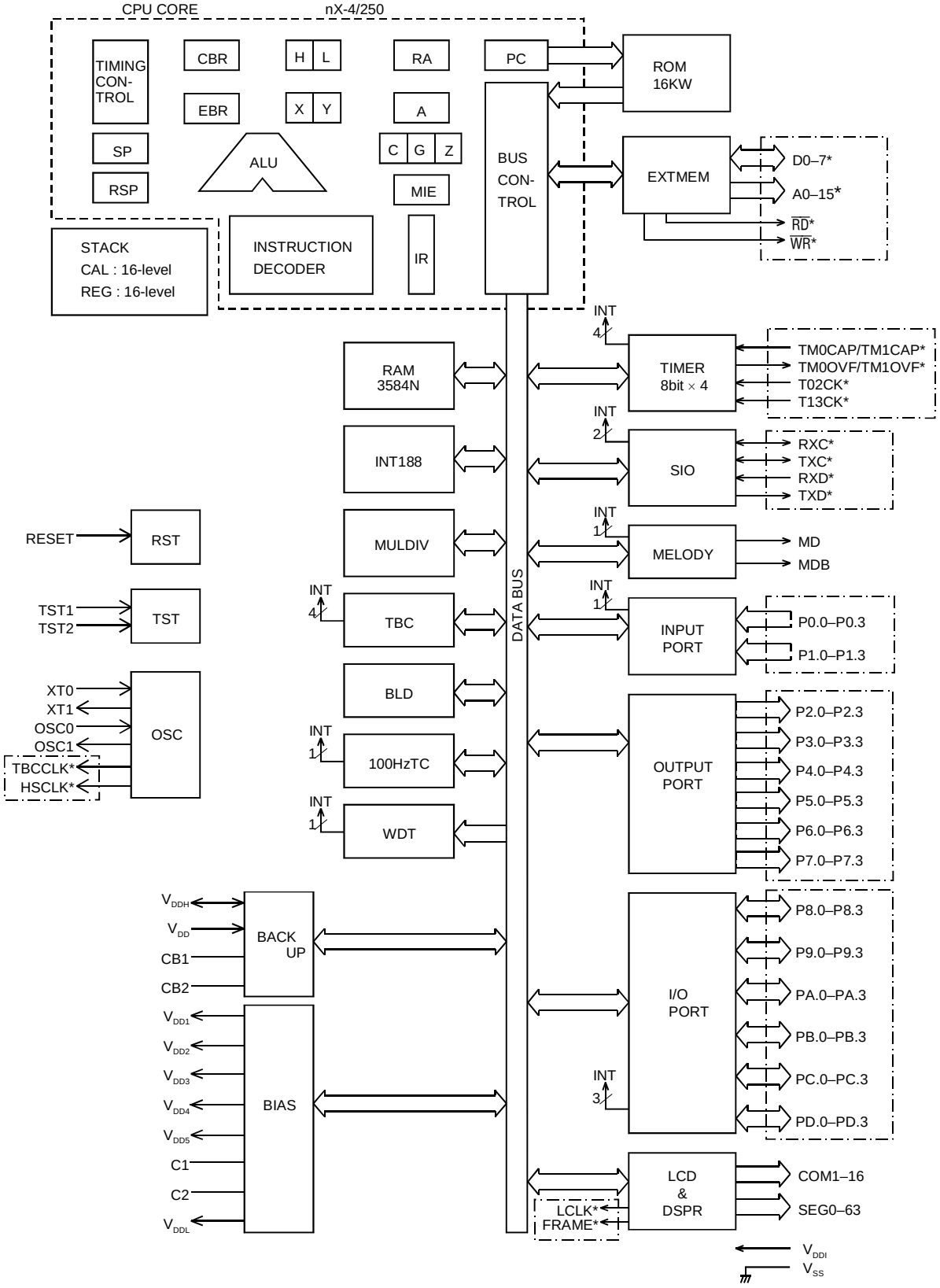


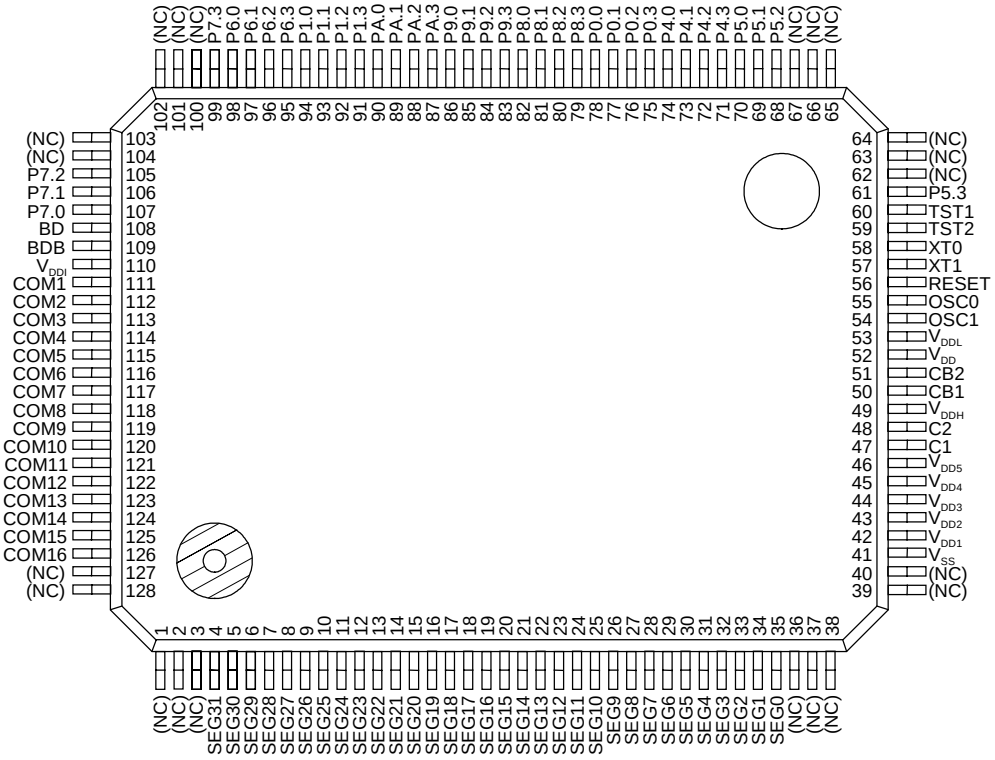
Figure 1-3 MSM63188A Block Diagram

1.4 Pin Configuration

1.4.1 MSM63182A pin configuration

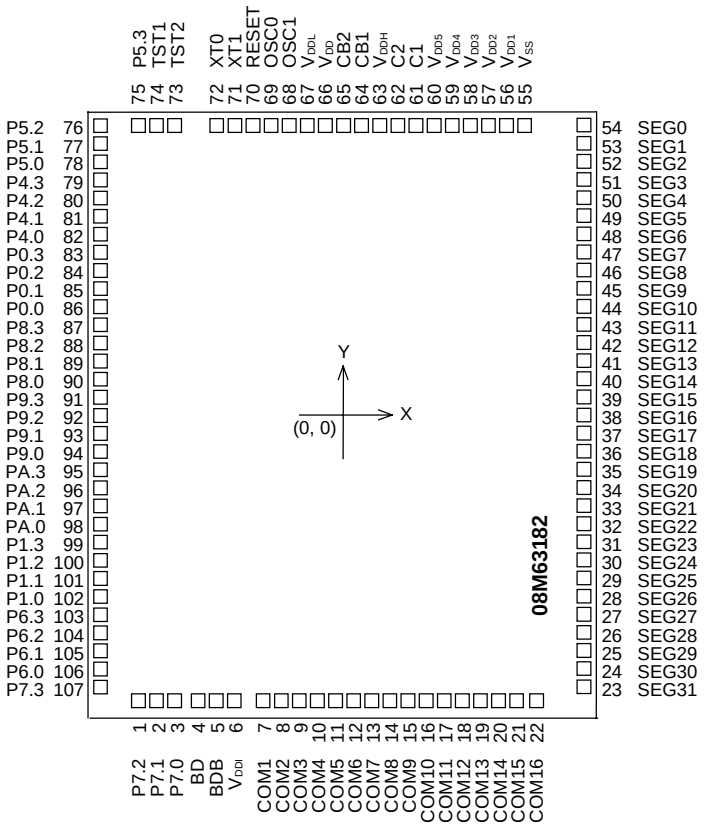
The MSM63182A pin configuration, chip pin configuration, and pad coordinates are shown in the Figures 1-4 and 1-5, and the Table 1-2, respectively.

Pins marked as NC are unused pins, which are left unconnected (open).



128-Pin Plastic FQP

Figure 1-4 MSM63182A-xxxGS-K Pin Configuration (Top View)



- Chip size : 4.44 mm × 4.92 mm
- Chip thickness : 350 µm (Typ.)
- Coordinate origin : center of chip
- Pad hole size : 100 µm × 100 µm
- Pad size : 110 µm × 110 µm
- Minimum pad pitch : 140 µm

Note: The chip substrate voltage is V_{SS}.

Figure 1-5 MSM63182A Chip Pin Configuration (Top View)

Table 1-2 MSM63182A Pad Coordinates

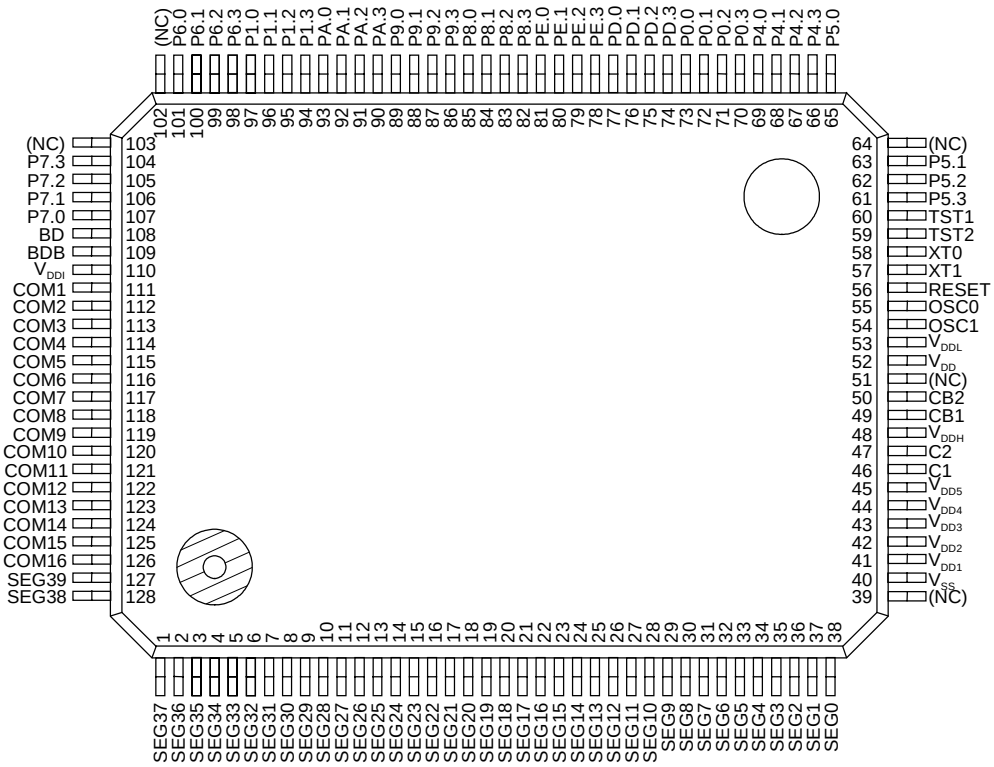
Center of chip: X = 0, Y = 0

Pad No.	Pad Name	X (μm)	Y (μm)	Pad No.	Pad Name	X (μm)	Y (μm)	Pad No.	Pad Name	X (μm)	Y (μm)
1	P7.2	–1547	–2265	37	SEG17	2075	–210	73	TST2	–1247	2265
2	P7.1	–1407	–2265	38	SEG16	2075	–70	74	TST1	–1387	2265
3	P7.0	–1267	–2265	39	SEG15	2075	70	75	P5.3	–1548	2265
4	BD	–1090	–2265	40	SEG14	2075	210	76	P5.2	–2075	2170
5	BDB	–950	–2265	41	SEG13	2075	350	77	P5.1	–2075	2030
6	V_{DDI}	–810	–2265	42	SEG12	2075	490	78	P5.0	–2075	1890
7	COM1	–630	–2265	43	SEG11	2075	630	79	P4.3	–2075	1750
8	COM2	–490	–2265	44	SEG10	2075	770	80	P4.2	–2075	1610
9	COM3	–350	–2265	45	SEG9	2075	910	81	P4.1	–2075	1470
10	COM4	–210	–2265	46	SEG8	2075	1050	82	P4.0	–2075	1330
11	COM5	–70	–2265	47	SEG7	2075	1190	83	P0.3	–2075	1190
12	COM6	70	–2265	48	SEG6	2075	1330	84	P0.2	–2075	1050
13	COM7	210	–2265	49	SEG5	2075	1470	85	P0.1	–2075	910
14	COM8	350	–2265	50	SEG4	2075	1610	86	P0.0	–2075	770
15	COM9	490	–2265	51	SEG3	2075	1750	87	P8.3	–2075	630
16	COM10	630	–2265	52	SEG2	2075	1890	88	P8.2	–2075	490
17	COM11	770	–2265	53	SEG1	2075	2030	89	P8.1	–2075	350
18	COM12	910	–2265	54	SEG0	2075	2170	90	P8.0	–2075	210
19	COM13	1050	–2265	55	V_{SS}	1575	2265	91	P9.3	–2075	70
20	COM14	1190	–2265	56	V_{DD1}	1425	2265	92	P9.2	–2075	–70
21	COM15	1330	–2265	57	V_{DD2}	1275	2265	93	P9.1	–2075	–210
22	COM16	1470	–2265	58	V_{DD3}	1125	2265	94	P9.0	–2075	–350
23	SEG31	2075	–2170	59	V_{DD4}	975	2265	95	PA.3	–2075	–490
24	SEG30	2075	–2030	60	V_{DD5}	825	2265	96	PA.2	–2075	–630
25	SEG29	2075	–1890	61	C1	675	2265	97	PA.1	–2075	–770
26	SEG28	2075	–1750	62	C2	525	2265	98	PA.0	–2075	–910
27	SEG27	2075	–1610	63	V_{DDH}	375	2265	99	P1.3	–2075	–1050
28	SEG26	2075	–1470	64	CB1	225	2265	100	P1.2	–2075	–1190
29	SEG25	2075	–1330	65	CB2	75	2265	101	P1.1	–2075	–1330
30	SEG24	2075	–1190	66	V_{DD}	–75	2265	102	P1.0	–2075	–1470
31	SEG23	2075	–1050	67	V_{DDL}	–225	2265	103	P6.3	–2075	–1610
32	SEG22	2075	–910	68	OSC1	–375	2265	104	P6.2	–2075	–1750
33	SEG21	2075	–770	69	OSC0	–525	2265	105	P6.1	–2075	–1890
34	SEG20	2075	–630	70	RESET	–675	2265	106	P6.0	–2075	–2030
35	SEG19	2075	–490	71	XT1	–825	2265	107	P7.3	–2075	–2170
36	SEG18	2075	–350	72	XT0	–975	2265				

1.4.2 MSM63184A pin configuration

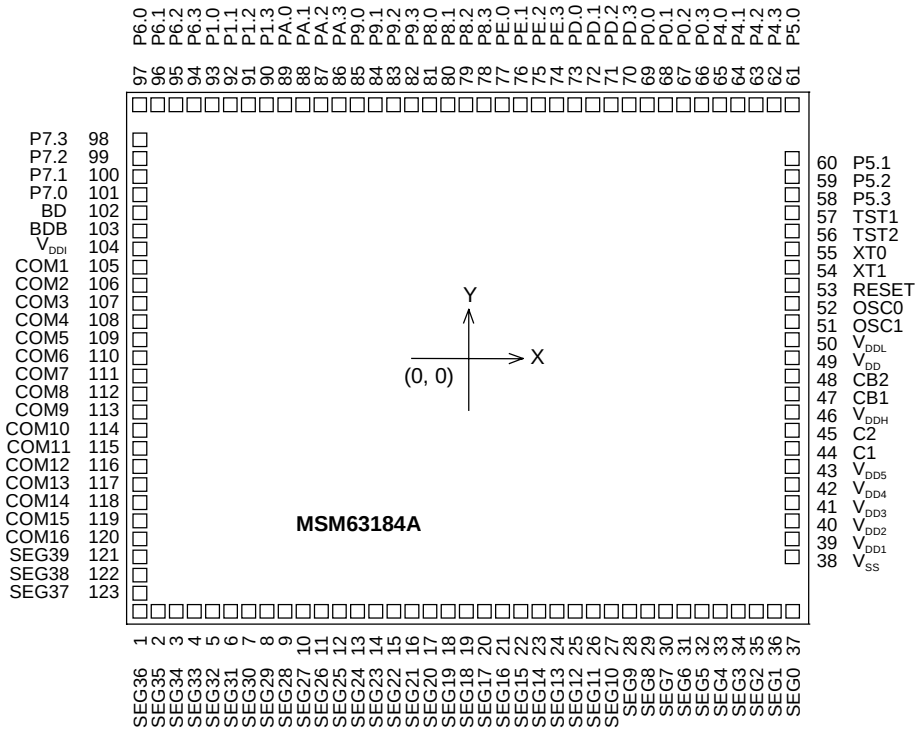
The MSM63184A pin configuration, chip pin configuration, and pad coordinates are shown in the Figures 1-6 and 1-7, and the Table 1-3, respectively.

Pins marked as NC are unused pins, which are left unconnected (open).



128-Pin Plastic QFP

Figure 1-6 MSM63184A-xxxGS-K Pin Configuration (Top View)



- Chip size : 5.35 mm × 4.66 mm
- Chip thickness : 350 μm (Typ.)
- Coordinate origin : center of chip
- Pad hole size : 100 μm × 100 μm
- Pad size : 110 μm × 110 μm
- Minimum pad pitch : 140 μm

Note: The chip substrate voltage is V_{SS}.

Figure 1-7 MSM63184A Chip Pin Configuration (Top View)

Table 1-3 MSM63184A Pad Coordinates

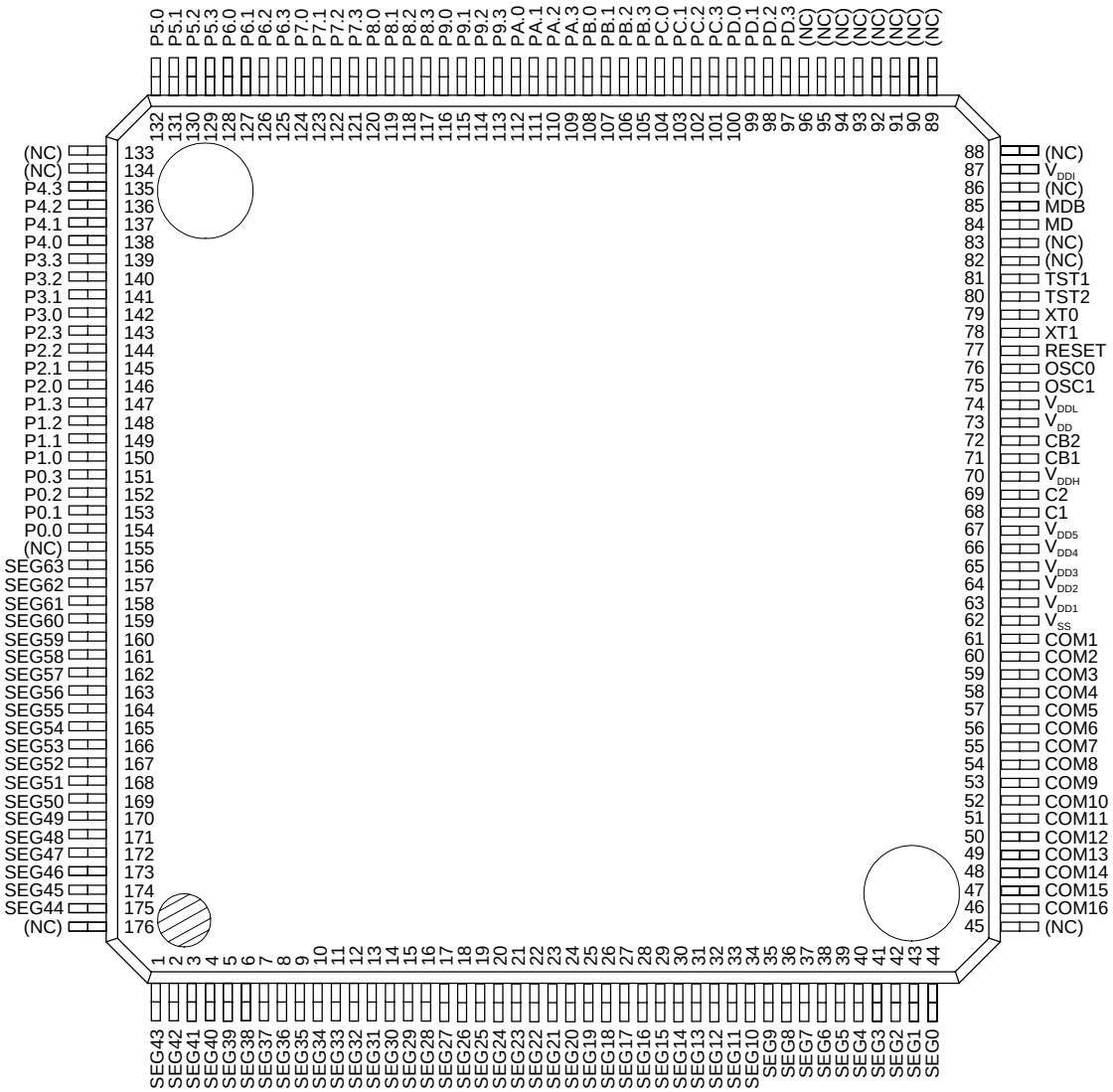
Center of chip: X = 0, Y = 0

Pad No.	Pad Name	X (μm)	Y (μm)	Pad No.	Pad Name	X (μm)	Y (μm)	Pad No.	Pad Name	X (μm)	Y (μm)
1	SEG36	–2520	–2135	42	V_{DD4}	2530	–1065	83	P9.2	–560	2135
2	SEG35	–2380	–2135	43	V_{DD5}	2530	–915	84	P9.1	–700	2135
3	SEG34	–2240	–2135	44	C1	2530	–765	85	P9.0	–840	2135
4	SEG33	–2100	–2135	45	C2	2530	–615	86	PA.3	–980	2135
5	SEG32	–1960	–2135	46	V_{DDH}	2530	–465	87	PA.2	–1120	2135
6	SEG31	–1820	–2135	47	CB1	2530	–315	88	PA.1	–1260	2135
7	SEG30	–1680	–2135	48	CB2	2530	–165	89	PA.0	–1400	2135
8	SEG29	–1540	–2135	49	V_{DD}	2530	–15	90	P1.3	–1540	2135
9	SEG28	–1400	–2135	50	V_{DDL}	2530	135	91	P1.2	–1680	2135
10	SEG27	–1260	–2135	51	OSC1	2530	285	92	P1.1	–1820	2135
11	SEG26	–1120	–2135	52	OSC0	2530	435	93	P1.0	–1960	2135
12	SEG25	–980	–2135	53	RESET	2530	585	94	P6.3	–2100	2135
13	SEG24	–840	–2135	54	XT1	2530	735	95	P6.2	–2240	2135
14	SEG23	–700	–2135	55	XT0	2530	885	96	P6.1	–2380	2135
15	SEG22	–560	–2135	56	TST2	2530	1030	97	P6.0	–2520	2135
16	SEG21	–420	–2135	57	TST1	2530	1170	98	P7.3	–2530	1607
17	SEG20	–280	–2135	58	P5.3	2530	1328	99	P7.2	–2530	1467
18	SEG19	–140	–2135	59	P5.2	2530	1468	100	P7.1	–2530	1327
19	SEG18	0	–2135	60	P5.1	2530	1608	101	P7.0	–2530	1187
20	SEG17	140	–2135	61	P5.0	2520	2135	102	BD	–2530	1029
21	SEG16	280	–2135	62	P4.3	2380	2135	103	BDB	–2530	889
22	SEG15	420	–2135	63	P4.2	2240	2135	104	V_{DDI}	–2530	749
23	SEG14	560	–2135	64	P4.1	2100	2135	105	COM1	–2530	609
24	SEG13	700	–2135	65	P4.0	1960	2135	106	COM2	–2530	469
25	SEG12	840	–2135	66	P0.3	1820	2135	107	COM3	–2530	329
26	SEG11	980	–2135	67	P0.2	1680	2135	108	COM4	–2530	189
27	SEG10	1120	–2135	68	P0.1	1540	2135	109	COM5	–2530	49
28	SEG9	1260	–2135	69	P0.0	1400	2135	110	COM6	–2530	–91
29	SEG8	1400	–2135	70	PD.3	1260	2135	111	COM7	–2530	–231
30	SEG7	1540	–2135	71	PD.2	1120	2135	112	COM8	–2530	–371
31	SEG6	1680	–2135	72	PD.1	980	2135	113	COM9	–2530	–511
32	SEG5	1820	–2135	73	PD.0	840	2135	114	COM10	–2530	–651
33	SEG4	1960	–2135	74	PE.3	700	2135	115	COM11	–2530	–791
34	SEG3	2100	–2135	75	PE.2	560	2135	116	COM12	–2530	–931
35	SEG2	2240	–2135	76	PE.1	420	2135	117	COM13	–2530	–1071
36	SEG1	2380	–2135	77	PE.0	280	2135	118	COM14	–2530	–1211
37	SEG0	2520	–2135	78	P8.3	140	2135	119	COM15	–2530	–1351
38	V_{SS}	2530	–1665	79	P8.2	0	2135	120	COM16	–2530	–1491
39	V_{DD1}	2530	–1515	80	P8.1	–140	2135	121	SEG39	–2530	–1631
40	V_{DD2}	2530	–1365	81	P8.0	–280	2135	122	SEG38	–2530	–1771
41	V_{DD3}	2530	–1215	82	P9.3	–420	2135	123	SEG37	–2530	–1970

1.4.3 MSM63188A pin configuration

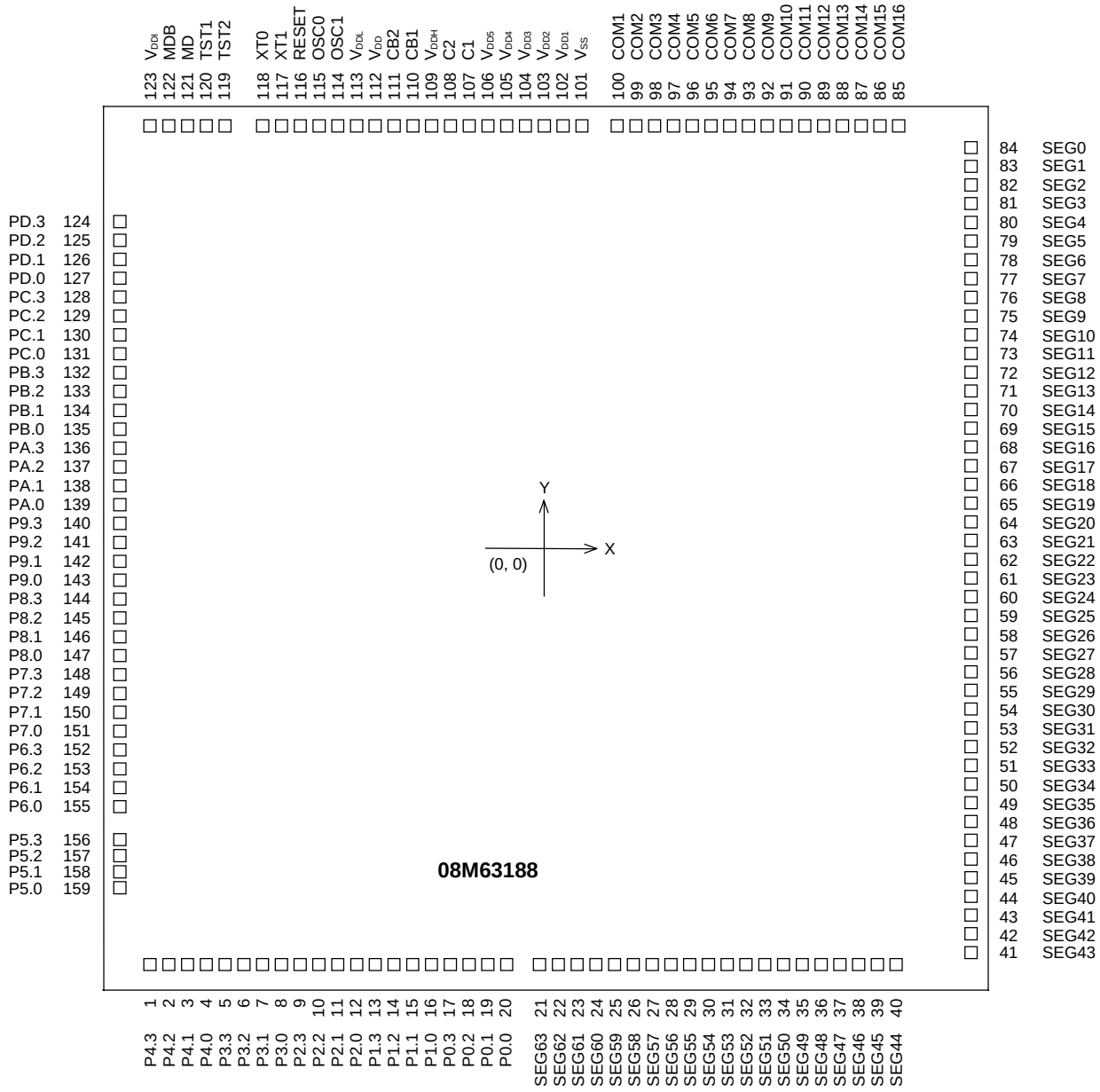
The MSM63188A pin configuration, chip pin configuration, and pad coordinates are shown in the Figures 1-8 and 1-9, and the Table 1-4, respectively.

Pins marked as NC are unused pins, which are left unconnected (open).



176-Pin Plastic LQFP

Figure 1-8 MSM63188A-xxxGS-BK Pin Configuration (Top View)



- Chip size : 6.60 mm × 6.60 mm
- Chip thickness : 350 μm (Typ.)
- Coordinate origin : center of chip
- Pad hole size : 100 μm × 100 μm
- Pad size : 110 μm × 110 μm
- Minimum pad pitch : 140 μm

Note: The chip substrate voltage is V_{SS}.

Figure 1-9 MSM63188A Chip Pin Configuration (Top View)

Table 1-4 MSM63188A Pad Coordinates

Center of chip: X = 0, Y = 0

Pad No.	Pad Name	X (μm)	Y (μm)	Pad No.	Pad Name	X (μm)	Y (μm)	Pad No.	Pad Name	X (μm)	Y (μm)
1	P4.3	–2837	–3105	42	SEG42	3155	–2870	83	SEG1	3155	2870
2	P4.2	–2697	–3105	43	SEG41	3155	–2730	84	SEG0	3155	3010
3	P4.1	–2557	–3105	44	SEG40	3155	–2590	85	COM16	2705	3105
4	P4.0	–2417	–3105	45	SEG39	3155	–2450	86	COM15	2565	3105
5	P3.3	–2277	–3105	46	SEG38	3155	–2310	87	COM14	2425	3105
6	P3.2	–2137	–3105	47	SEG37	3155	–2170	88	COM13	2285	3105
7	P3.1	–1997	–3105	48	SEG36	3155	–2030	89	COM12	2145	3105
8	P3.0	–1857	–3105	49	SEG35	3155	–1890	90	COM11	2005	3105
9	P2.3	–1717	–3105	50	SEG34	3155	–1750	91	COM10	1865	3105
10	P2.2	–1577	–3105	51	SEG33	3155	–1610	92	COM9	1725	3105
11	P2.1	–1437	–3105	52	SEG32	3155	–1470	93	COM8	1585	3105
12	P2.0	–1297	–3105	53	SEG31	3155	–1330	94	COM7	1445	3105
13	P1.3	–1157	–3105	54	SEG30	3155	–1190	95	COM6	1305	3105
14	P1.2	–1017	–3105	55	SEG29	3155	–1050	96	COM5	1165	3105
15	P1.1	–877	–3105	56	SEG28	3155	–910	97	COM4	1025	3105
16	P1.0	–737	–3105	57	SEG27	3155	–770	98	COM3	885	3105
17	P0.3	–597	–3105	58	SEG26	3155	–630	99	COM2	745	3105
18	P0.2	–457	–3105	59	SEG25	3155	–490	100	COM1	605	3105
19	P0.1	–317	–3105	60	SEG24	3155	–350	101	V_{SS}	420	3105
20	P0.0	–177	–3105	61	SEG23	3155	–210	102	V_{DD1}	270	3105
21	SEG63	54	–3105	62	SEG22	3155	–70	103	V_{DD2}	120	3105
22	SEG62	194	–3105	63	SEG21	3155	70	104	V_{DD3}	–30	3105
23	SEG61	334	–3105	64	SEG20	3155	210	105	V_{DD4}	–179	3105
24	SEG60	474	–3105	65	SEG19	3155	350	106	V_{DD5}	–329	3105
25	SEG59	614	–3105	66	SEG18	3155	490	107	C1	–479	3105
26	SEG58	754	–3105	67	SEG17	3155	630	108	C2	–629	3105
27	SEG57	894	–3105	68	SEG16	3155	770	109	V_{DDH}	–779	3105
28	SEG56	1034	–3105	69	SEG15	3155	910	110	CB1	–929	3105
29	SEG55	1174	–3105	70	SEG14	3155	1050	111	CB2	–1079	3105
30	SEG54	1314	–3105	71	SEG13	3155	1190	112	V_{DD}	–1229	3105
31	SEG53	1454	–3105	72	SEG12	3155	1330	113	V_{DDL}	–1379	3105
32	SEG52	1594	–3105	73	SEG11	3155	1470	114	OSC1	–1529	3105
33	SEG51	1734	–3105	74	SEG10	3155	1610	115	OSC0	–1679	3105
34	SEG50	1874	–3105	75	SEG9	3155	1750	116	RESET	–1829	3105
35	SEG49	2014	–3105	76	SEG8	3155	1890	117	XT1	–1979	3105
36	SEG48	2154	–3105	77	SEG7	3155	2030	118	XT0	–2129	3105
37	SEG47	2294	–3105	78	SEG6	3155	2170	119	TST2	–2324	3105
38	SEG46	2434	–3105	79	SEG5	3155	2310	120	TST1	–2464	3105
39	SEG45	2574	–3105	80	SEG4	3155	2450	121	MD	–2604	3105
40	SEG44	2714	–3105	81	SEG3	3155	2590	122	MDB	–2744	3105
41	SEG43	3155	–3010	82	SEG2	3155	2730	123	V_{DDI}	–2884	3105

Table 1-4 MSM63188A Pad Coordinates (continued)

Center of chip: X = 0, Y = 0

Pad No.	Pad Name	X (μm)	Y (μm)	Pad No.	Pad Name	X (μm)	Y (μm)	Pad No.	Pad Name	X (μm)	Y (μm)
124	PD.3	–3155	2428	136	PA.3	–3155	748	148	P7.3	–3155	–932
125	PD.2	–3155	2288	137	PA.2	–3155	608	149	P7.2	–3155	–1072
126	PD.1	–3155	2148	138	PA.1	–3155	468	150	P7.1	–3155	–1212
127	PD.0	–3155	2008	139	PA.0	–3155	328	151	P7.0	–3155	–1352
128	PC.3	–3155	1868	140	P9.3	–3155	188	152	P6.3	–3155	–1492
129	PC.2	–3155	1728	141	P9.2	–3155	48	153	P6.2	–3155	–1632
130	PC.1	–3155	1588	142	P9.1	–3155	–92	154	P6.1	–3155	–1772
131	PC.0	–3155	1448	143	P9.0	–3155	–232	155	P6.0	–3155	–1912
132	PB.3	–3155	1308	144	P8.3	–3155	–372	156	P5.3	–3155	–2172
133	PB.2	–3155	1168	145	P8.2	–3155	–51 2	157	P5.2	–3155	–2312
134	PB.1	–3155	1028	146	P8.1	–3155	–652	158	P5.1	–3155	–2452
135	PB.0	–3155	888	147	P8.0	–3155	–792	159	P5.0	–3155	–2592

1.5 Pin Descriptions

1.5.1 Descriptions of individual pins

The basic functions of each pin on the MSM63182A, MSM63184A, and MSM63188A are described in Table 1-5, and the secondary functions in Table 1-6.

Use of a slash ("/") in a pin name indicates that the pin has a secondary function. See Table 1-6 for the secondary functions.

In the I/O column, "—" indicates a power supply pin, "I" indicates an input pin, "O" indicates an output pin, and "I/O" indicates an input/output pin.

Table 1-5(a) Pin Descriptions (basic functions)

Classification	Pin name	MSM63182A		MSM63184A		MSM63188A		I/O	Function
		Pin	Pad	Pin	Pad	Pin	Pad		
Power Supply	V_{DD}	52	66	52	49	73	112	—	Positive power supply pin
	V_{SS}	41	55	40	38	62	101	—	Negative power supply pin
	V_{DD1}	42	56	41	39	63	102	—	Power supply pins for LCD bias (internally generated): Connect capacitors (0.1 μF) between these pins and V_{SS}.
	V_{DD2}	43	57	42	40	64	103		
	V_{DD3}	44	58	43	41	65	104		
	V_{DD4}	45	59	44	42	66	105		
	V_{DD5}	46	60	45	43	67	106		
	C1	47	61	46	44	68	107	—	Capacitor connection pins for LCD bias generation: Connect a capacitor (0.1 μF) between C1 and C2.
	C2	48	62	47	45	69	108		
	V_{DDI}	110	6	110	104	87	123	—	Positive power supply pin for external interface (Power supply for input, output, and I/O ports)
	V_{DDL}	53	67	53	50	74	113	—	Positive power supply pin for internal logic (internally generated): Connect a capacitor (0.1 μF) between this pin and V_{SS}.
	V_{DDH}	49	63	48	46	70	109	—	Multiplied power supply pin for power supply backup (internally generated): Connect a capacitor (1.0 μF) between this pin and V_{SS}.
	CB1	50	64	49	47	71	110	—	Capacitor connection pins for multiplied power supply: Connect a capacitor (1.0 μF) between CB1 and CB2.
	CB2	51	65	50	48	72	111		
Oscillator	XT0	58	72	58	55	79	118	I	Low-speed clock oscillation pins: Connect a crystal between XT0 and XT1, and connect capacitor (C_G: 5 to 25 pF) between XT0 and V_{SS}.
	XT1	57	71	57	54	78	117	O	
	OSC0	55	69	55	52	76	115	I	High-speed clock oscillation pins: Connect a ceramic resonator and capacitors (C_{L0}, C_{L1}) or external oscillation resistor (R_{OS}) to these pins.
	OSC1	54	68	54	51	75	114	O	
Test	TST1	60	74	60	57	81	120	I	Input pins for testing: Pull-down resistors are built-in. Not available to the user.
	TST2	59	73	59	56	80	119	I	
Reset	RESET	56	70	56	53	77	116	I	Reset input pin: Setting this pin to a "H" level causes internal circuitry settings and values to be initialized. Next, if this pin is set to a "L" level, the execution of instructions will begin from address 0000H. A pull-down resistor is built-in.
Buzzer	BD	108	4	108	102	—	—	O	Buzzer output pin (positive phase)
	BDB	109	5	109	103	—	—	O	Buzzer output pin (reversed phase)
Melody	MD	—	—	—	—	84	121	O	Melody output pin (positive phase)
	MDB	—	—	—	—	85	122	O	Melody output pin (reversed phase)

Table 1-5(b) Pin Descriptions (basic functions)

Classification	Pin name	MSM63182A		MSM63184A		MSM63188A		I/O	Function
		Pin	Pad	Pin	Pad	Pin	Pad		
Ports	P0.0/INT5	78	86	73	69	154	20	I	4-bit input ports: Each bit can be selected as the following. • Input with pull-up resistor • Input with pull-down resistor • High-impedance input
	P0.1/INT5	77	85	72	68	153	19		
	P0.2/INT5	76	84	71	67	152	18		
	P0.3/INT5	75	83	70	66	151	17		
	P1.0/INT5	94	1 02	97	93	150	16	I	
	P1.1/INT5	93	101	96	92	149	15		
	P1.2/INT5	92	100	95	91	148	14		
	P1.3/INT5	91	99	94	90	147	13		
	P2.0	—	—	—	—	146	12	O	4-bit output ports: Each bit can be selected as the following. • P-channel open drain output • N-channel open drain output • CMOS output • High-impedance output
	P2.1	—	—	—	—	145	11		
	P2.2	—	—	—	—	144	10		
	P2.3	—	—	—	—	143	9		
	P3.0	—	—	—	—	142	8	O	
	P3.1	—	—	—	—	141	7		
	P3.2	—	—	—	—	140	6		
	P3.3	—	—	—	—	139	5		
	P4.0/A0	74	82	69	65	138	4	O	
	P4.1/A1	73	81	68	64	137	3		
	P4.2/A2	72	80	67	63	136	2		
	P4.3/A3	71	79	66	62	135	1		
	P5.0/A4	70	78	65	61	132	159	O	
	P5.1/A5	69	77	63	60	131	158		
	P5.2/A6	68	76	62	59	130	157		
	P5.3/A7	61	75	61	58	129	156		
	P6.0/A8	98	106	101	97	128	155	O	
	P6.1/A9	97	105	100	96	127	154		
	P6.2/A10	96	104	99	95	126	153		
	P6.3/A11	95	103	98	94	125	152		
	P7.0/A12	107	3	107	101	124	151	O	
	P7.1/A13	106	2	106	100	123	150		
	P7.2/A14	105	1	105	99	122	149		
	P7.3/A15	99	107	104	98	121	148		
	P8.0/$\overline{RD}$	82	90	85	81	120	147	I/O	4-bit I/O ports: During the input mode, each bit can be selected as the following. • Input with pull-up resistor • Input with pull-down resistor • High-impedance input During the output mode, each bit can be selected as the following. • P-channel open drain output • N-channel open drain output • CMOS output • High-impedance output
	P8.1/$\overline{WR}$	81	89	84	80	119	146		
	P8.2	80	88	83	79	118	145		
	P8.3/INT4	79	87	82	78	117	144		
	P9.0/D0	86	94	89	85	116	143	I/O	
	P9.1/D1	85	93	88	84	115	142		
	P9.2/D2	84	92	87	83	114	141		
	P9.3/D3	83	91	86	82	113	140		

Table 1-5(c) Pin Descriptions (basic functions)

Classification	Pin name	MSM63182A		MSM63184A		MSM63188A		I/O	Function
		Pin	Pad	Pin	Pad	Pin	Pad		
Ports	PA.0/D4	90	98	93	89	112	139	I/O	4-bit I/O ports: During the input mode, each bit can be selected as the following. • Input with pull-up resistor • Input with pull-down resistor • High-impedance input During the output mode, each bit can be selected as the following. • P-channel open drain output • N-channel open drain output • CMOS output • High-impedance output
	PA.1/D5	89	97	92	88	111	138		
	PA.2/D6	88	96	91	87	110	137		
	PA.3/D7	87	95	90	86	109	136		
	PB.0/INT0/ TM0CAP/ TM0OVF	—	—	—	—	108	135	I/O	
	PB.1/INT0/ TM1CAP/ TM1OVF	—	—	—	—	107	134		
	PB.2/INT0/ T02CK	—	—	—	—	106	133		
	PB.3/INT0/ T13CK	—	—	—	—	105	132		
	PC.0/INT1/RXD	—	—	—	—	104	131	I/O	
	PC.1/INT1/TXC	—	—	—	—	103	130		
	PC.2/INT1/RXC	—	—	—	—	102	129		
	PC.3/INT1/TXD	—	—	—	—	101	128		
	PD.0/FRAME	—	—	77	73	100	127	I/O	
	PD.1/LCLK	—	—	76	72	99	126		
	PD.2/TBCCLK	—	—	75	71	98	125		
	PD.3/HSCLK	—	—	74	70	97	124		
	PE.0/SIN	—	—	81	77	—	—	I/O	
	PE.1/SOUT	—	—	80	76	—	—		
	PE.2/SCLK	—	—	79	75	—	—		
	PE.3/INT2	—	—	78	74	—	—		

Table 1-5(d) Pin Descriptions (basic functions)

Classification	Pin name	MSM63182A		MSM63184A		MSM63188A		I/O	Function
		Pin	Pad	Pin	Pad	Pin	Pad		
LCD	COM1	111	7	111	105	61	100	O	LCD common signal outputs
	COM2	112	8	112	106	60	99		
	COM3	113	9	113	107	59	98		
	COM4	114	10	114	108	58	97		
	COM5	115	11	115	109	57	96		
	COM6	116	12	116	110	56	95		
	COM7	117	13	117	111	55	94		
	COM8	118	14	118	112	54	93		
	COM9	119	15	119	113	53	92		
	COM10	120	16	120	114	52	91		
	COM11	121	17	121	115	51	90		
	COM12	122	18	122	116	50	89		
	COM13	123	19	123	117	49	88		
	COM14	124	20	124	118	48	87		
	COM15	125	21	125	119	47	86		
	COM16	126	22	126	120	46	85		
	SEG0	35	54	38	37	44	84	O	LCD segment signal outputs (Note) MSM63182A: SEG0–31 MSM63184A: SEG0–39 MSM63188A: SEG0–63
	SEG1	34	53	37	36	43	83		
	SEG2	33	52	36	35	42	82		
	SEG3	32	51	35	34	41	81		
	SEG4	31	50	34	33	40	80		
	SEG5	30	49	33	32	39	79		
	SEG6	29	48	32	31	38	78		
	SEG7	28	47	31	30	37	77		
	SEG8	27	46	30	29	36	76		
	SEG9	26	45	29	28	35	75		
	SEG10	25	44	28	27	34	74		
	SEG11	24	43	27	26	33	73		
	SEG12	23	42	26	25	32	72		
	SEG13	22	41	25	24	31	71		
	SEG14	21	40	24	23	30	70		
	SEG15	20	39	23	22	29	69		
	SEG16	19	38	22	21	28	68		
	SEG17	18	37	21	20	27	67		
	SEG18	17	36	20	19	26	66		
	SEG19	16	35	19	18	25	65		
	SEG20	15	34	18	17	24	64		
	SEG21	14	33	17	16	23	63		
	SEG22	13	32	16	15	22	62		
	SEG23	12	31	15	14	21	61		
	SEG24	11	30	14	13	20	60		
	SEG25	10	29	13	12	19	59		
	SEG26	9	28	12	11	18	58		

Table 1-5(e) Pin Descriptions (basic functions)

Classification	Pin name	MSM63182A		MSM63184A		MSM63188A		I/O	Function
		Pin	Pad	Pin	Pad	Pin	Pad		
LCD	SEG27	8	27	11	10	17	57	O	LCD segment signal outputs (Note) MSM63182A: SEG0–31 MSM63184A: SEG0–39 MSM63188A: SEG0–63
	SEG28	7	26	10	9	16	56		
	SEG29	6	25	9	8	15	55		
	SEG30	5	24	8	7	14	54		
	SEG31	4	23	7	6	13	53		
	SEG32	—	—	6	5	12	52		
	SEG33	—	—	5	4	11	51		
	SEG34	—	—	4	3	10	50		
	SEG35	—	—	3	2	9	49		
	SEG36	—	—	2	1	8	48		
	SEG37	—	—	1	123	7	47		
	SEG38	—	—	128	122	6	46		
	SEG39	—	—	127	121	5	45		
	SEG40	—	—	—	—	4	44		
	SEG41	—	—	—	—	3	43		
	SEG42	—	—	—	—	2	42		
	SEG43	—	—	—	—	1	41		
	SEG44	—	—	—	—	175	40		
	SEG45	—	—	—	—	174	39		
	SEG46	—	—	—	—	173	38		
	SEG47	—	—	—	—	172	37		
	SEG48	—	—	—	—	171	36		
	SEG49	—	—	—	—	170	35		
	SEG50	—	—	—	—	169	34		
	SEG51	—	—	—	—	168	33		
	SEG52	—	—	—	—	167	32		
	SEG53	—	—	—	—	166	31		
	SEG54	—	—	—	—	165	30		
	SEG55	—	—	—	—	164	29		
	SEG56	—	—	—	—	163	28		
	SEG57	—	—	—	—	162	27		
	SEG58	—	—	—	—	161	26		
	SEG59	—	—	—	—	160	25		
	SEG60	—	—	—	—	159	24		
	SEG61	—	—	—	—	158	23		
	SEG62	—	—	—	—	157	22		
	SEG63	—	—	—	—	156	21		

Table 1-6(a) Pin Descriptions (secondary functions)

Classification	Pin name	MSM63182A		MSM63184A		MSM63188A		I/O	Function
		Pin	Pad	Pin	Pad	Pin	Pad		
External interrupt	PB.0/INT0	—	—	—	—	108	135	I	External 0 interrupt input pins: Changes in the input signal level cause interrupts to be generated. Interrupts can be enabled or disabled for each bit by the port B interrupt enable register (PBIE).
	PB.1/INT0	—	—	—	—	107	134		
	PB.2/INT0	—	—	—	—	106	133		
	PB.3/INT0	—	—	—	—	105	132		
	PC.0/INT1	—	—	—	—	104	131	I	External 1 interrupt input pins: Changes in the input signal level cause interrupts to be generated. Interrupts can be enabled or disabled for each bit by the port C interrupt enable register (PCIE).
	PC.1/INT1	—	—	—	—	103	130		
	PC.2/INT1	—	—	—	—	102	129		
	PC.3/INT1	—	—	—	—	101	128		
	PE.3/INT2	—	—	78	74	—	—	I	External 2 interrupt input pin: Changes in the input signal level cause interrupts to be generated.
	P8.3/INT4	79	87	82	78	117	1 44	I	External 4 interrupt input pin: Changes in the input signal level cause interrupts to be generated.
	P0.0/INT5	78	86	73	69	154	20	I	External 5 interrupt input pins: Changes in the input signal level cause interrupts to be generated. Interrupts can be enabled or disabled for each bit by the port 0 interrupt enable register (P0IE) and port 1 interrupt enable register (P1IE).
	P0.1/INT5	77	85	72	68	153	19		
	P0.2/INT5	76	84	71	67	152	18		
	P0.3/INT5	75	83	70	66	151	17		
	P1.0/INT5	94	102	97	93	150	16		
	P1.1/INT5	93	101	96	92	149	15		
	P1.2/INT5	92	100	95	91	148	14		
	P1.3/INT5	91	99	94	90	147	13		
Capture	PB.0/TM0CAP	—	—	—	—	108	135	I	Timer 0 (TM0) capture trigger input pin.
	PB.1/TM1CAP	—	—	—	—	107	134	I	Timer 1 (TM1) capture trigger input pin.

Table 1-6(b) Pin Descriptions (secondary functions)

Classification	Pin name	MSM63182A		MSM63184A		MSM63188A		I/O	Function
		Pin	Pad	Pin	Pad	Pin	Pad		
Timer	PB.0/TM0OVF	—	—	—	—	108	135	O	Timer 0 (TM0) overflow flag output.
	PB.1/TM1OVF	—	—	—	—	107	134	O	Timer 1 (TM1) overflow flag output.
	PB.2/T02CK	—	—	—	—	106	133	I	Timer 0 (TM0) and Timer 2 (TM2) external clock input.
	PB.3/T13CK	—	—	—	—	105	132	I	Timer 1 (TM1) and Timer 3 (TM3) external clock input.
LCD external expansion	PD.0/FRAME	—	—	77	73	100	127	O	Frame output to expand LCD driver externally.
	PD.1/LCLK	—	—	76	72	99	126	O	Clock output to expand LCD driver externally.
Oscillation clock output	PD.2/TBCCLK	—	—	75	71	98	125	O	32.768 kHz crystal oscillation clock output.
	PD.3/HSCLK	—	—	74	70	97	124	O	High-speed oscillation clock output.
Serial Port	PC.0/RXD	—	—	—	—	104	131	I	Serial port receive data input.
	PC.1/TXC	—	—	—	—	103	130	I/O	Sync serial port clock input/output pin: This pin should be configured as the transmit clock output when this device is used as the master processor, or as the transmit clock input when used as a slave.
	PC.2/RXC	—	—	—	—	102	129	I/O	Sync serial port clock input/output pin: This pin should be configured as the receive clock output when this device is used as the master processor, or as the receive clock input when used as a slave.
	PC.3/TXD	—	—			101	128	O	Serial port send data output.
Shift register	PE.0/SIN	—	—	81	77	—	—	I	Shift register receive data input.
	PE.1/SOUT	—	—	80	76	—	—	O	Shift register send data output.
	PE.2/SCLK	—	—	79	75	—	—	I/O	Shift register clock input/output pin: This pin should be configured as the clock output when this device is used as the master processor, or as the clock input when used as a slave.

Table 1-6(c) Pin Descriptions (secondary functions)

Classification	Pin name	MSM63182A		MSM63184A		MSM63188A		I/O	Function
		Pin	Pad	Pin	Pad	Pin	Pad		
External memory	P4.0/A0	74	82	69	65	138	4	O	Address bus signals for external memory access
	P4.1/A1	73	81	68	64	137	3		
	P4.2/A2	72	80	67	63	136	2		
	P4.3/A3	71	79	66	62	135	1		
	P5.0/A4	70	78	65	61	132	159		
	P5.1/A5	69	77	63	60	131	158		
	P5.2/A6	68	76	62	59	130	157		
	P5.3/A7	61	75	61	58	129	156		
	P6.0/A8	98	106	101	97	128	155		
	P6.1/A9	97	105	100	96	127	154		
	P6.2/A10	96	104	99	95	126	153		
	P6.3/A11	95	103	98	94	125	152		
	P7.0/A12	107	3	107	101	124	151		
	P7.1/A13	106	2	106	100	123	150		
	P7.2/A14	105	1	105	99	122	149		
	P7.3/A15	99	107	104	98	121	148		
	P9.0/D0	86	94	89	85	116	143	I/O	Data bus signals for external memory access
	P9.1/D1	85	93	88	84	115	142		
	P9.2/D2	84	92	87	83	114	141		
	P9.3/D3	83	91	86	82	113	140		
	PA.0/D4	90	98	93	89	112	139		
	PA.1/D5	89	97	92	88	111	138		
	PA.2/D6	88	96	91	87	110	137		
	PA.3/D7	87	95	90	86	109	136		
	P8.0/$\overline{RD}$	82	90	85	81	120	147	O	Read signal (negative logic) for external memory access.
	P8.1/$\overline{WR}$	81	89	84	80	119	146	O	Write signal (negative logic) for external memory access.

1.5.2 Handling of unused pins

Table 1-7 shows how unused pins should be handled.

Table 1-7 Handling of Unused Pins

Pin	Recommended pin handling
OSC0, OSC1	Open
CB1, CB2	Open
C1, C2	Open
V_{DD1}, V_{DD3}, V_{DD4}, V_{DD5}	Open
TST1–2	Open or V_{SS}
P0.0–P1.3	Open
P2.0–P2.3	Open
P3.0–P3.3	Open
P4.0–P4.3	Open
P5.0–P5.3	Open
P6.0–P6.3	Open
P7.0–P7.3	Open
P8.0–P8.3	Open
P9.0–P9.3	Open
PA.0–PA.3	Open
PB.0–PB.3	Open
PC.0–PC.3	Open
PD.0–PD.3	Open
PE.0–PE.3	Open
BD, BDB	Open
MD, MDB	Open
COM1–16	Open
SEG0–63	Open

Notes:

1. If a pin set as a high impedance input is left unconnected, the supply current may become excessive. Therefore, it is recommended that unused input ports and input/output ports be set as inputs with either a pull-down or pull-up resistor.
2. When test pins TST1 and TST2 are left unconnected, malfunction may result if there is a large amount of external noise. Therefore, it is recommended to permanently connect TST1 and TST2 to V_{SS}.
3. Connect a capacitor (0.1 μF) between the V_{DD2} pin and the V_{SS} pin when the LCD drivers are not used.

1.6 Basic Timing

1.6.1 Basic timing of CPU operation

The low-speed oscillation clock from the XT0/XT1 pins or the high-speed oscillation clock from the OSC0/OSC1 pins are used without frequency division as the system clock (CLK). The system clock signal is in phase with the signal from the XT1 pin or the OSC1 pin.

As shown in Figure 1-10, a single machine cycle is composed of two states, S1 and S2. One state is the interval from a falling edge of CLK to the falling edge of the next CLK.

Instructions are processed in machine cycle units and each instruction is executed in 1 to 3 machine cycles. Instructions are classified according to the number of machine cycles: 1-machine-cycle instructions (M1), 2-machine-cycle instructions (M1 + M2), and 3-machine-cycle instructions (M1 + M2 + M3).
Most instructions are executed in 1 machine cycle.

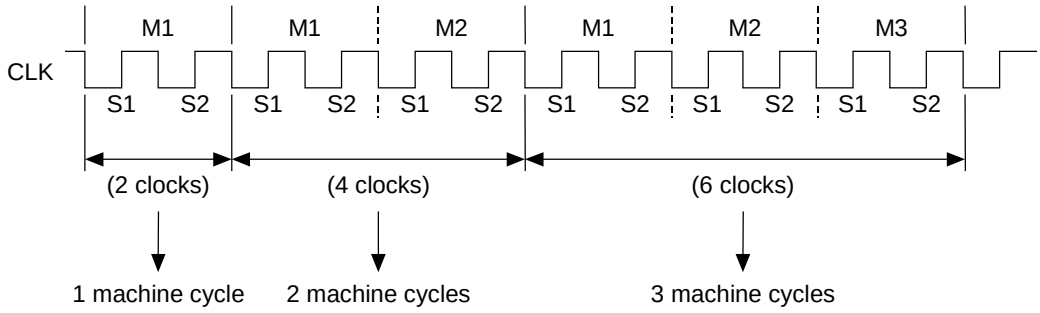


Figure 1-10 Clock Configuration of Each Machine Cycle

1.6.2 Port I/O basic timing

Figure 1-11 shows the basic I/O timing.

During the execution of an instruction that outputs data to a port, setting data (data A) is output at the rising edge of the clock in the S2 state during the machine cycle of that instruction.

During the execution of an instruction that inputs data from a port, data at the input pin (data B) is captured internally while the clock is at a "H" level in the S1 state during the machine cycle of that instruction. That data is transferred to the accumulator at the start of the next machine cycle.

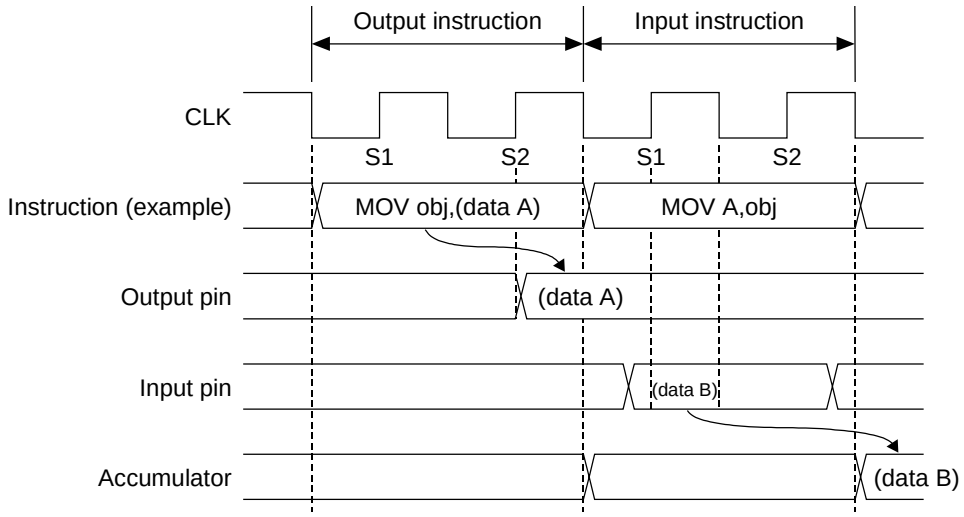


Figure 1-11 Port I/O Basic Timing

Note:

Regarding input signals
"0" will be captured in the internal register if a "L" level is input to the input pin even once (① of Figure 1-12) during the data capture interval.
"1" will be captured in the internal register only if a "H" level is maintained (② of Figure 1-12) throughout the data capture interval.
Therefore, if noise occurs in the input data, implement noise reduction measures with the program and peripheral devices.

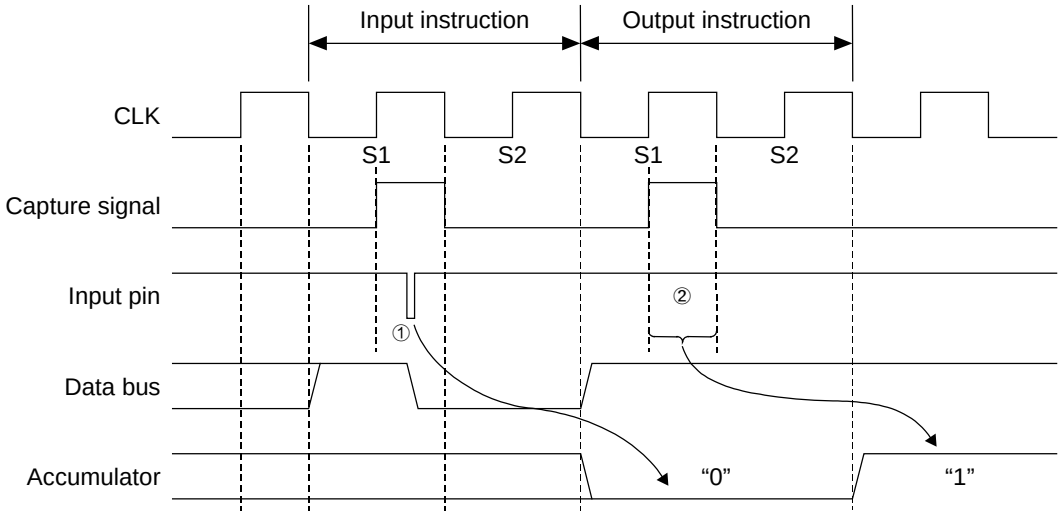


Figure 1-12 Input Data Example

1.6.3 Interrupt basic timing

Figure 1-13 shows the basic interrupt timing.

As shown in the figure, when an interrupt factor is generated, the interrupt factor is sampled at the falling edge of CLK and an interrupt request (IRQ) is set at the first half of S1.

When an interrupt condition is established and the CPU receives an interrupt, the interrupt routine will start beginning from the next machine cycle.

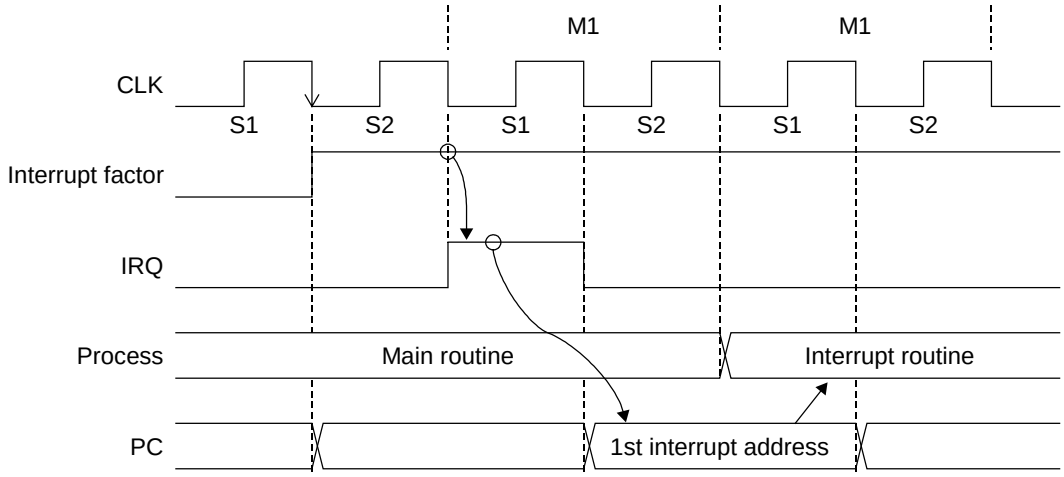


Figure 1-13 Interrupt Basic Timing

Chapter 2

CPU and Memory Spaces (nX-4/250, ROM, RAM, STACK)

Chapter 2 CPU and Memory Spaces (nX-4/250, ROM, RAM, STACK)

2.1 Overview

The MSM63180 family products have a built-in nX-4/250 CPU core.

The nX-4/250 CPU core instruction set consists of 439 instructions (MSM63182A/MSM63184A have 438 instructions without MSA instruction).

The memory space of the MSM63180 family device includes 16-bit width program memory space, 4-bit width data memory space, and 8-bit width external memory space.

The program counter save stack (call stack) for sub-routine call and interrupt and the register save stack (register stack) for the PUSH instruction are provided separately from the memory space.

The program memory space is used for program data, ROM table data, and melody output data (only for MSM63188A).

In the data memory space, special function registers (SFRs) are allocated in BANK 0, LCD display registers (DSPRs) are in BANK 1, and data RAM is in BANKS 2 to 15 (BANKS 2 to 3 for the MSM63182A, BANKS 2 to 4 for the MSM63184A, BANKS 2 to 15 for the MSM63188A).

2.2 Registers

The nX-4/250 performs various actions mainly using the Accumulator (A) and register set.

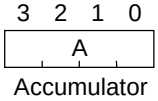
The register set constituting the programming model consists of HL register, XY register, current bank register (CBR), extra bank register (EBR) (these registers are used for data memory addressing), RA registers used for external memory and program memory addressings, program control registers, and flag/memory control registers.

2.2.1 Accumulator (A)

The Accumulator (A) is a key register for various operations.

The A register is initialized to "0" by reset.

The A register can be saved to the register stack by the PUSH HL instruction if an interrupt occurs. The A register can be returned by the POP HL instruction.



Accumulator

2.2.2 Flag registers

The flag register includes the carry flag (C), zero flag (Z), and G flag (G).

The flag register can be saved to the register stack by the PUSH HL instruction if an interrupt occurs. The flag registers can be returned by the POP HL instruction.

G	C	Z

Flag register

2.2.2.1 Carry flag (C)

The carry flag (C) is a 1-bit flag.

The C flag is set to "1" when addition or substraction results in a carry.

Upon system reset, the C flag is initialized to "0".

2.2.2.2 Zero flag (Z)

The zero flag (Z) is a 1-bit flag and is set to "1" when the contents of A register are set to "0H". When the contents of A register are set to an address other than "0H", the A register is reset to "0". Upon reset, the Z flag is reset to "0".

2.2.2.3 G flag (G)

The G flag (G) changes to "1" when the HL, XY or RA register overflows as the result of execution of a post-increment register indirect addressing instruction or as the result of an increment instruction for the HL, XY or RA register. At system reset, the G flag is initialized to "0".

2.2.3 Master interrupt enable flag (MIE)

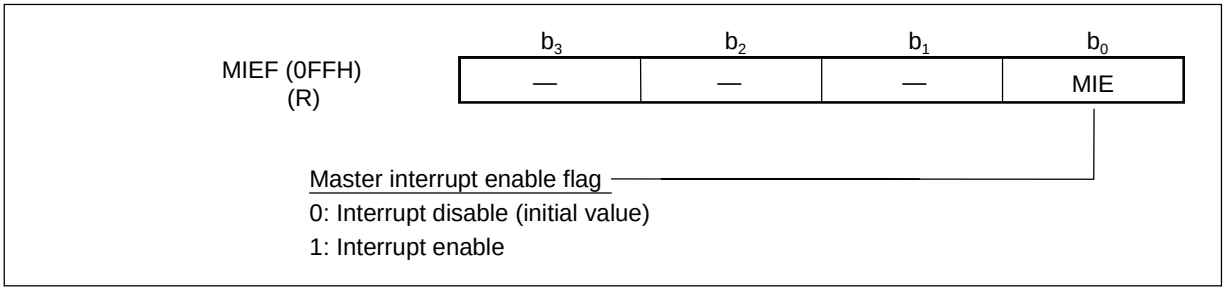
MIE (bit 0 of MIEF) is a flag that disables or enables all interrupts except for the watchdog timer interrupt. MIEF is a 4-bit register in which bit 0 is the master interrupt enable flag (MIE).

If MIE is "0", all interrupts are disabled. If MIE is "1", all interrupts are enabled (with the exception of the watchdog timer).

When any interrupt is received, MIE is cleared to "0". MIE is set to "1" by execution of a return from interrupt instruction (RTI instruction).

If multi-level interrupt processing is to be performed, execute a RTI instruction (MIE ← "1") during the interrupt processing routines.

At system reset, MIE is initialized to "0". MIEF only supports data reference (R) of data memory through addressing instructions.



Note:

When setting MIE, use "EI" instructions (MIE ← "1") and "DI" instructions (MIE ← "0").

2.2.4 Current bank register (CBR), extra bank register (EBR), HL register (HL), XY register (XY)

The current bank register (CBR), extra bank register (EBR), HL register (HL) and XY register (XY) are used for indirect addressing of data memory. CBR and EBR registers indicate the data memory bank, and HL and XY are registers indicating addresses within the bank. The CBR can be used with 8-bit data in the instruction code to directly address the current bank.

Register combinations are indicated in Figure 2-1.

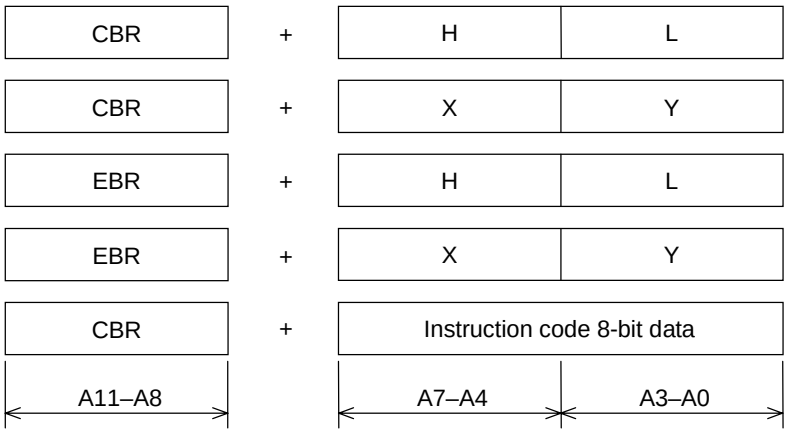


Figure 2-1 Register Combinations

A11 to A0 in Figure 2-1 indicate data memory addresses (4K nibbles max.).

The CBR, EBR, HL, and XY registers are reset to "0" at reset, and can be saved to the stack register by execution of the PUSH HL or PUSH XY instruction if an interrupt occurs.

These registers can be returned by execution of the POP HL or POP XY instruction.

These registers are allocated to addresses 0F9H through 0FEH of special function registers (SFRs).

	b_3	b_2	b_1	b_0
EBR (0FEH) (R/W)	e_3	e_2	e_1	e_0
CBR (0FDH) (R/W)	c_3	c_2	c_1	c_0
H (0FCH) (R/W)	h_3	h_2	h_1	h_0
L (0FBH) (R/W)	l_3	l_2	l_1	l_0
X (0FAH) (R/W)	x_3	x_2	x_1	x_0
Y (0F9H) (R/W)	y_3	y_2	y_1	y_0

EBR, CBR, HL and XY registers are initialized to "0" at reset. Do not use the CBR, EBR, HL or XY registers for indirect addressing mode with post-increment.

2.2.5 Program counter

The program counter (PC) has 14 effective bits, and can specify program memory space.

2.2.6 RA registers (RA3, RA2, RA1, RA0)

The RA registers are used for indirect program memory addressing (ROM table reference instruction) and indirect external memory addressing (external memory transfer instruction).

Figure 2-2 indicates the address configuration for the RA registers.

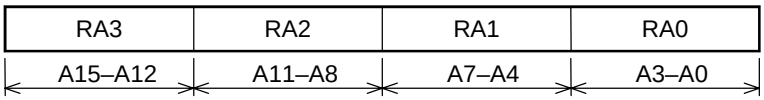
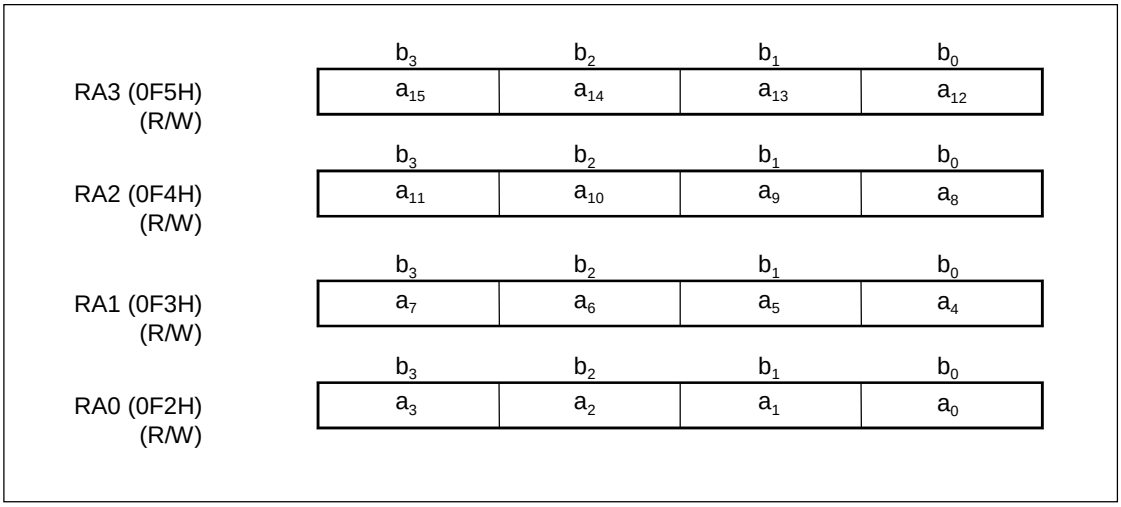


Figure 2-2 Address Configuration for Registers RA3 through RA0

A15 through A0 indicate program memory (16K words) or external memory (64K bytes max.) addresses.

RA3 through RA0 are allocated to addresses 0F2H through 0F5H of the special function register (SFR).



The RA registers are initialized to "0" at system reset.

Note:

When executing a ROM table reference instruction or external memory transfer instruction using RA registers, avoid transferring ROM table data or external memory data to RA registers using addresses allocated to SFR. Otherwise, program memory indirect addressing and external memory indirect addressing are not correctly performed.

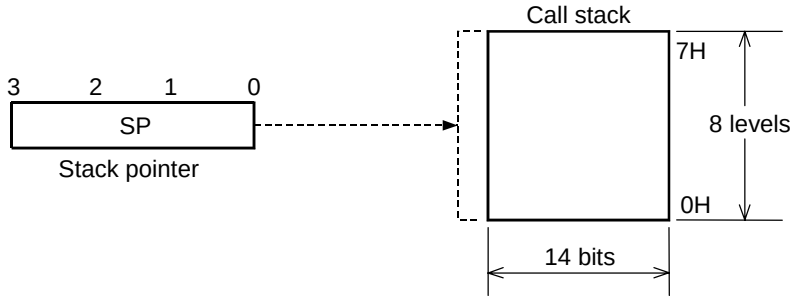
2.2.7 Stack pointer (SP) and call stack

The stack pointer (SP) is the pointer indicating the head address of the call stack, which is used to save the program counter for a subroutine call or interrupt.

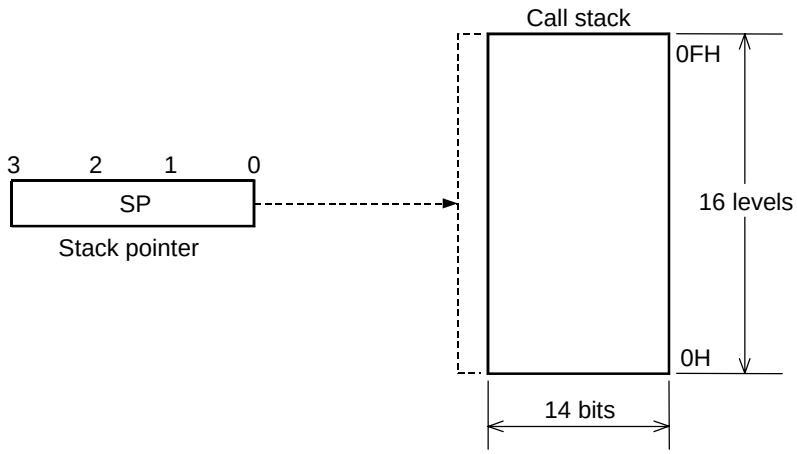
The SP is a 4-bit up/down counter, counted up for stack save and down for stack restore.

For MSM63182A and MSM63184A, the call stack is allocated to addresses 0H–7H. For MSM63188A, it is allocated to addresses 0H–0FH. However, as hardware requirements, one level of the call stack is required during execution of a program. Accordingly, only 7 levels of the call stack for the MSM63182A and the MSM63184A and 15 levels for the MSM63188A can be used for stack saving. The contents of the call stack cannot be read or written by a program.

Figure 2-3 indicates the relation between the SP and the call stack.



(MSM63182A and MSM63184A)



(MSM63188A)

Figure 2-3 Relation Between SP and Call Stack

SP is assigned to special function register (SFR) address 0F7H.

	bit 3	bit 2	bit 1	bit 0
SP (0F7H) (R)	SP3	SP2	SP1	SP0

At system reset, SP is initialized to "0" and points to address "0H" of the call stack. SP is a read-only register and writes are invalid.

2.2.8 Register stack pointer (RSP) and register stack

The register stack pointer (RSP) indicates the head address of the register stack, used for saving various registers.

The RSP is a 4-bit up/down counter, counting up at stack save (PUSH instruction) and down at a stack restore (POP instruction).

The register stack is allocated to addresses 0H–0FH. The contents of the register stack cannot be read or written by a program.

Figure 2-4 indicates the relation between the RSP and the register stack.

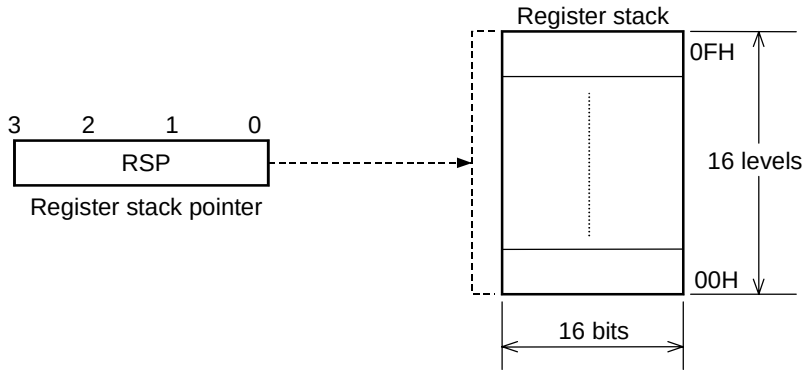


Figure 2-4 Relation between RSP and Register Stack

The PUSH/POP instructions can be used to save various registers to the register stack, and restore them, as indicated in Figure 2-5.

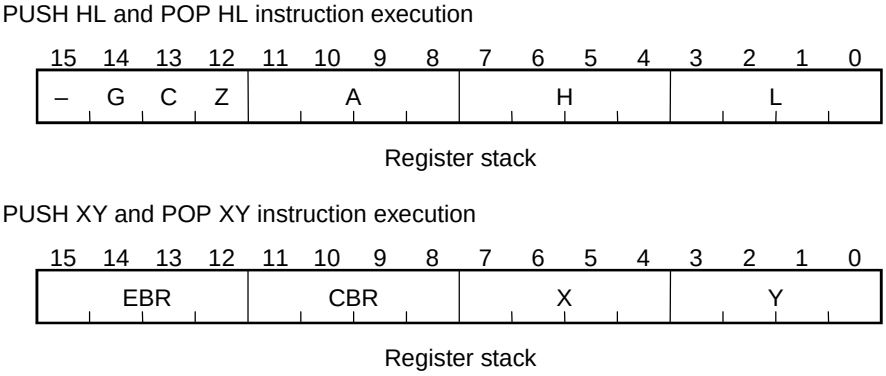


Figure 2-5 Save/Restore Registers with PUSH/POP Instructions

The RSP is allocated to address 0F6H of the special function register (SFR).

RSP (0F6H) (R/W)

b3	b2	b1	b0
rsp3	rsp2	rsp1	rsp0

The RSP is initialized to "0" at reset, and points to address 00H in the call stack.

2.3 Memory Space

2.3.1 Program memory space

The program memory space is used for storing program data, ROM table data, and interrupt area.

The program memory space has a 16-bit data length and is allocated to addresses 0000H–0FFFH in the MSM63182A, addresses 0000H–1FFFH in the MSM63184A, and addresses 0000H–3FFFH in the MSM63188A.

In addition to program data, the program memory can store ROM table data and melody data (MSM63188A only). The program memory space configuration is shown in Figure 2-6.

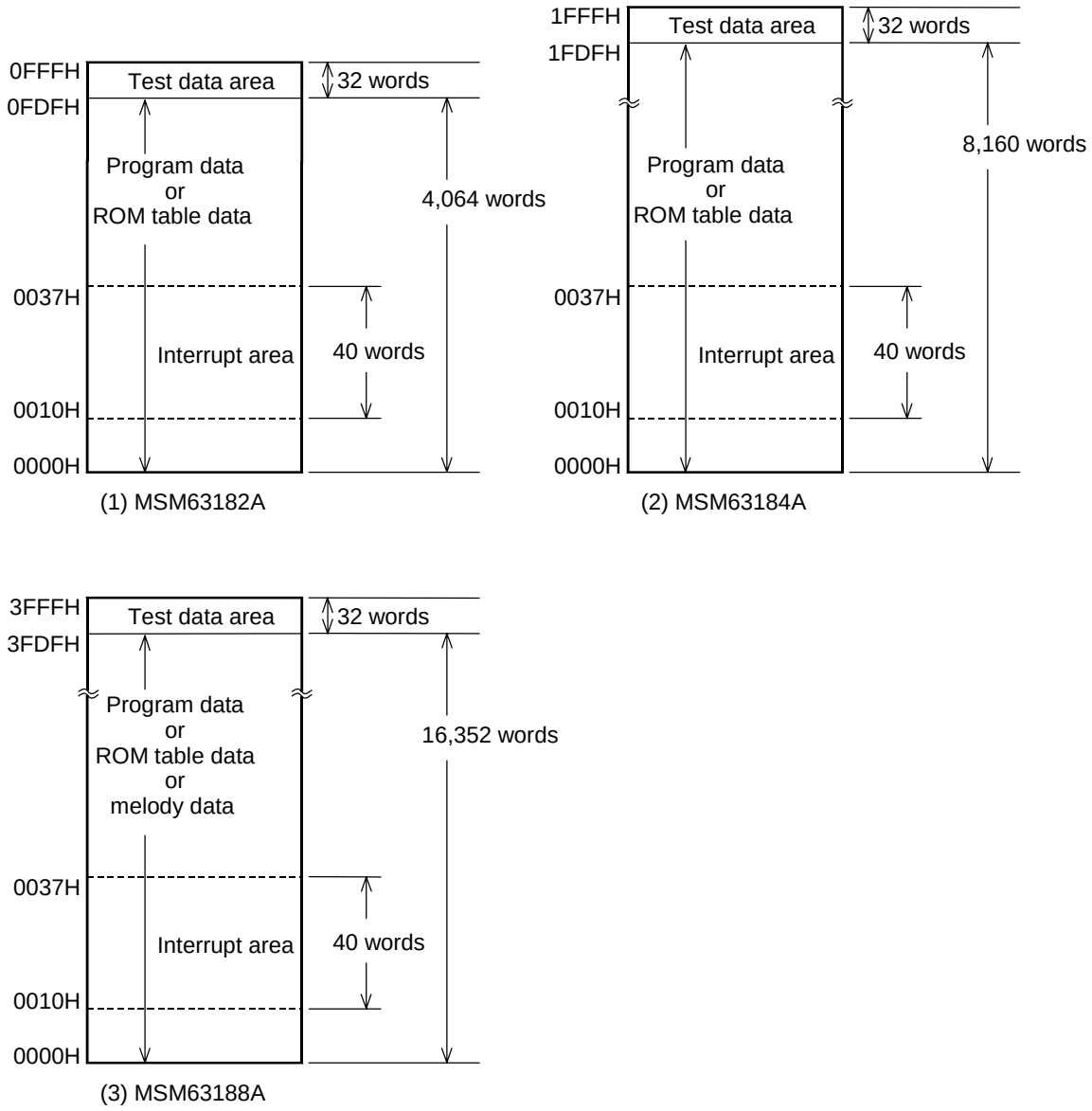


Figure 2-6 Program Memory Space Configuration

Address 0000H is the instruction execution start address used after system reset. The interrupt area from 0010H to 0037H includes the interrupt processing routine start address when an interrupt is generated. (See Chapter 4 "MSM63182A Interrupt", Chapter 5 MSM63184A Interrupt", and the Chapter 6 "MSM63188A Interrupt".)

ROM table data is transferred to data memory by the ROM table reference instruction.

The melody data defines tone, tone length, and end tone used in a melody circuit of MSM63188A. The melody data is automatically sent to the melody circuit when a melody data interrupt is generated, after the MSA instruction specifies the start address. (See Chapter 14 "Melody Driver".)

The test data area used for program test data cannot be used as a program data area.

2.3.2 Data memory space

Data memory space contains the data RAM and special function register (SFR).

The data memory consists of 16 banks. Each bank unit is 256 nibbles. BANK 0 is assigned to SFR space, BANK 1 is assigned to LCD display register, and BANK 2 and the following banks are assigned to data RAM.

Figure 2-7 shows data memory space configuration.

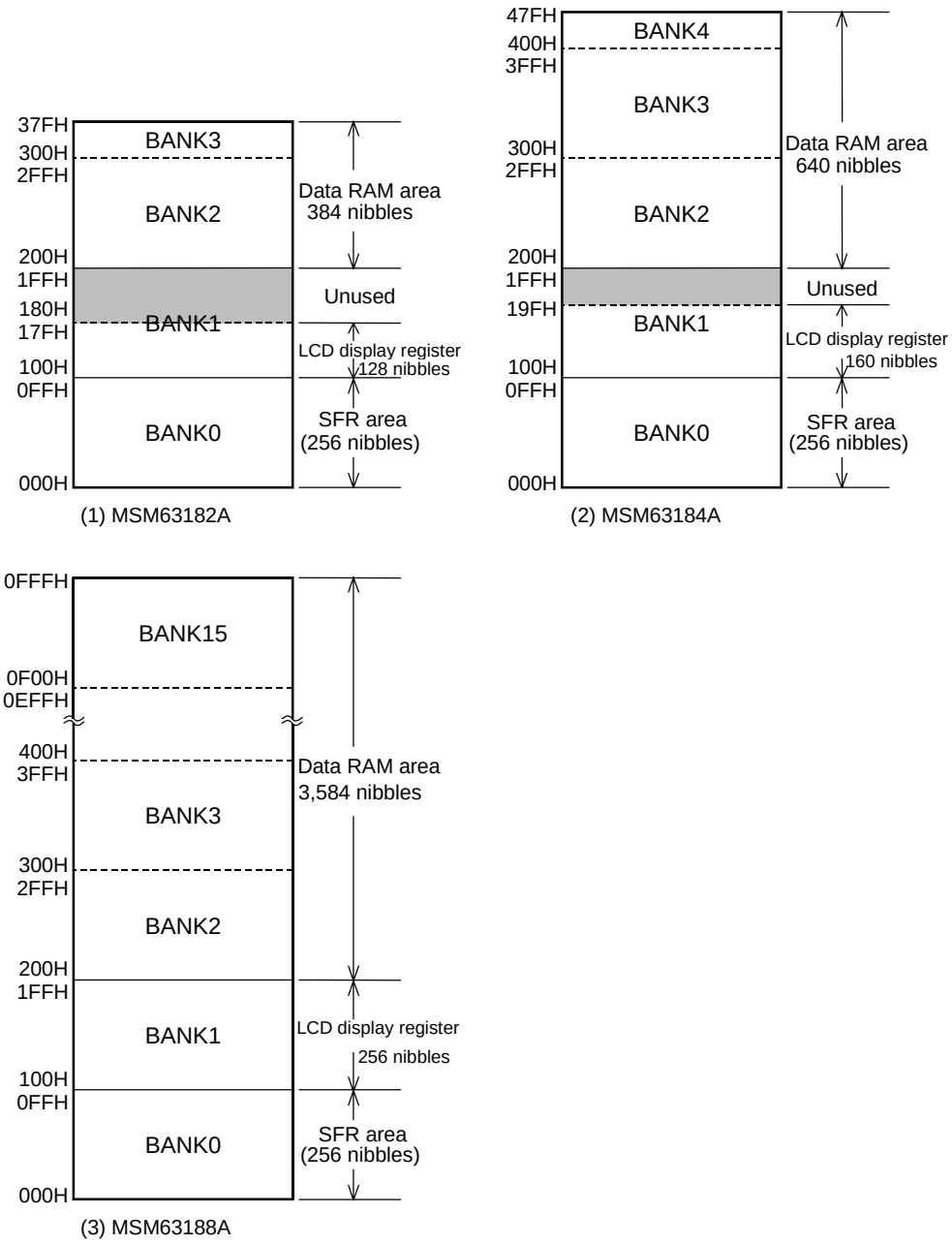


Figure 2-7 Data Memory Space Configuration

2.3.3 External memory space

The external memory space has an 8-bit data length, allocated from address 0 to address 0FFFFH. See Chapter 13 "External Memory Interface" for details.

The external memory space is configured as indicated in Figure 2-8.

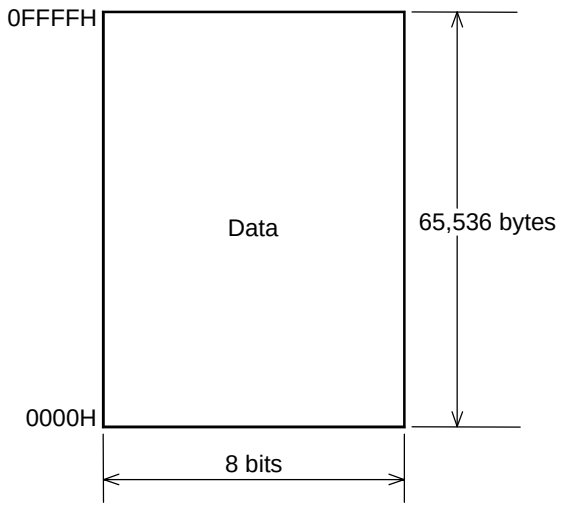


Figure 2-8 External Memory Space Configuration

Chapter 3

CPU Control Functions

Chapter 3 CPU Control Functions

3.1 Overview

Operational states, including system reset, are classified as follows:

- Normal operation mode
- System reset mode
- Halt mode

Transitions between the various states are indicated in Figure 3-1.

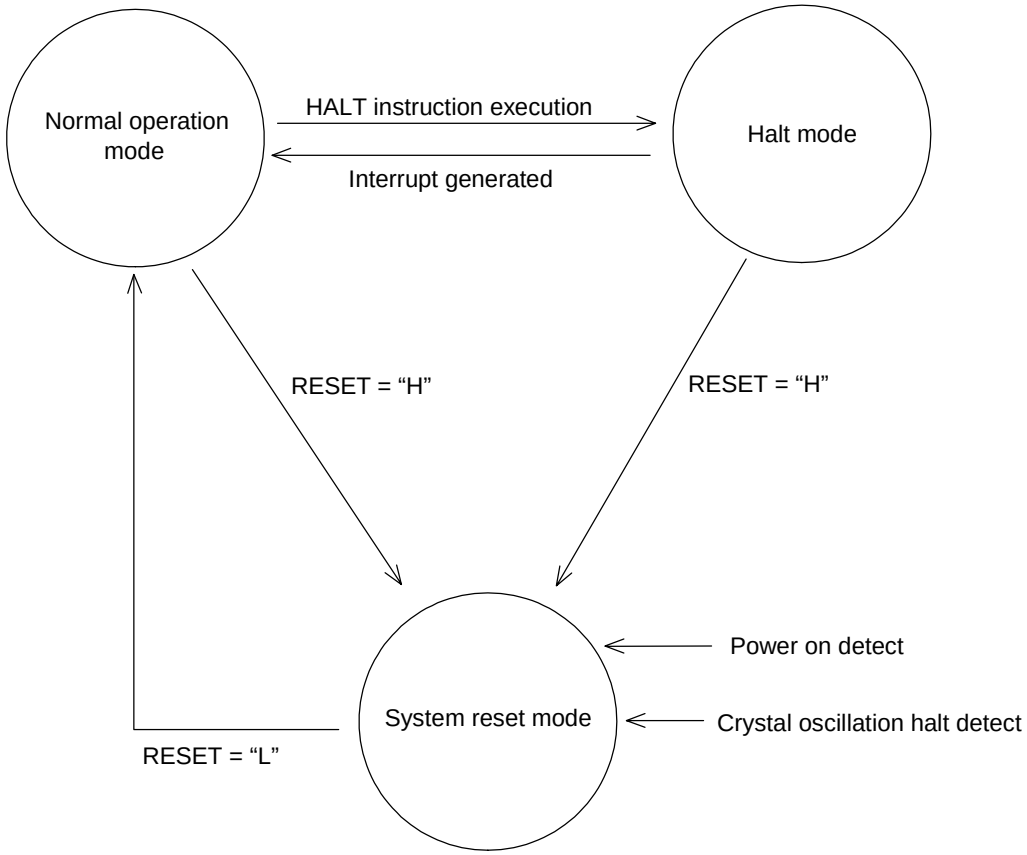


Figure 3-1 Operating State Transition Diagram

In the normal operation mode the CPU executes instructions sequentially. In the system reset mode a reset input causes the CPU to begin system reset processing. This initializes register pins and readies the system for instruction execution. After system reset processing, execution begins from address 0000H.

In the halt mode the CPU is halted and no instructions are executed. The PC is not incremented, but internal peripheral functions continue to operate. Transition to the halt mode is accomplished by executing the HALT instruction.

Even in halt mode, the port and peripheral functions do not change.

3.2 System Reset Function (RST)

The system reset mode is triggered by a power on detect, crystal oscillation halt detect and the RESET pin switching to high level. In the reset mode the following operations are implemented:

(1) The CPU is initialized.
(2) Back-up flag is set to "1", entering back-up state.
(3) Bias reference voltage supply (VR) energized.
(4) All LCD driver outputs are turned off and set to V_{SS} level.
(5) All special function registers (SFRs) are initialized. Note that data RAM and display registers are not initialized.

After system reset processing, instruction execution begins at address 0000H. System reset generator circuit and signals used in system reset are indicated in Figures. 3-2 and 3-3.

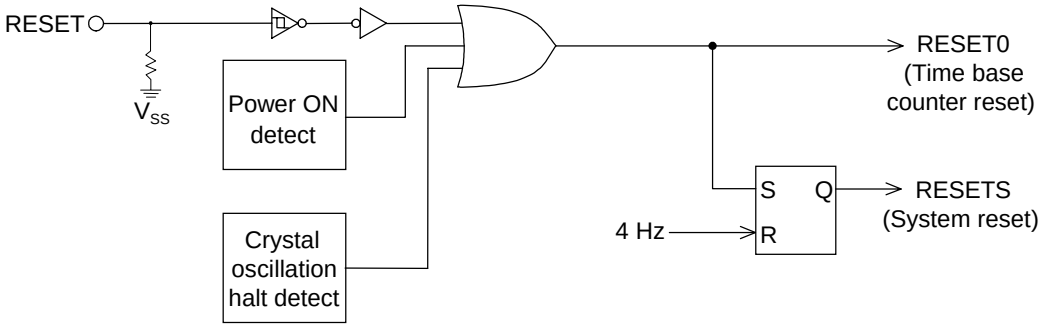


Figure 3-2 System Reset Generator Circuit

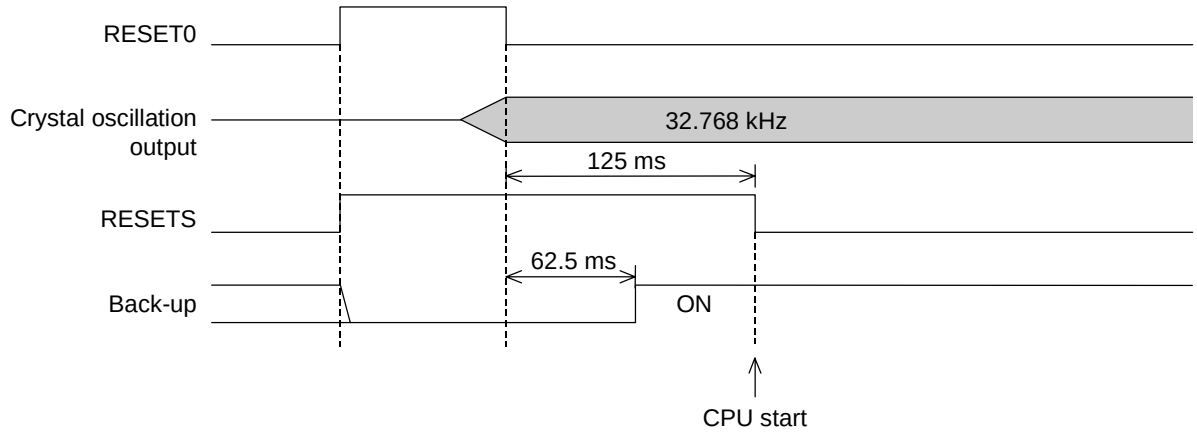


Figure 3-3 System Reset Signals

[Caution]
System reset takes priority over all other processing and interrupts all processing. As a result, the contents of RAM and display registers (which are not initialized) are undefined after system reset.

3.3 Halt Mode

3.3.1 Halt mode setting

Transfer to the halt mode is performed by the software when a HALT instruction is executed.

When a HALT instruction is executed, the CPU enters the HALT mode at the S2 state of the HALT instruction.

Oscillation and time base counter operation continue while in the halt mode.

If an interrupt request occurs at the same time as execution of a HALT instruction, interrupt processing has priority and the HALT instruction will not be executed. After the HALT instruction performs the equivalent operation of a NOP instruction, the interrupt routine is entered. When an RTI instruction is used to complete the interrupt routine, the main routine is resumed beginning from the instruction immediately following the HALT instruction.

Figure 3-4 shows the timing when a HALT instruction and interrupt request occur simultaneously.

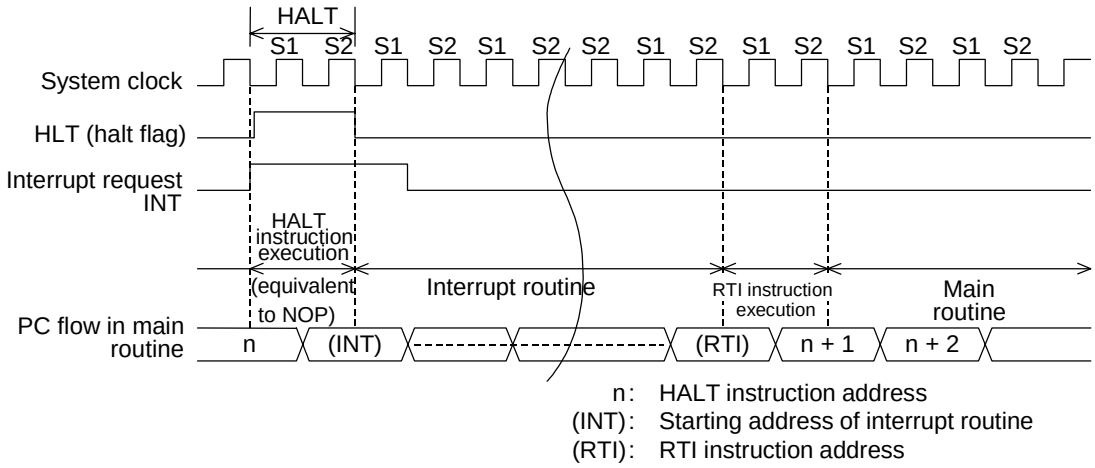


Figure 3-4 Timing of Simultaneous HALT Instruction and Interrupt Request

Note:

While an interrupt request is generated, execution of a HALT instruction will not transfer operation to the halt mode.

3.3.2 Halt mode release

The following two methods are available to release the halt mode.

- Release by interrupt generation (transfer to normal operation mode)
- Release by RESET pin (transfer to system reset mode)

3.3.2.1 Release of halt mode by interrupt

If the halt mode is to be released by an interrupt, the enable flag of the interrupt used for release must be set to "1" prior to entering the halt mode. When the halt mode is released by an interrupt, operation transfers to the normal operation mode.

Figure 3-5 shows the timing of transferring to the halt mode by execution of a HALT instruction and of releasing the halt mode by an interrupt.

When the halt mode is released by an interrupt request, the first instruction immediately following the HALT instruction is executed and then the interrupt routine is entered. When an RTI instruction is used to complete the interrupt routine, the main routine is resumed beginning from the second instruction after the HALT instruction.

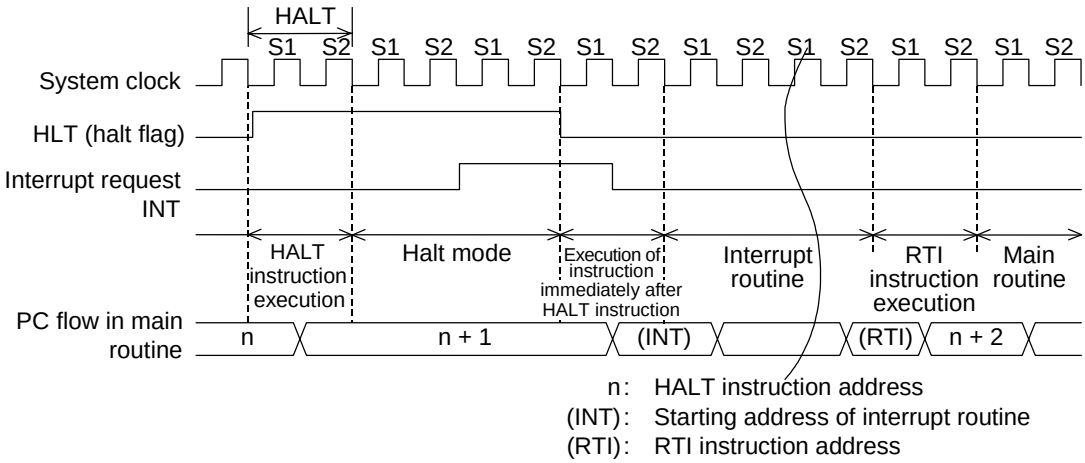


Figure 3-5 Timing of Transfer to Halt Mode and Release of Halt Mode by Interrupt

Note:

If the halt mode is to be released, set individual interrupt enable flags to "1". If an individual interrupt enable flag is "0", the corresponding interrupt request signal cannot reset the HLT flag, regardless of whether the master interrupt enable flag (MIE) is "0" or "1".

3.3.2.2 Release of halt mode by RESET pin

If a high-level is input to the RESET pin, the CPU is released from the halt mode and transfers to the system reset mode.

3.3.3 Melody data interrupt and halt mode (MSM63188A only)

The halt mode is not released by a melody data interrupt.

The melody data interrupt is different from a conventional interrupt in that the melody data interrupt is a hardware processing interrupt used for transfer of melody data to the melody circuit. It is not dependent on the program.

When this interrupt is generated, the instruction immediately after the HALT instruction is executed, then the melody data is transferred to the melody circuit, and the HALT instruction is executed again. This sequence is indicated in Figure 3-6.

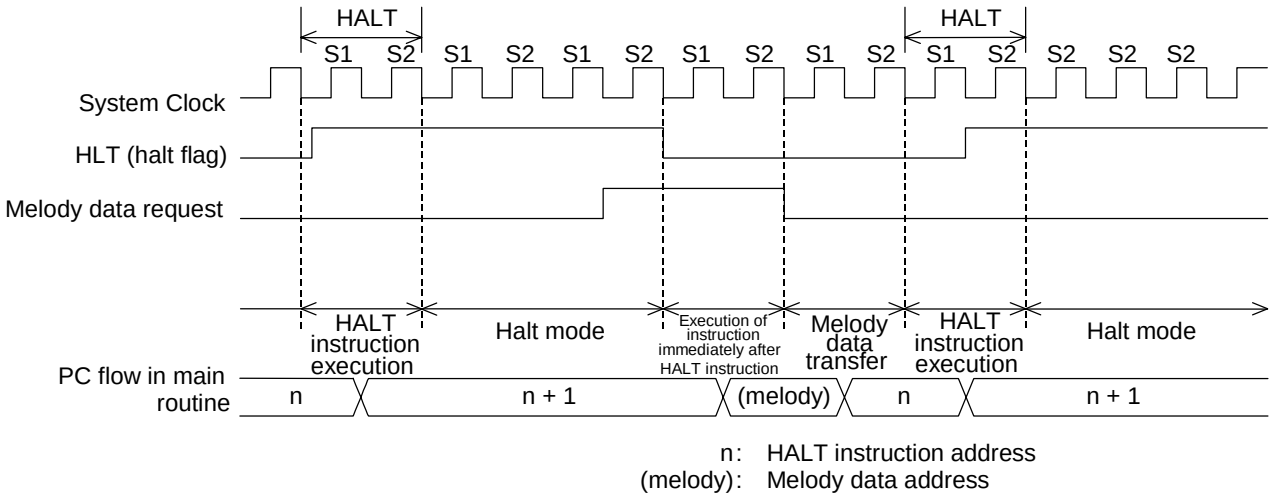


Figure 3-6 Melody Data Request Interrupt Operation

3.3.4 Note concerning HALT instruction

As described above, the instruction immediately after the HALT instruction may be executed any number of times. For this reason, always place an NOP instruction immediately after the HALT instruction.

(Example)

•
•
•
HALT
NOP
•
•
•

Chapter 4

MSM63182A Interrupt (INT182)

Chapter 4 MSM63182A Interrupt (INT182)

4.1 Overview

The MSM63182A supports 8 interrupt factors: 2 external interrupts and 6 internal interrupts.

With the exception of the watchdog timer interrupt, interrupt enable/disable is controlled by the master interrupt enable flag (MIE) and the individual interrupt enable registers (IE1, 3, 4). When an interrupt is accepted, the interrupt routine is executed from the interrupt start address.

Table 4-1 lists interrupt factors, and Figure 4-1 shows the interrupt control equivalent circuit.

Table 4-1 List of Interrupt Factors

Priority	Interrupt factor	Symbol	Interrupt start address
1	Watchdog timer interrupt	WDTINT	0010H
2	External 4 interrupt (P8.3)	XI4INT	001CH
3	External 5 interrupt (P0, P1 8-bit OR input)	XI5INT	001EH
4	T10 Hz interrupt	T10HzINT	002EH
5	32 Hz interrupt	32HzINT	0030H
6	16 Hz interrupt	16HzINT	0032H
7	4 Hz interrupt	4HzINT	0034H
8	2 Hz interrupt	2HzINT	0036H

If multiple interrupts are detected simultaneously, the lowest interrupt start address is given priority.

For details on interrupt operation, refer to Chapter 8 (Time Base Counter), Chapter 10 (100 Hz Timer Counter), Chapter 11 (Watchdog Timer), and Chapter 12 (Ports).

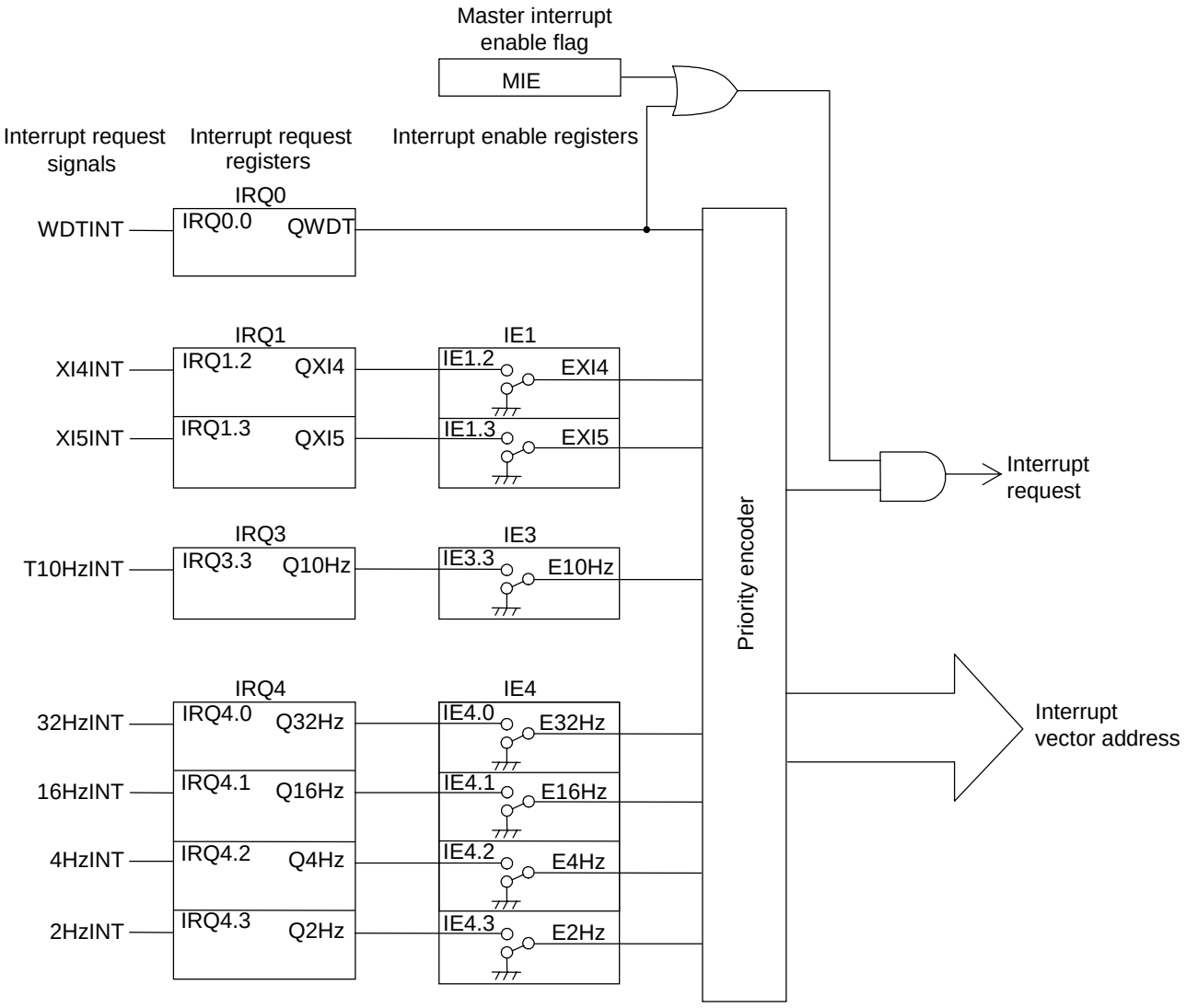


Figure 4-1 MSM63182A Interrupt Control Equivalent Circuit

4.2 Interrupt Sequence

4.2.1 Interrupt processing

Execution shifts to interrupt processing when the MIE flag is set to "1". This generates an individual interrupt factor.

The watchdog timer interrupt is a non-maskable interrupt, and execution will shift to interrupt processing regardless of the MIE flag state.

When an interrupt is generated the following processing is executed. Interrupt processing is executed in zero machine cycles.

(1) MIE flag and individual interrupt request flag reset to "0".
(2) Program counter (PC) saved to call stack.
(3) Call stack pointer (SP) incremented by one. (SP←SP + 1)
(4) Interrupt head address loaded into program counter (PC).

Figure 4-2 indicates the content of the stack after an interrupt is generated.

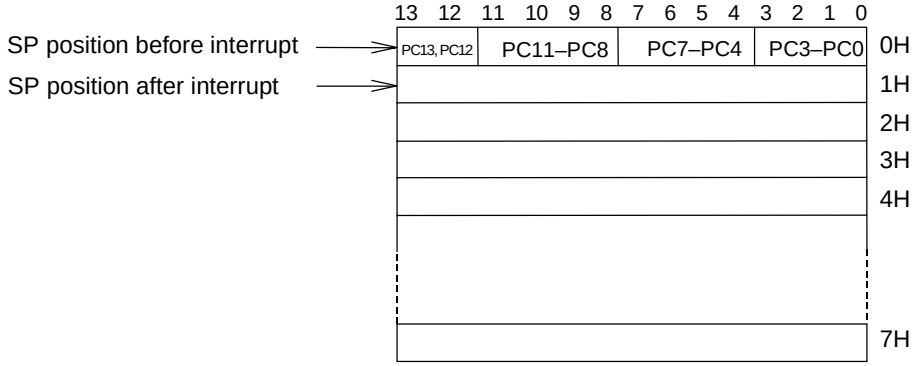


Figure 4-2 Call Stack Content after Interrupt Generation

4.2.2 Return from interrupt routine

Return from a watchdog timer interrupt routine is performed with an "RTNMI" instruction.

Return from all other interrupt routines is performed with an "RTI" instruction.

Execution of "RTI" and "RTNMI" instructions both require 1 machine cycle.

When returning from an interrupt routine, the CPU performs the following processes.

(1) The call stack pointer (SP) is decremented by 1. (SP ← SP–1)
(2) MIE is set to "1" (when an "RTNMI" instruction is used, MIE is restored to its state prior to the interrupt).
(3) 1 is added to the call stack contents and that value is loaded into the program counter (PC).

Notes:

- While the MIE flag is "0" (interrupt disabled state), if a watchdog timer interrupt is processed and an "RTI" instruction is executed, the MIE flag will be set to "1" and interrupts enabled.
- Use "RTNMI" instructions to return from watchdog timer interrupts only. Use "RTI" instructions for normal interrupts.

4.2.3 Interrupt hold instructions

Interrupt requests are not received after execution of interrupt hold instruction.

The interrupt hold instructions follow.

- ROM table reference instructions
- External memory transfer instructions
- Stack operation instructions
- Jump instructions
- Conditional branch instructions
- Call/return instructions
- "EI" (set MIE flag) instructions, "DI" (clear MIE flag) instructions and "MSA cadr14" (start melody output) instructions within control instructions

Note:

If interrupt hold instructions are to be used consecutively, consider that an interrupt, when generated, will be put on hold for a certain amount of time before the interrupt routine begins. Interrupt requests are received after execution of an instruction other than interrupt hold instructions.

4.3 Interrupt Control Registers

4.3.1 Interrupt request registers (IRQ0, IRQ1, IRQ3, IRQ4)

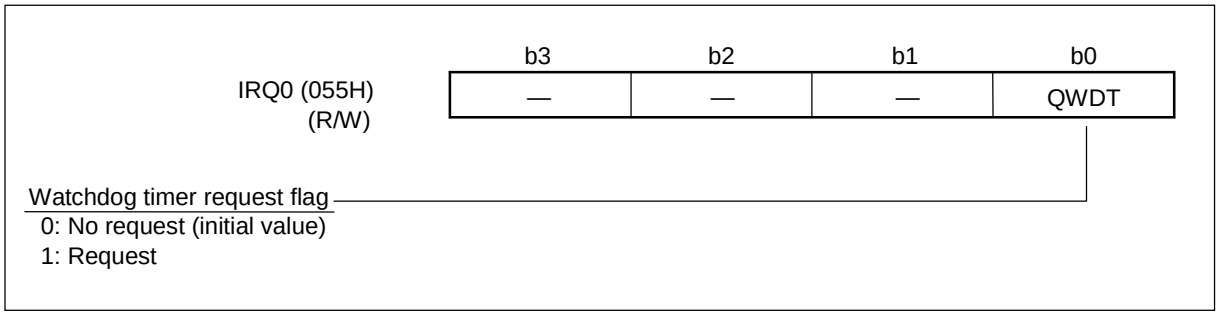
The interrupt request registers (IRQ0, IRQ1, IRQ3, IRQ4) are 4-bit registers. When an interrupt request is generated the corresponding bit is set to "1" in the first half of the S1 state of the next instruction. If the corresponding flag of the interrupt enable register (IE1, IE3, IE4) is set to "1" and the master interrupt enable flag (MIE) is also set to "1", an interrupt request is sent to the CPU.

The watchdog timer interrupt is a non-maskable interrupt, not dependent on the interrupt enable register or master interrupt enable flag (MIE).

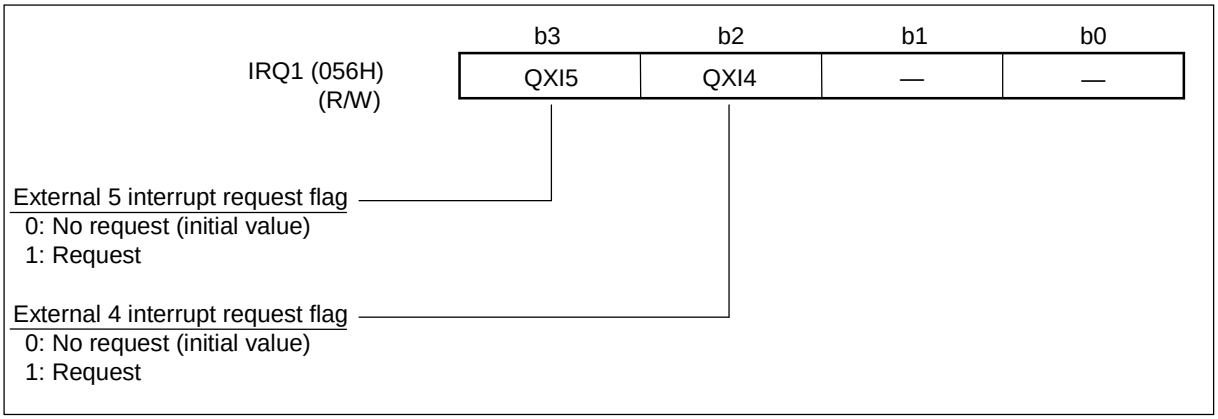
Setting the interrupt request register to "1" allows software interrupts to be generated.

When an interrupt request is accepted, hardware resets the corresponding bit of IRQ0, IRQ1, IRQ3, and IRQ4 to "0".

IRQ0, IRQ1, IRQ3, and IRQ4 are initialized to 0H at system reset.

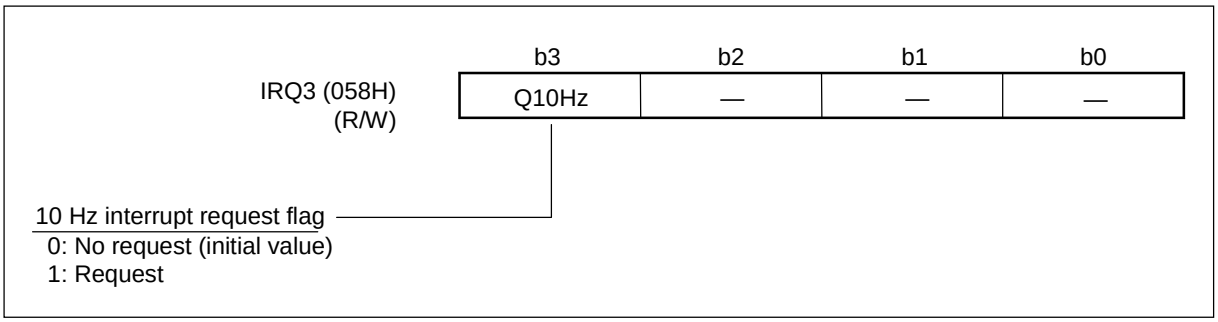


Bit 0: QWDT
Watchdog timer interrupt request flag. When the watchdog timer is started and an overflow occurs, the interrupt is requested. The watchdog timer is a non-maskable interrupt not dependent on the interrupt enable register or master interrupt enable flag.

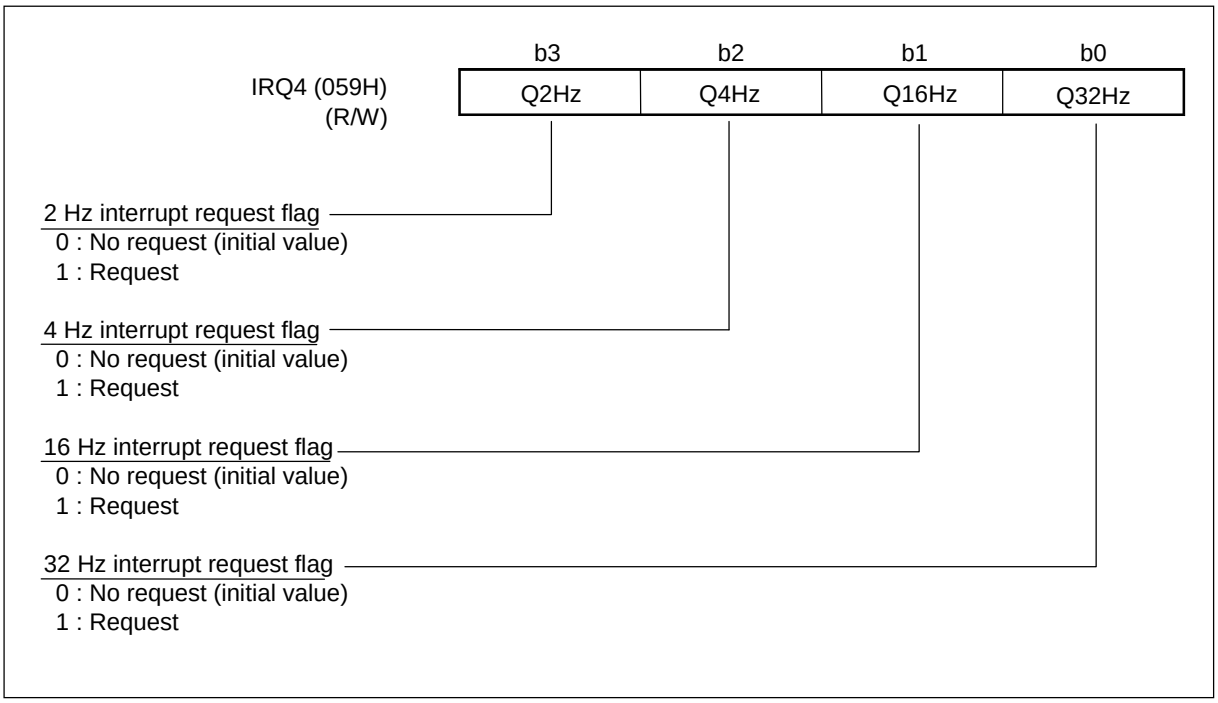


Bit 3: QXI5
The external 5 interrupt request flag. The external 5 interrupt is an 8-bit OR input external interrupt assigned to ports 0 and 1.

Bit 2: QXI4
The external 4 interrupt request flag. This external interrupt is allocated to port 8.3.



Bit 3: Q10Hz
The 10 Hz interrupt request flag. This interrupt is requested when the 10 Hz counter in the 1/100 timer overflows.



Bit 3: Q2Hz
The 2 Hz interrupt request flag. The 2 Hz interrupt is requested at the 2 Hz output falling edge of the time base counter.

Bit 2: Q4Hz
The 4 Hz interrupt request flag. The 4 Hz interrupt is requested at the 4 Hz output falling edge of the time base counter.

Bit 1: Q16Hz
The 16 Hz interrupt request flag. The 16 Hz interrupt is requested at the 16 Hz output falling edge of the time base counter.

Bit 0: Q32Hz
The 32 Hz interrupt request flag. The 32 Hz interrupt is requested at the 32 Hz output falling edge of the time base counter.

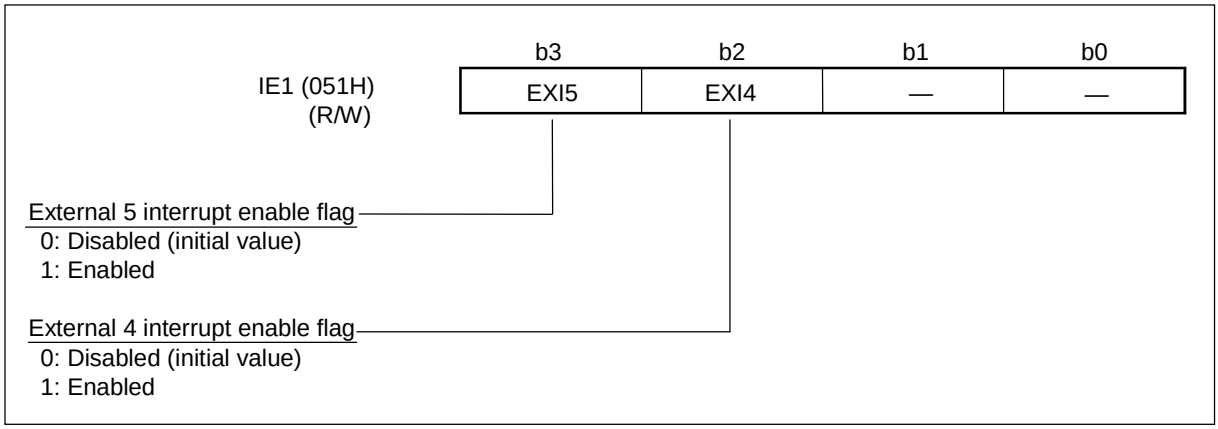
4.3.2 Interrupt enable registers (IE1, IE3, IE4)

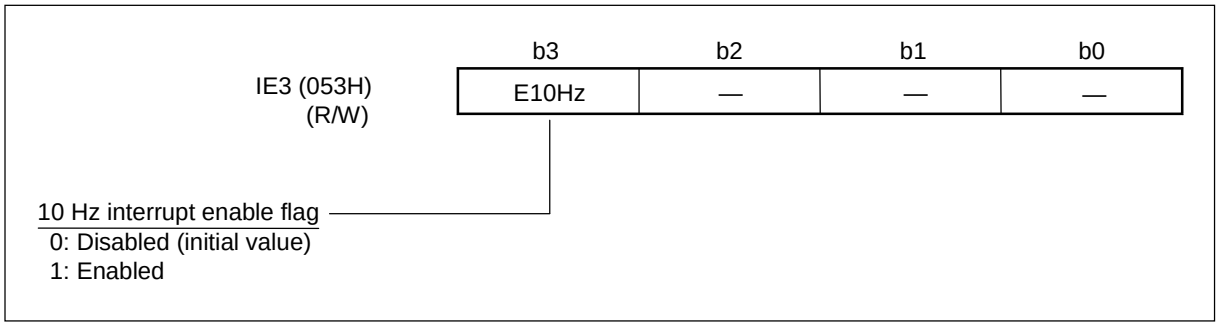
The interrupt enable registers (IE1, IE3, IE4) are 4-bit registers, and determine whether or not an interrupt request is issued to the CPU through an AND operation with the bit corresponding to the interrupt request registers (IRQ1, IRQ3, IRQ4). The watchdog timer interrupt is a non-maskable interrupt, and is therefore not dependent on the interrupt enable registers and the master interrupt enable flag (MIE).

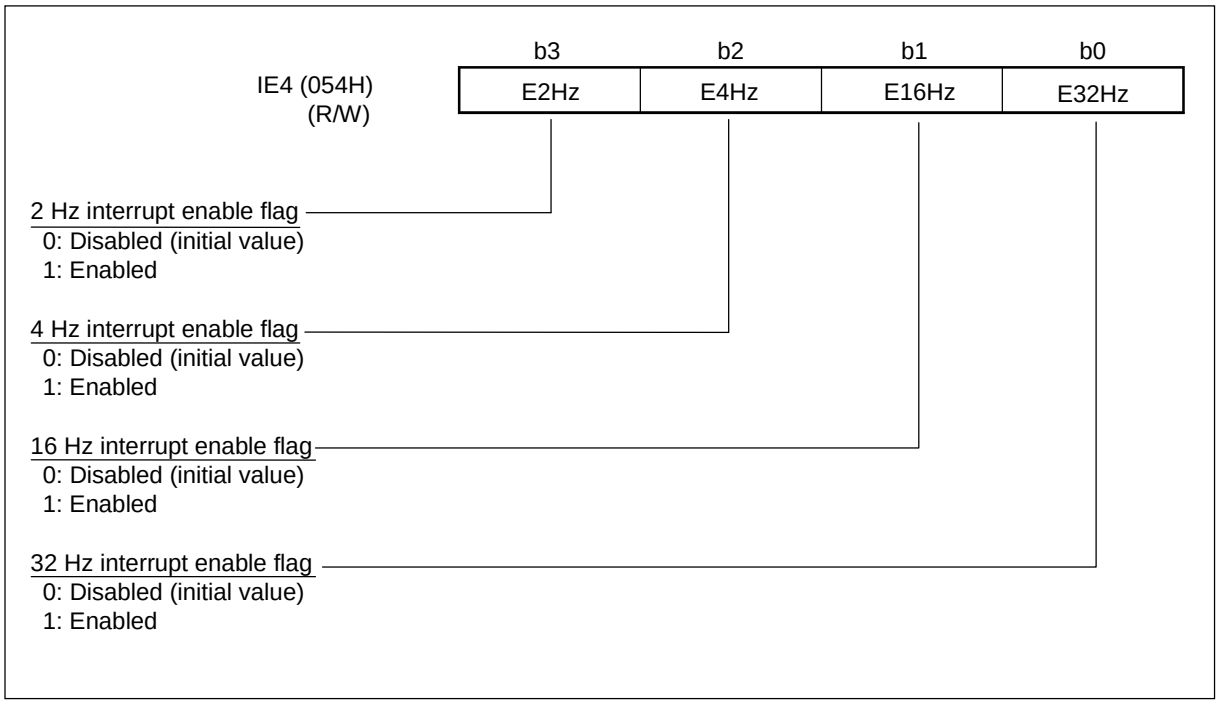
If multiple interrupts are requested simultaneously, the CPU will accept them in the priority order indicated in Table 4-1, and the interrupts with lower priorities will be held.

When an interrupt is accepted the master interrupt enable flag is reset to "0", but the related bits of IE1, IE3, and IE4 are not reset.

IE1, IE3, and IE4 are initialized to 0H at system reset.




b3
b2
b1
b0
IE3 (053H)
(R/W)
E10Hz
—
—
—
10 Hz interrupt enable flag
0: Disabled (initial value)
1: Enabled


b3
b2
b1
b0
IE4 (054H)
(R/W)
E2Hz
E4Hz
E16Hz
E32Hz
2 Hz interrupt enable flag
0: Disabled (initial value)
1: Enabled
4 Hz interrupt enable flag
0: Disabled (initial value)
1: Enabled
16 Hz interrupt enable flag
0: Disabled (initial value)
1: Enabled
32 Hz interrupt enable flag
0: Disabled (initial value)
1: Enabled

Chapter 5

MSM63184A Interrupt (INT184)

Chapter 5 MSM63184A Interrupt (INT184)

5.1 Overview

The MSM63184A supports 10 interrupt factors: 3 external port interrupts and 7 internal interrupts.

With the exception of the watchdog timer interrupt, interrupt enable/disable is controlled by the master interrupt enable flag (MIE) and the individual interrupt enable registers (IE1, 3, 4). When interrupt conditions are met, the interrupt routine is executed from the interrupt start address.

Table 5-1 indicates a list of interrupt factors, and Figure 5-1 shows the interrupt control equivalent circuit.

Table 5-1 List of Interrupt Factors

Priority	Interrupt factor	Symbol	Interrupt start address
1	Watchdog timer interrupt	WDTINT	0010H
2	External 2 interrupt (PE.3)	XI2INT	0018H
3	External 4 interrupt (P8.3)	XI4INT	001CH
4	External 5 interrupt (P0, P1 8-bit OR input)	XI5INT	001EH
5	Shift register interrupt	SFTINT	002CH
6	T10 Hz interrupt	T10HzINT	002EH
7	32 Hz interrupt	32HzINT	0030H
8	16 Hz interrupt	16HzINT	0032H
9	4 Hz interrupt	4HzINT	0034H
10	2 Hz interrupt	2HzINT	0036H

If multiple interrupts are detected simultaneously, the lowest interrupt start address is given priority.

For details on interrupt operation, refer to Chapter 8 (Time Base Counter), Chapter 10 (100 Hz Timer Counter), Chapter 11 (Watchdog Timer), Chapter 12 (Ports), and Chapter 17 (Shift Register).

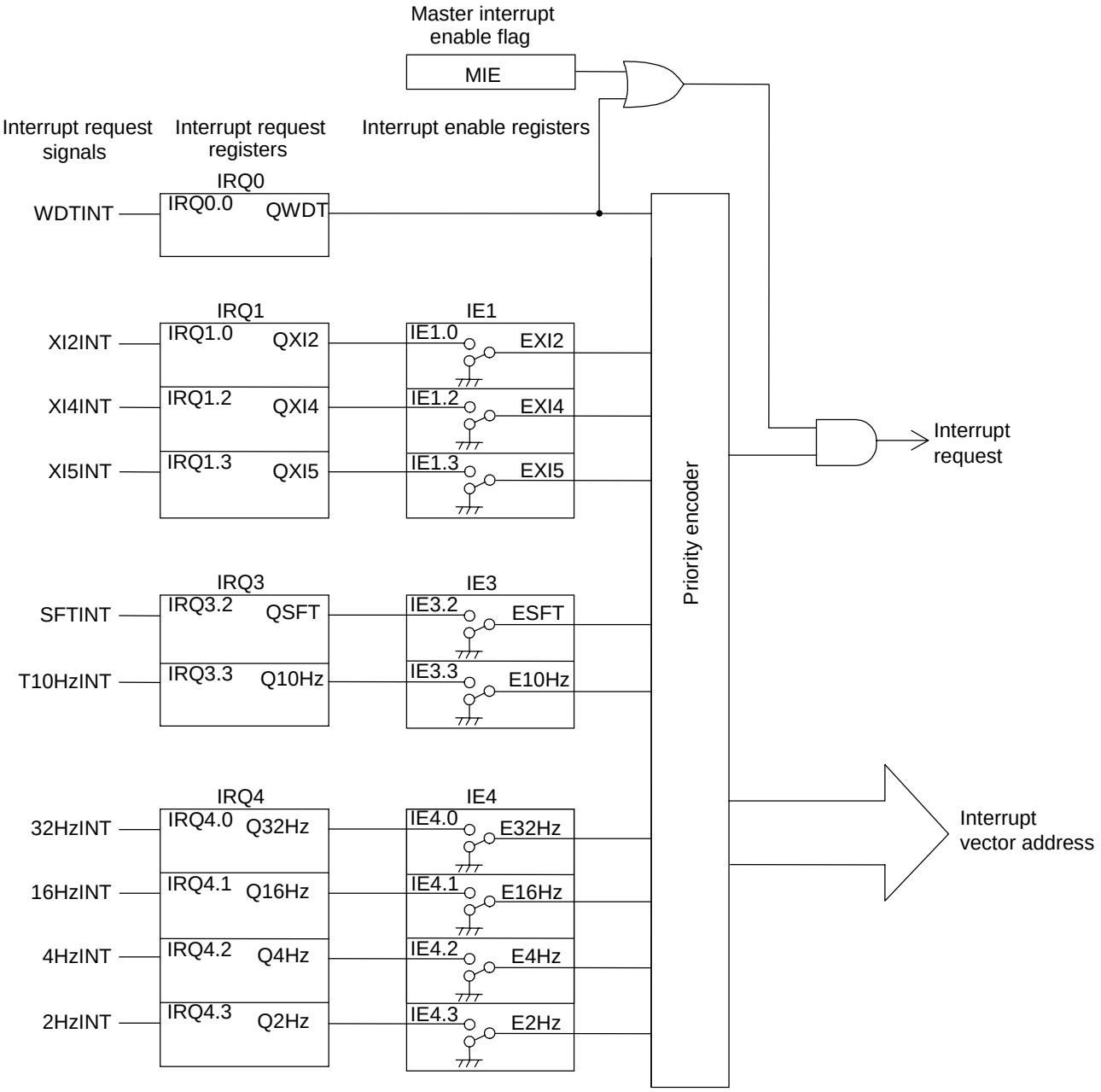


Figure 5-1 MSM63184A Interrupt Control Equivalent Circuit

5.2 Interrupt Sequence

5.2.1 Interrupt processing

Execution shifts to interrupt processing when the MIE flag is set to "1" and an individual interrupt factor is generated.

The watchdog timer interrupt is a non-maskable interrupt, and execution will shift to interrupt processing regardless of the MIE flag state.

When an interrupt is generated the following processing will be executed. Interrupt processing is executed in zero machine cycles.

(1) MIE flag and individual interrupt request flag reset to "0".
(2) Program counter (PC) saved to call stack.
(3) Call stack pointer (SP) incremented by one. (SP←SP+1)
(4) Interrupt head address loaded into program counter (PC).

Figure 5-2 indicates the content of the stack after an interrupt is generated.

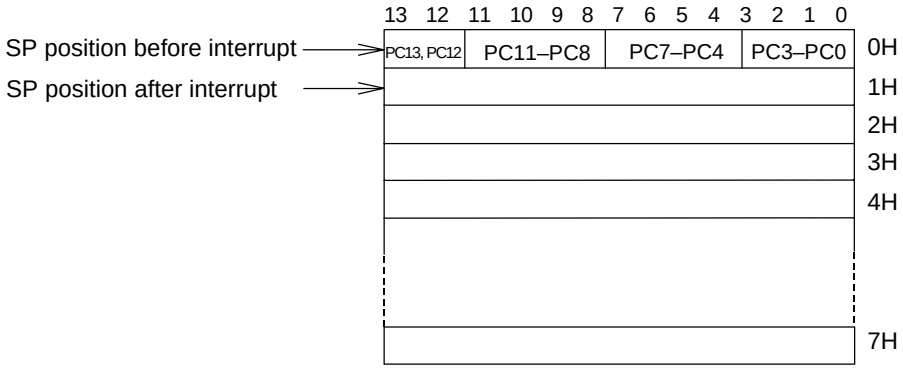


Figure 5-2 Call Stack Content after Interrupt Generation

5.2.2 Return from interrupt routine

Return from a watchdog timer interrupt routine is performed with an "RTNMI" instruction.

Return from all other interrupt routines is performed with an "RTI" instruction.

Execution of "RTI" and "RTNMI" instructions both require 1 machine cycle.

When returning from an interrupt routine, the CPU performs the following processes.

(1) The call stack pointer (SP) is decremented by 1. (SP←SP–1)
(2) MIE is set to "1" (when an "RTNMI" instruction is used, MIE is restored to its state prior to the interrupt).
(3) 1 is added to the call stack contents and that value is loaded into the program counter (PC).

Notes:

- While the MIE flag is "0" (interrupt disabled state), if a watchdog timer interrupt is processed and an "RTI" instruction is executed, the MIE flag will be set to "1" and interrupts enabled.
- Use "RTNMI" instructions to return from watchdog timer interrupts only. Use "RTI" instructions for normal interrupts.

5.2.3 Interrupt hold instructions

Interrupt requests are not received after execution of interrupt hold instruction.

The interrupt hold instructions follow.

- ROM table reference instructions
- External memory transfer instructions.
- Stack operation instructions
- Jump instructions
- Conditional branch instructions
- Call/return instructions
- "EI" (set MIE flag) instructions, "DI" (clear MIE flag) instructions and "MSA cadr14" (start melody output) instructions within control instructions

Note:

If interrupt hold instructions are to be used consecutively, consider that an interrupt, when generated, will be put on hold for a certain amount of time before the interrupt routine begins. Interrupt requests are received after execution of an instruction other than interrupt hold instructions.

5.3 Interrupt Control Registers

5.3.1 Interrupt request registers (IRQ0, IRQ1, IRQ3, IRQ4)

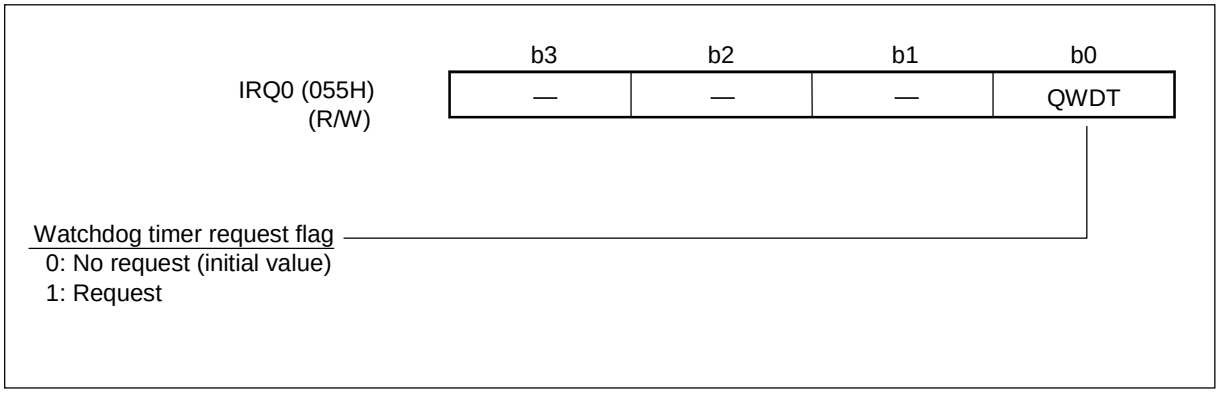
The interrupt request registers (IRQ0, IRQ1, IRQ3, IRQ4) are 4-bit registers. When an interrupt request is generated the corresponding bit is set to "1" in the first half of the S1 state of the next instruction. If the corresponding flag of the interrupt enable register (IE1, IE3, IE4) is set to "1" and the master interrupt enable flag (MIE) is also set to "1", an interrupt request will be sent to the CPU.

The watchdog timer interrupt is a non-maskable interrupt, not dependent on the interrupt enable register or master interrupt enable flag (MIE).

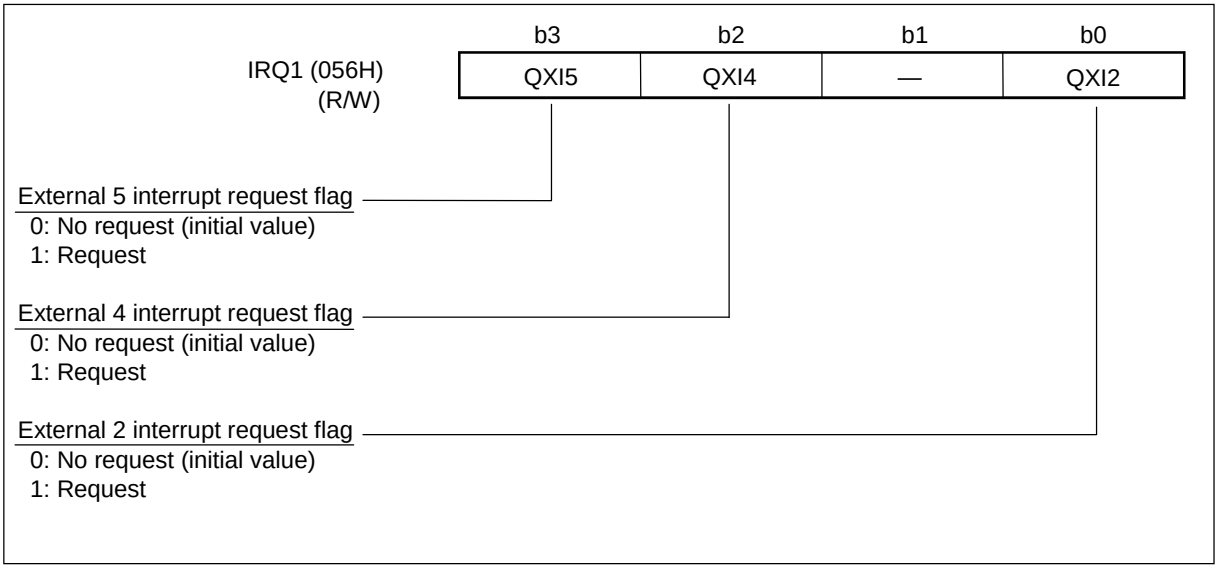
Setting the interrupt request register to "1" allows software interrupts to be generated.

When an interrupt request is accepted, hardware resets the corresponding bit of IRQ0, IRQ1, IRQ3, IRQ4 to 0.

IRQ0, IRQ1, IRQ3, and IRQ4 are initialized to 0H at system reset.



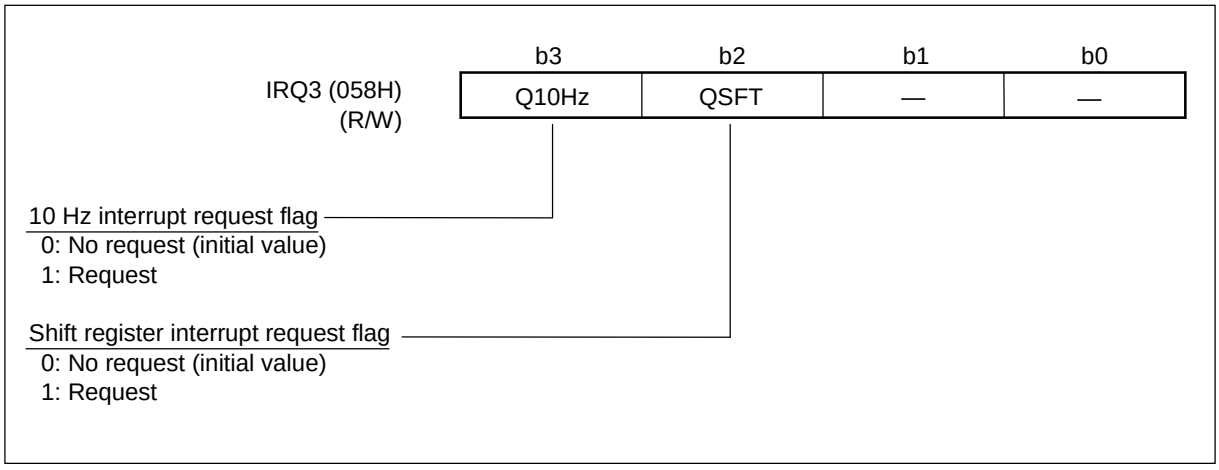
Bit 0: QWDT
Watchdog timer interrupt request flag. When the watchdog timer is started and an overflow occurs, an interrupt is requested. The watchdog timer is a non-maskable interrupt not dependent on the interrupt enable register or master interrupt enable flag.



Bit 3: QXI5
The external 5 interrupt request flag. The external 5 interrupt is an 8-bit OR input external interrupt assigned to ports 0 and 1.

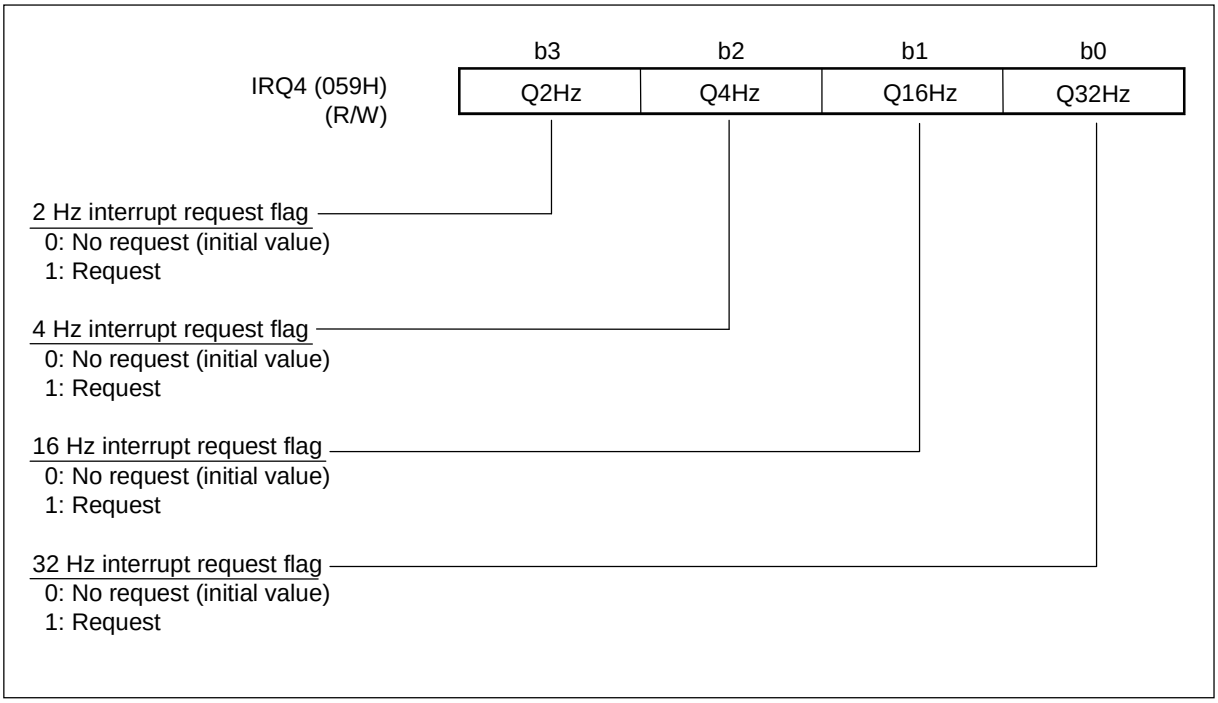
Bit 2: QXI4
The external 4 interrupt request flag. It is an external interrupt allocated to port 8.3.

Bit 0: QXI2
The external 2 interrupt request flag. It is an external interrupt allocated to port E.3.



Bit 3: Q10Hz
The 10 Hz interrupt request flag. This interrupt is requested when the 10 Hz counter in the 1/100 timer overflows.

Bit 2: QSFT
The shift register interrupt request flag. This interrupt is requested when shift register 8-bit data transfer is complete.



Bit 3: Q2Hz
The 2 Hz interrupt request flag. The 2 Hz interrupt is requested when at the 2 Hz output falling edge of the time base counter.

Bit 2: Q4Hz
The 4 Hz interrupt request flag. The 4 Hz interrupt is requested when at the 4 Hz output falling edge of the time base counter.

Bit 1: Q16Hz
The 16 Hz interrupt request flag. The 16 Hz interrupt is requested when at the 16 Hz output falling edge of the time base counter.

Bit 0: Q32Hz
The 32 Hz interrupt request flag. The 32 Hz interrupt is requested when at the 32 Hz output falling edge of the time base counter.

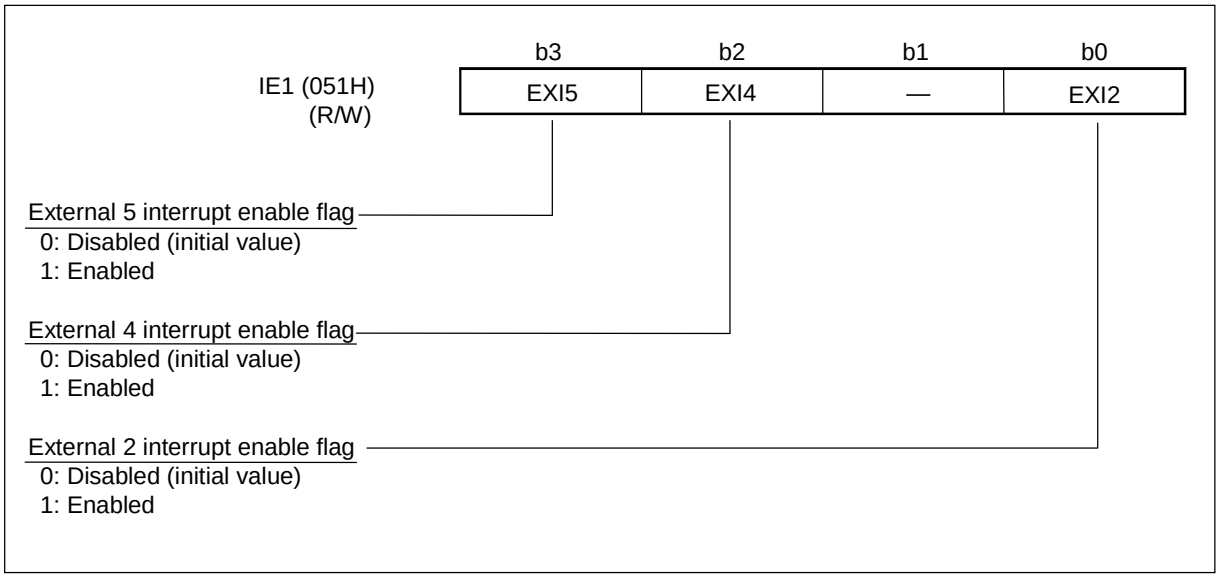
5.3.2 Interrupt enable registers (IE1, IE3, IE4)

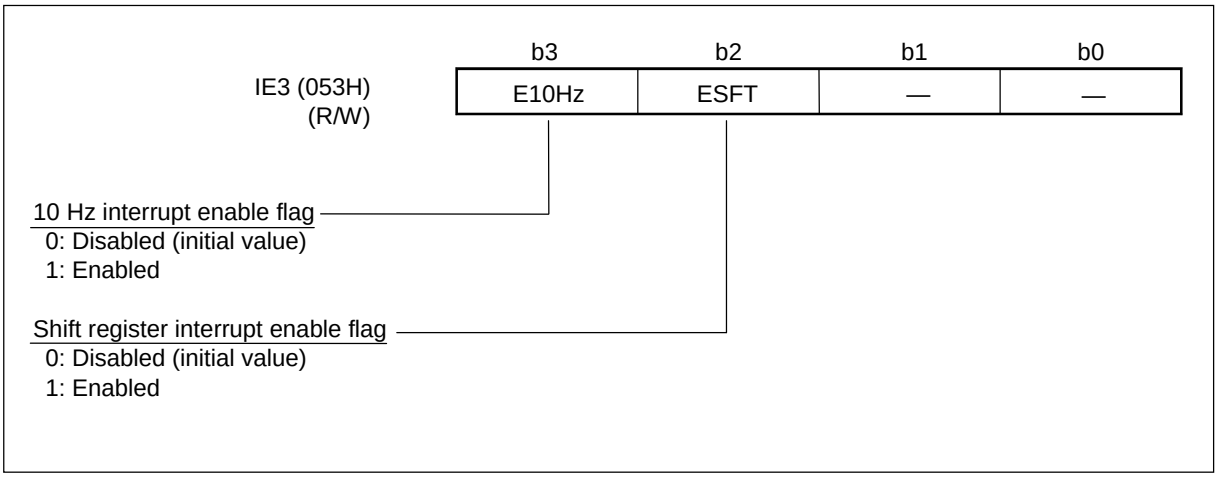
The interrupt enable registers (IE1, IE3, IE4) are 4-bit registers, and determine whether or not an interrupt request is issued to the CPU through an AND operation with the bit corresponding to the interrupt request registers (IRQ1, IRQ3, IRQ4). The watchdog timer interrupt is a non-maskable interrupt, and is therefore not dependent on the interrupt enable registers and the master interrupt enable flag (MIE).

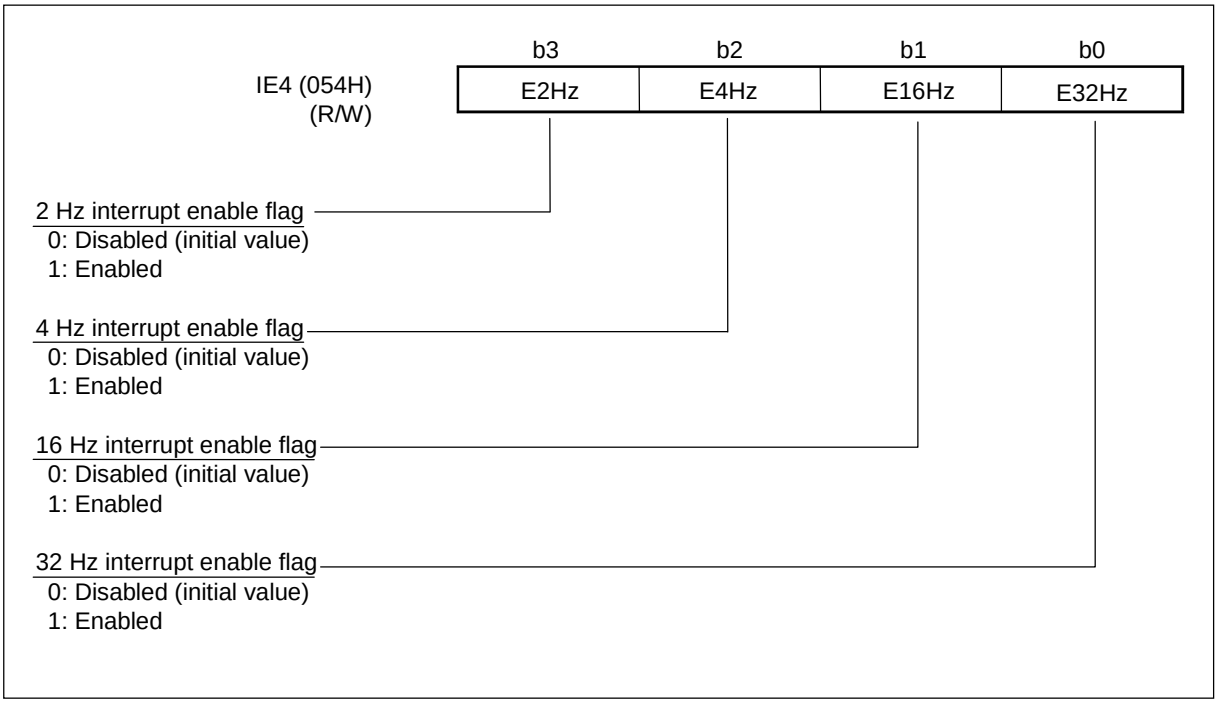
If multiple interrupts are requested simultaneously, the CPU will accept them in the priority order indicated in Table 5-1, and the interrupts with lower priorities will be held.

When an interrupt is accepted the master interrupt enable flag is reset to 0, but the related bits of IE1, IE3, and IE4 are not reset.

IE1, IE3, and IE4 are initialized to 0H at system reset.




IE3 (053H)
(R/W)
b3
b2
b1
b0
E10Hz
ESFT
—
—
10 Hz interrupt enable flag
0: Disabled (initial value)
1: Enabled
Shift register interrupt enable flag
0: Disabled (initial value)
1: Enabled


IE4 (054H)
(R/W)
b3
b2
b1
b0
E2Hz
E4Hz
E16Hz
E32Hz
2 Hz interrupt enable flag
0: Disabled (initial value)
1: Enabled
4 Hz interrupt enable flag
0: Disabled (initial value)
1: Enabled
16 Hz interrupt enable flag
0: Disabled (initial value)
1: Enabled
32 Hz interrupt enable flag
0: Disabled (initial value)
1: Enabled

Chapter 6

MSM63188A Interrupt (INT188)

Chapter 6 MSM63188A Interrupt (INT188)

6.1 Overview

The MSM63188A supports 17 interrupt factors: 4 external port interrupts and 13 internal interrupts.

With the exception of the watchdog timer interrupt, interrupt enable/disable is controlled by the master interrupt enable flag (MIE) and the individual interrupt enable registers (IE0 to IE4). When interrupt conditions are met, the interrupt routine is executed from the interrupt start address.

Table 6-1 indicates a list of interrupt factors, and Figure 6-1 shows the interrupt control equivalent circuit.

Table 6-1 List of Interrupt Factors

Priority	Interrupt factor	Symbol	Interrupt start address
1	Watchdog timer interrupt	WDTINT	0010H
2	Melody end interrupt	MDINT	0012H
3	External 0 interrupt (PB 4-bit OR input)	XI0INT	0014H
4	External 1 interrupt (PC 4-bit OR input)	XI1INT	0016H
5	External 4 interrupt (P8.3)	XI4INT	001CH
6	External 5 interrupt (P0, P1 8-bit OR input)	XI5INT	001EH
7	Timer 0 interrupt	TM0INT	0020H
8	Timer 1 interrupt	TM1INT	0022H
9	Timer 2 interrupt	TM2INT	0024H
10	Timer 3 interrupt	TM3INT	0026H
11	Serial port receive interrupt	SRINT	0028H
12	Serial port send interrupt	STINT	002AH
13	T10 Hz interrupt	T10HzINT	002EH
14	32 Hz interrupt	32HzINT	0030H
15	16 Hz interrupt	16HzINT	0032H
16	4 Hz interrupt	4HzINT	0034H
17	2 Hz interrupt	2HzINT	0036H

If multiple interrupts are detected simultaneously, the lowest interrupt start address is given priority.

For details on interrupt operation, refer to Chapter 8 (Time Base Counter), Chapter 9 (Timers), Chapter 10 (100 Hz Timer Counter), Chapter 11 (Watchdog Timer), Chapter 12 (Ports), Chapter 14 (Melody Driver), and Chapter 16 (Serial Port).

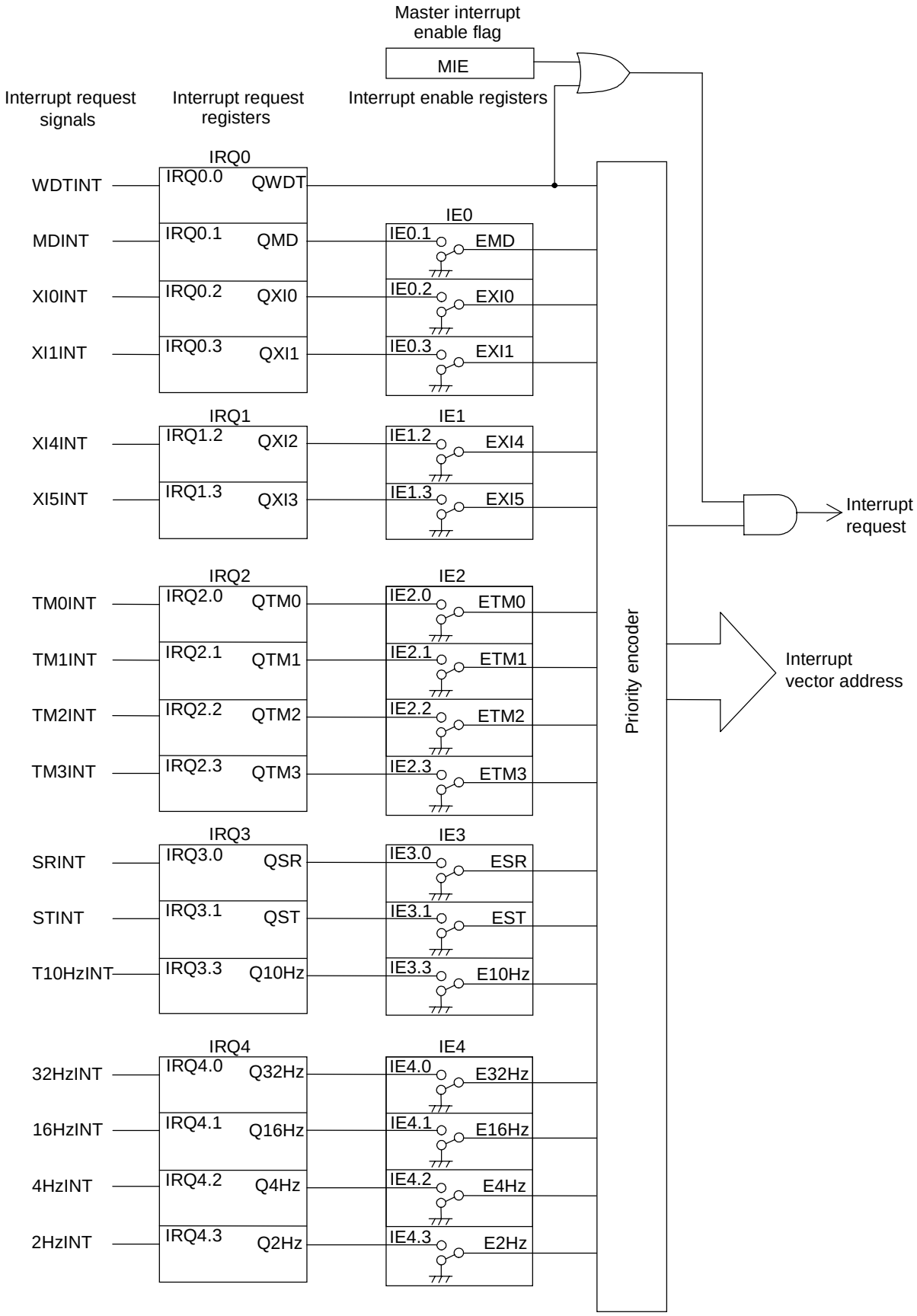


Figure 6-1 MSM63188A Interrupt Control Equivalent Circuit

6.2 Interrupt Sequence

6.2.1 Interrupt processing

Execution shifts to interrupt processing when the MIE flag is set to "1" and an individual interrupt factor is generated.

The watchdog timer interrupt is a non-maskable interrupt, and execution will shift to interrupt processing regardless of the MIE flag state.

When an interrupt is generated the following processing will be executed. Interrupt processing is executed in zero machine cycles.

(1) MIE flag and individual interrupt request flag reset to "0".
(2) Program counter (PC) saved to call stack.
(3) Call stack pointer (SP) incremented by one. (SP←SP+1)
(4) Interrupt head address loaded into program counter (PC).

Figure 6-2 indicates the content of the stack after an interrupt is generated.

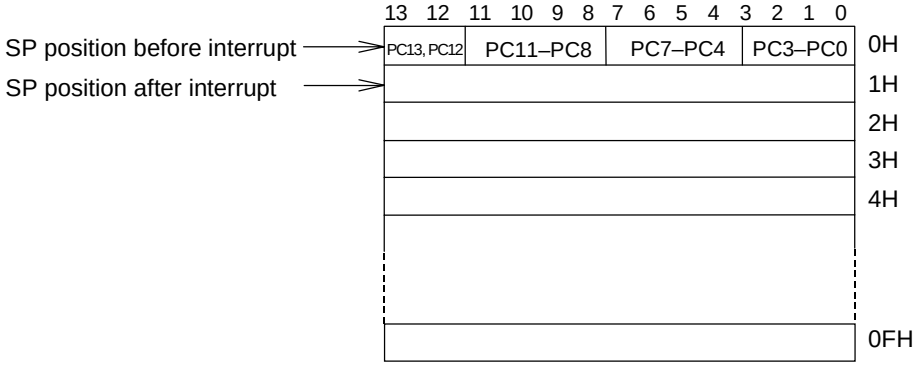


Figure 6-2 Call Stack Content after Interrupt Generation

6.2.2 Return from interrupt routine

Return from a watchdog timer interrupt routine is performed with an "RTNMI" instruction.

Return from all other interrupt routines is performed with an "RTI" instruction.

Execution of "RTI" and "RTNMI" instructions both require 1 machine cycle.

When returning from an interrupt routine, the CPU performs the following processes.

(1) The call stack pointer (SP) is decremented by 1. (SP←SP–1)
(2) MIE is set to "1" (when an "RTNMI" instruction is used, MIE is restored to its state prior to the interrupt).
(3) 1 is added to the call stack contents and that value is loaded into the program counter (PC).

Notes:

- While the MIE flag is "0" (interrupt disabled state), if a watchdog timer interrupt is processed and an "RTI" instruction is executed, the MIE flag will be set to "1" and interrupts enabled.
- Use "RTNMI" instructions to return from watchdog timer interrupts only. Use "RTI" instructions for normal interrupts.

6.2.3 Interrupt hold instructions

Interrupt requests are not received after execution of interrupt hold instruction.

The interrupt hold instructions follow.

- ROM table reference instructions
- External memory transfer instruction
- Stack operation instructions
- Jump instructions
- Conditional branch instructions
- Call/return instructions
- "EI" (set MIE flag) instructions, "DI" (clear MIE flag) instructions and "MSA cadr14" (start melody output) instructions within control instructions

Note:

If interrupt hold instructions are to be used consecutively, consider that an interrupt, when generated, will be put on hold for a certain amount of time before the interrupt routine begins. Interrupt requests are received after execution of an instruction other than interrupt hold instructions.

6.3 Interrupt Control Registers

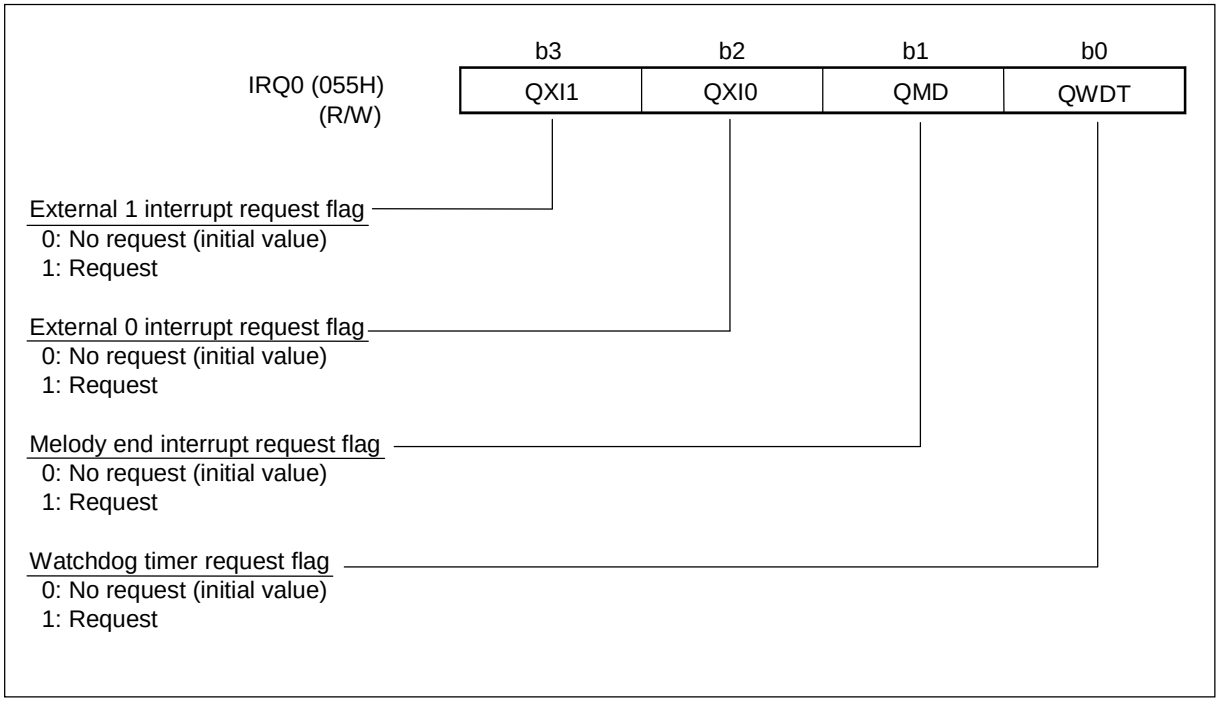
6.3.1 Interrupt request registers (IRQ0 to IRQ4)

The interrupt request registers (IRQ0 to IRQ4) are 4-bit registers. When an interrupt request is generated the corresponding bit is set to "1" in the first half of the S1 state of the next instruction. If the corresponding flag of the interrupt enable register (IE0 to IE4) is set to "1" and the master interrupt enable flag (MIE) is also set to "1", an interrupt request will be sent to the CPU.

The watchdog timer interrupt is a non-maskable interrupt, not dependent on the interrupt enable register or master interrupt enable flag (MIE).

Setting the interrupt request register to "1" allows software interrupts to be generated.

When an interrupt request is accepted, hardware resets the corresponding bit of IRQ0 to IRQ4 to "0". IRQ0 to IRQ4 are initialized to 0H at system reset.

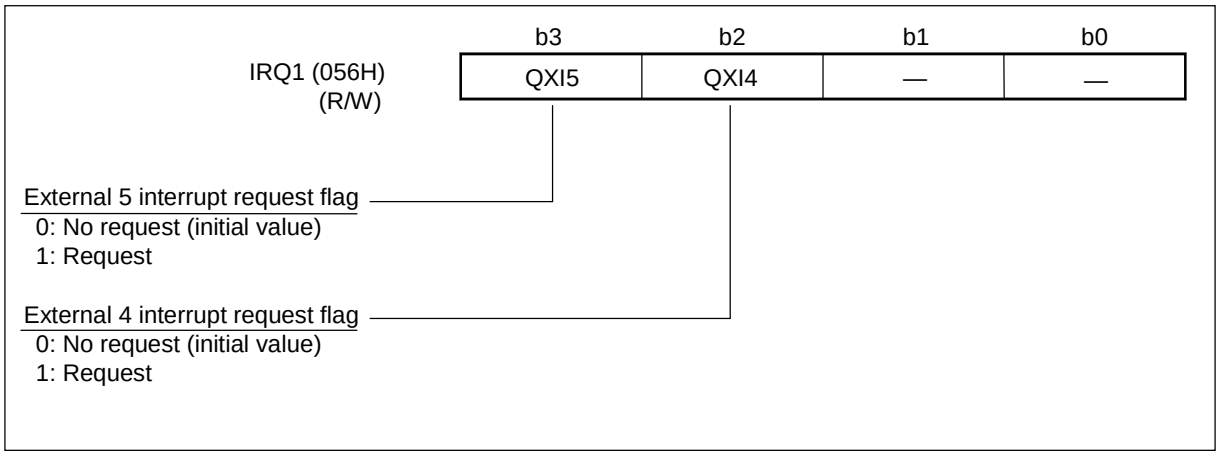


Bit 3: QXI1
The external 1 interrupt request flag. The external 1 interrupt is a 4-bit OR input external interrupt allocated to port C.

Bit 2: QXI0
The external 0 interrupt request flag. The external 0 interrupt is a 4-bit OR input external interrupt allocated to port B.

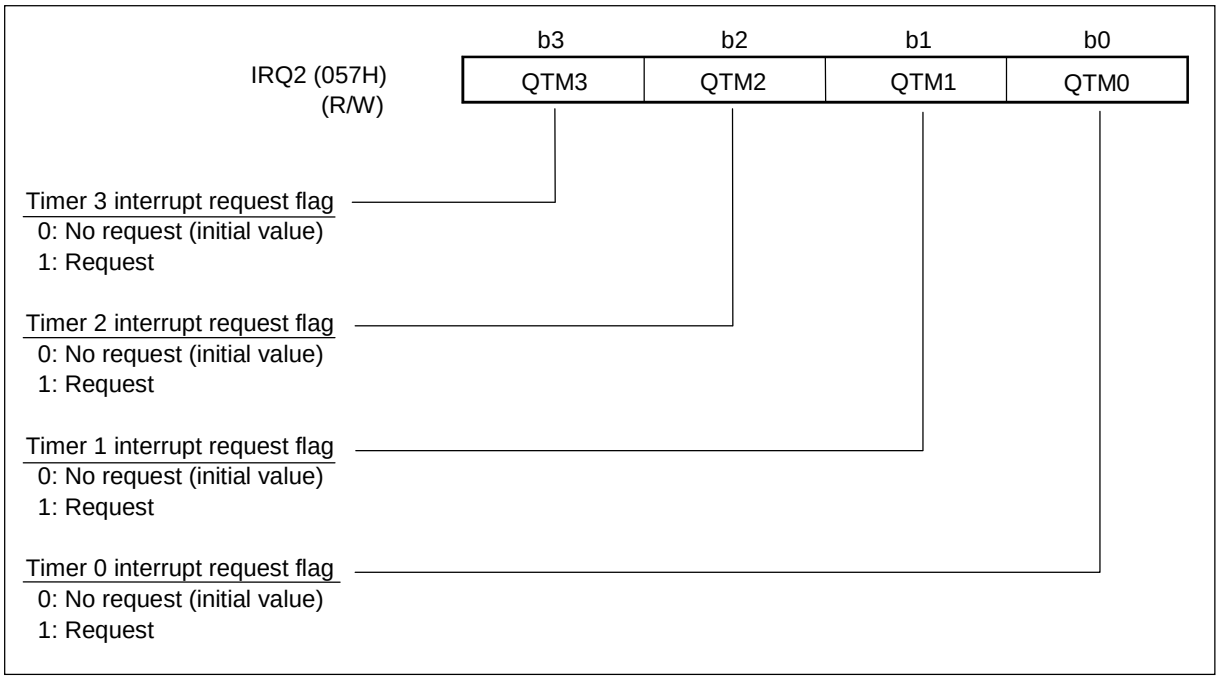
Bit 1: QMD
The melody end interrupt request flag. The melody end interrupt is requested when the melody driver outputs the last melody data (END bit = 1).

Bit 0: QWDT
Watchdog timer interrupt request flag. When the watchdog timer is started and an overflow occurs, the interrupt is requested. The watchdog timer is a non-maskable interrupt not dependent on the interrupt enable register or master interrupt enable flag.



Bit 3: QXI5
The external 5 interrupt request flag. The external 5 interrupt is an 8-bit OR input external interrupt assigned to ports 0 and 1.

Bit 2: QXI4
The external 4 interrupt request flag. It is an external interrupt allocated to port 8.3.

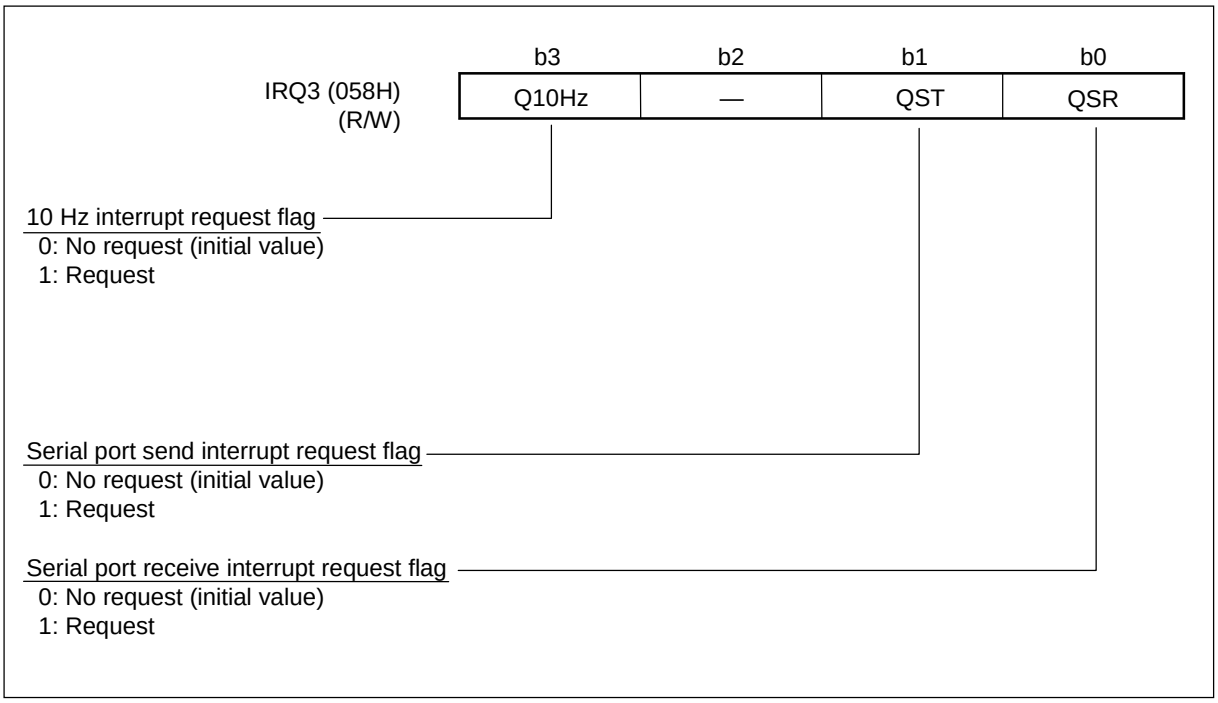


Bit 3: QTM3
Timer 3 interrupt request flag. The timer 3 interrupt is requested when timer 3 overflows.

Bit 2: QTM2
Timer 2 interrupt request flag. The timer 2 interrupt is requested when timer 2 overflows.

Bit 1: QTM1
Timer 1 interrupt request flag. The timer 1 interrupt is requested when timer 1 overflows.

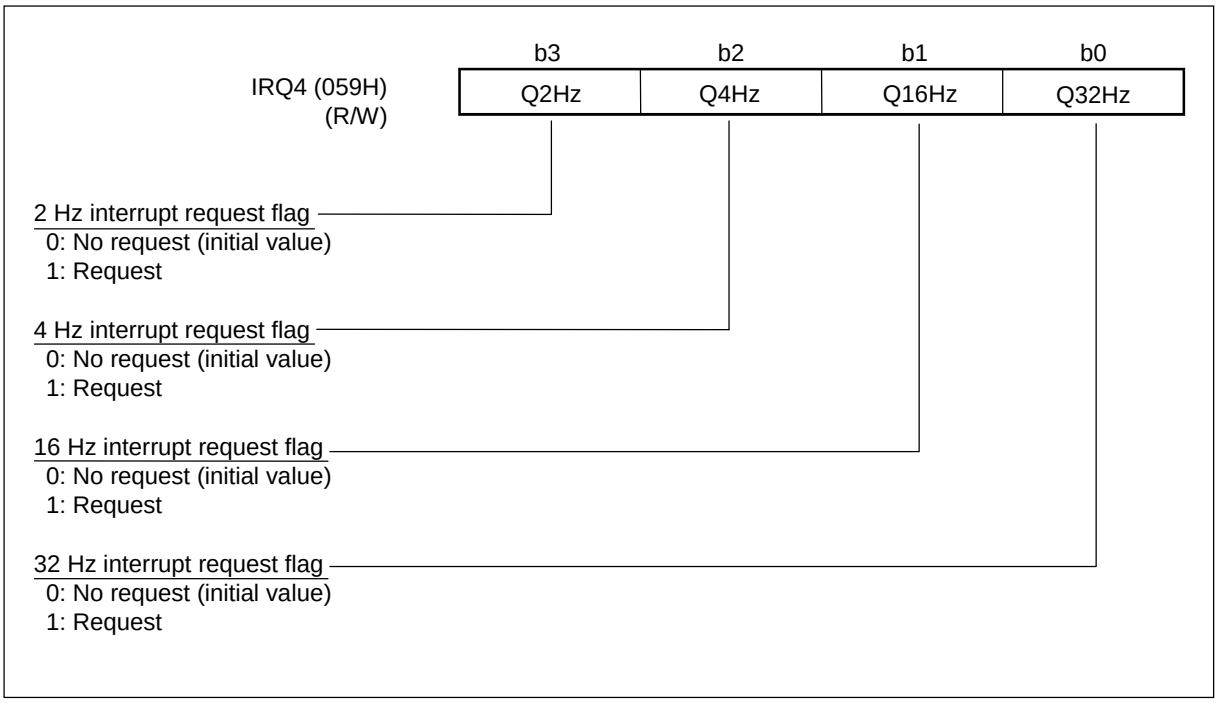
Bit 0: QTM0
Timer 0 interrupt request flag. The timer 0 interrupt is requested when timer 0 overflows.



Bit 3: Q10Hz
The 10 Hz interrupt request flag. This interrupt is requested when the 10 Hz counter in the 1/100 timer overflows.

Bit 1: QST
The serial port send interrupt request flag. This interrupt is requested when serial port send is complete.

Bit 0: QSR
The serial port receive interrupt request flag. This interrupt is requested when serial port reception is complete.



Bit 3: Q2Hz
The 2 Hz interrupt request flag. The 2 Hz interrupt is requested when at the 2 Hz output falling edge of the time base counter.

Bit 2: Q4Hz
The 4 Hz interrupt request flag. The 4 Hz interrupt is requested when at the 4 Hz output falling edge of the time base counter.

Bit 1: Q16Hz
The 16 Hz interrupt request flag. The 16 Hz interrupt is requested when at the 16 Hz output falling edge of the time base counter.

Bit 0: Q32Hz
The 32 Hz interrupt request flag. The 32 Hz interrupt is requested when at the 32 Hz output falling edge of the time base counter.

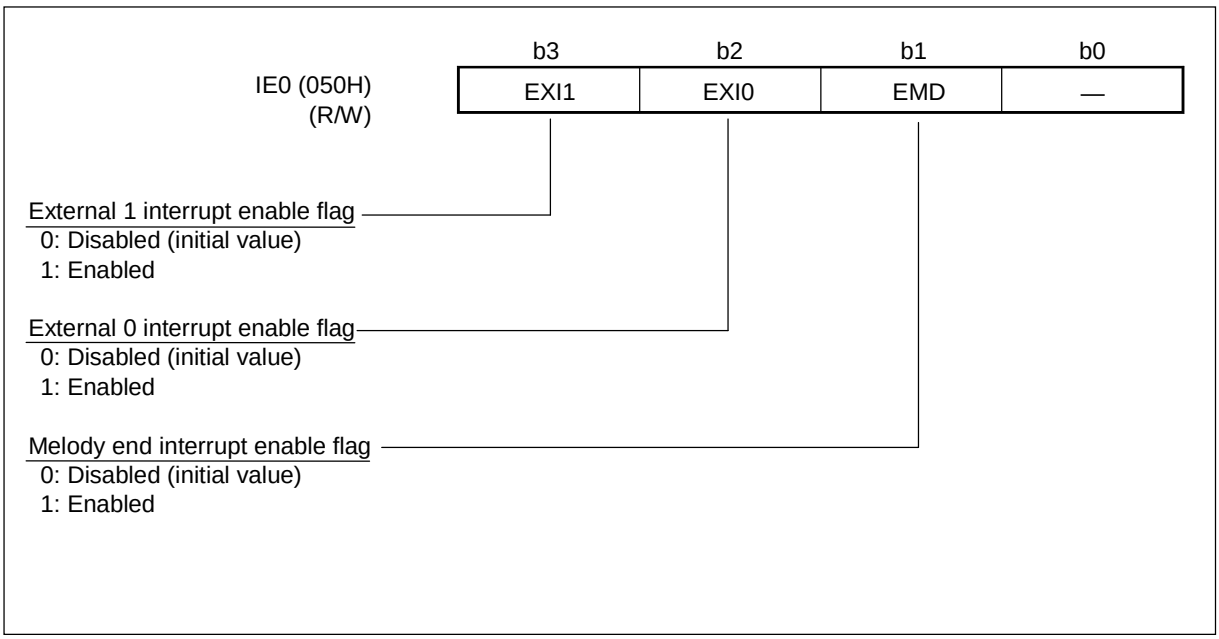
6.3.2 Interrupt enable registers (IE0 to IE4)

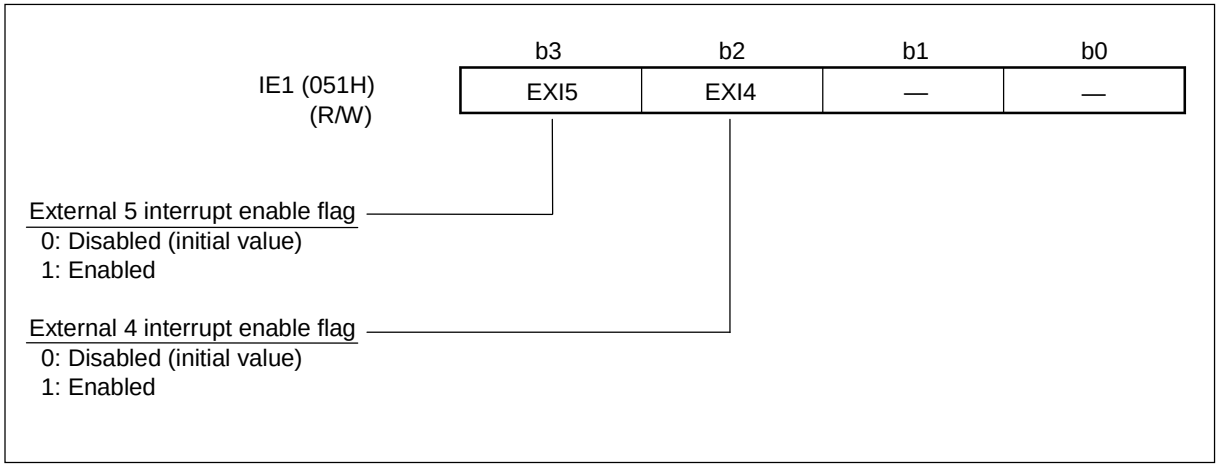
The interrupt enable registers (IE0 to IE4) are 4-bit registers, and determine whether or not an interrupt request is issued to the CPU through an AND operation with the bit corresponding to the interrupt request register (IRQ0 to IRQ4). The watchdog timer interrupt is a non-maskable interrupt, and is therefore not dependent on the interrupt enable registers and the master interrupt enable flag (MIE).

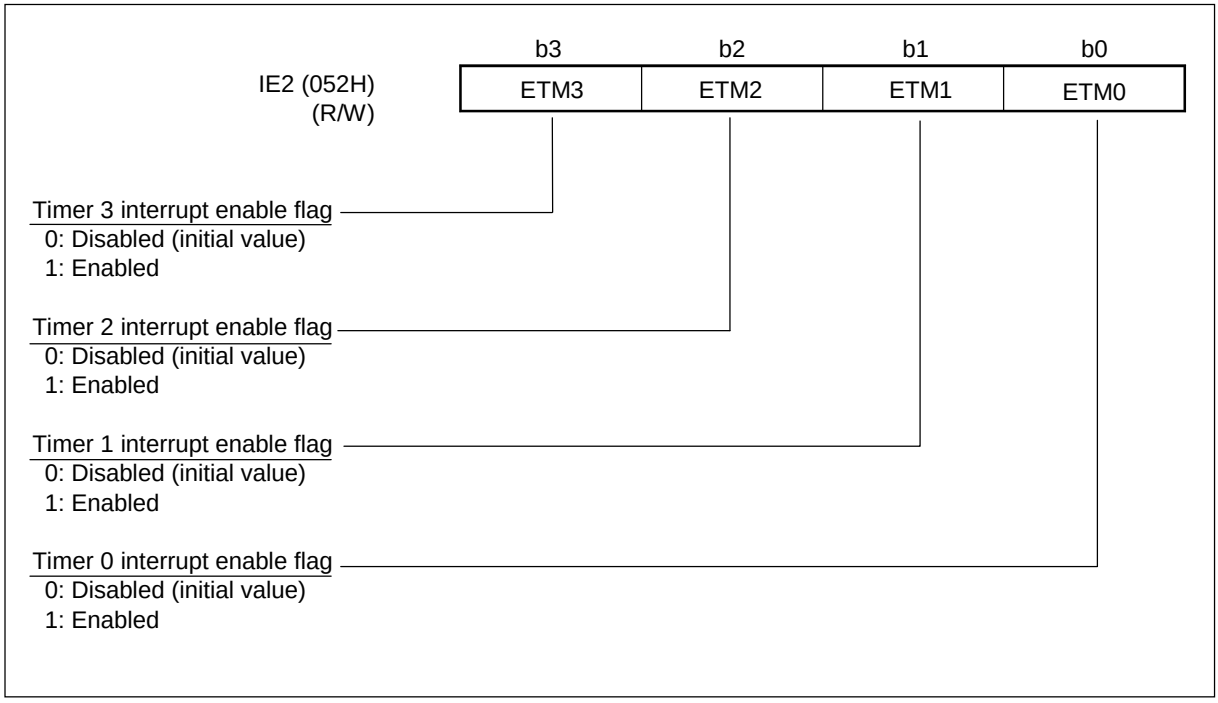
If multiple interrupts are requested simultaneously, the CPU will accept them in the priority order indicated in Table 6-1, and the interrupts with lower priorities will be held.

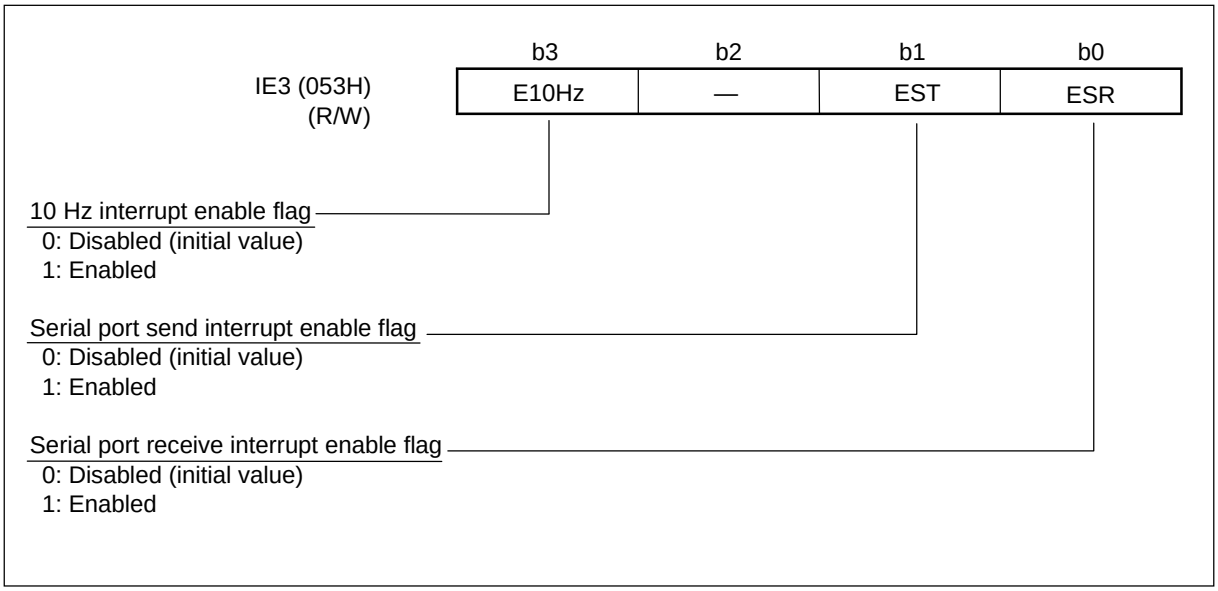
When an interrupt is accepted the master interrupt enable flag is reset to "0", but the related bits of IE0 to IE4 are not reset.

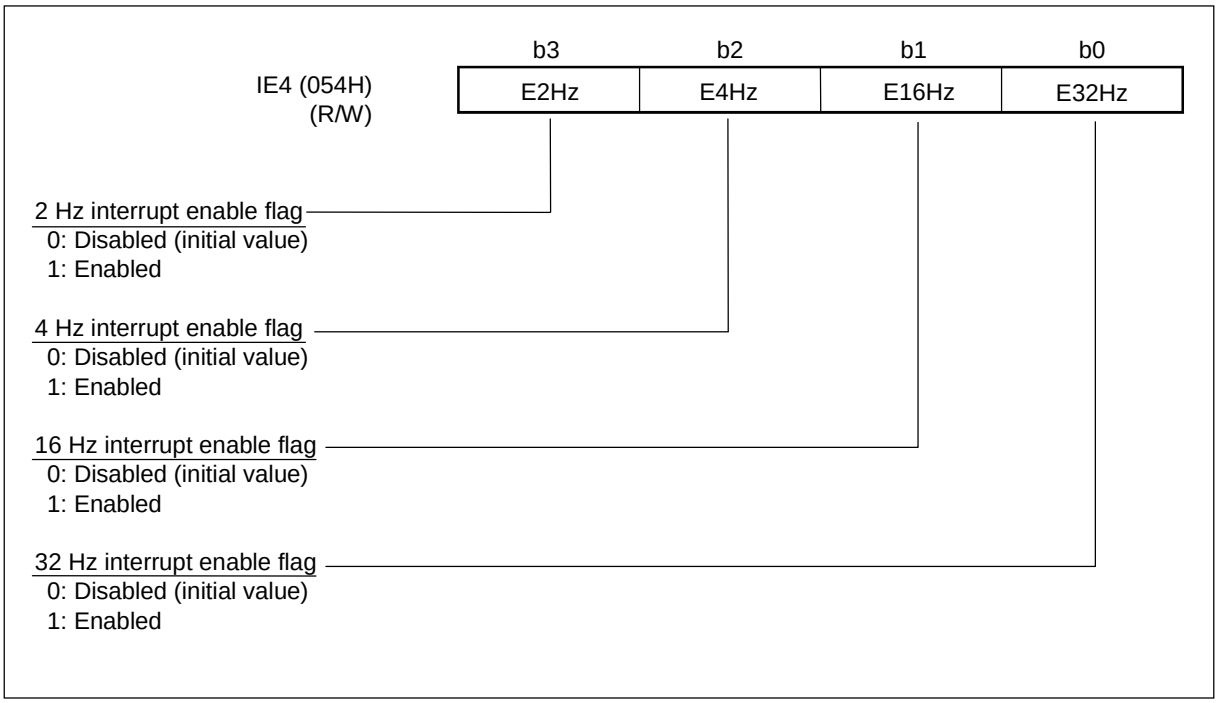
IE0 to IE4 are initialized to 0H at system reset.




IE1 (051H)
(R/W)
b3
b2
b1
b0
EXI5
EXI4
—
—
External 5 interrupt enable flag
0: Disabled (initial value)
1: Enabled
External 4 interrupt enable flag
0: Disabled (initial value)
1: Enabled


IE2 (052H)
(R/W)
b3
b2
b1
b0
ETM3
ETM2
ETM1
ETM0
Timer 3 interrupt enable flag
0: Disabled (initial value)
1: Enabled
Timer 2 interrupt enable flag
0: Disabled (initial value)
1: Enabled
Timer 1 interrupt enable flag
0: Disabled (initial value)
1: Enabled
Timer 0 interrupt enable flag
0: Disabled (initial value)
1: Enabled


IE3 (053H)
(R/W)
b3
b2
b1
b0
E10Hz
—
EST
ESR
10 Hz interrupt enable flag
0: Disabled (initial value)
1: Enabled
Serial port send interrupt enable flag
0: Disabled (initial value)
1: Enabled
Serial port receive interrupt enable flag
0: Disabled (initial value)
1: Enabled


IE4 (054H)
(R/W)
b3
b2
b1
b0
E2Hz
E4Hz
E16Hz
E32Hz
2 Hz interrupt enable flag
0: Disabled (initial value)
1: Enabled
4 Hz interrupt enable flag
0: Disabled (initial value)
1: Enabled
16 Hz interrupt enable flag
0: Disabled (initial value)
1: Enabled
32 Hz interrupt enable flag
0: Disabled (initial value)
1: Enabled

Chapter 7

Clock Generator Circuit (OSC)

Chapter 7 Clock Generator Circuit (OSC)

7.1 Overview

The clock generator circuit (OSC) consists of a 32.768 kHz crystal oscillator circuit, a high-speed clock generator circuit and a clock controller and generates the system clock (CLK), the time base clock (TBCCLK) and the high-speed clock (HSCLK). The high-speed clock generator circuit has two modes: RC oscillation and ceramic oscillation (either one is selected by software).

The system clock is the basic operation clock for the CPU, and the time base clock is the basic operation clock for counters and so on.

The system clock frequency is set by the frequency control register (FCON) to either the crystal oscillator circuit output (TBCCLK) or the output of the high-speed clock (HSCLK) generator.

The high-speed clock generator circuit mode is also controlled by the frequency control register (FCON).

7.2 Clock Generator Circuit

The clock generator circuit is shown in Figure 7-1.

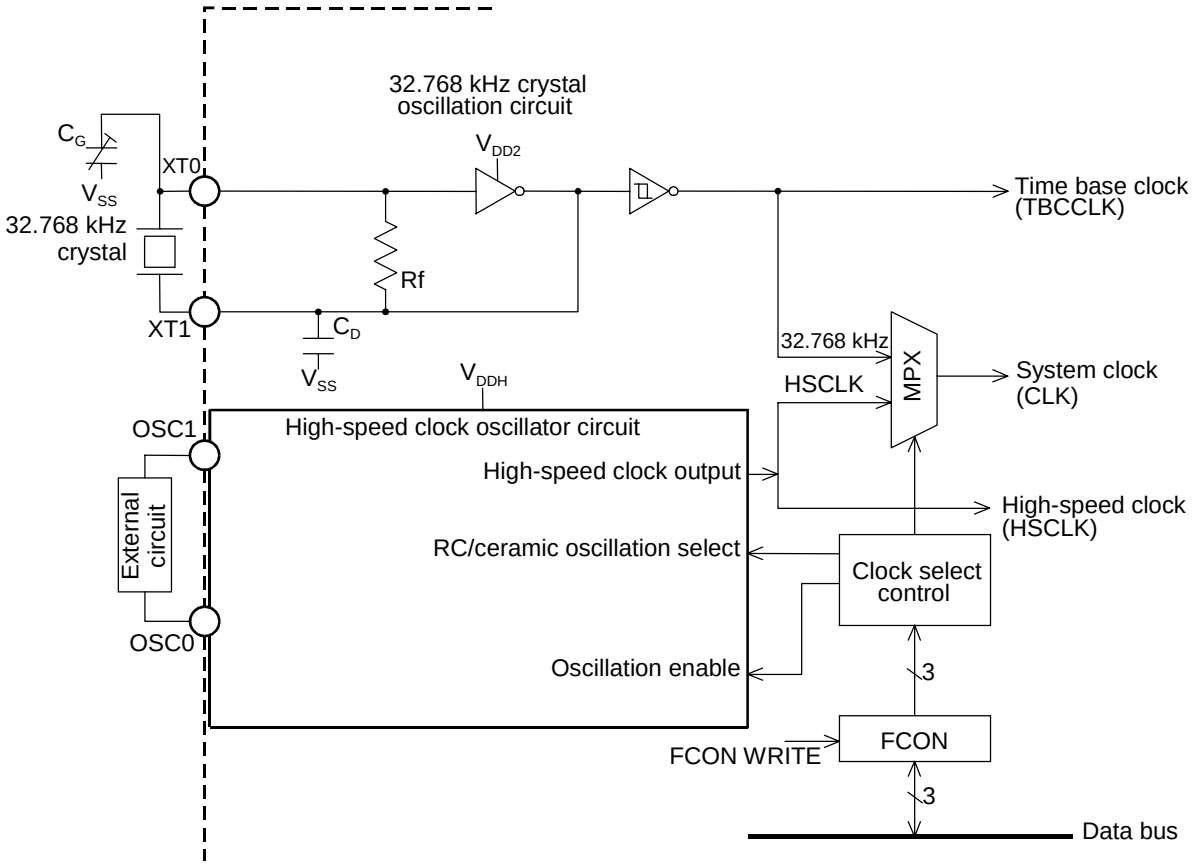


Figure 7-1 Clock Generator Circuit

7.3 Crystal Oscillator Circuit

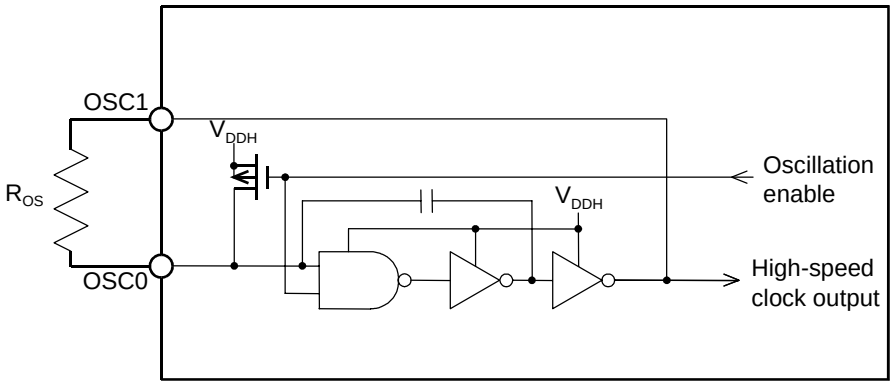
The 32.768 kHz crystal oscillation circuit oscillates with an external 32.768 kHz crystal oscillator. An external capacitor can be used to adjust the frequency.

7.4 High-speed Clock Oscillator Circuit

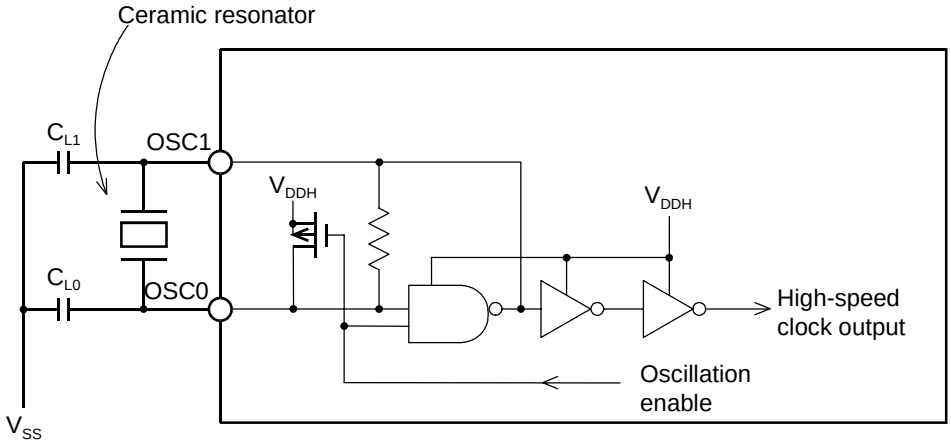
The high-speed clock oscillator circuit has two modes (RC and ceramic oscillation modes), selected by bit 2 (OSCSEL) of the frequency control register (FCON). When OSCCEL is reset to "0" the RC oscillation mode is selected. When set to "1", the ceramic oscillation mode is selected. The peak oscillation frequency is 2 MHz.

In the RC oscillation mode, external resistance R_{OS} is connected (Figure 7-2a).

In the ceramic oscillation mode (Figure 7-2b), an external ceramic resonator and capacitors are connected.



(a) RC oscillation mode external circuit



(b) Ceramic oscillation mode external circuit

Figure 7-2 High-Speed Clock Oscillation External Circuits

Table 7-1 shows the typical oscillation frequencies in the RC oscillation mode and Table 7-2 shows typical external component parts required in the ceramic oscillation mode.

Table 7-1 Typical Oscillation Frequencies in the RC Oscillation Mode

R_{OS} (kΩ)	V_{DD} (V)	Backup	f_{OSC} (kHz)
51	1.5	ON	760 ±30%
100	1.5	ON	440 ±30%
51	3.0	OFF	795 ±30%
100	3.0	OFF	450 ±30%

Table 7-2 Typical External Component Parts Required in the Ceramic Oscillation Mode

C_{L0} (pF)	C_{L1} (pF)	Ceramic unit
330	470	CSB200D (200 kHz)*
220	220	CSB300D (300 kHz)*
150	150	CSB500E (500 kHz)*
68	68	CSB1000J (1 MHz)*
30	30	CSA2.00MG (2 MHz)*

Note) *: Ceramic unit manufactured by Murata MFG. Co., Ltd.

7.5 System Clock Control

The system clock is the basic operation clock of the CPU.

The clock can be selected as follows with the CPUCLK (bit 0 of FCON) setting.

- CPUCLK = "0" (initial value)
  The output of the low-speed clock generator circuit (TBCCLK) is the system clock.
- CPUCLK = "1"
  The output of the high-speed clock generator circuit (HSCLK) is the system clock.

When HSCLK is selected as the system clock, the high-speed clock must be in the oscillating state (ENOSC = "1"). The crystal generator circuit will continue to oscillate even when the high-speed generator circuit is selected.

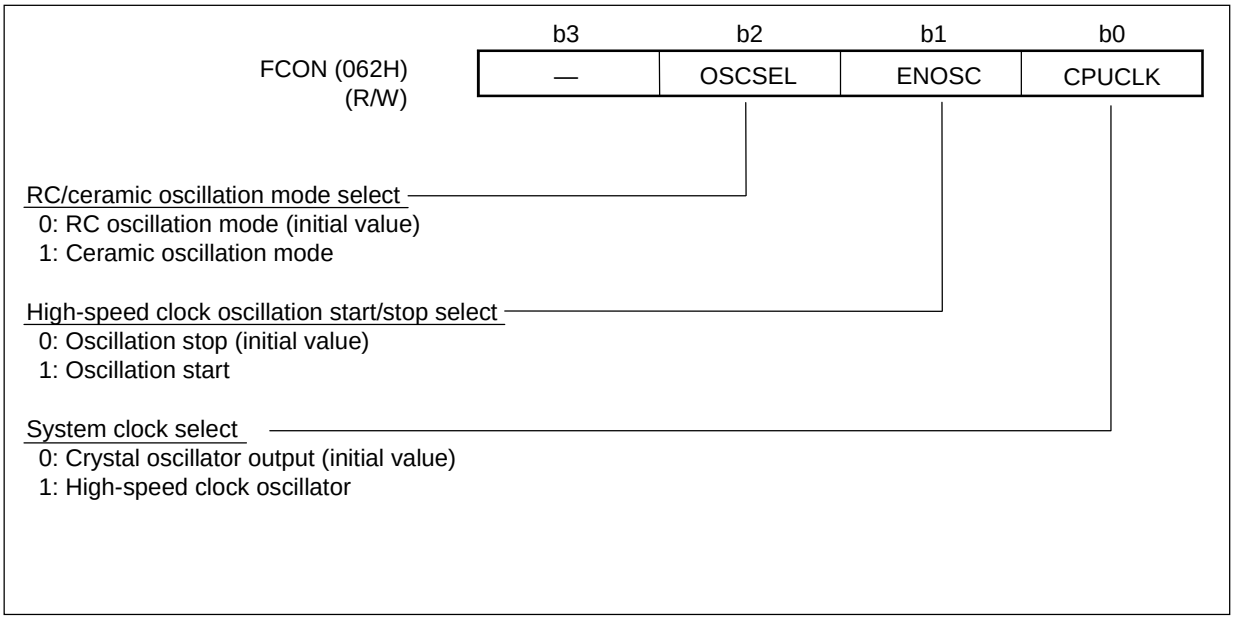
To reduce the total power consumption in applications that use the high-speed clock generator circuit, the following clock controls are generally implemented in software.

- During normal operation, the output of the low-speed clock generator circuit (CPUCLK = "0") should be the system clock.
- Only when high-speed operation is necessary should the high-speed clock oscillate (ENOSC = "1") and output of the high-speed clock generator circuit (CPUCLK = "1") should be selected.

For details of the system clock select timing, refer to section 7.7, "System Clock Select Timing".

7.6 Frequency Control Register (FCON)

The frequency control register (FCON) is a special function register (SFR) that handles system clock selection.



Bit 2: OSCSEL
This bit selects the RC or ceramic oscillation. This bit is reset to "0" at system reset, selecting the RC oscillation mode.

Bit 1: ENOSC
This bit starts and stops high-speed oscillation. This bit is reset to "0" at system reset, stopping high-speed clock oscillation circuit operation.

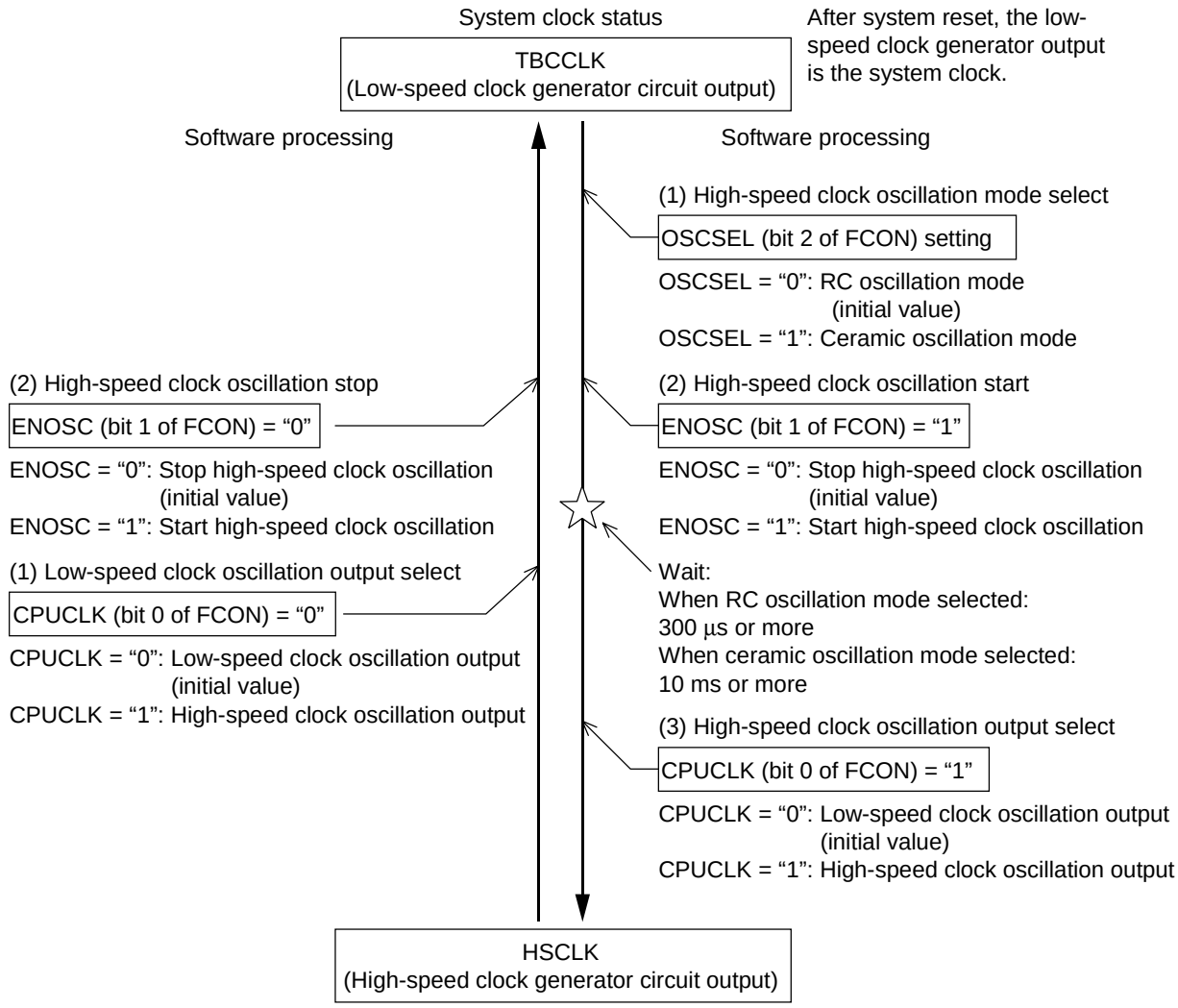
Bit 0: CPUCLK
This bit selects the system clock. This bit is reset to "0" at system reset, selecting the crystal oscillator output.

7.7 System Clock Select Timing

After system reset, the system clock is TBCCLK.

When high-speed operation is necessary, switch the system clock to HSCLK.

A flowchart of system clock operation is shown below.



When the ENOSC bit of the frequency control register (FCON) is set to "1", oscillation starts in the mode set by the OSCSEL bit. When the CPUCLK bit is set to "1" in this state, the internal logic supply (V_{DDL}) switches from the constant voltage circuit output level (about 1.3 V) to the V_{DDH} level. And, the system clock switches from the crystal oscillator output (TBCCLK) to the high-speed clock (HSCLK).

Figure 7-3 shows system clock select timing and the status of the internal logic power supply (V_{DDL}).

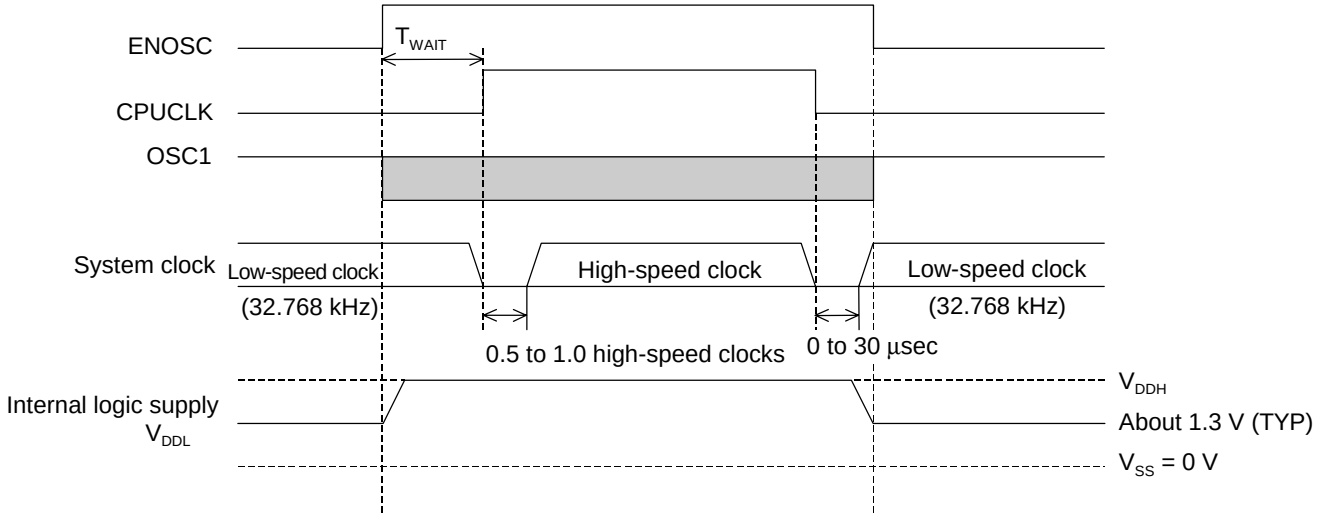


Figure 7-3 System Clock Select Timing

In the ceramic oscillation mode it takes about 10 ms to enter the high-speed clock oscillation mode after setting the ENOSC bit to "1". For this reason, when switching the CPUCLK bit to the high-speed setting, use a T_{WAIT} = 10 ms or longer after the ENOSC bit is set.

In the RC oscillation mode oscillation begins immediately after setting the ENOSC bit to "1". When switching the CPUCLK bit to the high-speed setting from this mode, use a T_{WAIT} = 300 µs or longer after setting the ENOSC bit.

Switching from high-speed mode to the low-speed mode requires no wait.

For details of a constant-voltage circuit for internal logic power supply, see Chapter 21, "Backup Circuit".

Chapter 8

Time Base Counter (TBC)

Chapter 8 Time Base Counter (TBC)

8.1 Overview

The time base counter (TBC) is a 15-bit internal counter, which generates the clock supplied to internal peripheral functions.

The TBC clock is a time base clock (TBCCLK: 32.768 kHz).

TBC outputs are used for functions such as time base interrupts and various other circuits. TBC8–11 and TBC12–15 can be read/reset by software.

The TBC generates an interrupt request at 32 Hz/16 Hz/4 Hz/2 Hz output falling edge (transition from "1" to "0").

The TBC is initialized to 0000H at system reset.

8.2 Time Base Counter Configuration

The configuration of the time base counter (TBC) is shown in Figure 8-1.

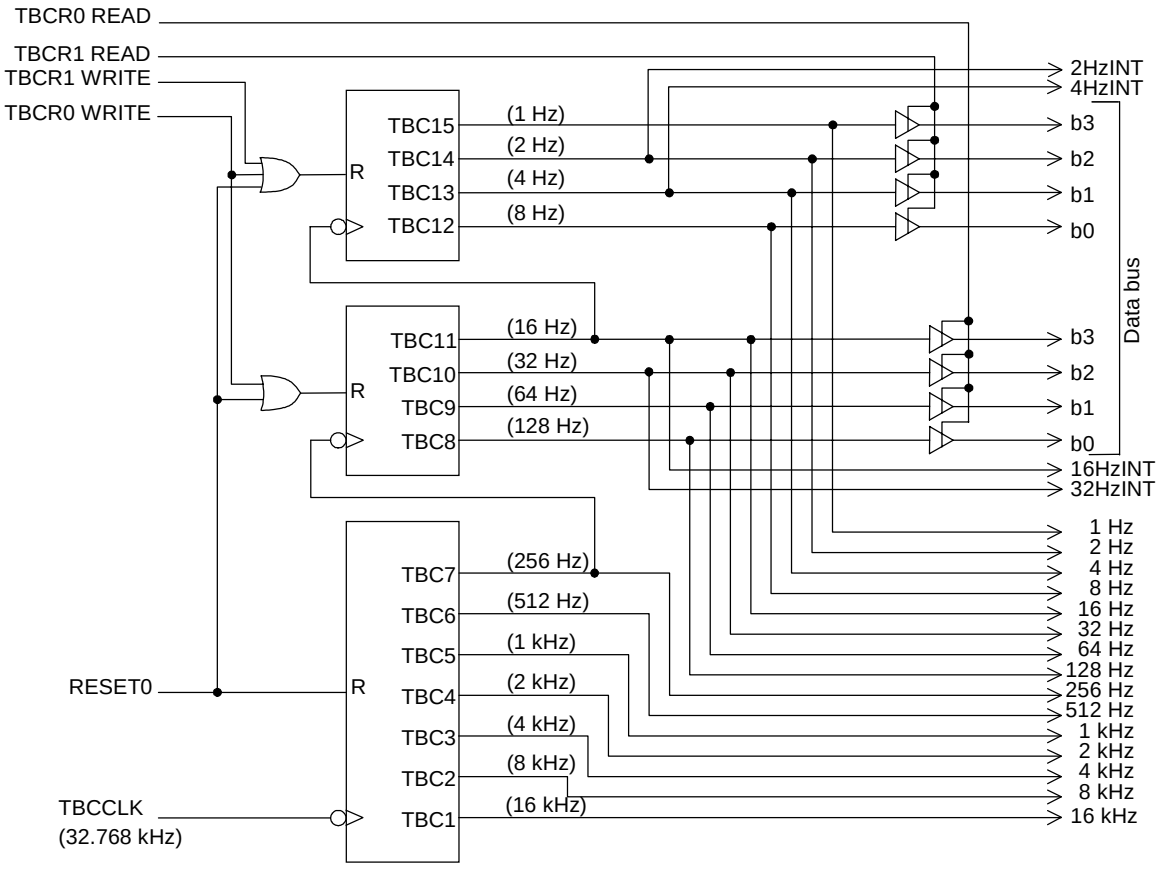


Figure 8-1 Time Base Counter (TBC) Configuration

8.3 Time Base Counter Operation

After system reset the time base counter (TBC) begins to count up from 0000H. The count is incremented at the falling edge of the time base clock.

TBC 32 Hz/16 Hz/4 Hz/2 Hz outputs are treated as time base interrupts. At each output falling edge, four bits of interrupt request register 4 are set, namely bit 3 (Q32 Hz), bit 2 (Q16 Hz), bit 1 (Q4 Hz) and bit 0 (Q2 Hz), requesting an interrupt to the CPU. TBC outputs are also used as operating clocks for various circuits.

TBC 1 to 8 Hz outputs and 16 to 128 Hz outputs can be read through the time base counter registers 0/1 (TBCR0/TBCR1).

A write operation to TBCR1 resets the 1 to 8 Hz output counter to "0", and a write operation to TBCR0 resets both the 1 to 8 Hz and 16 to 128 Hz output counters. The actual write data in these write operations has no significance. For example, the "MOV TBCR0, A" instruction can be used to write, but is not dependent on accumulator content in any way. When write is executed to TBCR0 and TBCR1 and the 1 to 8 Hz and 16 to 128 Hz output counters reset, interrupt requests are generated if 32 Hz/16 Hz/4 Hz/2 Hz outputs have been set to "1". To disable this interrupt first reset the master interrupt enable flag (MIE) or interrupt enable register 4 (IE4) to "0", execute the write to TBCR 0/1, and reset the interrupt request flag 4 (IRQ4) to "0".

Figure 8-2 shows interrupt generation timing and time base counter output reset timing by writing "1" to TBCR0 and TBCR1.

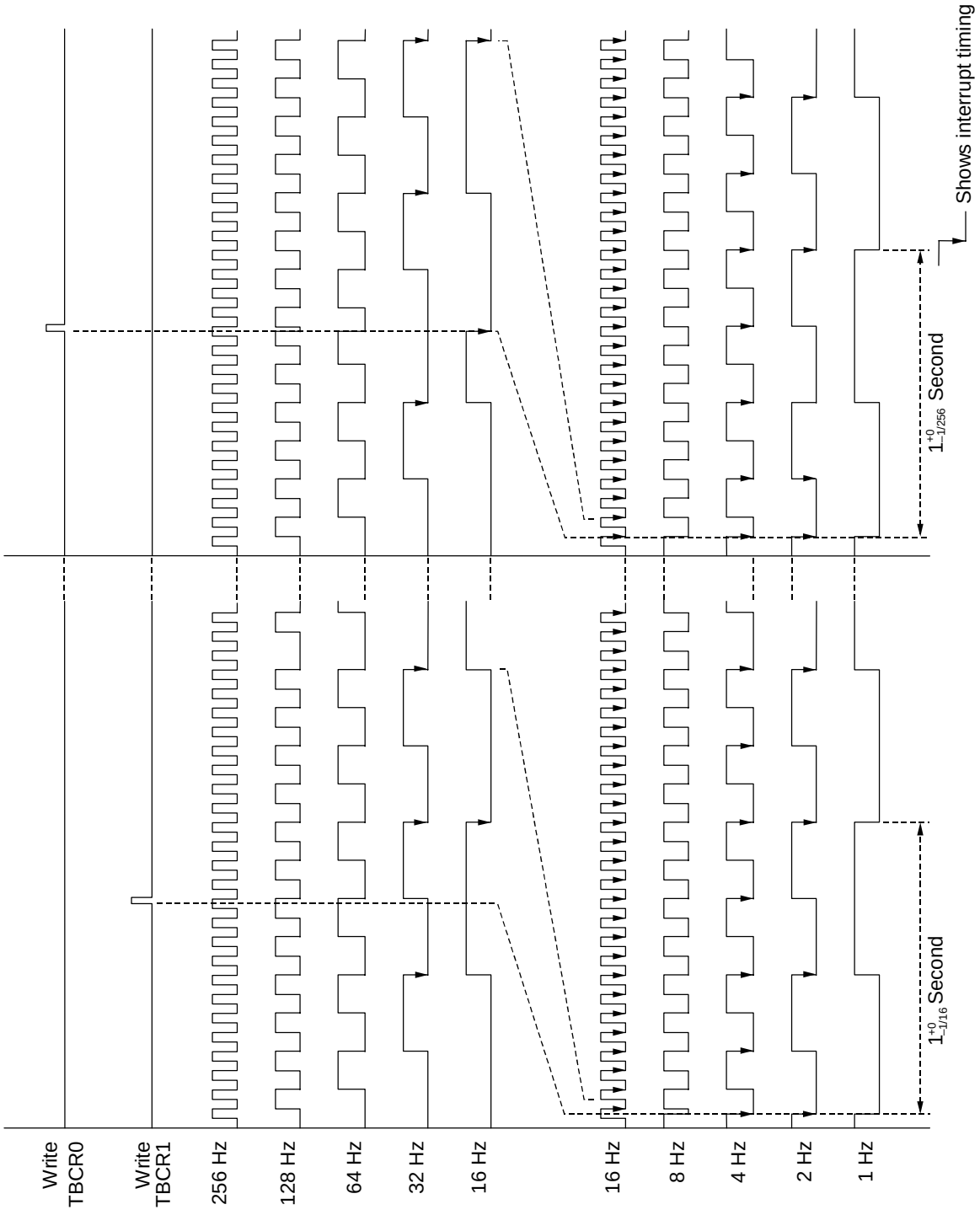


Figure 8-2 Interrupt Timing and Reset Timing by Writing "1" to TBCR0/TBCR1

8.4 Time Base Counter Registers

Time base counter registers 0/1 (TBCR0, TBCR1)

These 4-bit special function registers (SFRs) are used to read the 1 to 8 Hz and 16 to 128 Hz outputs of the time base counter.

A write operation to TBCR1 resets the 8 to 1 Hz outputs to "0", and a write operation to TBCR0 resets both the 1 to 8 Hz and 16 to 128 Hz outputs.

	b3	b2	b1	b0
TBCR0 (060H) (R/W)	16 Hz	32 Hz	64 Hz	128 Hz
TBCR1 (061H) (R/W)	1 Hz	2 Hz	4 Hz	8 Hz

Chapter 9

Timers (TIMER)

Chapter 9 Timers (TIMER)

9.1 Overview

The MSM63188A has four internal 8-bit timers (0 to 3). Timers 0 and 1, or timers 2 and 3, can be used in tandem as a 16-bit timer.

Timers 0 and 1 have three operation modes: auto-reload mode, capture mode and frequency measurement mode. Timers 2 and 3 have two modes: auto-reload and frequency measurement. Timer clock may be set to the time base clock (TBCCLK: 32.768 kHz), the high-speed clock (HSCLK), or an external clock. When using the timers as a 16-bit timer, the overflow signals for timer 0 and timer 2 are used as the clocks for timers 1 and 3, respectively.

In addition to pulse generation and time measurement, timers can also be used as baud rate generators for serial communication.

9.2 Timer Configuration

Figures 9-1 through 9-4 show the configuration of timers 0 to 3.

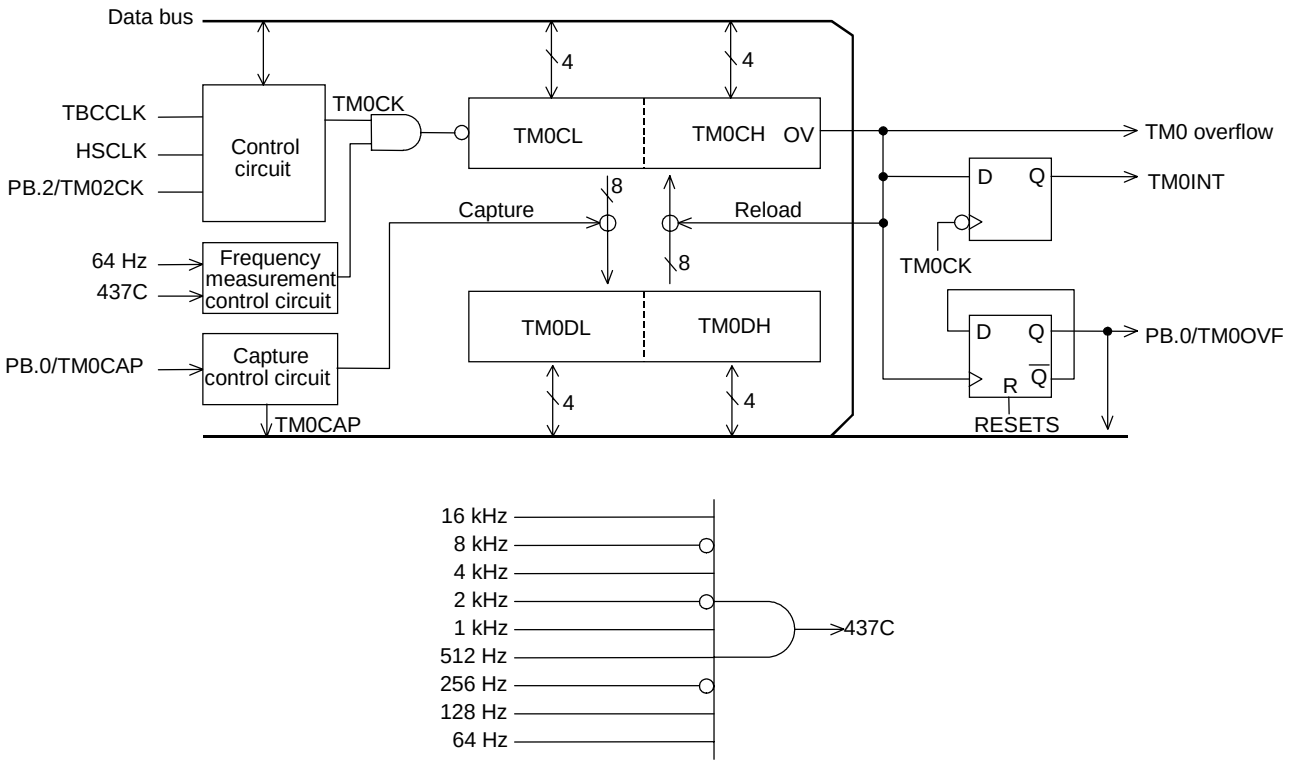


Figure 9-1 Timer 0 Configuration

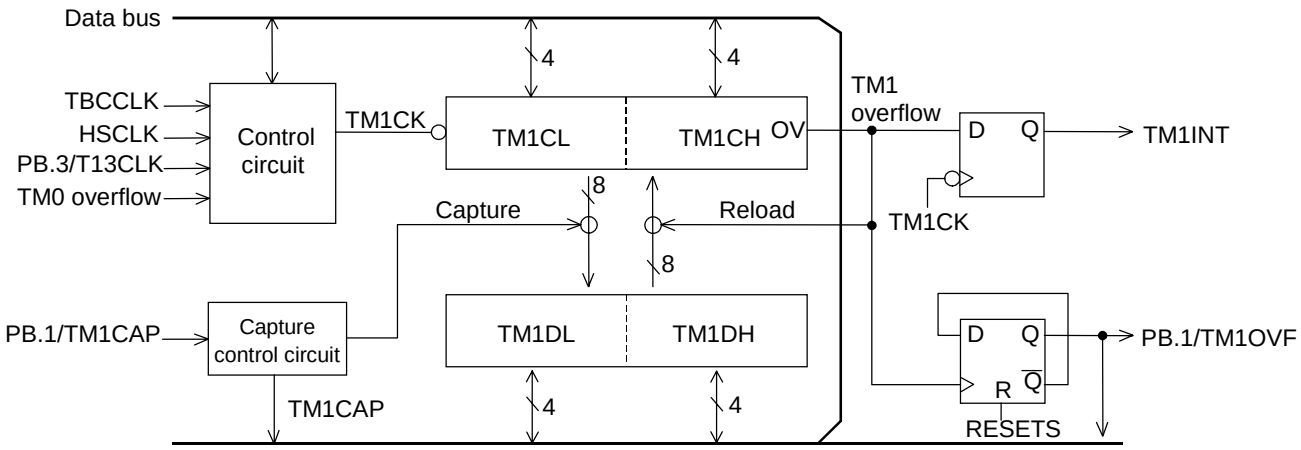


Figure 9-2 Timer 1 Configuration

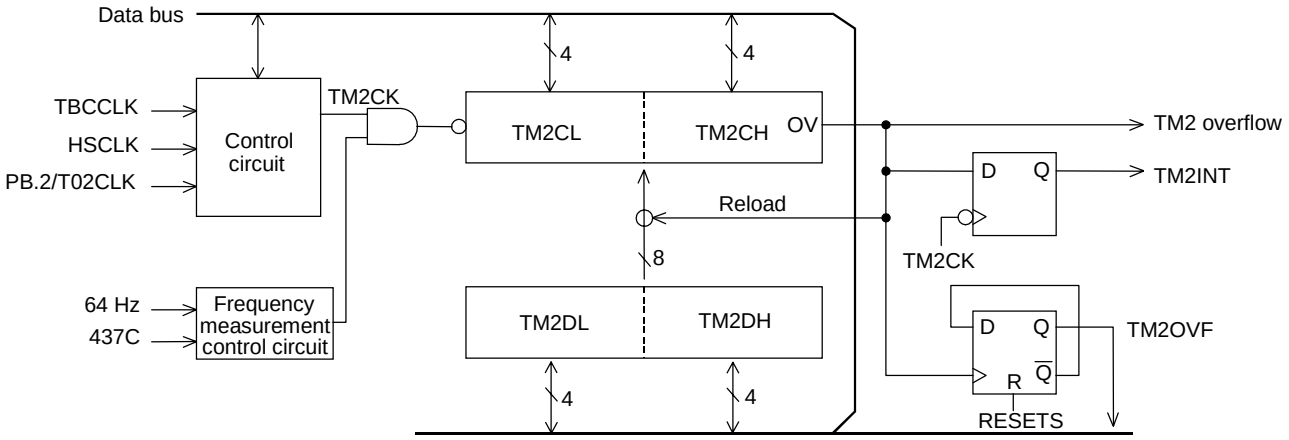


Figure 9-3 Timer 2 Configuration

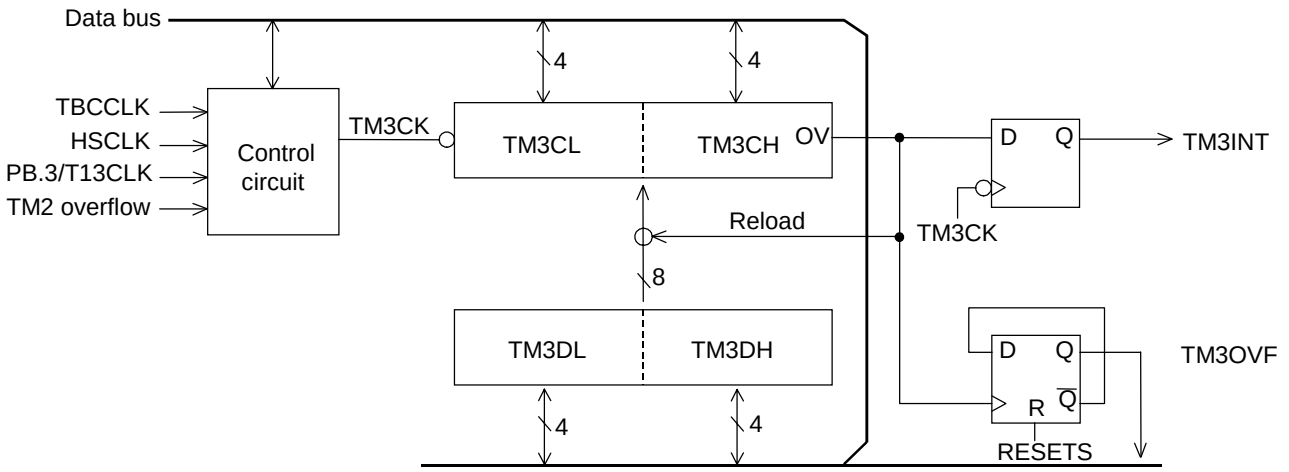


Figure 9-4 Timer 3 Configuration

9.3 Timer Operation

9.3.1 Timer clock

The timer clock can be set to the time base clock (TBCCLK: 32.768 kHz), the high-speed clock (HSCLK) or external clock. By using timer 0 and timer 2 overflow signals as clocks for timers 1 and 3, respectively, the timers can be used in pairs as 16-bit timers.

To use the high-speed clock (HSCLK), first activate the bit 1 (ENOSC) of the frequency control register (FCON), wait 10 ms or more in the ceramic oscillation mode or 300 μs or more in the RC oscillation mode, then start the timer.

The External clock is the input clock allocated as a secondary port function, with timers 0 and 2 using PB.2/T02CK as the input pin, and timers 1 and 3 using PB.3/T13CK. The external clock is sampled by the system clock (CLK), so the lengths for "L" and "H" level of the external clock should be applied more than one cycle period of the system clock.

9.3.2 Timer counter register

TM0CL and TM0CH, TM1CL and TM1CH, TM2CL and TM2CH, and TM3CL and TM3CH are 8-bit binary counters that are incremented at the falling edge of the timer clock.

Each timer counter register can be read/written by software. However, if the CPU clock and timer clock are different, values that are read or written during the count operation cannot be guaranteed. If an external clock is used as the timer clock, reading/writing is always possible.

When a value is written to any timer counter register, the same value is also written to the corresponding timer data register.

9.3.3 Timer data register

TM0DL, TM0DH, TM1DL TM1DH, TM2DL, TM2DH, TM3DL and TM3DH are 4-bit registers.

In the auto-reload mode the timer data registers are used to store the value reloaded to the timer counter registers when the timer counter registers overflow.

In the capture mode the timer data registers are used to store the timer counter register value when a capture signal is input. Timer data registers can be read/written by software. If a timer data register is written, the value of the timer counter register remains unchanged.

9.3.4 Timer interrupt requests and overflow flags

Timers generate timer interrupt requests when the timer counter register overflows. The overflow flag toggles between "1" and "0" at each overflow. The output of the overflow flag for timers 0 and 1 can be output to secondary port functions PB.0/TM0OVF and PB.1/TM1OVF pins.

Figure 9-5 indicates the operation timing for timer counter register overflow. Table 9-1 lists timer interrupts.

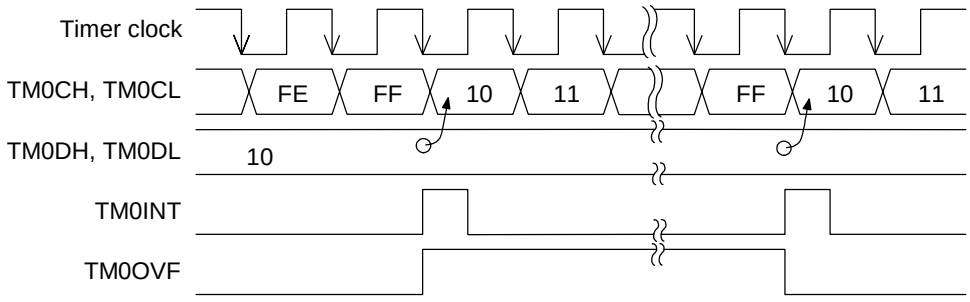


Figure 9-5 Timer Counter Register Overflow Timing (for timer 0)

Table 9-1 List of Timer Interrupts

Interrupt factor	Symbol	IRQ flag (IRQ2)	IE flag (IE2)	Interrupt vector address
Timer 0 interrupt	TM0INT	QTM0	ETM0	0020H
Timer 1 interrupt	TM1INT	QTM1	ETM1	0022H
Timer 2 interrupt	TM2INT	QTM2	ETM2	0024H
Timer 3 interrupt	TM3INT	QTM3	ETM3	0026H

When the master interrupt enable flag (MIE) is set to "1" with the interrupt enable flags (ETM0–3) set to "1", and a timer overflow occurs, a CPU interrupt request is generated.

9.3.5 Auto-reload mode operation

Timers 0 to 3 can be used as auto-reload mode timers. The setup method is as follows.

- Timer 0: Reset timer 0 control register 0 (TM0CON0) bit 2 (FMEAS0) and bit 1 (TM0ECAP) to "0".
- Timer 1: Reset timer 1 control register 0 (TM1CON0) bit 1 (TM1ECAP) to "0".
- Timer 2: Reset timer 2 control register 0 (TM2CON0) bit 2 (FMEAS2) to "0".
- Timer 3: No setup needed.

In the auto-reload mode, each time the timer counter register overflows, the timer data register value is reloaded into the timer counter register, and counting begins from value. Setting the RUN bits (TM0RUN, TM1RUN, TM2RUN, TM3RUN) for each timer control register to "1" will restart the count, and resetting to "0" stops the count.

In the 16-bit timer mode for timers 0 and 1 the TM1RUN bit is disabled, and start/stop is controlled with the TM0RUN bit. In the 16-bit timer mode for timers 2 and 3 the TM3RUN bit is disabled, and start/stop is controlled with the TM2RUN bit.

Figure 9-6 shows auto-reload mode timing when timers 0 and 1 are used as a 16-bit timer.

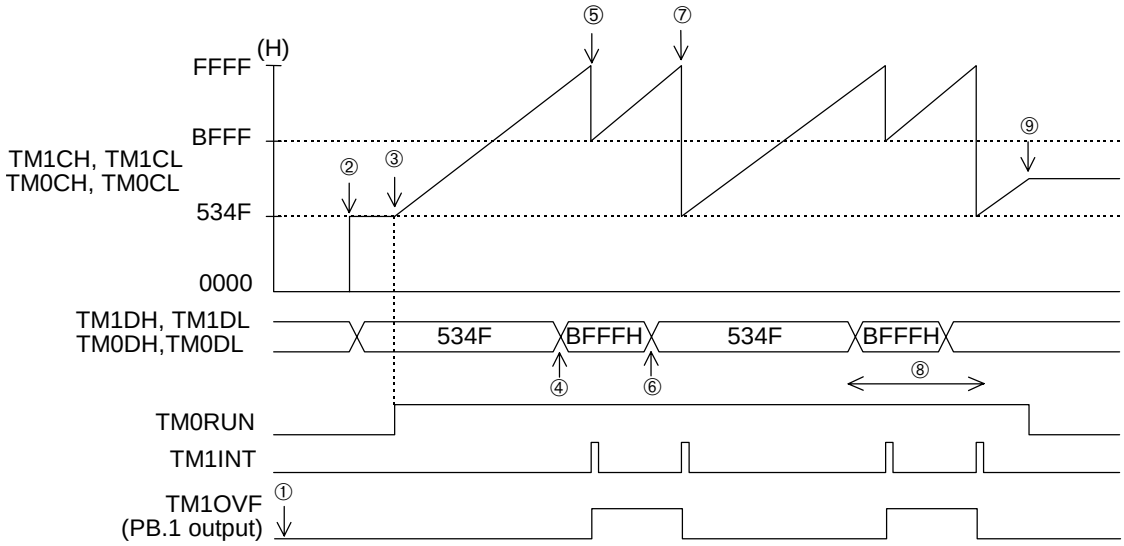


Figure 9-6 Auto-reload Mode Timing

Figure 9-6 is an example using the auto-reload mode for pulse generation, with the following operation.

① Set PB.1 to the output mode (TM1OVF) secondary function.

② Write 534FH to the timer data and timer counter registers.
TM1DH = TM1CH = 5H (bits 15–12)
TM1DL = TM1CL = 3H (bits 11–8)
TM0DH = TM0CH = 4H (bits 7–4)
TM0DL = TM0CL = FH (bits 3–0)

③ If TM0CON and TM1CON are set to auto-reload mode and TM0RUN is set to "1", the timer counter register will begin counting from 534FH.

④ Before the timer counter register overflows, write the next reload value BFFFH to the timer data register.

⑤ TM1INT is generated and timer 1 overflow flag TM1OVF toggles. The timer counter register continues to count up from BFFFH.

⑥ Before the timer counter register overflows, write the next reload value 543FH to the timer data register.

⑦ When the timer counter register overflows, 543FH is set to the timer counter register, timer interrupt TM1INT is generated and timer 1 overflow flag TM1OVF toggles. The timer counter register continues to count up from 543FH.

⑧ Repeat steps ④ through ⑦. This allows a user-defined pulse to be output from PB.1/TM1OVF.

⑨ Halt the count by resetting TM0RUN to "0".

Figure 9-7 shows TM0RUN count start/halt timing.

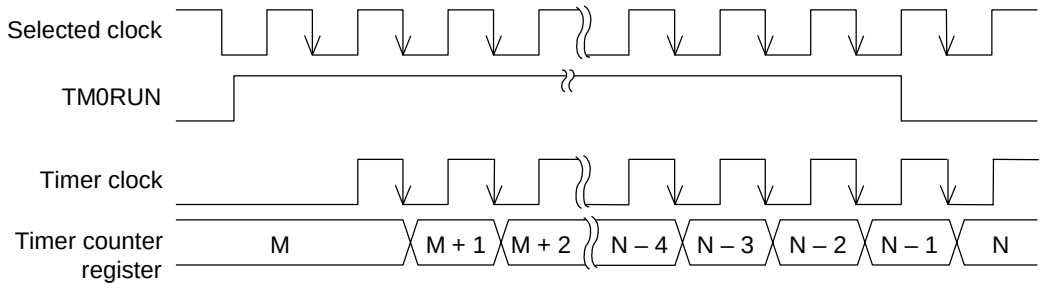


Figure 9-7 TM0RUN Count Start/Halt Timing

When TM0RUN is set to "1", the first count-up is as the fall of the second clock. When TM0RUN is reset to "0", count-up starts at the fall of the next clock, and then the count halts.

9.3.6 Capture mode operation

Timer 0 and timer 1 can be used as capture mode timers. Set them for this use as described below.

Timer 0: Set timer 0 control register 0 (TM0CON0) bit 1 (TM0ECAP) to "1", and reset bit 2 (FMEAS0) to "0".
Timer 1: Set timer 1 control register 0 (TM1CON0) bit 1 (TM1ECAP) to "1".

In the capture mode reload of data from the timer data register to the timer counter register is disabled, and each time the timer counter register overflows it restarts from 00H.

If the capture input (PB.0/TM0CAP, PB.1/TM1CAP) level changes during timer counter register operation, the capture trigger is detected, and the value of the timer counter register is stored to the timer data register. This operation is referred to as capture.

When a capture occurs the capture flags (TM0CAP, TM1CAP) of the timer status registers (TM0STAT, TM1STAT) are set to "1". While the capture flag is "1" capture is disabled. The capture flag is allocated to timer status register bit 0, and is automatically reset to "0" by reading the timer status register.

If both TM1CL1 and TM1CL0 bits of timer 1 control register 1 (TM1CON1) are set to "1", and timer 0 overflow selected as clock, the capture mode will also be 16-bit. In this case the capture trigger input is the PB.0/TM0CAP pin.

Figure 9-8 indicates capture mode timing.

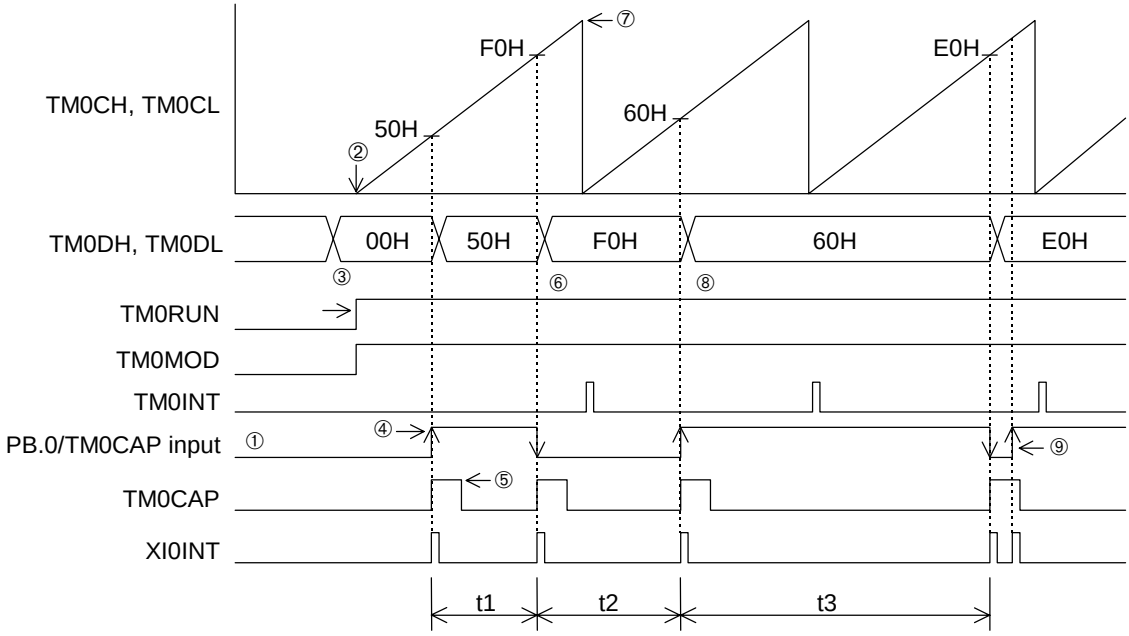


Figure 9-8 Capture Mode Timing

Figure 9-8 is an example using the timer 0 capture mode for pulse width measurement, with the following operation.

① Set PB.0/TM0CAP to input mode, and enable XI0INT and TM0INT.

② Clear the timer data and timer counter registers.

③ Set TM0CON0 capture mode and set TM0RUN to "1" to begin counting up.

④ When the PB.0/TM0CAP input changes, the value of TM0CH/TM0CL is captured to TM0DH/TM0DL, and TM0CAP is set to "1" (first capture). The CPU detects this through XI0INT, and reads the values of TM0DH/TM0DL.

⑤ When TM0DH/TM0DL read is complete, TM0CAP is reset to "0" for the next capture.

⑥ When PB.0/TM0CAP input changes, steps ④ and ⑤ are repeated (second capture). The H pulse width t1 for the PB.0 input can be determined as:

$$t1 = (F0H - 50H) \times tCLK$$

where tCLK is the TMCLK cycle.

⑦ When the timer counter register overflows TM0INT is generated, and this is stored. The timer counter register changes from FFH to 00H and continues counting.

⑧ When PB.0/TM0CAP input changes, steps ④ and ⑤ are repeated (third capture). Because the counter has overflowed once between the second and third captures, the L pulse width t2 for the PB.0 input can be determined as:

$$t2 = (60H - F0H + 100H) \times tCLK$$

⑨ When TM0CAP is set to "1", no capture occurs even when PB.0/TM0CAP changes.

Figure 9-9 shows the capture timing, and Figure 9-10 shows the capture signal (CAPT) generator circuit.

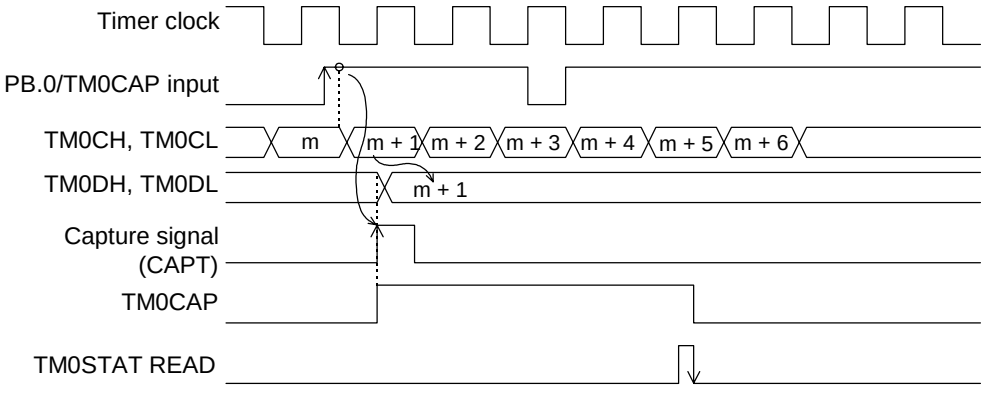


Figure 9-9 Capture Timing

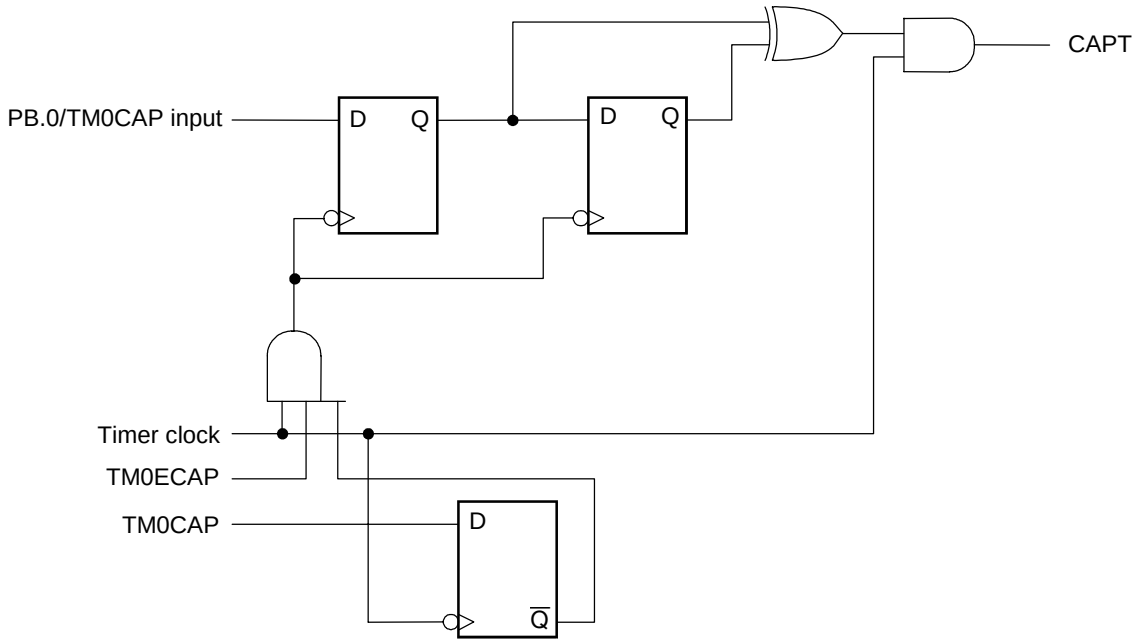


Figure 9-10 Capture Signal (CAPT) Generator Circuit

Notes:

- The maximum delay between PB.0/TM0CAP input level change and capture is one timer clock cycle.
- Set the pulse width of the capture trigger signal to be input to not less than two cycles of the timer clock. Depending on the pulse width of the capture trigger input, repeated capturing may occur after the capture trigger is detected, irrespective of the trigger signal.

  Typical examples of valid pulse widths of the trigger signal are shown below.
  - When a low-speed clock (32.768 kHz) is used as the timer clock, a pulse width of 62 μs or more is required.
  - When a high-speed clock (2 MHz) is used as the timer clock, a pulse width of 1 μs or more is required.
  - When an external clock is used as the timer clock, a pulse width of not less than two cycles of the external clock is required.

  The trouble described above will happen also when there is a noise caused by chattering etc. whose length is within the valid pulse width. If it happens, eliminate the noise with an input pin.

9.3.7 Frequency measurement mode operation

Timers 0 and 1, and timers 2 and 3 can be used in the frequency measurement mode. These timers are set as follows for the frequency measurement mode:

- Timer 0: Set timer 0 control register 0 (TM0CON0) bit 2 (FMEAS0) to "1", and reset bit 1 (TM0ECAP) and bit 0 (TM0RUN) to "0".
- Timer 1: Set timer 1 control register 0 (TM1CON0) bit 1 (TM1ECAP) and bit 0 (TM1RUN) to "0".
- Timer 2: Set timer 2 control register 0 (TM2CON0) bit 2 (FMEAS2) to "1", and reset bit 0 (TM2RUN) to "0".
- Timer 3: Reset timer 3 control register 0 (TM3CON0) bit 0 (TM3RUN) to "0".

The frequency measurement mode measures the frequency of the RC oscillator clock, which varies because of production line variation. The count can be used to determine the auto-reload mode timer data register value, and overflow the timer at the Baud rate needed for serial transmission.

Figure 9-11 indicates frequency measurement mode timing when using timers 2 and 3 as a 16-bit timer.

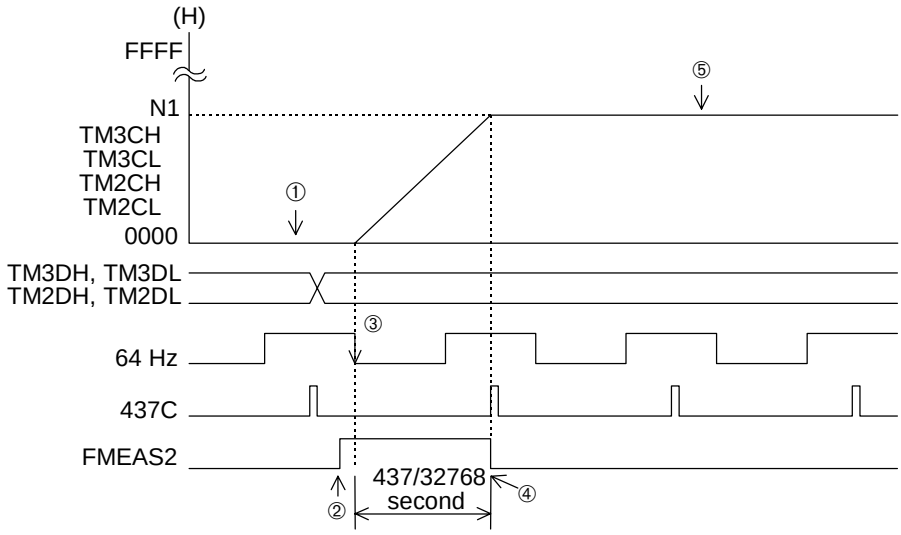


Figure 9-11 Frequency Measurement Mode Timing

The operation sequence for Figure 9-11 is as follows.

① Timer 3 control registers 0 and 1 (TM3CON0, TM3CON1) are set for 16-bit timer mode, and the timer counter and timer data register are cleared to zero. Enable the high-speed clock by the frequency control register (FCON) and the timer clock is set to HSCLK.

② Wait 10 ms or more in the ceramic oscillation mode or 300 μs or more in the RC oscillation mode after starting the high-speed clock and set FMEAS2 to "1" to enter the frequency measurement mode.

③ When FMEAS2 is "1", count-up begins at the 64 Hz falling edge.

④ When the 437C signal is "1", FMEAS2 is reset to "0", and the counter stops at the falling edge of the next clock. The 437C signal rises 437/32768 second after the 64 Hz falling edge.

⑤ Timer counter register value N1 is read.

Assuming that the ceramic oscillation clock is exactly 2 MHz, value N1 read from the timer counter register is:

$$N1 = 2000000 \times 437/32768 = 26672 \text{ (decimal)}$$
$$= 6830 \text{ (hexadecimal)}$$
$$= 0110\ \ 1000\ \ 0011\ \ 0000 \text{ (binary)}$$
$$\text{(truncated)}$$

Because 437/32768 second is equivalent to 128 clocks at 9600 Hz (more precisely, 9598 Hz), a division of the count by 128 provides the frequency ratio (N2) between 2 MHz and 9600 Hz. Because $128 = 2^7$, that can be determined by merely truncating the righthand seven digits of N1 (binary), yielding

$$N2 = 26672/128 = 011010000 \text{ (binary)}$$
$$= D0 \text{ (hexadecimal)}$$
$$= 208 \text{ (decimal)}$$

This indicates that 9600 Hz is about 208 times the cycle of 2 MHz, which means that the timer data register should be set to FF30H so that the counter overflows every 208 counts of the 2 MHz clock in auto-reload mode. As a result, overflow produces a TM3INT cycle t_{TM3INT} of

$$t_{TM3INT} = 1/2000000 \times 208 = 0.104 \text{ ms (9615 Hz)}$$

In the same way, assuming that RC oscillation clock is 600 kHz due to manufacturing variation, we get

$$N1 = 600000 \times 437/32768 = 8001 \text{ (decimal)}$$
$$= 1F41 \text{ (hexadecimal)}$$
$$= 0001\ \ 1111\ \ 0100\ \ 0001 \text{ (binary)}$$
$$\text{(truncated)}$$

Truncating the righthand seven digits of N1 (binary), we get

$$N2 = 8001/128 = 000111110 \text{ (binary)}$$
$$= 3E \text{ (hexadecimal)}$$
$$= 62 \text{ (decimal)}$$

Set the timer data register to FFC2H so that the counter overflows every 62 counts of the 600 kHz clock in auto-reload mode. As a result, overflow produces a TM3INT cycle t_{TM3INT} of

$$t_{TM3INT} = 1/600000 \times 62 = 0.10333 \text{ ms (9677 Hz)}$$

In this way the frequency measurement mode can be applied to generate TM3INT signals with precision cycles even from RC oscillators with large variation. These TM3INT signals can be supplied to the serial port as a Baud rate clock. Changing the value of N2 makes it possible to generate Baud rates of 4800 Hz, 2400 Hz or user-defined rates. The precision of the generated Baud rate clock is within ±2% for 9600 Hz, and within ±1% for 4800 Hz or lower.

Figure 9-12 illustrates the operation of Baud rate generation for a RC oscillator clock frequency of 600 kHz.

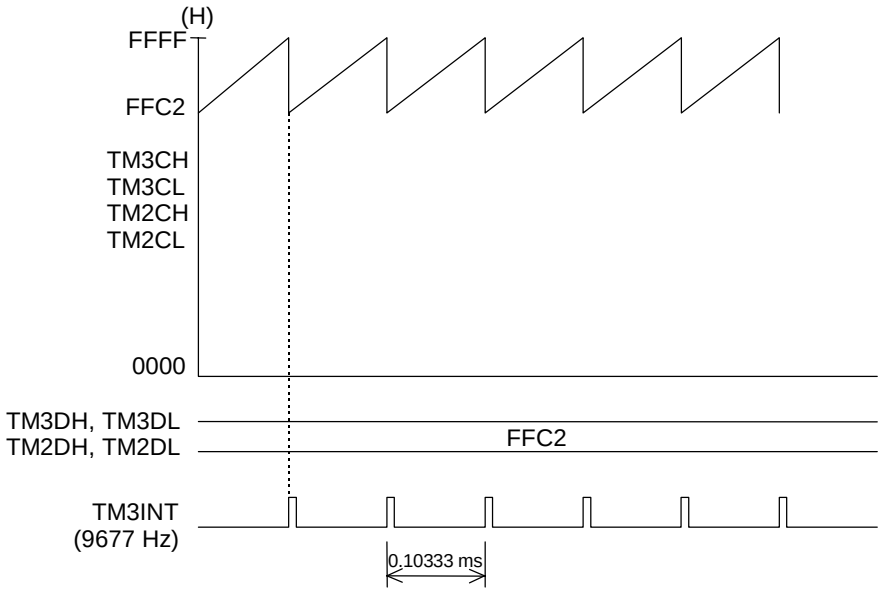


Figure 9-12 Baud Rate Clock Generation

9.4 Timer Registers

(1) Timer data registers (TM0DL, TM0DH, TM1DL, TM1DH, TM2DL, TM2DH, TM3DL, TM3DH)

The timer data registers store the reload values for the timer counter registers when using the auto-reload mode. In the capture mode they are used to store timer counter register capture data. Each timer data register is a 4-bit special function register (SFR).

Timer data registers are reset to "0" at system reset.

The timer data register value will not change even if a write is executed to the timer counter register. Timer data register write for timers 0 and 1 in the capture mode will transfer the contents of the timer counter registers to the timer data registers.

TM0DL (068H) (R/W)

b3	b2	b1	b0
T0D3	T0D2	T0D1	T0D0

Values for timer 0 data register bits 3 to 0

TM0DH (069H) (R/W)

b3	b2	b1	b0
T0D7	T0D6	T0D5	T0D4

Values for timer 0 data register bits 7 to 4

TM1DL (06AH) (R/W)

b3	b2	b1	b0
T1D3	T1D2	T1D1	T1D0

Values for timer 1 data register bits 3 to 0

TM1DH (06BH) (R/W)

b3	b2	b1	b0
T1D7	T1D6	T1D5	T1D4

Values for timer 1 data register bits 7 to 4

TM2DL (076H) (R/W)

b3	b2	b1	b0
T2D3	T2D2	T2D1	T2D0

Values for timer 2 data register bits 3 to 0

TM2DH (077H) (R/W)

b3	b2	b1	b0
T2D7	T2D6	T2D5	T2D4

Values for timer 2 data register bits 7 to 4

TM3DL (078H) (R/W)

b3	b2	b1	b0
T3D3	T3D2	T3D1	T3D0

Values for timer 3 data register bits 3 to 0

TM3DH (079H) (R/W)

b3	b2	b1	b0
T3D7	T3D6	T3D5	T3D4

Values for timer 3 data register bits 7 to 4

(2) Timer counter registers (TM0CL, TM0CH, TM1CL, TM1CH, TM2CL, TM2CH, TM3CL, TM3CH)

The timer counter registers are 4-bit special function registers (SFRs), which function as 8-bit binary counters.

Timer counter registers are initialized to "0" at system reset.

When a value is written to any timer counter register, the same value is written to the corresponding timer data register.

TM0CL (06CH) (R/W)

b3	b2	b1	b0
T0C3	T0C2	T0C1	T0C0

Values for timer 0 counter bits 3 to 0

TM0CH (06DH) (R/W)

b3	b2	b1	b0
T0C7	T0C6	T0C5	T0C4

Values for timer 0 counter bits 7 to 4

TM1CL (06EH) (R/W)

b3	b2	b1	b0
T1C3	T1C2	T1C1	T1C0

Values for timer 1 counter bits 3 to 0

TM1CH (06FH) (R/W)

b3	b2	b1	b0
T1C7	T1C6	T1C5	T1C4

Values for timer 1 counter bits 7 to 4

TM2CL (07AH) (R/W)

b3	b2	b1	b0
T2C3	T2C2	T2C1	T2C0

Values for timer 2 counter bits 3 to 0

TM2CH (07BH) (R/W)

b3	b2	b1	b0
T2C7	T2C6	T2C5	T2C4

Values for timer 2 counter bits 7 to 4

TM3CL (07CH) (R/W)

b3	b2	b1	b0
T3C3	T3C2	T3C1	T3C0

Values for timer 3 counter bits 3 to 0

TM3CH (07DH) (R/W)

b3	b2	b1	b0
T3C7	T3C6	T3C5	T3C4

Values for timer 3 counter bits 7 to 4

(3) Timer control registers (TM0CON0/1, TM1CON0/1, TM2CON0/1, TM3CON0/1)

The timer control registers are 4-bit special function registers (SFRs) which control the operation modes of timers 0 to 3.

The timer control register bits are initialized to "0" at system reset.

TM0CON0 (070H) (R/W)

b3	b2	b1	b0
—	FMEAS0	TM0ECAP	TM0RUN

Timer 0 mode select

b2	b1	b0		
0	0	0	:	Auto-reload mode stop (initial value)
0	0	1	:	Auto-reload mode operation
0	1	0	:	Capture mode stop
0	1	1	:	Capture mode operation
1	0	0	:	Frequency measurement mode operation
1	0	1	:	Not used
1	1	0	:	Not used
1	1	1	:	Not used

TM0CON1 (071H) (R/W)

b3	b2	b1	b0
—	—	TM0CL1	TM0CL0

Timer 0 clock select

b1	b0		
0	0	:	TBCCLK (initial value)
0	1	:	HSCLK
1	0	:	External clock
1	1	:	Not used

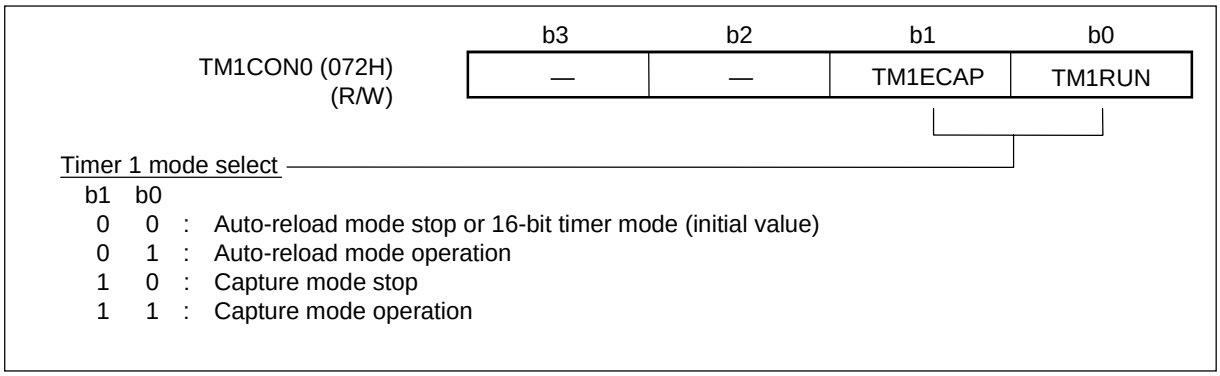
TM0CON0 bits 2 to 0: FMEAS0, TM0ECAP, TM0RUN

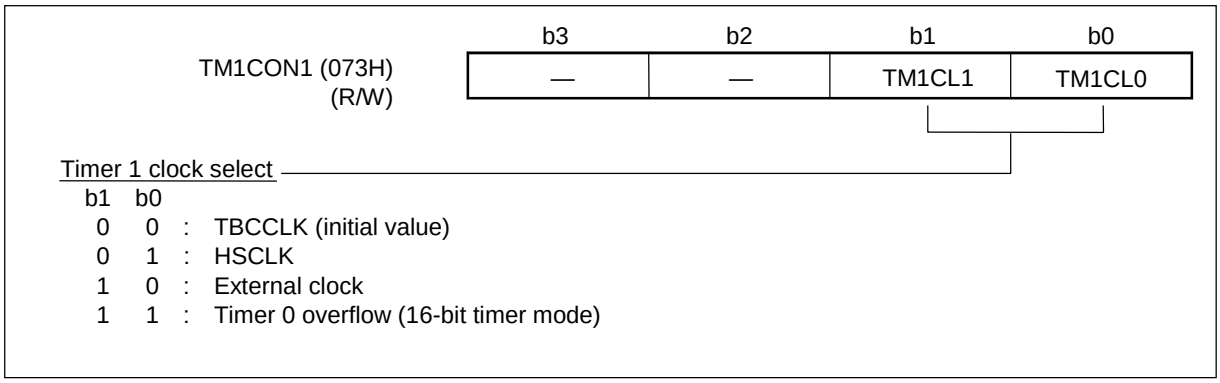
These bits select the timer 0 operation mode. Timer 0 can be used in auto-reload mode, capture mode and frequency measurement mode. Timer 0 can be used with timer 1 as a 16-bit timer, controlled by timer 1 control register 0, 1 (TM1CON0, TM1CON1).

TM0CON1 bits 1 to 0: TM0CL1, TM0CL0

These bits select the timer 0 clock as TBCCLK, HSCLK or external clock. When external clock is selected, the signal from the PB.2/T02CK pin is used as the timer 0 clock.

To use the high-speed clock (HSCLK), first activate the bit 1 (ENOSC) of the frequency control register (FCON), wait 10 ms or more in the ceramic oscillation mode or 300 μs or more in the RC oscillation mode, then start the timer.





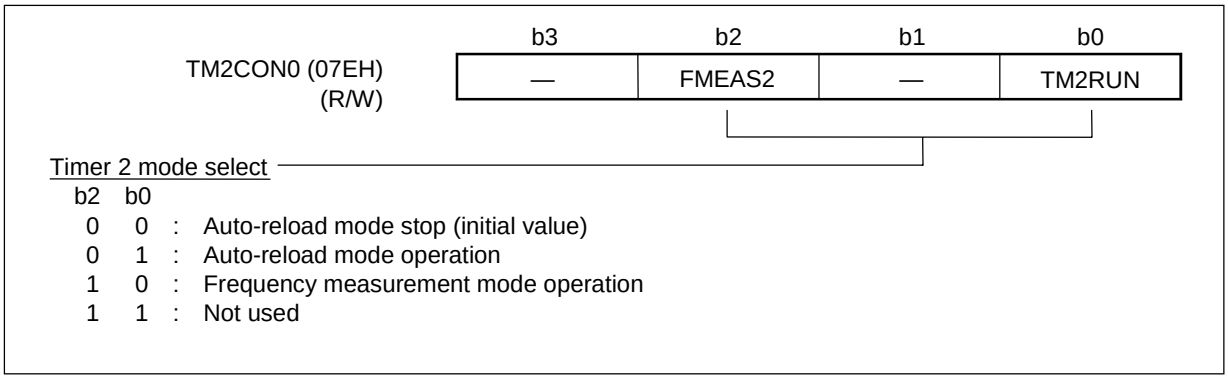
TM1CON0 bits 1 to 0: TM1ECAP, TM1RUN

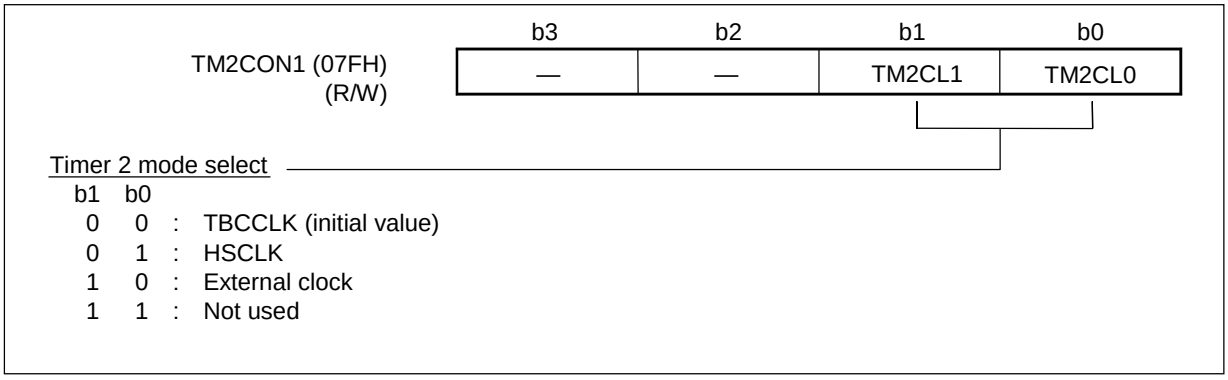
These bits select the timer 1 operation mode. Timer 1 can be run in auto-reload, capture or 16-bit timer modes.

TM1CON1 bits 1 to 0: TM1CL1, TM1CL0

These bits select the timer 1 clock as TBCCLK, HSCLK, external clock or timer 0 overflow. Timer 0 overflow is selected when used as a 16-bit timer. When external clock is selected, the signal from the PB.3/T13CK pin is used as the timer 1 clock.

To use the high-speed clock (HSCLK), first activate the bit 1 (ENOSC) of the frequency control register (FCON), wait 10 ms or more in the ceramic oscillation mode or 300 μs or more in the RC oscillation mode, then start the timer.





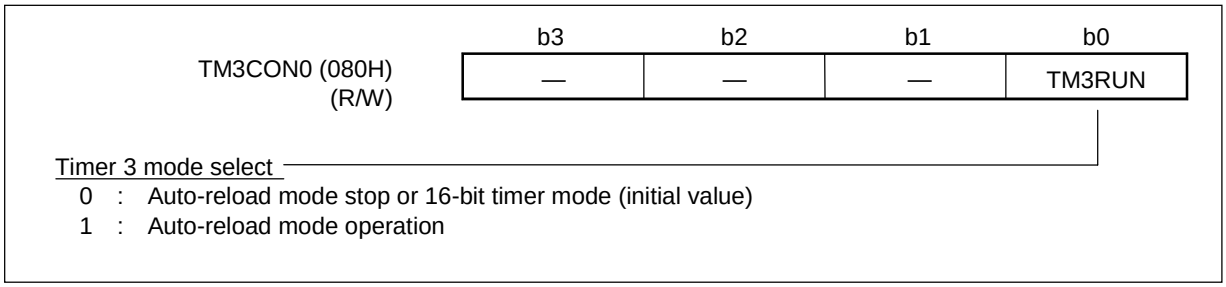
TM2CON0 bits 2, 0: FMEAS2, TM2RUN

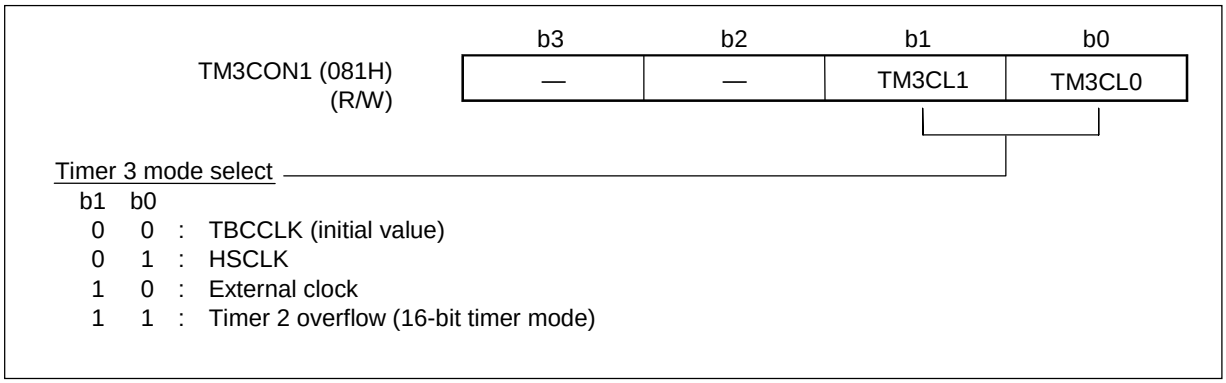
These bits select the timer 2 operation mode. Timer 2 can be used in auto-reload mode and frequency measurement mode. It can be used with timer 3 as a 16-bit timer, controlled by timer 3 control register 0, 1 (TM3CON0, TM3CON1)

TM2CON1 bits 1 to 0: TM2CL1, TM2CL0

These bits select the timer 2 clock as TBCCLK, HSCLK or external clock. When external clock is selected, the signal from the PB.2/T02CK pin is used as the timer 2 clock.

To use the high-speed clock (HSCLK), first activate the bit 1 (ENOSC) of the frequency control register (FCON), wait 10 ms or more in the ceramic oscillation mode or 300 μs or more in the RC oscillation mode, then start the timer.





TM3CON0 bit 0: TM3RUN

This bit selects the timer 3 operation mode. Timer 3 can be run in auto-reload and 16-bit timer modes.

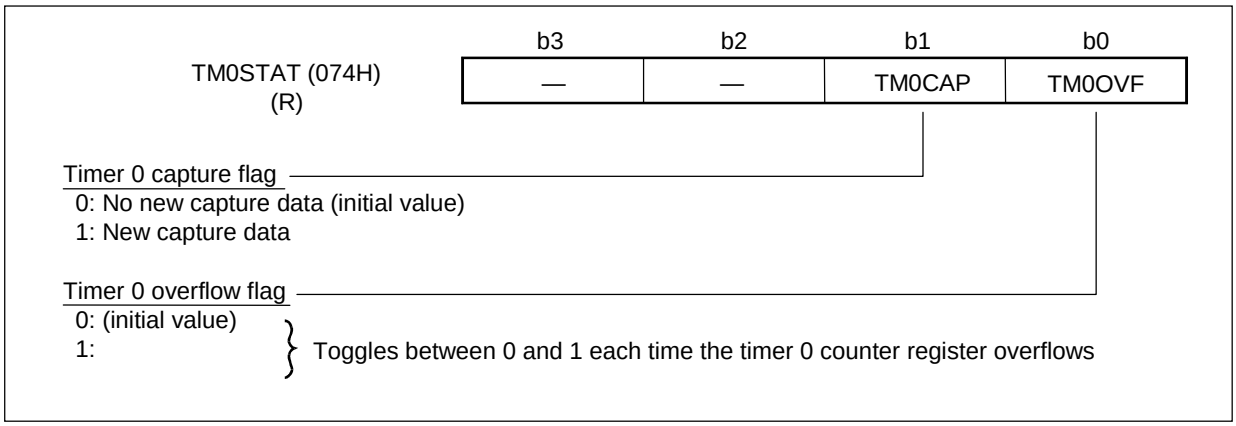
TM3CON1 bits 1 to 0: TM3CL1, TM3CL0

These bits select the timer 3 clock as TBCCLK, HSCLK, external clock or timer 2 overflow. Timer 2 overflow is selected when used as a 16-bit timer. When external clock is selected, the signal from the PB.3/T13CK pin is used as the timer 3 clock.

To use the high-speed clock (HSCLK), first activate the bit 1 (ENOSC) of the frequency control register (FCON), wait 10 ms or more in the ceramic oscillation mode or 300 μs or more in the RC oscillation mode, then start the timer.

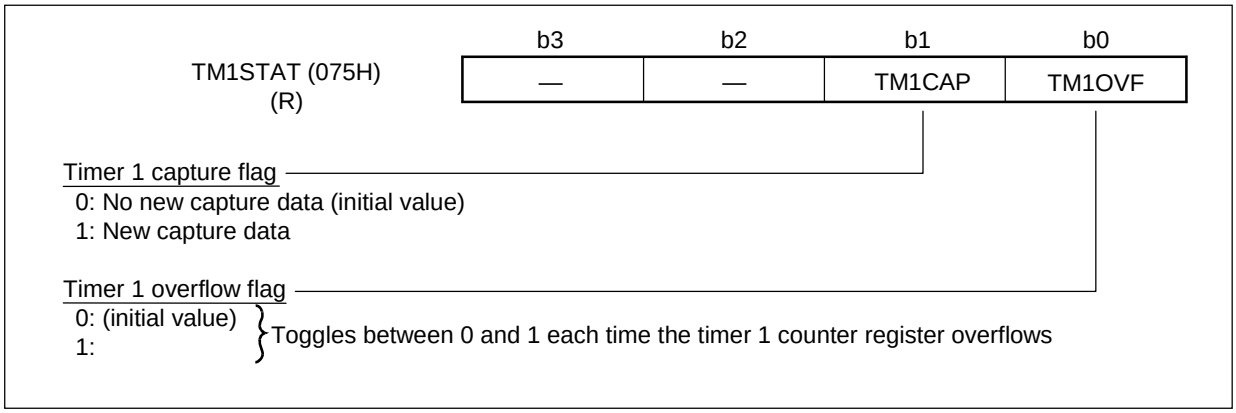
(4) Timer status registers (TM0STAT, TM1STAT, TM2STAT, TM3STAT)

The timer status registers are 4-bit special function registers (SFRs) indicating the timer status.



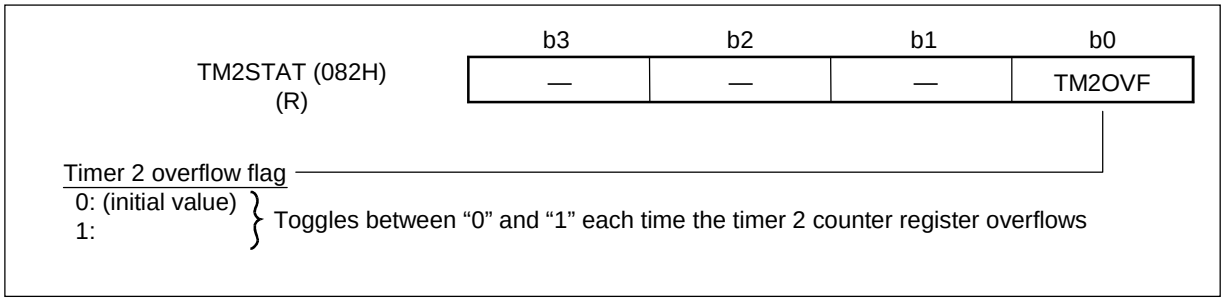
Bit 1: TM0CAP
This bit indicates whether or not new capture data is present. When TM0CAP is "0" it indicates there has been no new capture data since system reset or since the last time TM0CAP was read. When it is set to "1", it indicates new capture data. When TM0CAP is set to "1" additional captures are disabled. TM0CAP is reset to "0" at system reset. In the capture mode if the PB.0 input level changes and a capture is generated, TM0CAP is automatically set to "1". When TM0STAT is read, TM0CAP is automatically reset to "0".

Bit 0: TM0OVF
This flag indicates that the timer counter register has overflowed. Each time it overflows the bit toggles between "0" and "1". This flag is reset to "0" at system reset.

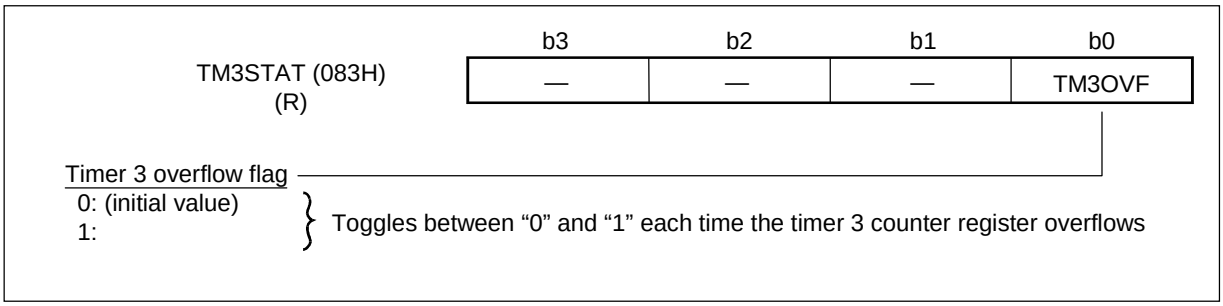


Bit 1: TM1CAP
This bit indicates whether or not new capture data is present. When TM1CAP is "0" it indicates no new capture data since system reset or since the last time TM1CAP was read. When it is set to "1", it indicates new capture data. When TM1CAP is set to "1" additional captures are disabled. TM1CAP is reset to "0" at system reset. In the capture mode if the PB.1 input level changes and a capture is generated, TM1CAP is automatically set to "1". When TM1STAT is read, TM1CAP is automatically reset to "0".

Bit 0: TM1OVF
This flag indicates that the timer counter register has overflowed. Each time it overflows the bit toggles between "0" and "1". This flag is reset to "0" at system reset.



Bit 0: TM2OVF
This flag indicates that the timer counter register has overflowed. Each time it overflows the bit toggles between "0" and "1". It is reset to "0" at system reset.



Bit 0: TM3OVF
This flag indicates that the timer counter register has overflowed. Each time it overflows the bit toggles between "0" and "1". This flag is reset to "0" at system reset.

Chapter 10

100 Hz Timer Counter (100HzTC)

Chapter 10 100 Hz Timer Counter (100HzTC)

10.1 Overview

The 100 Hz timer counter has a circuit that divides the TBC6 output (512 Hz) of the time base counter to generate a 10 Hz interrupt. The 100 Hz timer consists of a 5/6-base counter and two decimal counters.

10.2 100 Hz Timer Counter Configuration

Figure 10-1 indicates the configuration of the 100 Hz timer counter.

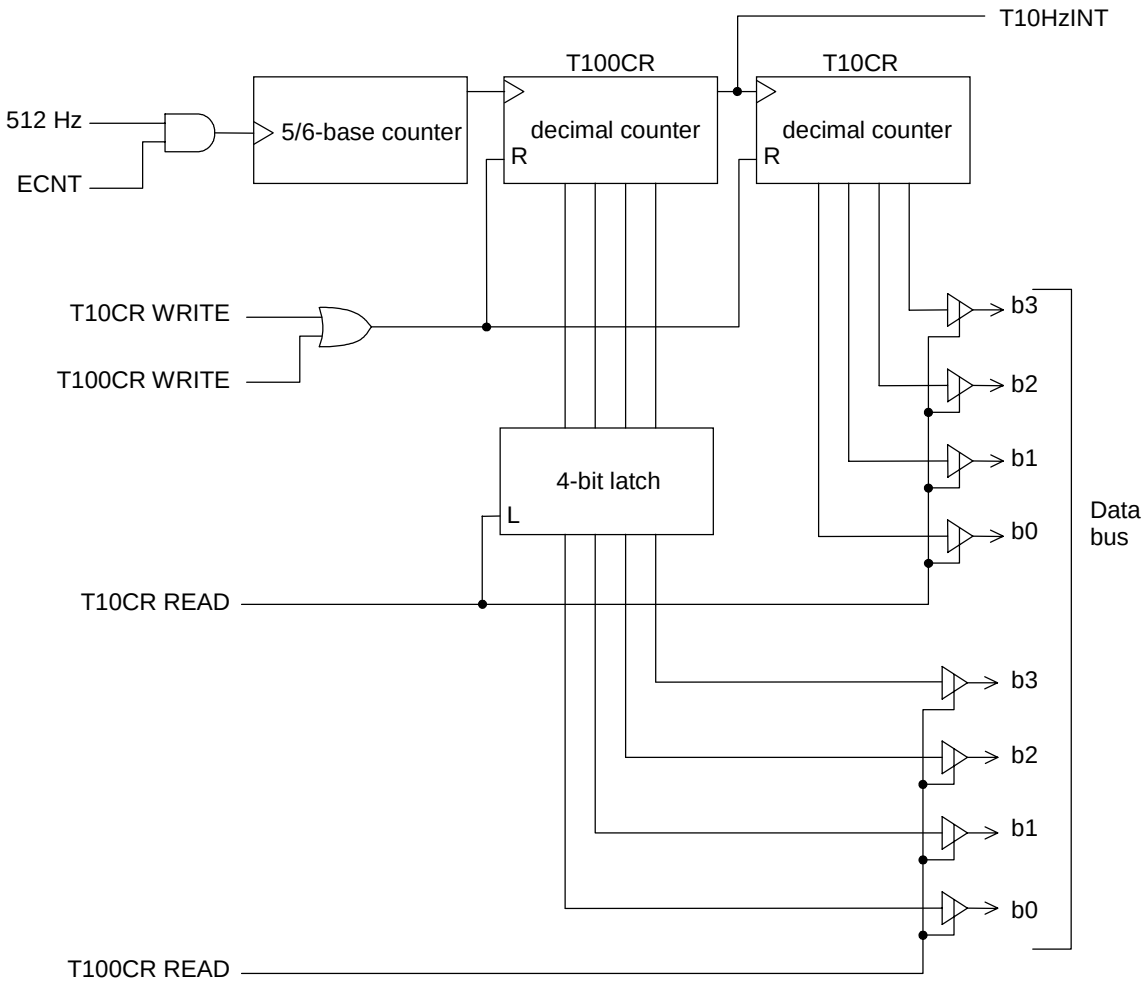


Figure 10-1 100 Hz Timer Counter Configuration

10.3 100 Hz Timer Counter Operation

The 100 Hz timer counter begins counting when bit 0 (ECNT) of the 100 Hz timer counter control register (T100CON) is set to "1". The 512 Hz output of the time base counter is divided into 100 Hz by the 5/6-base counter.

The 100 Hz signal is input to the 100 Hz counter (T100CR) and the carry output of that counter is input to the 10 Hz counter (T10CR). The 10HzINT signal, which is the carry output (10 Hz) of the T100CR 100 Hz counter also generates an interrupt request, setting bit 3 (Q10Hz) of interrupt request register 3 to "1".

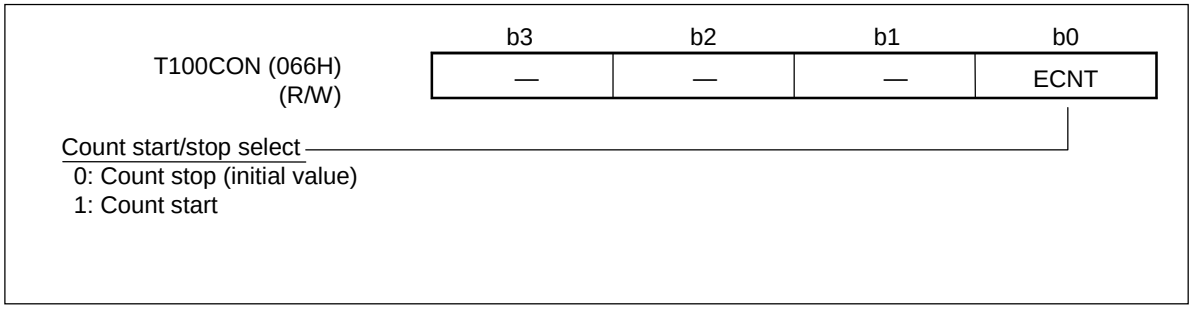
If either T100CR or T10CR is written to, both are reset to "0". The write data used has no significance. For example, the "MOV T10CR, A" instruction is not dependent on the contents of the accumulator.

If T10CR is read, the contents of T100CR at that time are latched to the 4-bit latch. Therefore, the contents of T100CR at the time T10CR is read can be read correctly.

10.4 100 Hz Timer Counter Registers

(1) 100 Hz timer counter control register (T100CON)

This is a 4-bit special function register (SFR) controlling the 100 Hz timer counter.



Bit 0: ECNT
This bit controls count start/stop for the 100 Hz timer counter internal counter.
Count starts when set to "1". At system reset the value is reset to "0" and counting is stopped.

(2) 100 Hz counter register (T100CR)

This is a 4-bit special function register (SFR) to read the 100 Hz counter of the 100 Hz timer counter. The content of the T100CR is latched by a 4-bit latch in T10CR read operation, so the value of the T100CR must always be read after reading T10CR.

When data is written in T100CR, both T100CR and T10CR are reset to "0".

T100CR (064H) (R/W)

b3	b2	b1	b0
100C3	100C2	100C1	100C0

(3) 10 Hz counter register (T10CR)

A 4-bit special function register (SFR) to read the 10 Hz counter in the 100 Hz timer counter.

When data is written in T10CR, both T100CR and T10CR are reset to "0".

T10CR (065H) (R/W)

b3	b2	b1	b0
10C3	10C2	10C1	10C0

Chapter 11

Watchdog Timer (WDT)

Chapter 11 Watchdog Timer (WDT)

11.1 Overview

The watchdog timer is a circuit to detect CPU malfunction. The WDT consists of a 9-bit watchdog timer counter (WTDC) counting the 256 Hz output of the TBC7 of the time base counter (TBC), and a watchdog timer control register (WDTCON) to start and clear WDTC.

11.2 Watchdog Timer Configuration

Figure 11-1 shows the configuration of the watchdog timer.

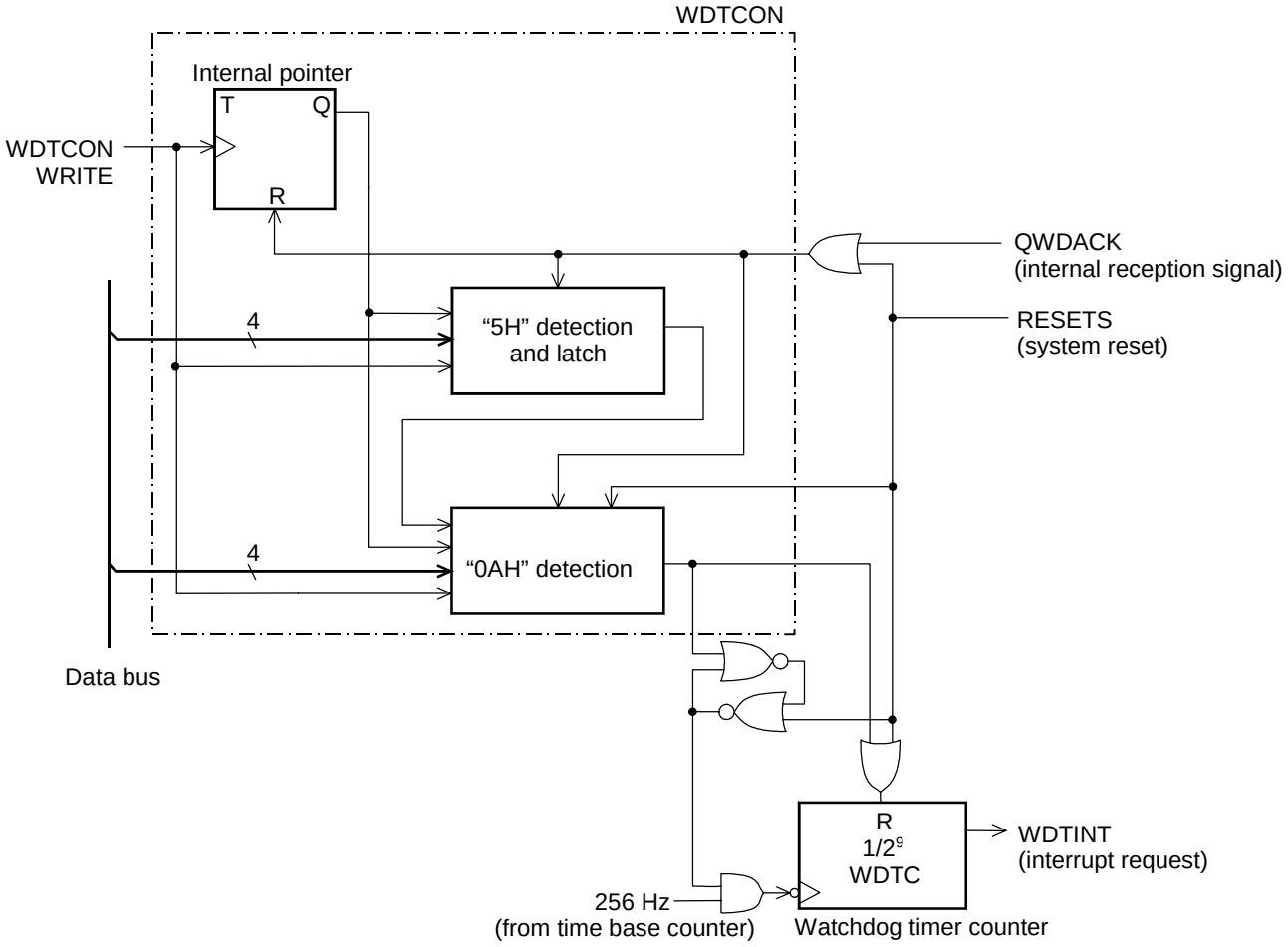


Figure 11-1 Watchdog Timer Configuration

11.3 Watchdog Timer Operation

The watchdog timer counter (WDTC) ceases operation at system reset. The watchdog timer counter (WDTC) starts counting up by writing "5H" in the watchdog timer control register (WDTCON) while the internal pointer is set at "0" and writing "0AH" in the register while the internal pointer is set at "1".

The internal pointer is reset to "0" at system reset or WDTC overflow, and toggles every time WDTCON is written to.

After WDTC start, the WDTC is cleared by writing "5H" in the watchdog timer control register (WDTCON) while the internal pointer is set at "0" and writing "0AH" in the register while the internal pointer is set at "1". When the WDTC overflows (1FFH $\rightarrow$ 000H), the watchdog timer interrupt request (WDTINT) is generated. WDTINT cannot be disabled by software (non-maskable interrupt), and has maximum reception priority.

The WDTC overflow cycle (T) is given by:

$$T = \frac{128 \times 512}{32768\ (Hz)} = 2\ s$$

The minus deviation (t) for the WDTC overflow cycle is given by:

$$t = \frac{128}{32768\ (Hz)} = \text{Approximately } 3.9\ ms$$

As a result, the WDTC clear cycle (Ct) is:

$$Ct = T - t = 2\ s - 3.9\ ms = 1.9961\ s$$

As indicated above, when 32.768 kHz is the low-speed clock, the program must be able to clear the WDTC within 1.9961 s.

If a CPU malfunction occurs as a result of a power fault or other factor and the WDTC cannot be cleared normally, the WDTC overflows and generates a watchdog timer interrupt. The watchdog timer interrupt routine should handle recovery operations to return to the normal routine.

Note:

The watchdog timer cannot detect all abnormal states. If the WDTC can still be cleared, but the CPU has effectively crashed, the fault will not be detected.

Figure 11-2 is a flowchart of watchdog timer processing.

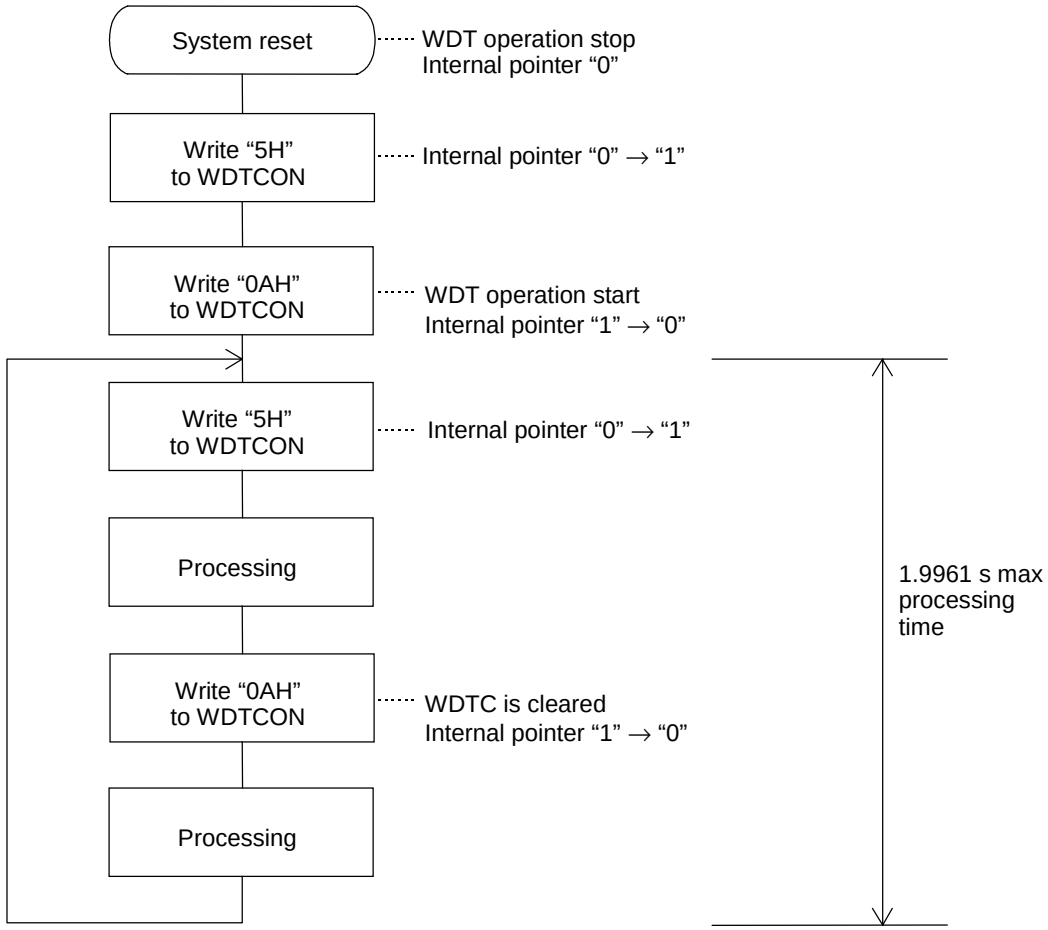


Figure 11-2 Watchdog Timer Processing Flowchart

Figure 11-3 shows the timing chart for watchdog timer operation.

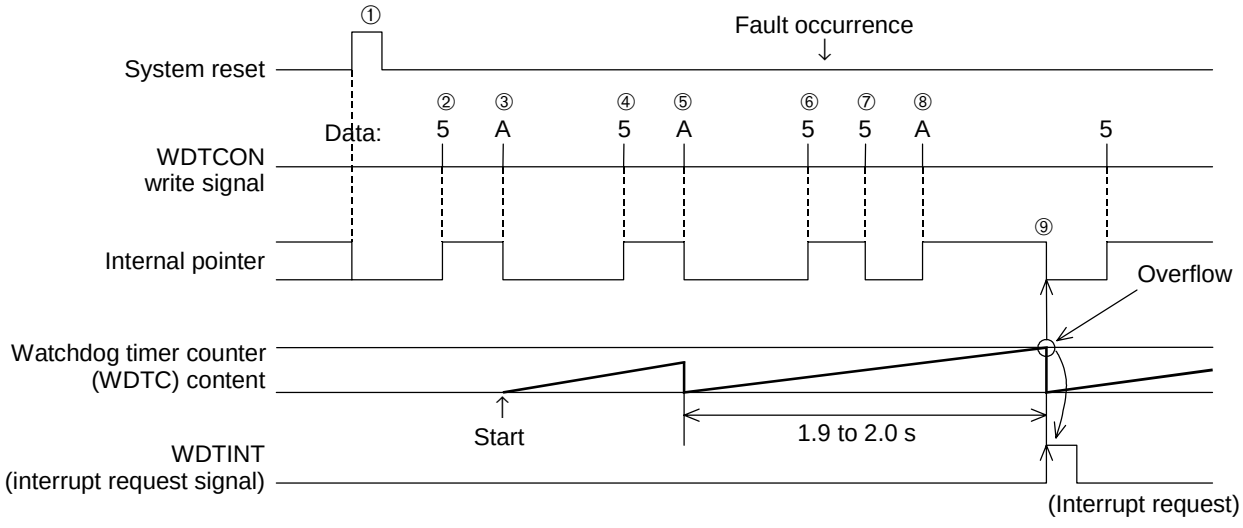


Figure 11-3 Watchdog Timer Operation Timing Chart

The watchdog timer operation consists of the following sequence.

① System reset clears the internal pointer and watchdog timer counter (WDTC).

② Write "5H" to WDTCON. (Internal pointer "0" → "1")

③ Start the WDTC by writing "0AH" to WDTCON. (Internal pointer "1" → "0")

④ Write "5H" to WDTCON. (Internal pointer "0" → "1")

⑤ Clear the WDTC by writing "0AH" to WDTCON. (Internal pointer "1" → "0")

⑥ Write "5H" to WDTCON. (Internal pointer "0" → "1")

⑦ When an error occurs, "5H" is to be written in the WDTCON, but it is not written as the internal pointer is set at "1". (Internal pointer "1" → "0")

⑧ "0AH" is written in the WDTCON, but the WDTC is not cleared as the internal pointer is set at "0" and "5H" has not been written in the WDTCON (in the above step 7). (Internal pointer "0" → "1")

⑨ WDTC is not cleared, and WDTC overflows, causing the watchdog timer interrupt WDTINT to be generated. The internal pointer is cleared to "0" at that time.

11.4 Watchdog Timer Control Register (WDTCON)

The watchdog timer control register (WDTCON) is a 4-bit special function register (SFR) used only to start/clear the watchdog timer counter (WDTC).

WDTCON (09FH) (W)

b3	b2	b1	b0
d3	d2	d1	d0

Chapter 12

Ports (INPUT, OUTPUT, I/O PORT)

Chapter 12 Ports (INPUT, OUTPUT, I/O PORT)

12.1 Overview

The MSM63182A has two 4-bit input ports, four 4-bit output ports, and three 4-bit I/O ports.

The MSM63184A has two 4-bit input ports, four 4-bit output ports, and five 4-bit I/O ports.

The MSM63188A has two 4-bit input ports, six 4-bit output ports, and six 4-bit I/O ports.

The V_{DDI} (interface power supply) pin supplies power to the ports.

If a port is to be connected to an external device that operates on a different power supply, the power supply of the external device must be fed to the V_{DDI} pin.

Note:

Since V_{DDI} is separated from the positive power supply pin (V_{DD}), power must be supplied to the V_{DDI} pin.

12.2 MSM63180 Family Ports List

The ports of the MSM63180 family products are shown in Table 12-1.

Table 12-1 MSM63180 Family Ports List

Port	I/O	Interrupt	Secondary function	MSM63182A	MSM63184A	MSM63188A	Page
Port 0	I	●	●	●	●	●	12-2
Port 1			●	●	●	●	
Port 2	O					●	12-10
Port 3						●	
Port 4			●	●	●	●	12-14
Port 5				●	●	●	
Port 6				●	●	●	
Port 7				●	●	●	
Port 8	I/O	●	●	●	●	●	12-22
Port 9				●	●	●	
Port A				●	●	●	
Port B		●	●			●	12-31
Port C		●	●			●	12-38
Port D		●	●		●	●	12-46
Port E		●	●		●		12-50

12.3 Ports 0–1 (P0.0–P0.3, P1.0–P1.3)

12.3.1 Port 0–1 configuration

The MSM63182A, MSM63184A, and MSM63188A have the 4-bit input-only ports Port 0 and Port 1.

The circuit configurations of port 0 and port 1 are shown in Figure 12-1.

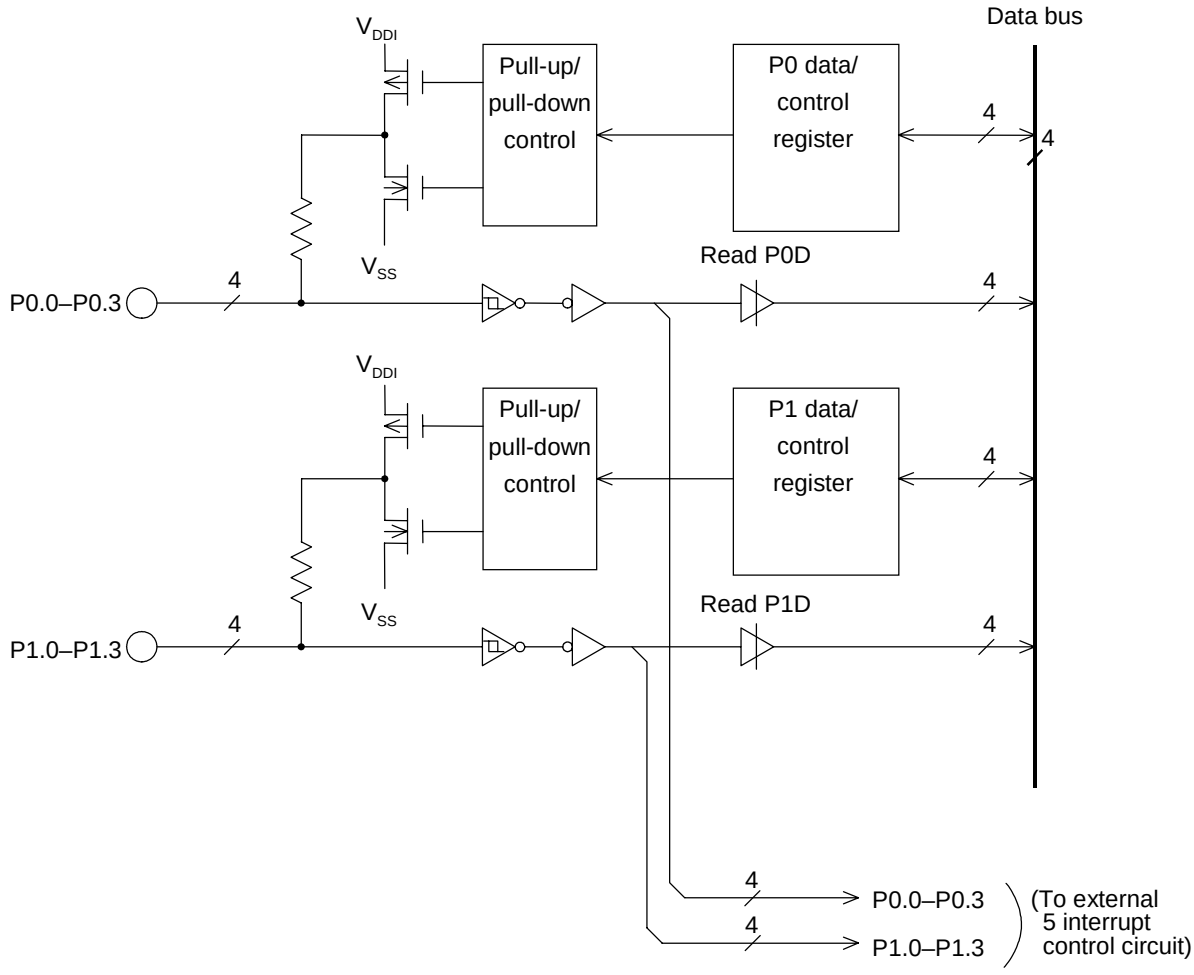
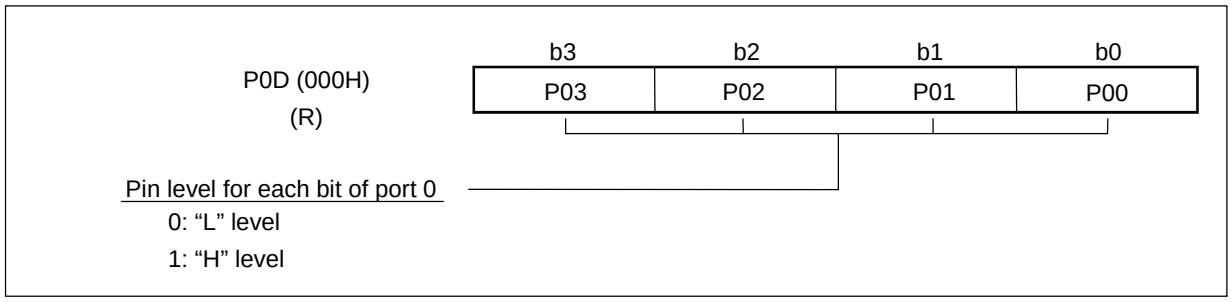


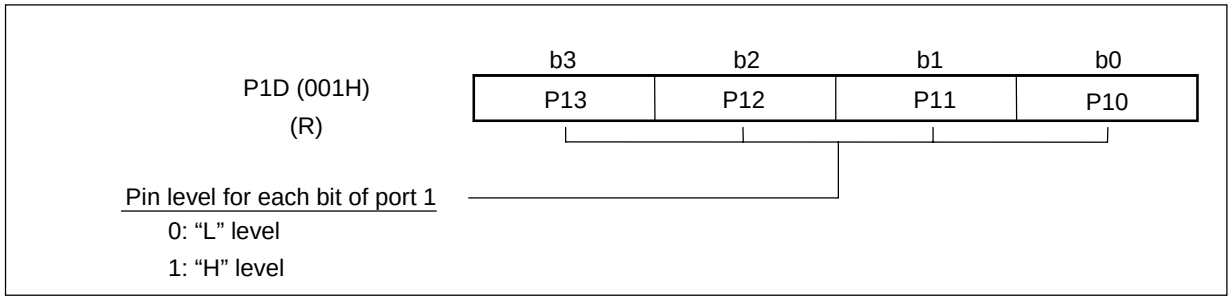
Figure 12-1 Port 0–1 Configuration

12.3.2 Port 0–1 registers

(1) Port 0–1 registers (P0D, P1D)

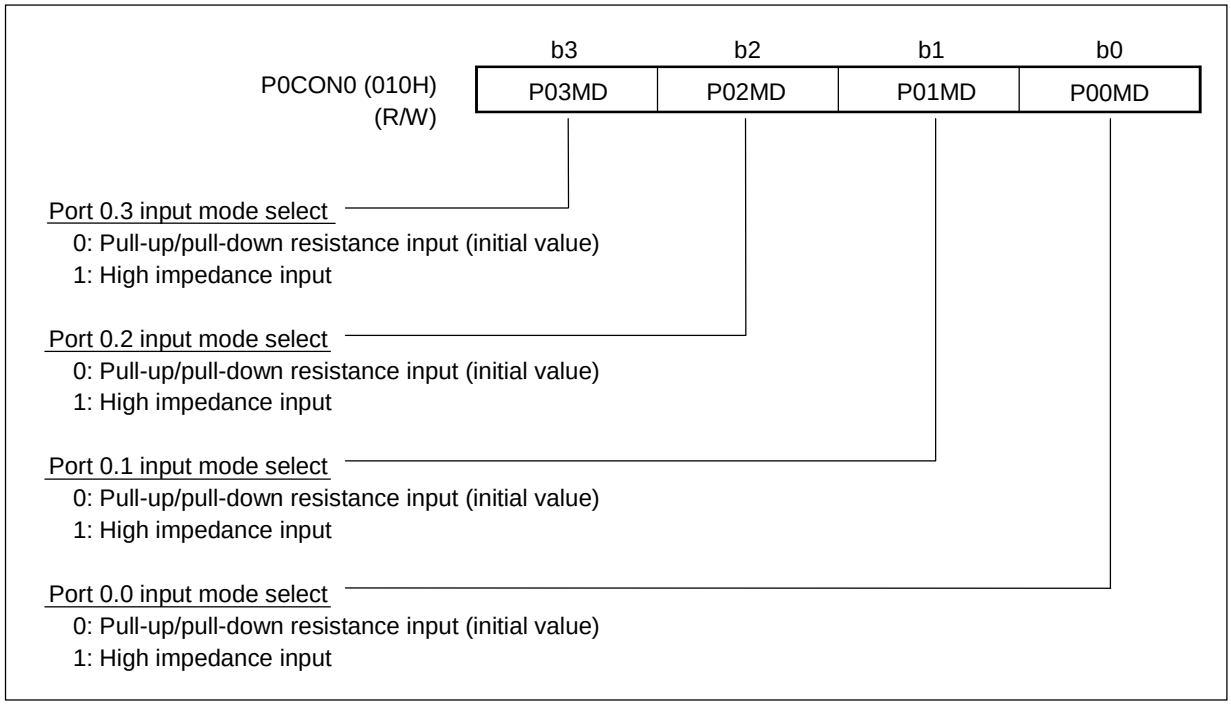
The port 0 data register (P0D) and port 1 data register (P1D) are read-only 4-bit special function registers (SFRs) used to read the levels of pins of ports 0 and 1.

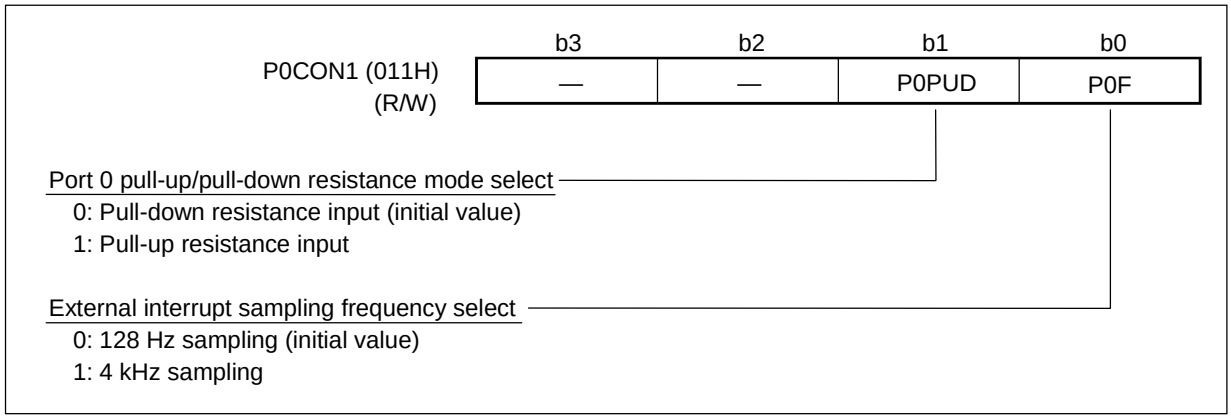




(2) Port 0–1 control registers 0/1 (P0CON0, P0CON1, P1CON0, P1CON1)

The port 0 control registers 0/1 (P0CON0, P0CON1) and port 1 control registers 0/1 (P1CON0, P1CON1) are special function registers (SFRs) to select pull-up resistance or pull-down resistance for each port, or sampling frequency for the port secondary function of external interrupt.

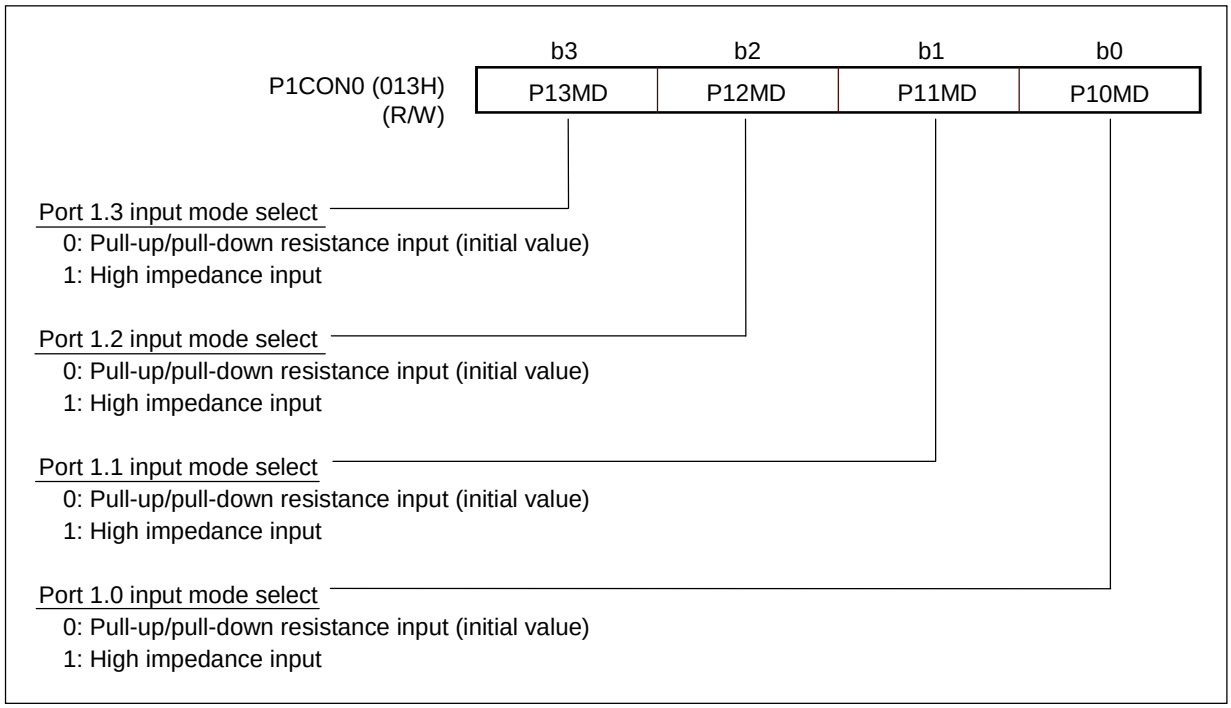


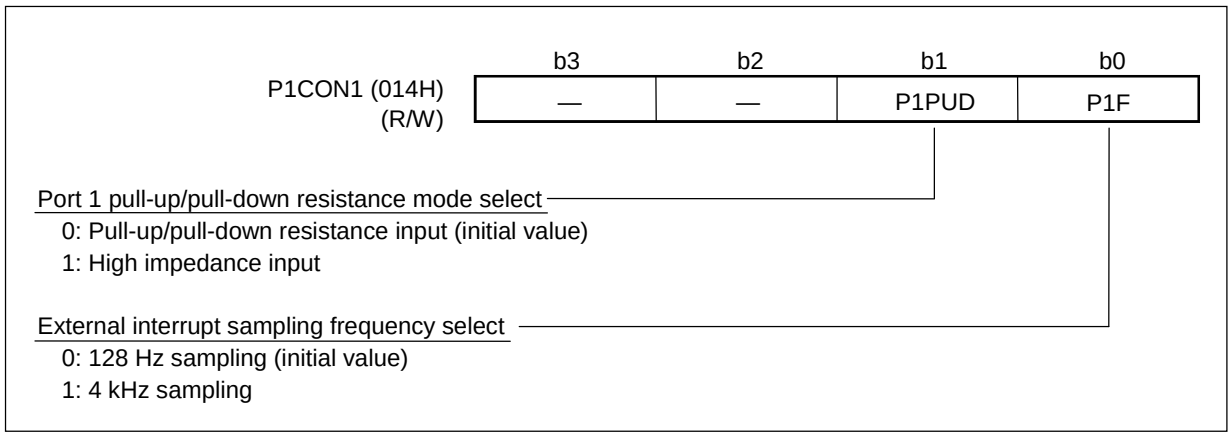


P0CON1 Bit1: P0PUD

This bit selects pull-up resistance or pull-down resistance when one of the pins of port 0 is specified as pull-up/pull-down resistance input by P0CON0. When P0PUD is reset to "0", this bit is selected as pull-down resistance input; when P0PUD is set to "1", the bit is selected as pull-up resistance input.

Note that specification of pull-down resistance input and pull-up resistance input of Ports 0.0 to 0.3 cannot be done independently for each pin.





P1CON1 Bit1: P1PUD

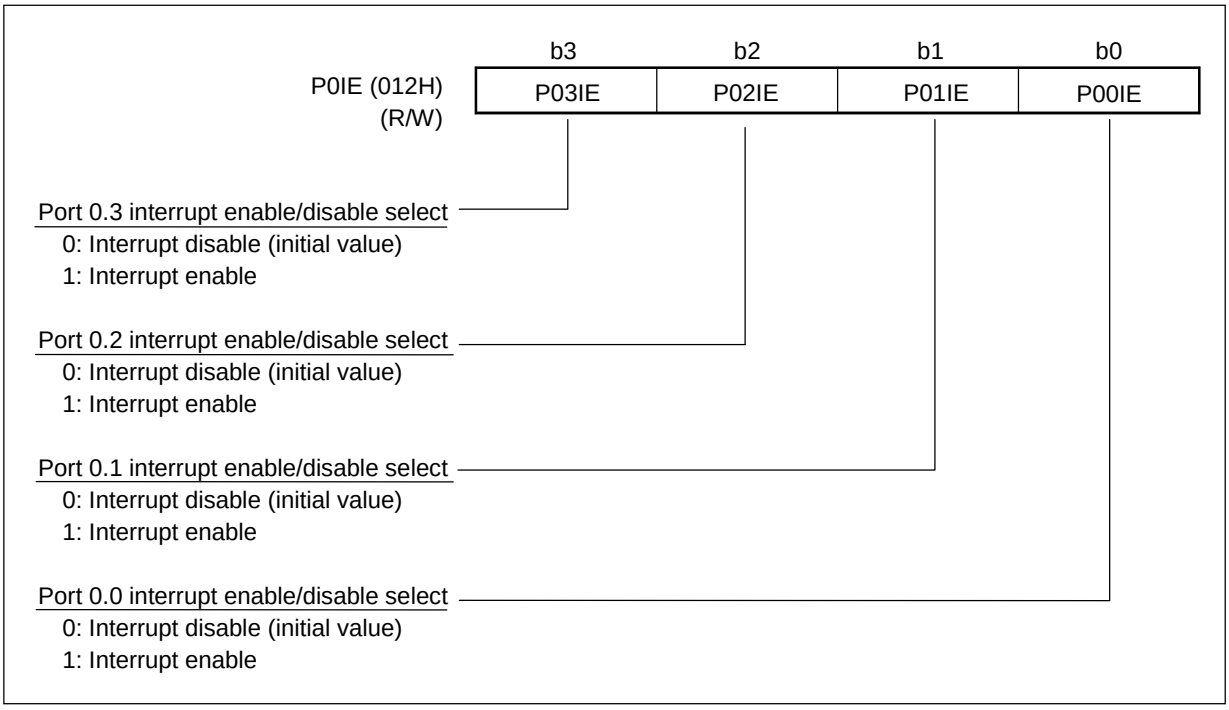
This is a bit for selecting pull-up resistance or pull-down resistance when one of the pins of port 1 is specified as pull-up/pull-down resistance input by P1CON1. When P1PUD is reset to "0", this bit is selected as pull-down resistance input; when P1PUD is set to "1", the bit is selected as pull-up resistance input.

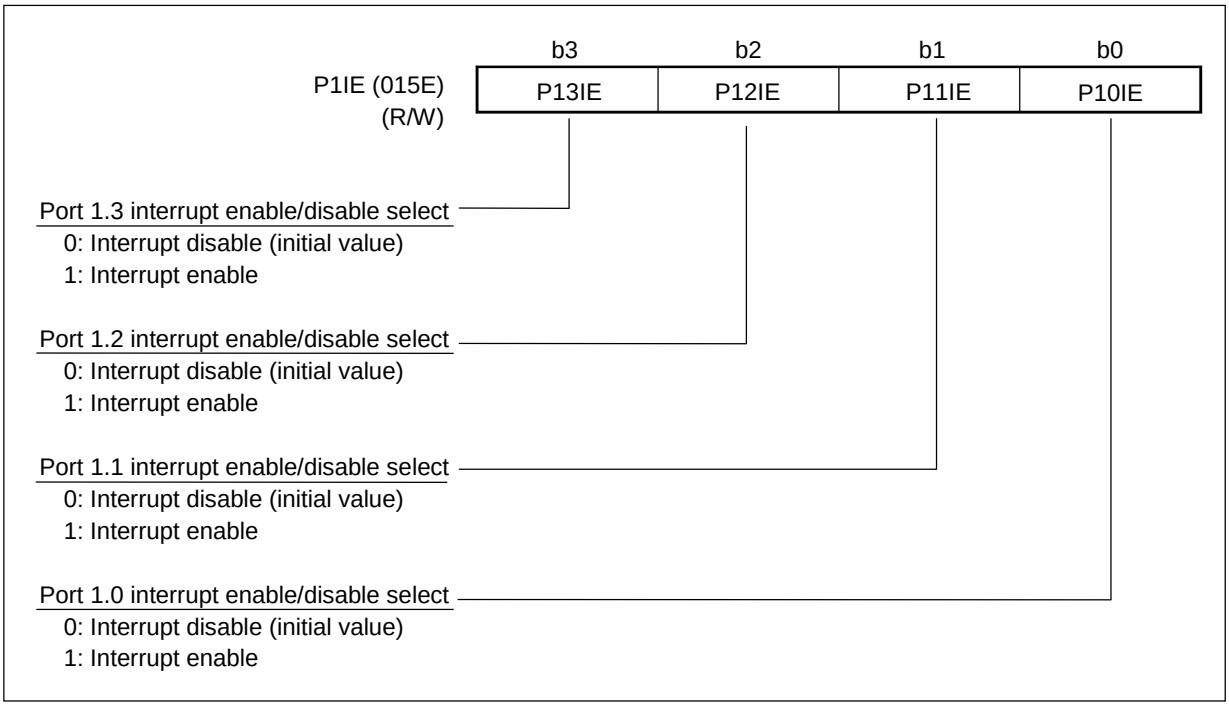
Note that specification of pull-down resistance input and pull-up resistance input of Ports 1.0 to 1.3 cannot be done independently for each pin.

(3) Port 0–1 interrupt enable register (P0IE, P1IE)

The port 0 interrupt enable register (P0IE) and port 1 interrupt enable register (P1IE) are 4-bit special function registers (SFRs) that enable/disable individual bits when the ports are used for external interrupt.

At system reset P0IE and P1IE are reset to "0", and ports 0 and 1 are all initialized to the interrupt disable state.





12.3.3 External interrupt function of ports 0–1 (External 5 interrupt)

An external 5 interrupt is assigned to port 0 and port 1 as a secondary function. Individual bits can be enabled/disabled for external 5 interrupt.

External interrupt generation for each input of ports 0 and 1 is triggered by the falling edge of either the 128 Hz or 4 kHz sampling clock from the time base counter.

After the port level changes, interrupt request signal XI5INT is output and external 5 interrupt request flag (QXI5) is set. The maximum time delay from the change in port level until setting QXI5 is one cycle of the sampling clock (128 Hz or 4 kHz).

Because the port 0 and port 1 external 5 interrupt is set by a level change at any of the port 0 and port 1 inputs, each bit of the ports must be read to determine which bit of the ports generated the interrupt.

The interrupt vector address for external 5 interrupt is 001EH.

Figure 12-2 shows an equivalent circuit of external 5 interrupt control.

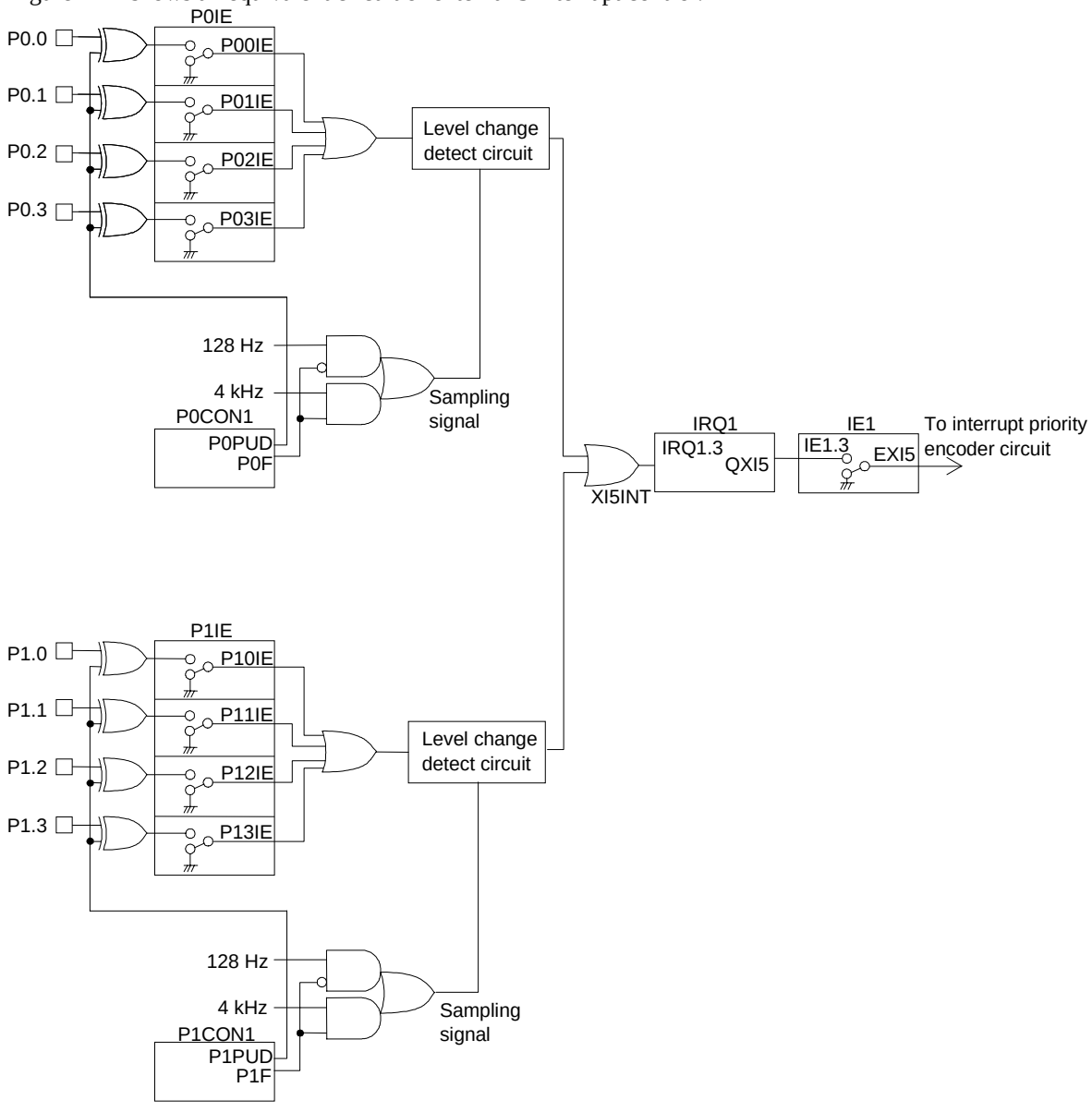
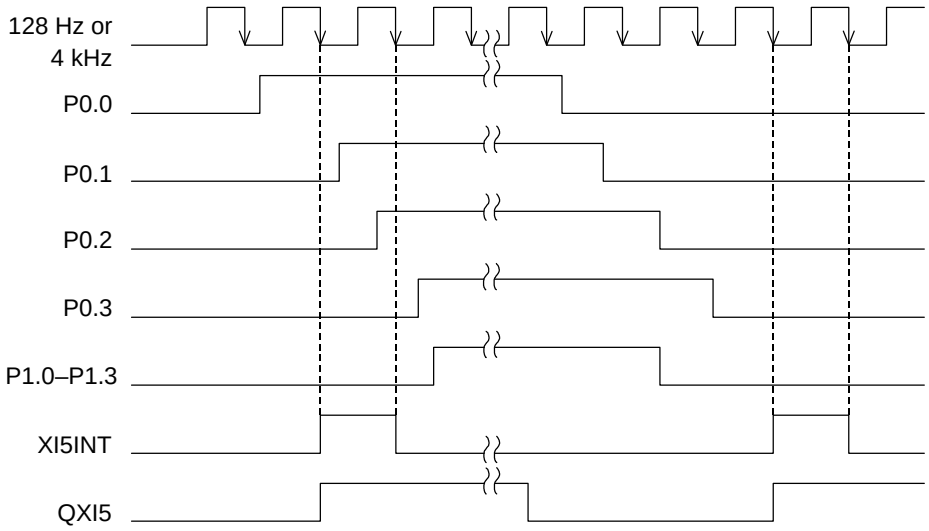


Figure 12-2 External 5 Interrupt Control Equivalent Circuit

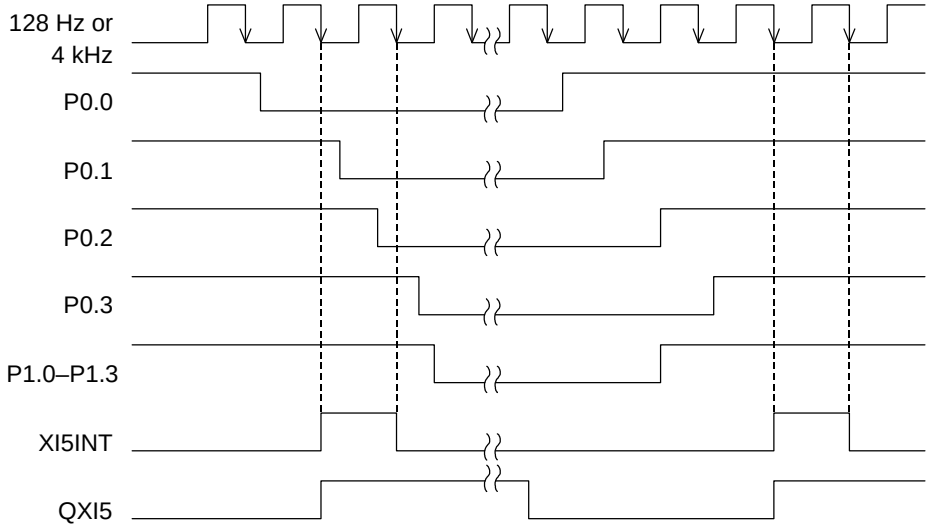
Figure 12-3 shows the timing for generation of external 5 interrupt.

(a) P0PUD = "0" and P1PUD = "0" (initial value: inputs with pull-down resistors) setting
- When all P0.0 to P0.3 and P1.0 to P1.3 inputs are at a "H" level
  External 5 interrupt is generated when all the port 0 and 1 inputs change to a "L" level.
- When all P0.0 to P0.3 and P1.0 to P1.3 inputs are at a "L" level
  External 5 interrupt is generated when any port 0 or 1 input changes to a "H" level.

(b) P0PUD = "1" and P1PUD = "1" (inputs with pull-up resistors) setting
- When all P0.0 to P0.3 and P1.0 to P1.3 inputs are at a "H" level
  External 5 interrupt is generated when any port 0 or 1 input changes to a "L" level.
- When all P0.0 to P0.3 and P1.0 to P1.3 inputs are at a "L" level
  External 5 interrupt is generated when all the port 0 or 1 inputs change to a "H" level.



(a) When P0PUD = "0" and P1PUD = "0"



(b) When P0PUD = "1" and P1PUD = "1"

Figure 12-3 External 5 Interrupt Generation Timing

12.4 Ports 2–3 (P2.0–P2.3, P3.0–P3.3)

12.4.1 Port 2–3 configuration

The MSM63188A has 4-bit output ports Port 2 and Port 3.

The circuit configuration of ports 2 and 3 are shown in Figure 12-4.

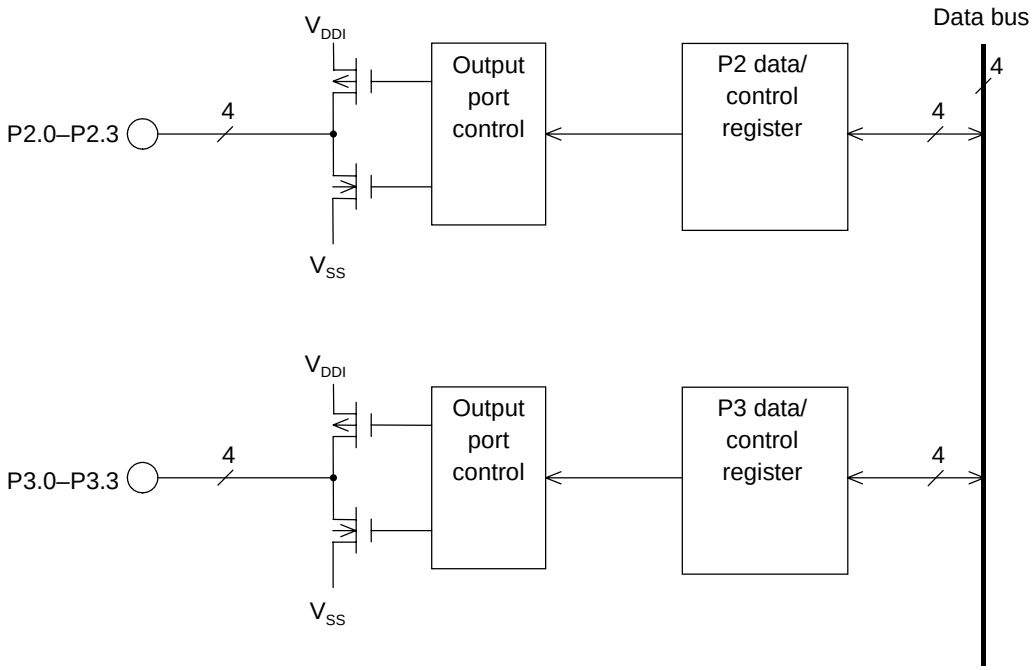
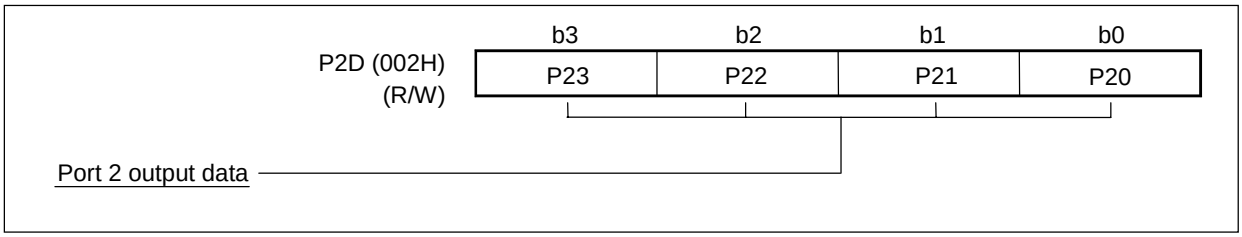


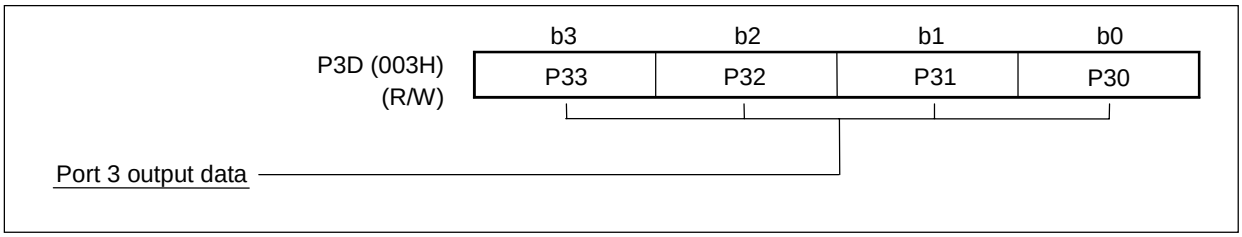
Figure 12-4 Configuration of Ports 2 and 3

12.4.2 Port 2–3 registers

(1) Port 2–3 data registers (P2D, P3D)

The port 2 data register (P2D) and port 3 data register (P3D) are 4-bit special function registers (SFRs) used to set the output values for ports 2 and 3.





At system reset P2D and P3D are reset to "0". When data is written to P2D and P3D, the actual pin change timing is the rising edge of the system clock for state 2 (S2) of the write instruction.

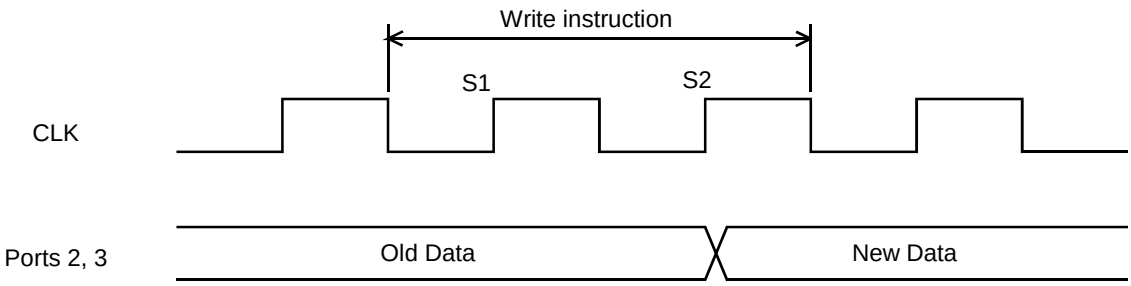


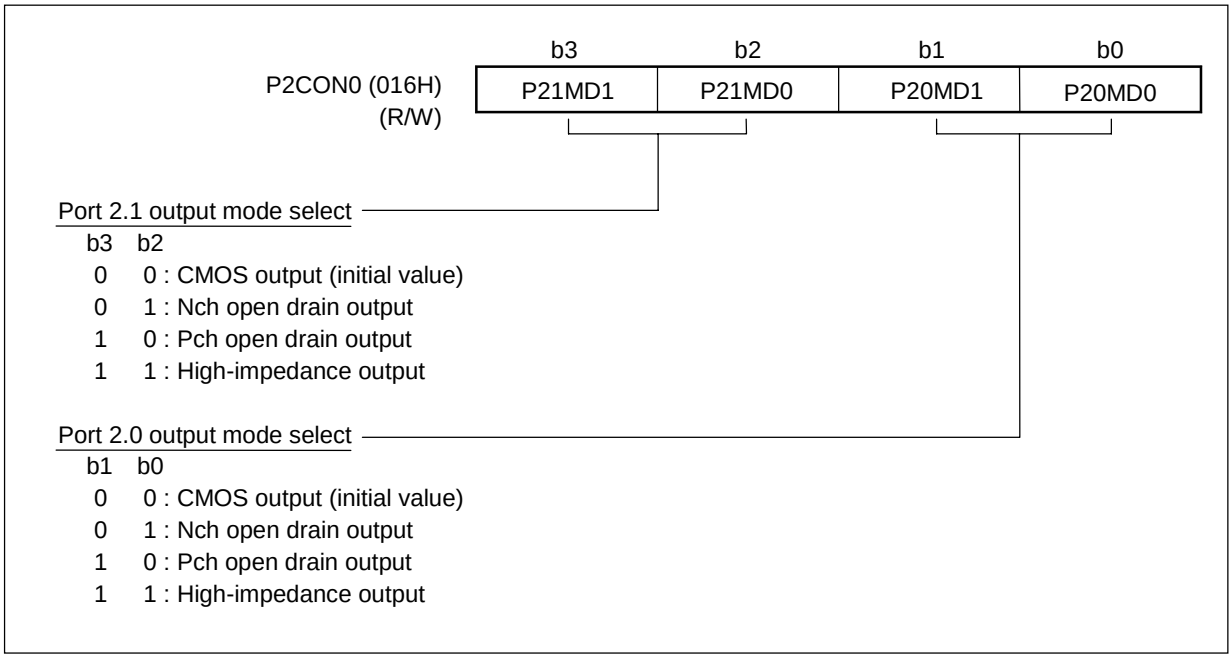
Figure 12-5 Port Change Timing

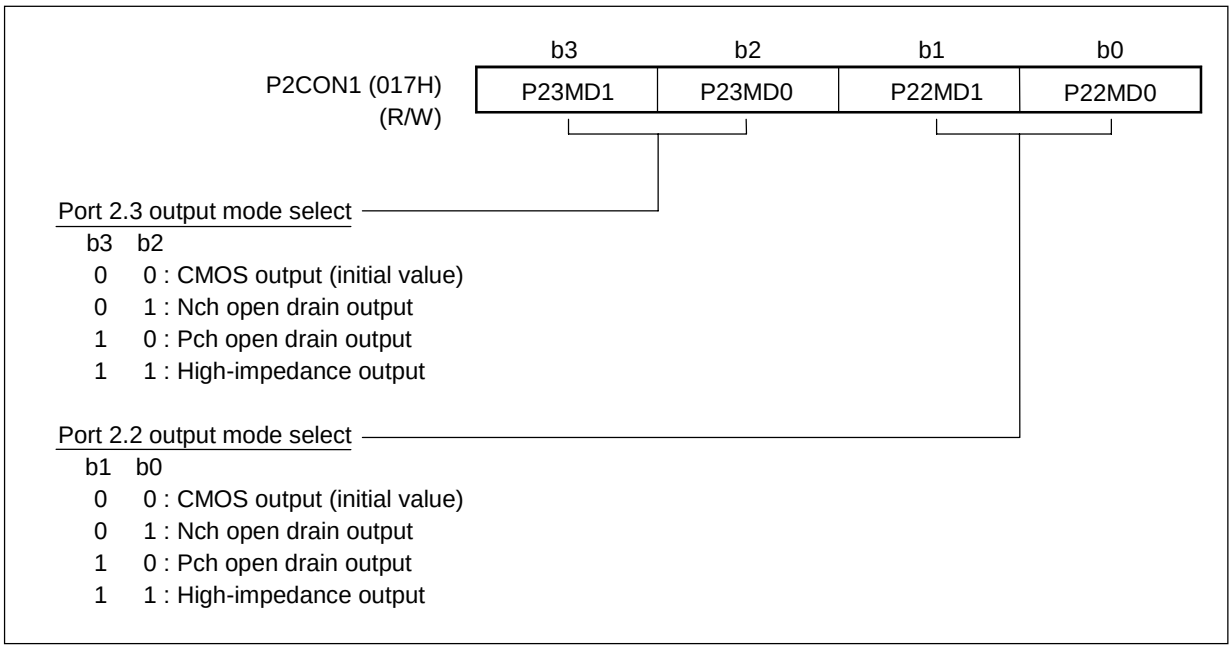
(2) Port 2–3 control registers 0/1 (P2CON0, P2CON1, P3CON0, P3CON1)

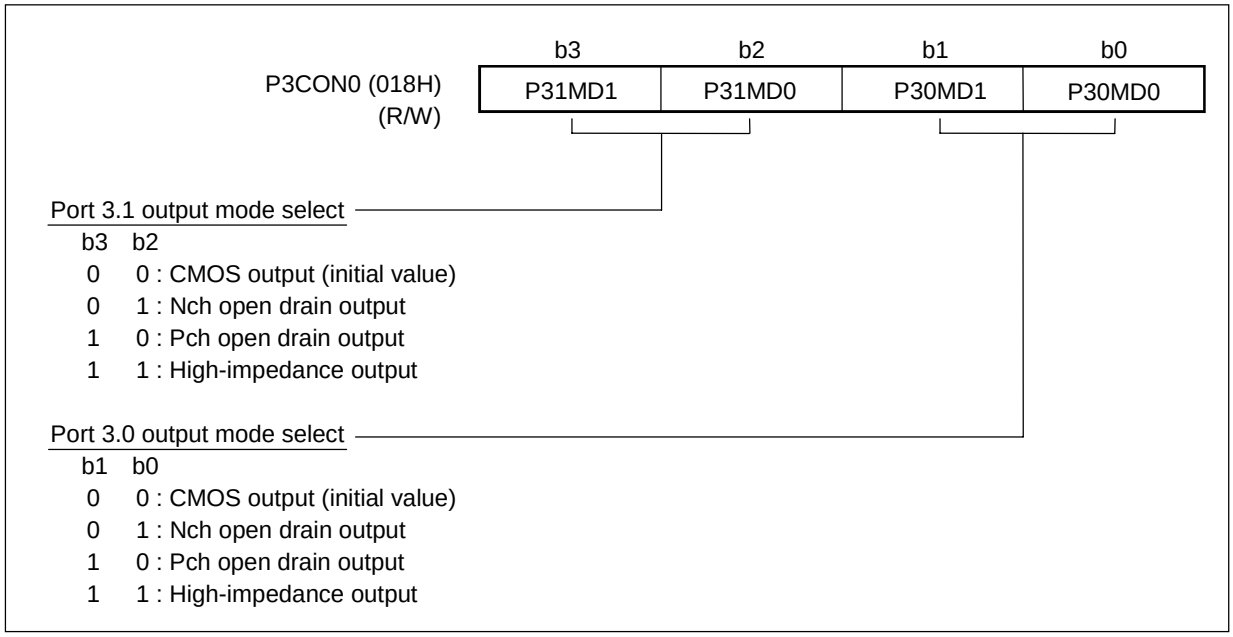
The port 2 control registers 0/1 (P2CON0, P2CON1) and port 3 control registers 0/1 (P3CON0, P3CON1) are 4-bit special function registers (SFRs) used to select port output modes.

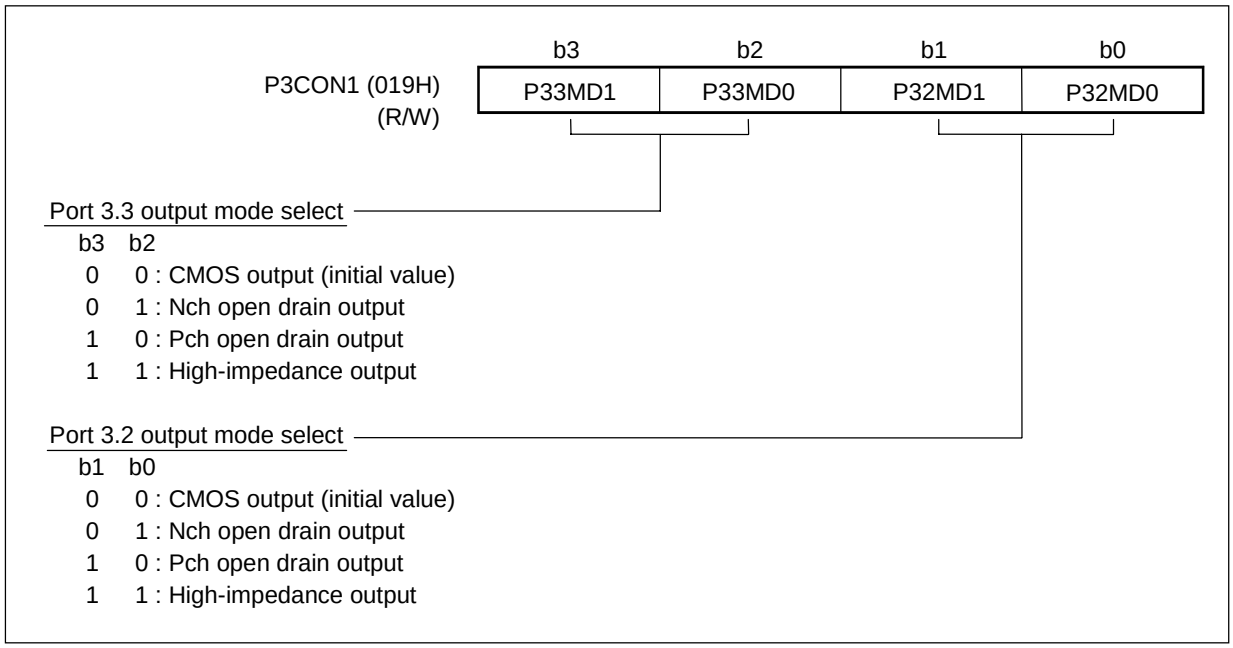
The output mode can be set to CMOS output, Nch open drain output, Pch open drain output, or high-impedance output.

At system reset P2CON0, P2CON1, P3CON0, and P3CON1 are reset to "0", and all ports are initialized to CMOS output mode.






b3
b2
b1
b0
P3CON0 (018H)
(R/W)
P31MD1
P31MD0
P30MD1
P30MD0
Port 3.1 output mode select
b3 b2
0 0 : CMOS output (initial value)
0 1 : Nch open drain output
1 0 : Pch open drain output
1 1 : High-impedance output
Port 3.0 output mode select
b1 b0
0 0 : CMOS output (initial value)
0 1 : Nch open drain output
1 0 : Pch open drain output
1 1 : High-impedance output


b3
b2
b1
b0
P3CON1 (019H)
(R/W)
P33MD1
P33MD0
P32MD1
P32MD0
Port 3.3 output mode select
b3 b2
0 0 : CMOS output (initial value)
0 1 : Nch open drain output
1 0 : Pch open drain output
1 1 : High-impedance output
Port 3.2 output mode select
b1 b0
0 0 : CMOS output (initial value)
0 1 : Nch open drain output
1 0 : Pch open drain output
1 1 : High-impedance output

12.5 Ports 4–7 (P4.0–P4.3, P5.0–P5.3, P6.0–P6.3, P7.0–P7.3)

12.5.1 Port 4–7 configuration

The MSM63182A, MSM63184A, and MSM63188A have 4-bit output ports Port 4, Port 5, Port 6, and Port 7.

The circuit configurations for ports 4, 5, 6, and 7 are shown in Figure 12-6.

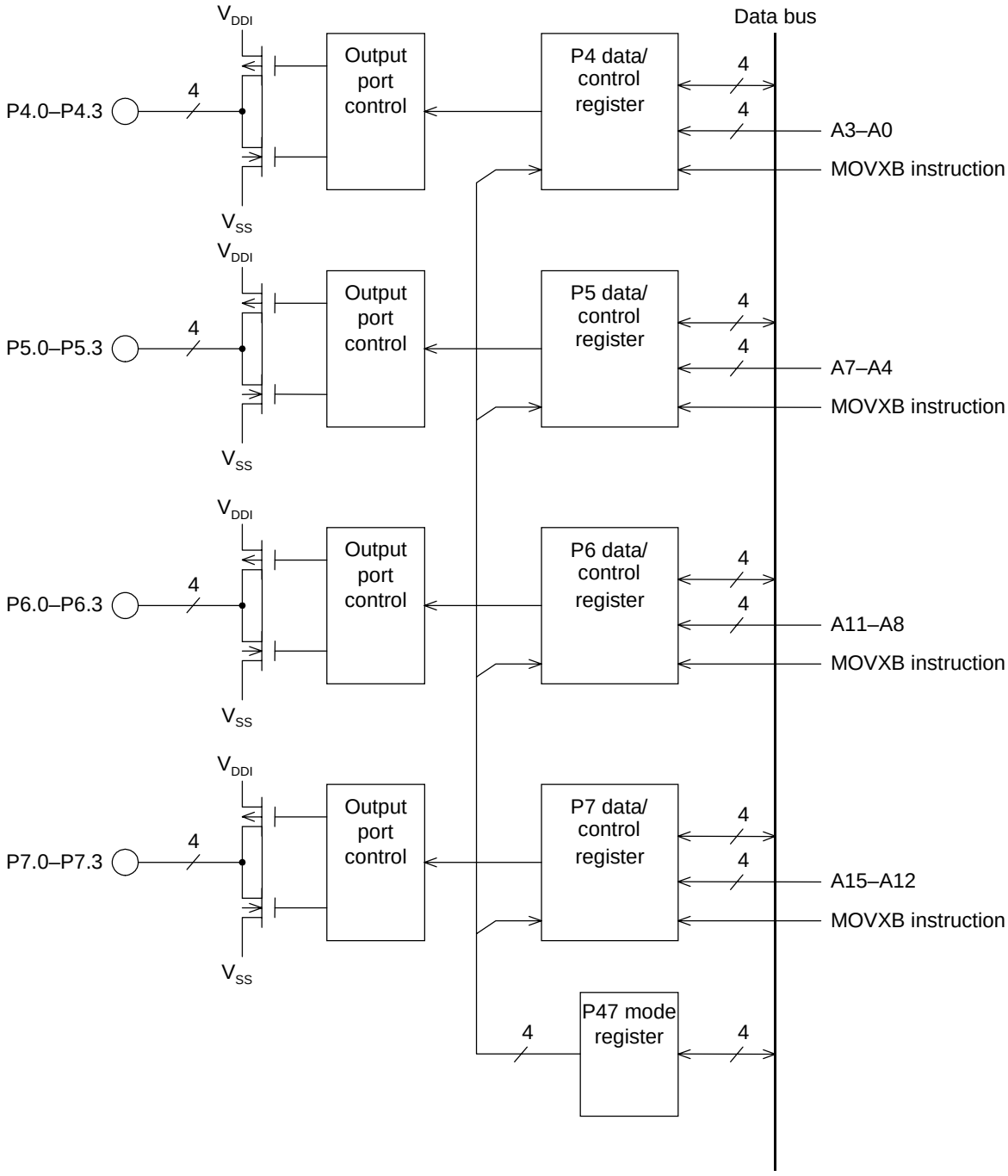
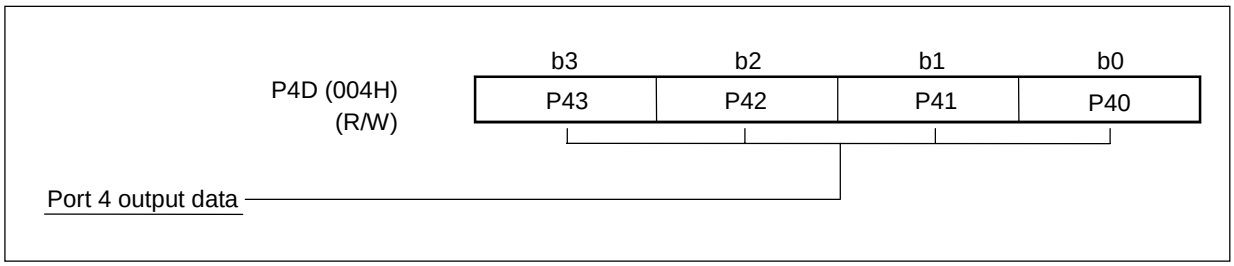


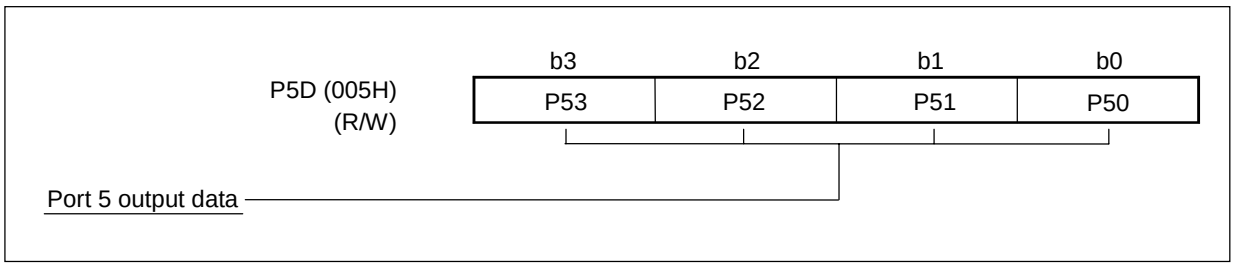
Figure 12-6 Configuration of Ports 4–7

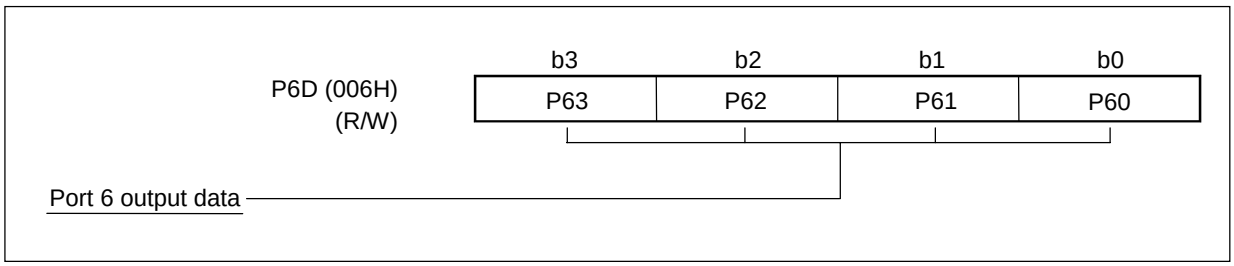
12.5.2 Port 4–7 registers

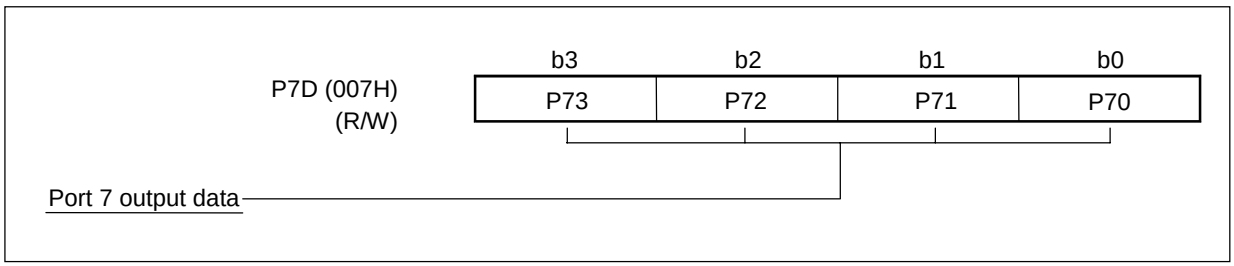
(1) Port 4–7 data registers (P4D, P5D, P6D, P7D)

The port 4 data register (P4D), port 5 data register (P5D), port 6 data register (P6D) and port 7 data register (P7D) are 4-bit special function registers (SFRs) used to set the output values for ports 4–7.









At system reset P4D, P5D, P6D, and P7D are reset to "0". When data is written to a port data register, the actual pin change timing is at the rising edge of the system clock for state 2 (S2) of the write instruction.

Figure 12-7 indicates port change timing.

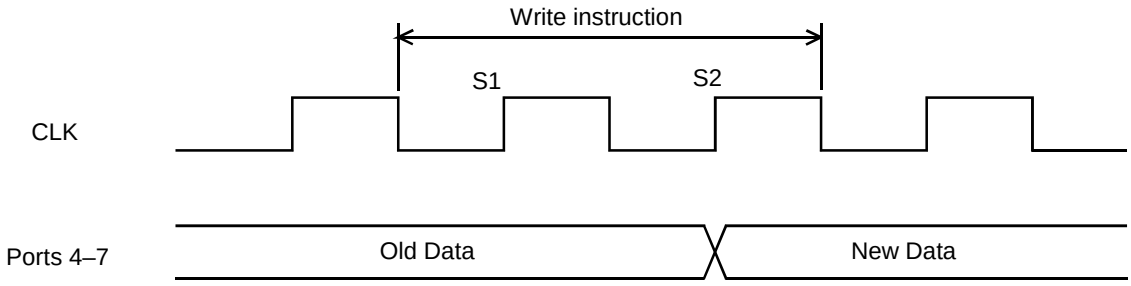


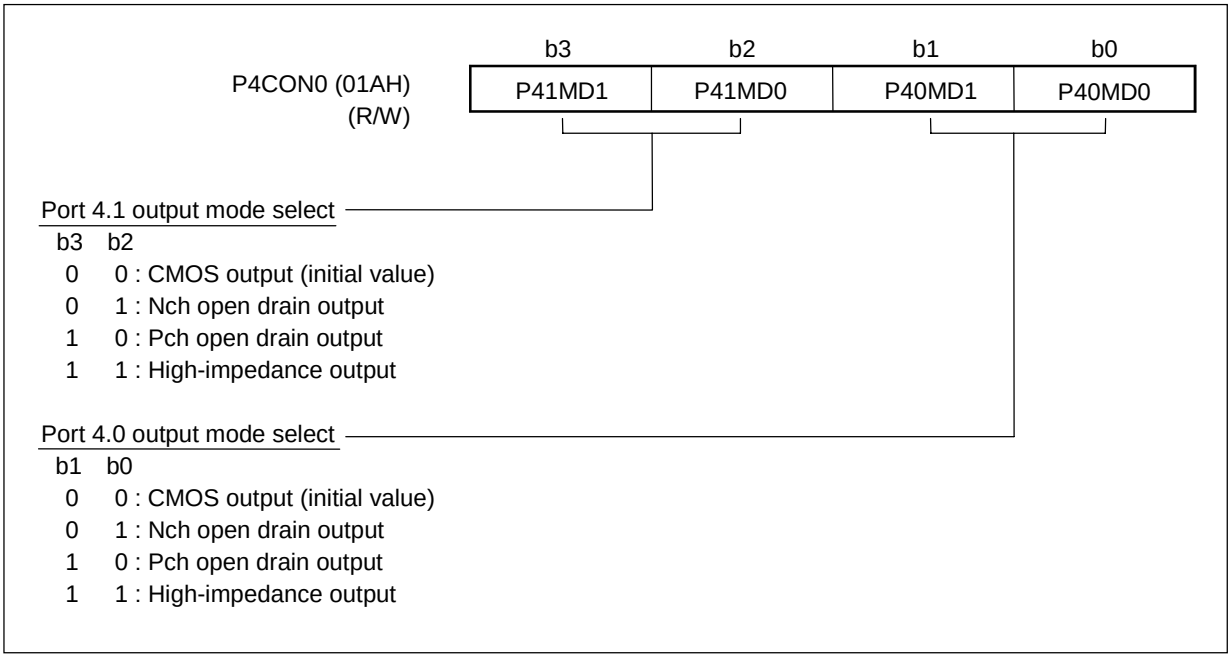
Figure 12-7 Port Change Timing

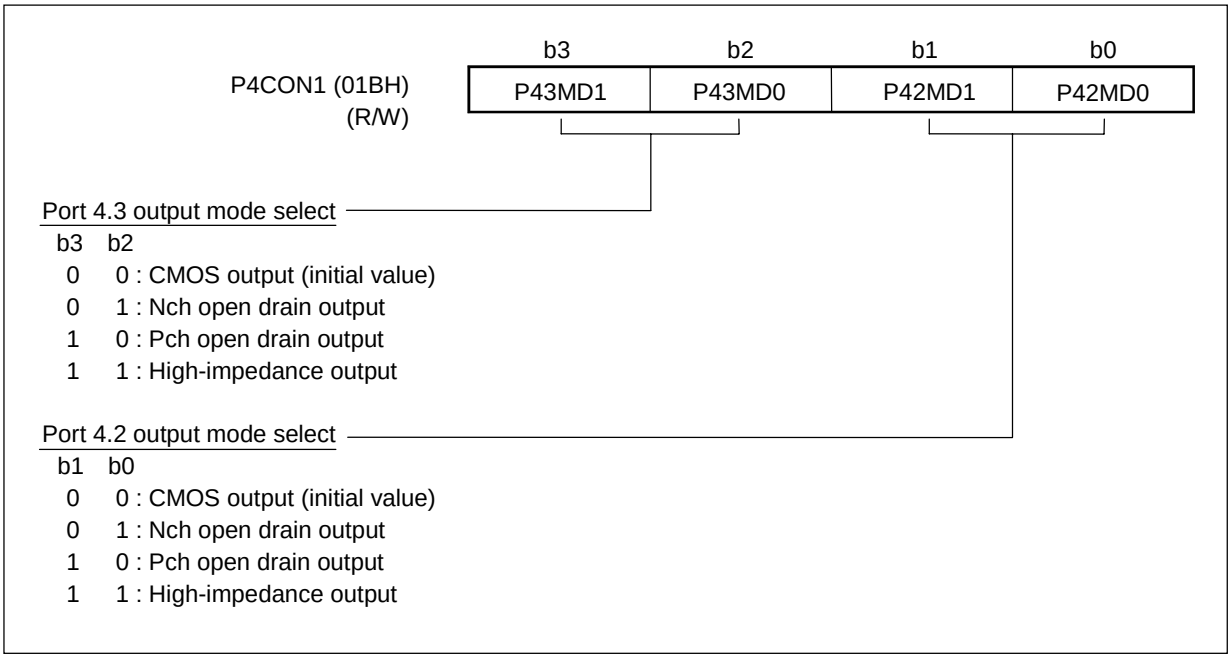
(2) Port 4–7 control registers 0/1 (P4CON0, P4CON1, P5CON0, P5CON1, P6CON0, P6CON1, P7CON0, P7CON1)

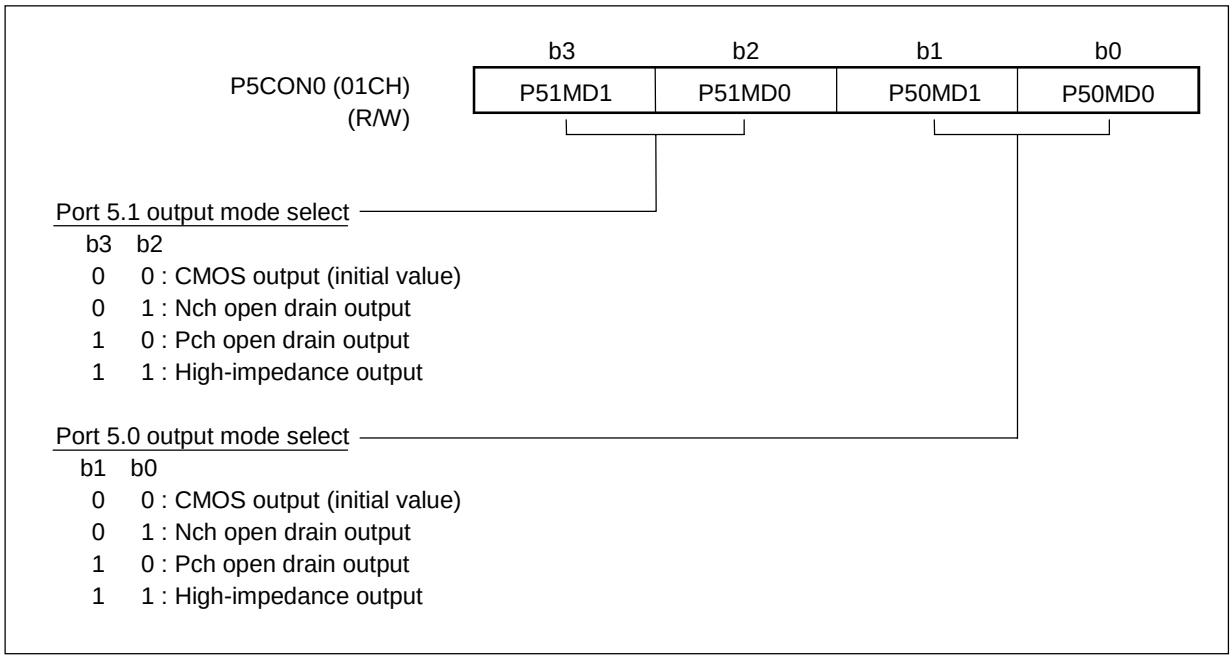
The port 4 control registers 0/1 (P4CON0, P4CON1), port 5 control registers 0/1 (P5CON0, P5CON1), port 6 control registers 0/1 (P6CON0, P6CON1) and port 7 control registers (P7CON0, P7CON1) are 4-bit special function registers (SFRs) used to select port output mode.

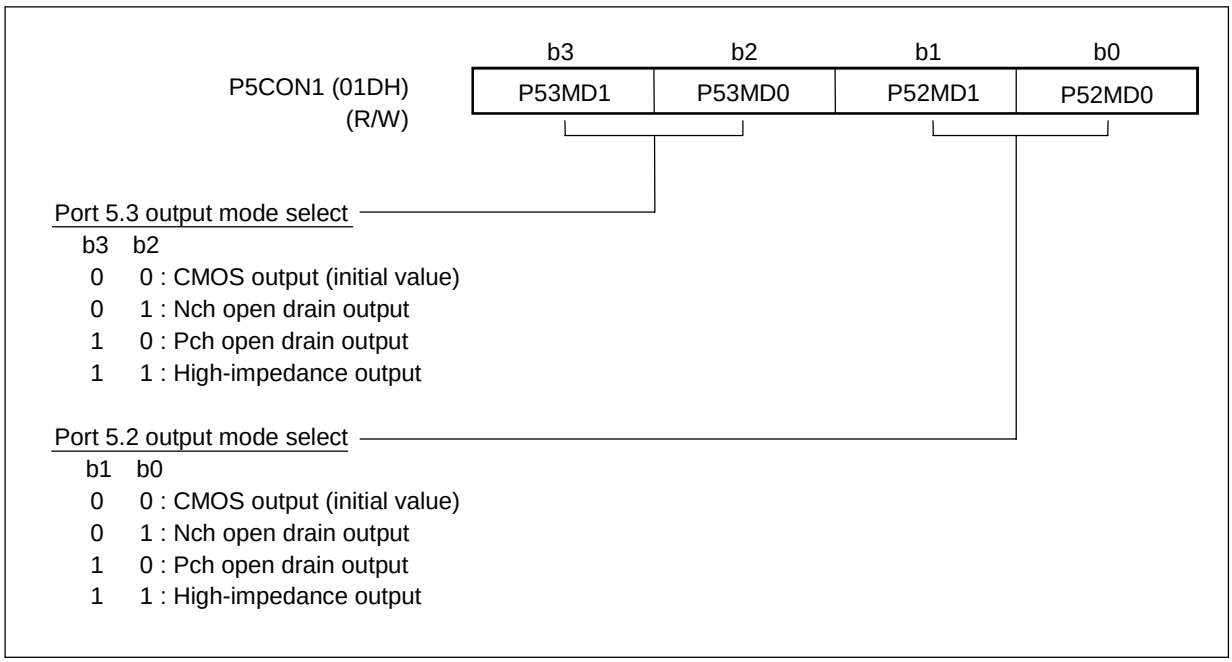
The output mode may be CMOS output, Nch open drain output, Pch open drain output or high-impedance output.

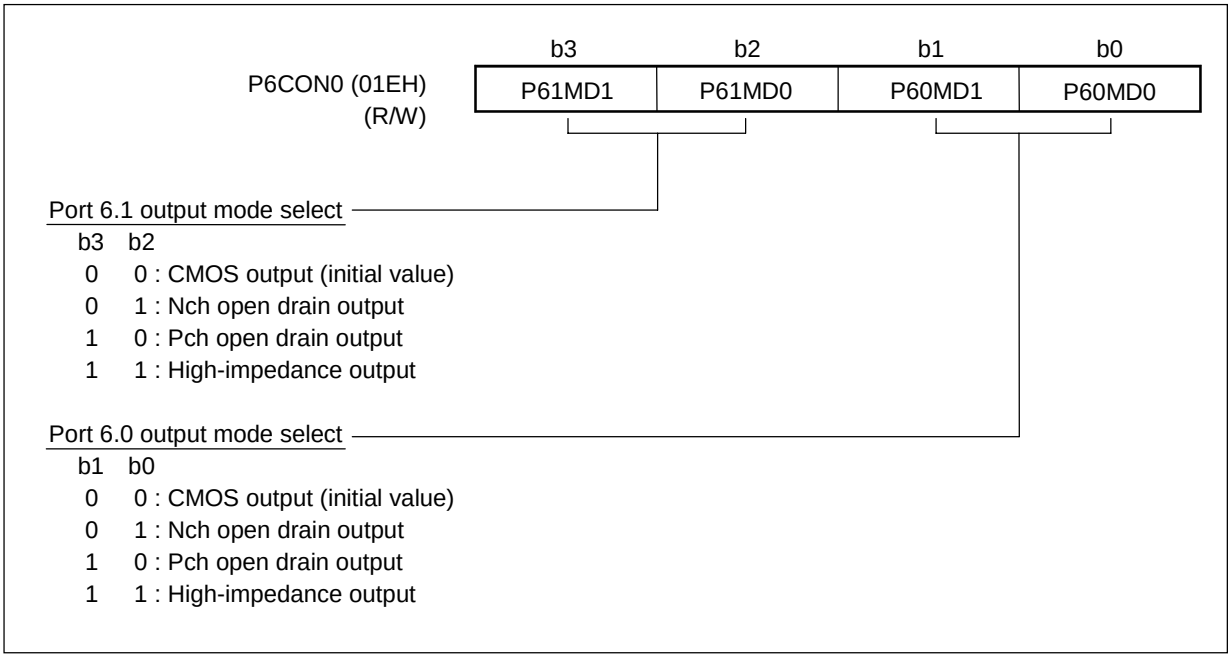
At system reset the port control registers are reset to "0", and ports 4–7 are all initialized to the CMOS output mode.

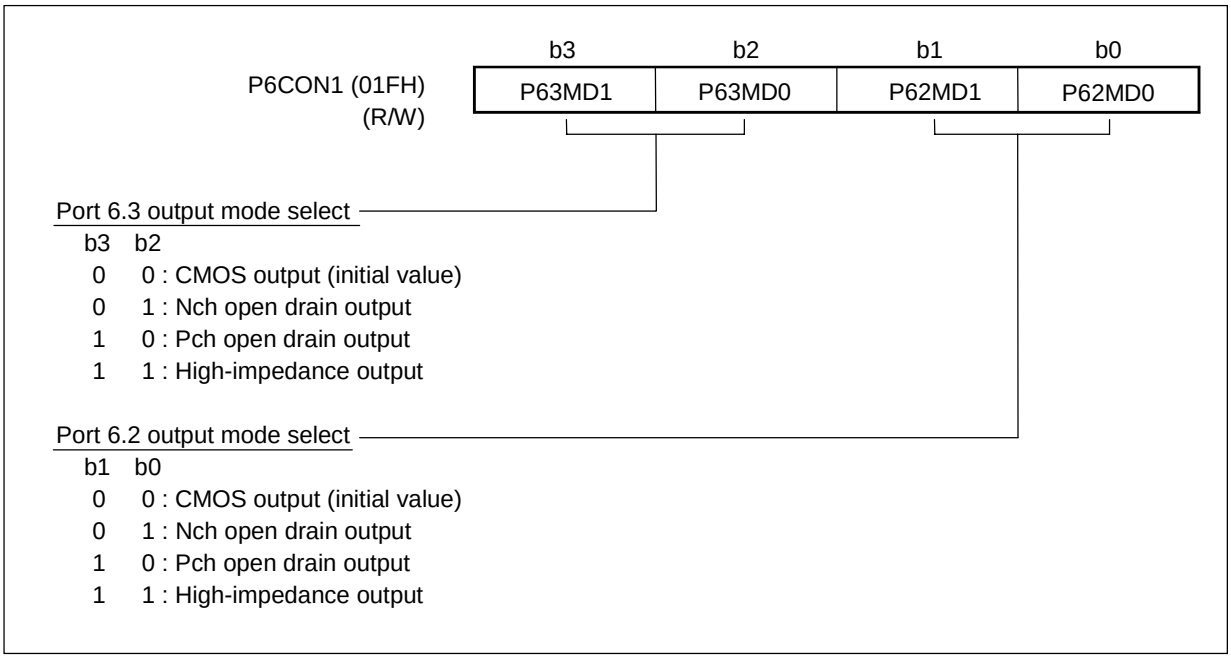


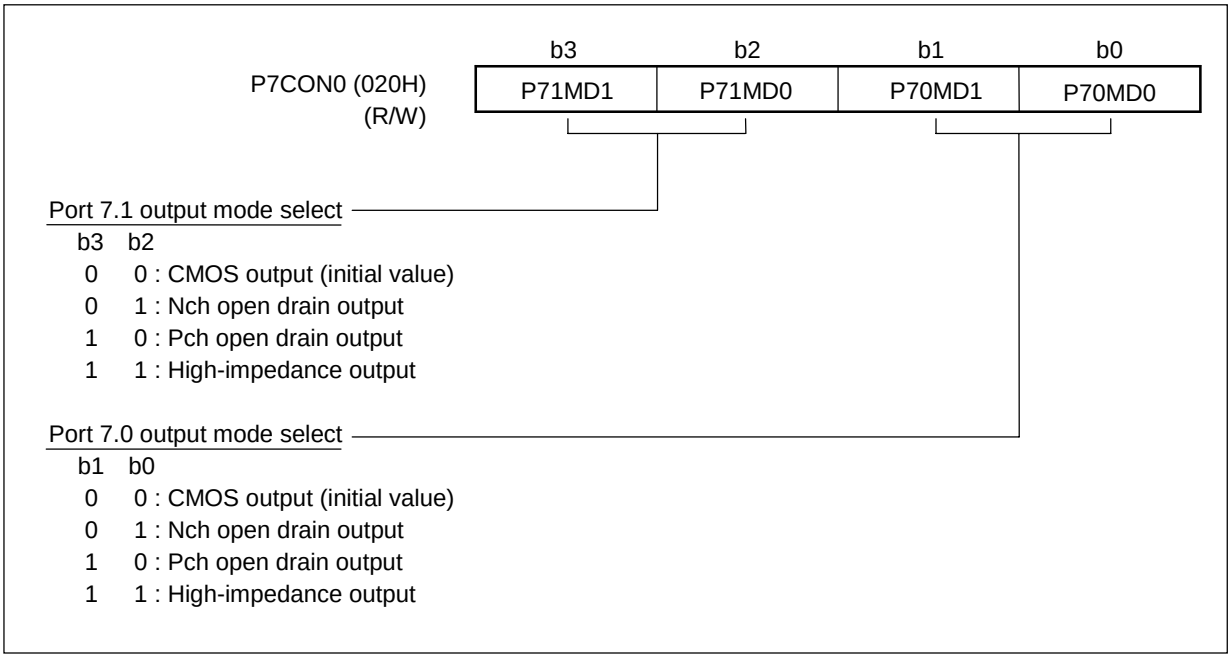


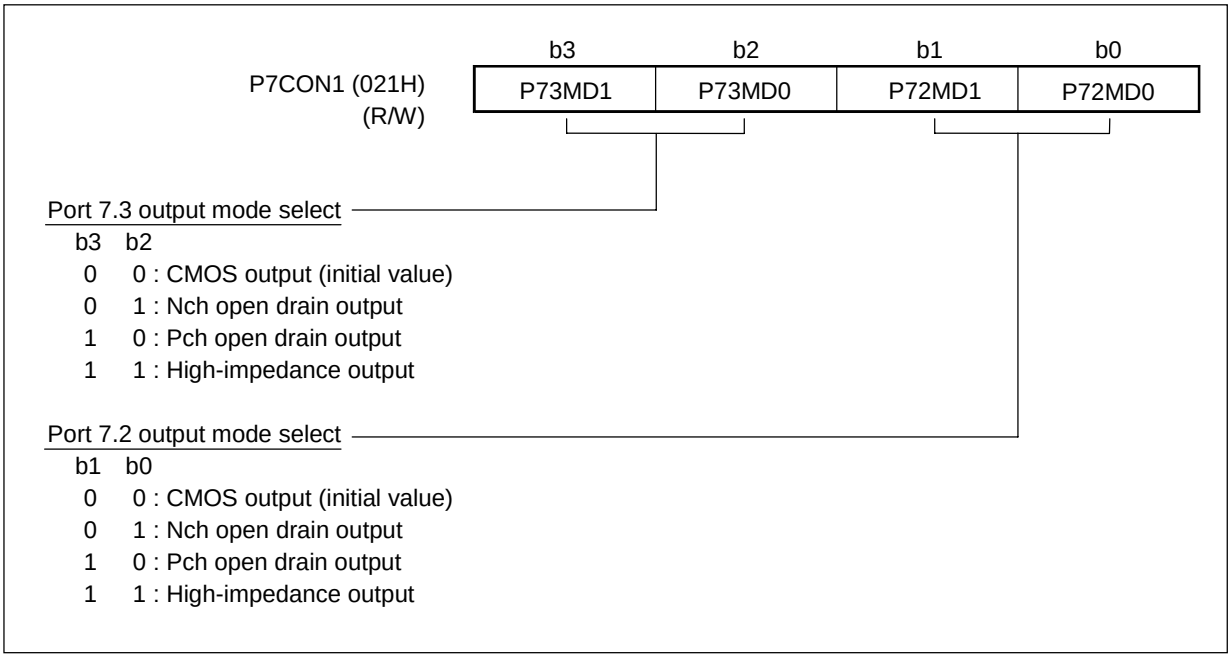

b3
b2
b1
b0
P5CON0 (01CH)
(R/W)
P51MD1
P51MD0
P50MD1
P50MD0
Port 5.1 output mode select
b3 b2
0 0 : CMOS output (initial value)
0 1 : Nch open drain output
1 0 : Pch open drain output
1 1 : High-impedance output
Port 5.0 output mode select
b1 b0
0 0 : CMOS output (initial value)
0 1 : Nch open drain output
1 0 : Pch open drain output
1 1 : High-impedance output


b3
b2
b1
b0
P5CON1 (01DH)
(R/W)
P53MD1
P53MD0
P52MD1
P52MD0
Port 5.3 output mode select
b3 b2
0 0 : CMOS output (initial value)
0 1 : Nch open drain output
1 0 : Pch open drain output
1 1 : High-impedance output
Port 5.2 output mode select
b1 b0
0 0 : CMOS output (initial value)
0 1 : Nch open drain output
1 0 : Pch open drain output
1 1 : High-impedance output


b3
b2
b1
b0
P6CON0 (01EH)
(R/W)
P61MD1
P61MD0
P60MD1
P60MD0
Port 6.1 output mode select
b3 b2
0 0 : CMOS output (initial value)
0 1 : Nch open drain output
1 0 : Pch open drain output
1 1 : High-impedance output
Port 6.0 output mode select
b1 b0
0 0 : CMOS output (initial value)
0 1 : Nch open drain output
1 0 : Pch open drain output
1 1 : High-impedance output

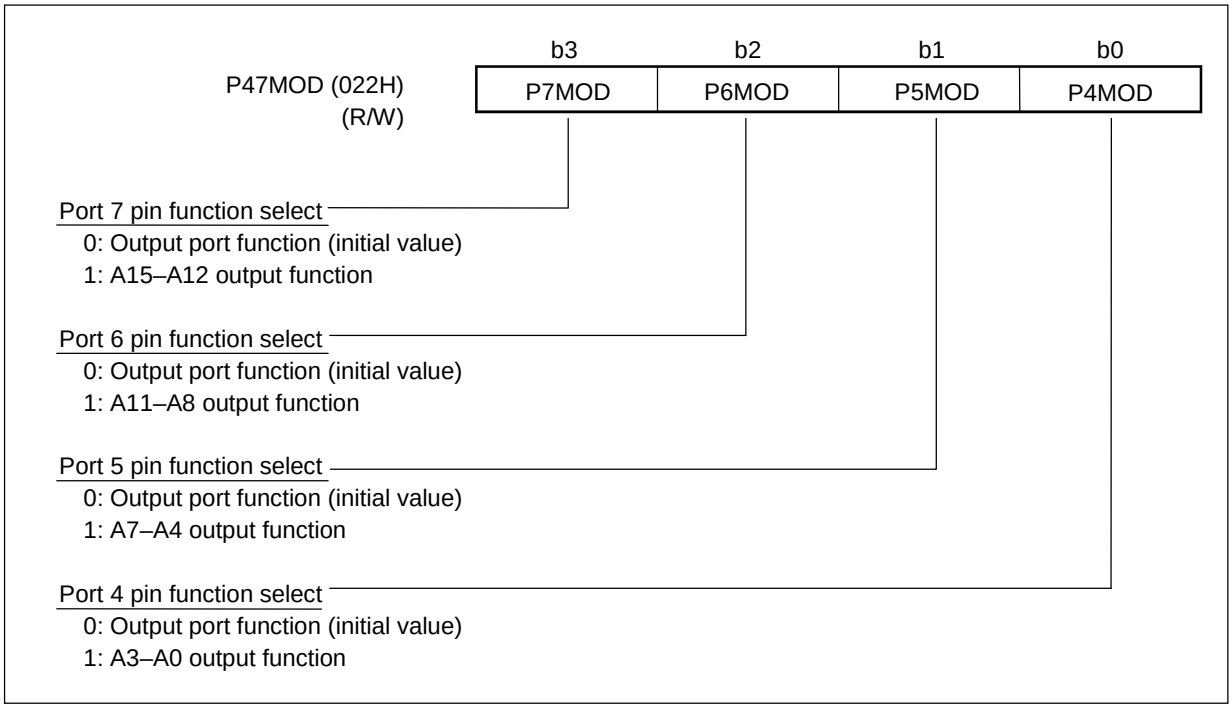

b3
b2
b1
b0
P6CON1 (01FH)
(R/W)
P63MD1
P63MD0
P62MD1
P62MD0
Port 6.3 output mode select
b3 b2
0 0 : CMOS output (initial value)
0 1 : Nch open drain output
1 0 : Pch open drain output
1 1 : High-impedance output
Port 6.2 output mode select
b1 b0
0 0 : CMOS output (initial value)
0 1 : Nch open drain output
1 0 : Pch open drain output
1 1 : High-impedance output


b3
b2
b1
b0
P7CON0 (020H)
(R/W)
P71MD1
P71MD0
P70MD1
P70MD0
Port 7.1 output mode select
b3 b2
0 0 : CMOS output (initial value)
0 1 : Nch open drain output
1 0 : Pch open drain output
1 1 : High-impedance output
Port 7.0 output mode select
b1 b0
0 0 : CMOS output (initial value)
0 1 : Nch open drain output
1 0 : Pch open drain output
1 1 : High-impedance output


b3
b2
b1
b0
P7CON1 (021H)
(R/W)
P73MD1
P73MD0
P72MD1
P72MD0
Port 7.3 output mode select
b3 b2
0 0 : CMOS output (initial value)
0 1 : Nch open drain output
1 0 : Pch open drain output
1 1 : High-impedance output
Port 7.2 output mode select
b1 b0
0 0 : CMOS output (initial value)
0 1 : Nch open drain output
1 0 : Pch open drain output
1 1 : High-impedance output

(3) Port 4–7 mode register (P47MOD)

The port 4–7 mode register (P47MOD) is a 4-bit special function register (SFR) that enables the external memory address bus function, which is the secondary function of ports 4–7.



At system reset the P47MOD register is reset to "0", and ports 4–7 are all set as normal output ports. When P47MOD bits are set to "1" and the MOVXB instruction executed, external memory addresses are output to the ports. If the MOVXB instruction is not executed, data register contents are output to the ports.

12.6 Ports 8–A (P8.0–P8.3, P9.0–P9.3, PA.0–PA.3)

12.6.1 Port 8–A configuration

The MSM63182A, MSM63184A, and MSM63188A have 4-bit input/output ports Port 8, Port 9, and Port A.

The circuit configurations for ports 8–A are shown in Figure 12-8.

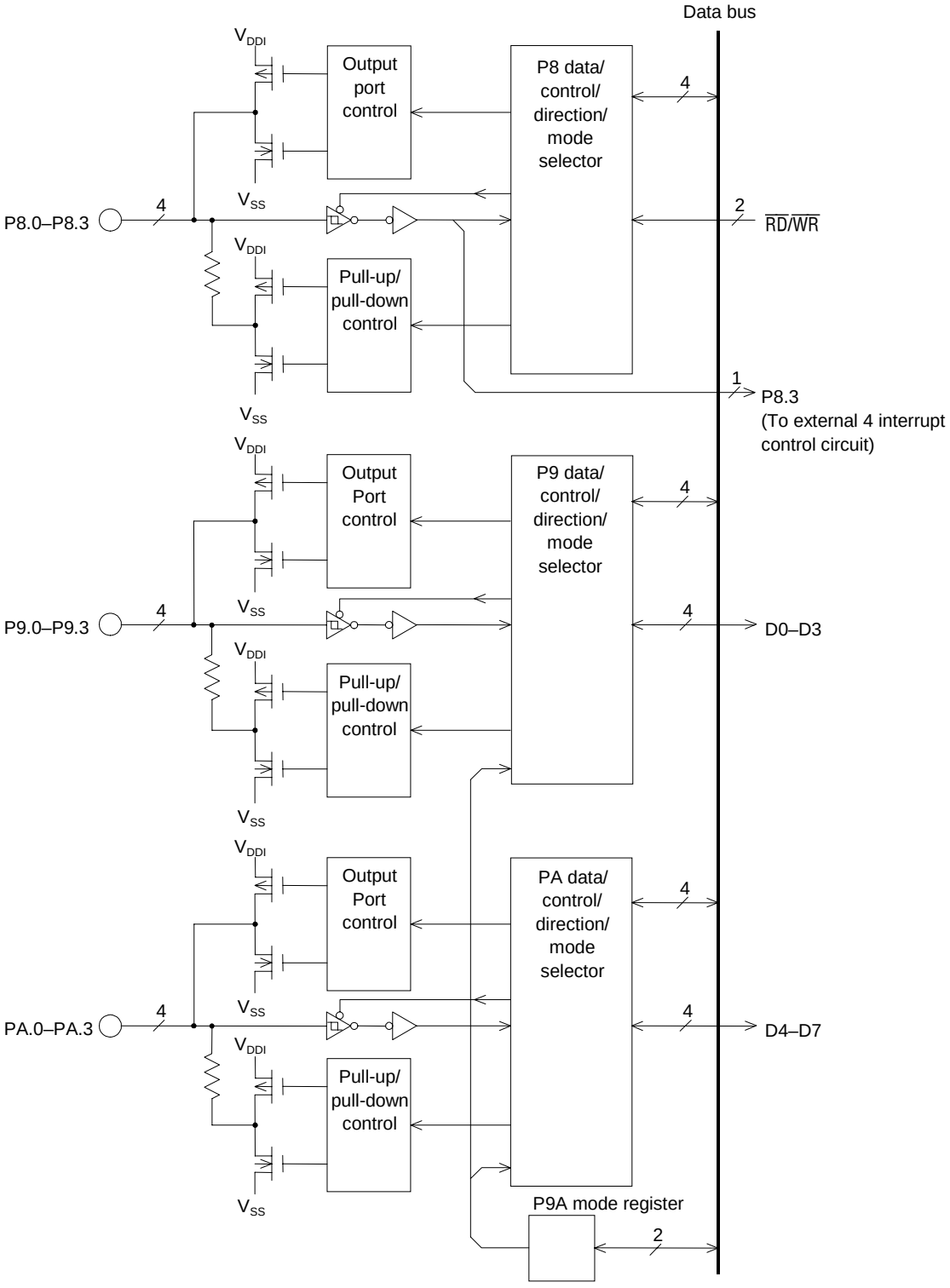


Figure 12-8 Configuration of Ports 8–A

12.6.2 Port 8–A registers

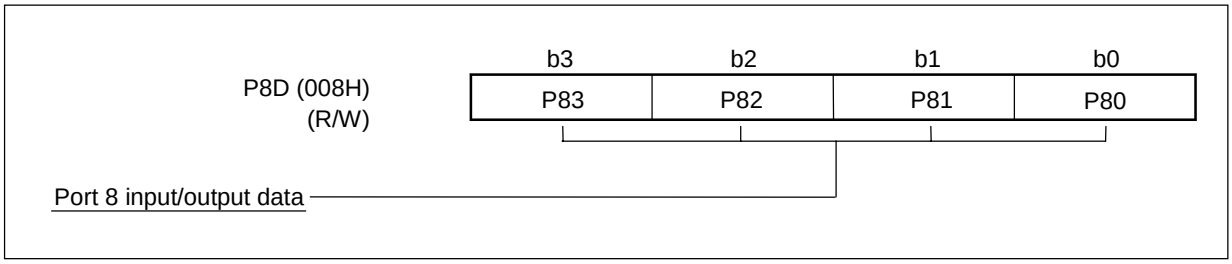
(1) Port 8–A data registers (P8D, P9D, PAD)

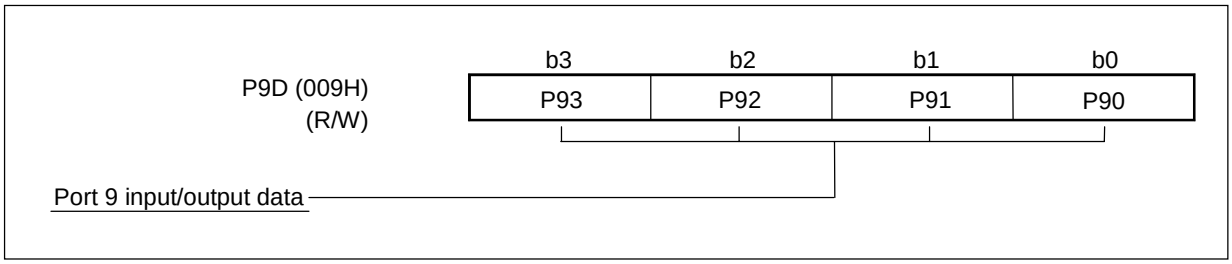
The port 8 data register (P8D), port 9 data register (P9D) and port A data register (PAD) are 4-bit special function registers (SFRs) used to set the output values for ports 8–A.

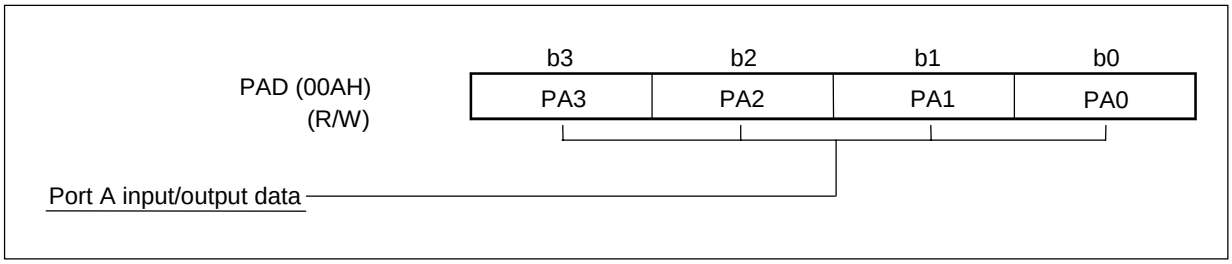
When port direction register (P8DIR, P9DIR, PADIR) bits are set to "1" and the output mode selected, the contents of the port data registers are output to the ports.

When the output mode is selected and P8D, P9D, and PAD read, the contents of P8D, P9D, and PAD are read.

If P8DIR, P9DIR, and PADIR bits are reset to "0", the input mode selected and the P8D, P9D, and PAD read, the port pin level is read.







At system reset P8D, P9D, and PAD are reset to "0". When data is written to a port data register, the actual pin change timing is at the rising edge of the system clock for state 2 (S2) of the write instruction.

Figure 12-9 shows port change timing.

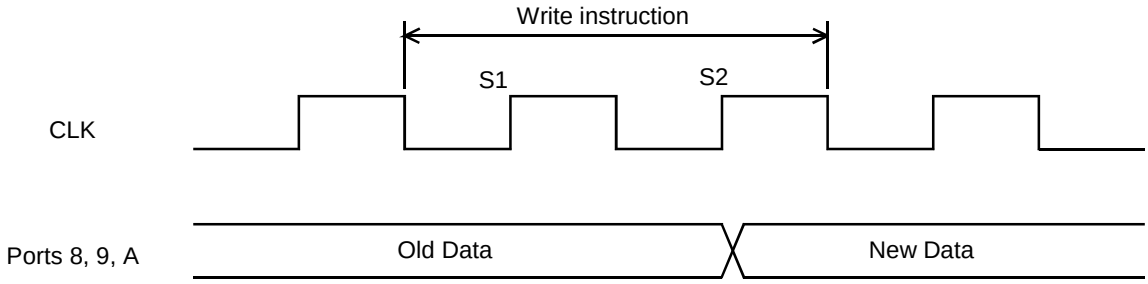
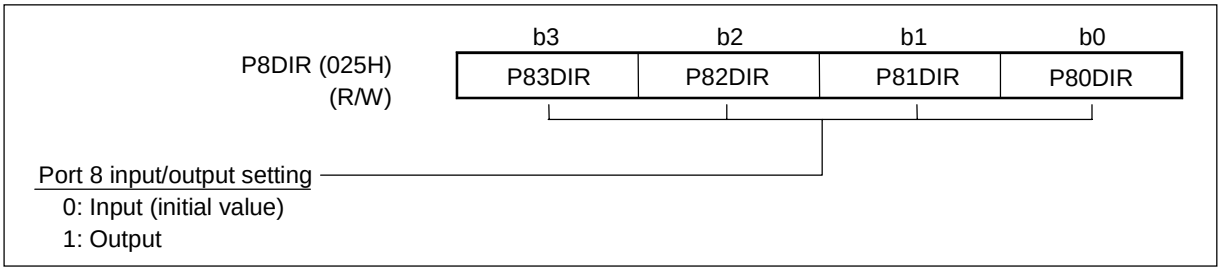


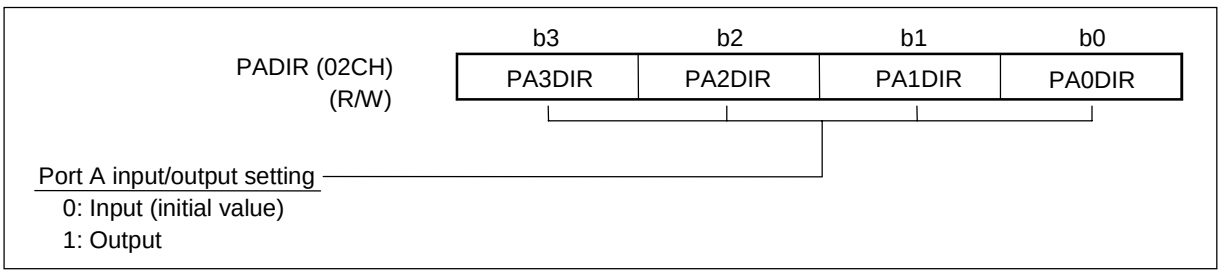
Figure 12-9 Port Change Timing

(2) Port 8–A direction registers (P8DIR, P9DIR, PADIR)

The port 8 direction register (P8DIR), port 9 direction register (P9DIR), and port A direction register (PADIR) are 4-bit special function registers (SFRs) which specify the port input/output direction in bit units. Pins corresponding to P8DIR, P9DIR, and PADIR bits reset to "0" are input, and those corresponding to bits set to "1" are output.

At system reset P8DIR, P9DIR, and PADIR are reset to "0", and ports 8, 9, and A are all initialized to input mode.





(3) Port 8–A control registers 0/1 (P8CON0, P8CON1, P9CON0, P9CON1, PACON0, PACON1)

The port 8 control registers 0/1 (P8CON0, P8CON1), port 9 control registers 0/1 (P9CON0, P9CON1), and port A control registers 0/1 (PACON0, PACON1) are 4-bit special function registers (SFRs) used to select port input/output mode.

The input mode may be pull-down resistance input, pull-up resistance input or high-impedance input.

The output mode may be CMOS output, Nch open drain output, Pch open drain output or high-impedance output.

P8CON0 (023H) (R/W)

b3	b2	b1	b0
P81MD1	P81MD0	P80MD1	P80MD0

Port 8.1 input/output mode select

Input mode		Output mode	
b3	b2	b3	b2
0	0: Pull-down resistance (initial value)	0	0: CMOS output (initial value)
1	0: Pull-up resistance	0	1: Nch open drain output
×	1: High-impedance input	1	0: Pch open drain output
		1	1: High-impedance output

Port 8.0 input/output mode select

Input mode		Output mode	
b1	b0	b1	b0
0	0: Pull-down resistance (initial value)	0	0: CMOS output (initial value)
1	0: Pull-up resistance	0	1: Nch open drain output
1	×: High-impedance input	1	0: Pch open drain output
		1	1: High-impedance output

P8CON1 (024H) (R/W)

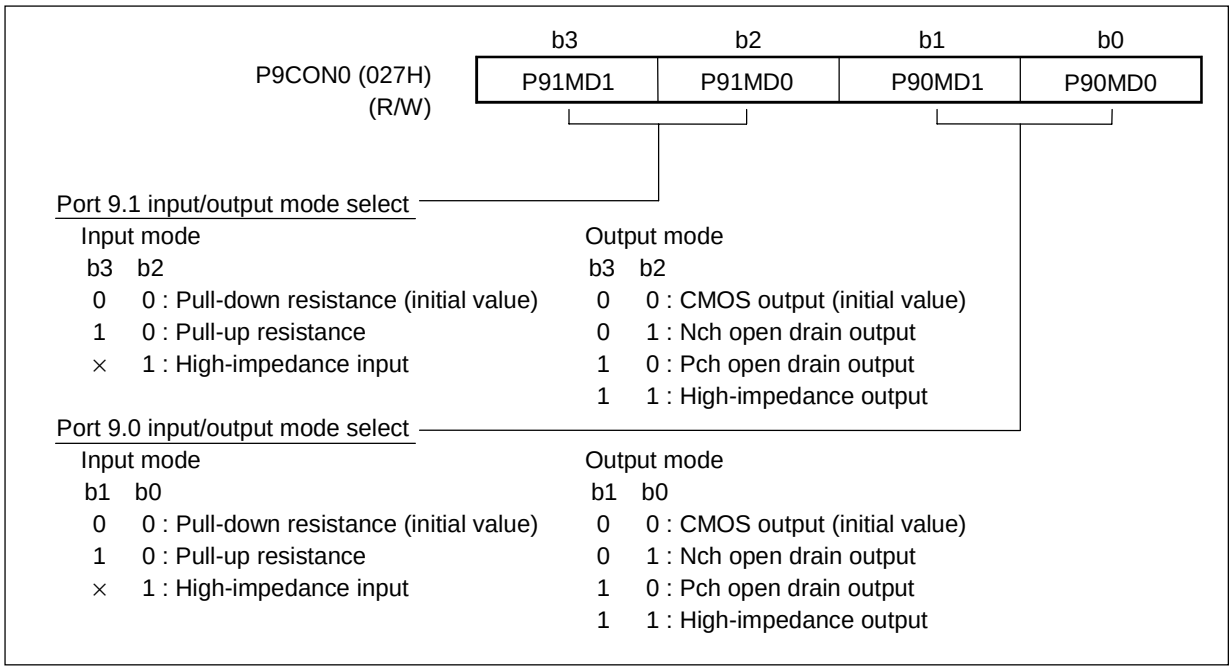
b3	b2	b1	b0
P83MD1	P83MD0	P82MD1	P82MD0

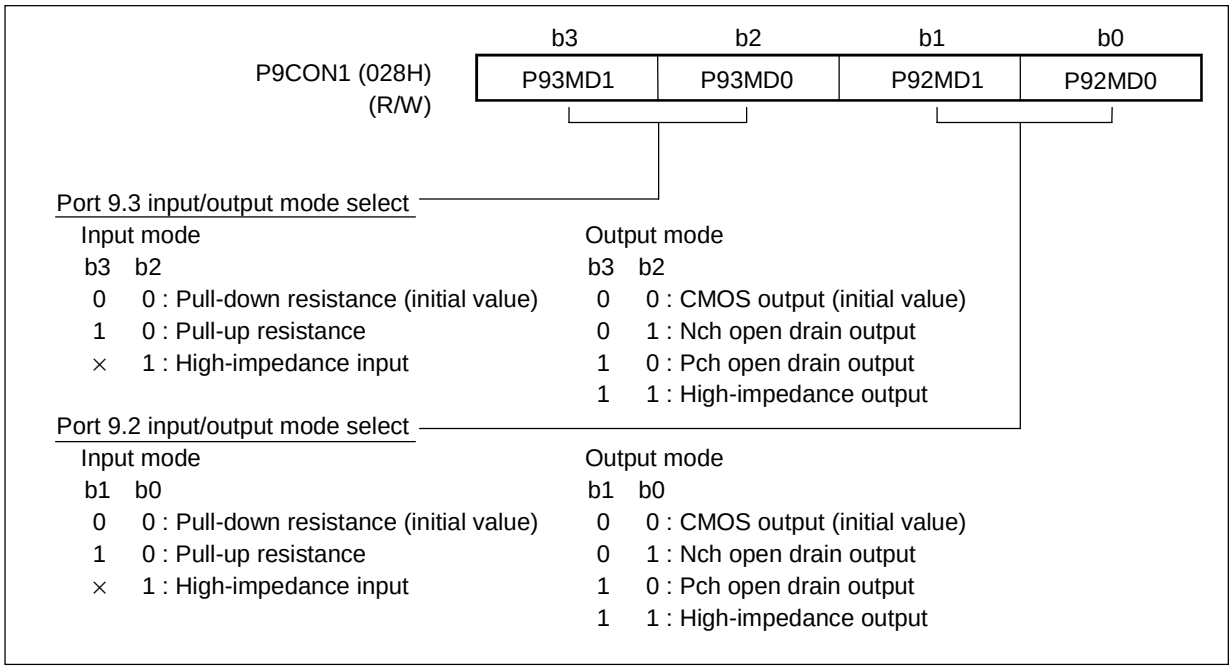
Port 8.3 input/output mode select

Input mode		Output mode	
b3	b2	b3	b2
0	0: Pull-down resistance (initial value)	0	0: CMOS output (initial value)
1	0: Pull-up resistance	0	1: Nch open drain output
×	1: High-impedance input	1	0: Pch open drain output
		1	1: High-impedance output

Port 8.2 input/output mode select

Input mode		Output mode	
b1	b0	b1	b0
0	0: Pull-down resistance (initial value)	0	0: CMOS output (initial value)
1	0: Pull-up resistance	0	1: Nch open drain output
×	1: High-impedance input	1	0: Pch open drain output
		1	1: High-impedance output


b3 b2 b1 b0
P9CON0 (027H)
(R/W)
P91MD1 P91MD0 P90MD1 P90MD0
Port 9.1 input/output mode select
Input mode
b3 b2
0 0 : Pull-down resistance (initial value)
1 0 : Pull-up resistance
× 1 : High-impedance input
Output mode
b3 b2
0 0 : CMOS output (initial value)
0 1 : Nch open drain output
1 0 : Pch open drain output
1 1 : High-impedance output
Port 9.0 input/output mode select
Input mode
b1 b0
0 0 : Pull-down resistance (initial value)
1 0 : Pull-up resistance
× 1 : High-impedance input
Output mode
b1 b0
0 0 : CMOS output (initial value)
0 1 : Nch open drain output
1 0 : Pch open drain output
1 1 : High-impedance output


b3 b2 b1 b0
P9CON1 (028H)
(R/W)
P93MD1 P93MD0 P92MD1 P92MD0
Port 9.3 input/output mode select
Input mode
b3 b2
0 0 : Pull-down resistance (initial value)
1 0 : Pull-up resistance
× 1 : High-impedance input
Output mode
b3 b2
0 0 : CMOS output (initial value)
0 1 : Nch open drain output
1 0 : Pch open drain output
1 1 : High-impedance output
Port 9.2 input/output mode select
Input mode
b1 b0
0 0 : Pull-down resistance (initial value)
1 0 : Pull-up resistance
× 1 : High-impedance input
Output mode
b1 b0
0 0 : CMOS output (initial value)
0 1 : Nch open drain output
1 0 : Pch open drain output
1 1 : High-impedance output

PACON0 (02AH) (R/W)

b3	b2	b1	b0
PA1MD1	PA1MD0	PA0MD1	PA0MD0

Port A.1 input/output mode select

Input mode

b3	b2	
0	0	: Pull-down resistance (initial value)
1	0	: Pull-up resistance
×	1	: High-impedance input

Output mode

b3	b2	
0	0	: CMOS output (initial value)
0	1	: Nch open drain output
1	0	: Pch open drain output
1	1	: High-impedance output

Port A.0 input/output mode select

Input mode

b1	b0	
0	0	: Pull-down resistance (initial value)
1	0	: Pull-up resistance
×	1	: High-impedance input

Output mode

b1	b0	
0	0	: CMOS output (initial value)
0	1	: Nch open drain output
1	0	: Pch open drain output
1	1	: High-impedance output

PACON1 (02BH) (R/W)

b3	b2	b1	b0
PA3MD1	PA3MD0	PA2MD1	PA2MD0

Port A.3 input/output mode select

Input mode

b3	b2	
0	0	: Pull-down resistance (initial value)
1	0	: Pull-up resistance
×	1	: High-impedance input

Output mode

b3	b2	
0	0	: CMOS output (initial value)
0	1	: Nch open drain output
1	0	: Pch open drain output
1	1	: High-impedance output

Port A.2 input/output mode select

Input mode

b1	b0	
0	0	: Pull-down resistance (initial value)
1	0	: Pull-up resistance
×	1	: High-impedance input

Output mode

b1	b0	
0	0	: CMOS output (initial value)
0	1	: Nch open drain output
1	0	: Pch open drain output
1	1	: High-impedance output

(4) Port 8–A mode registers (P8MOD, P9AMOD)

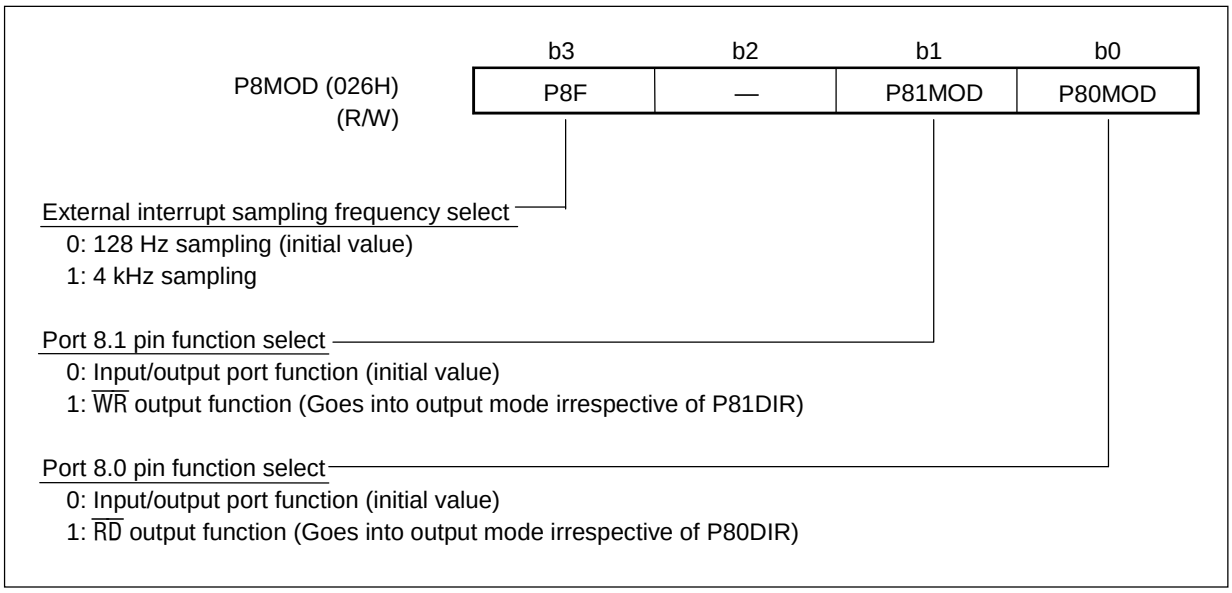
The port 8 mode register (P8MOD) and port 9A mode register (P9AMOD) are 4-bit special function registers (SFRs) used to select the sampling frequency when P8.3 is used for external interrupt and the secondary function of each port.

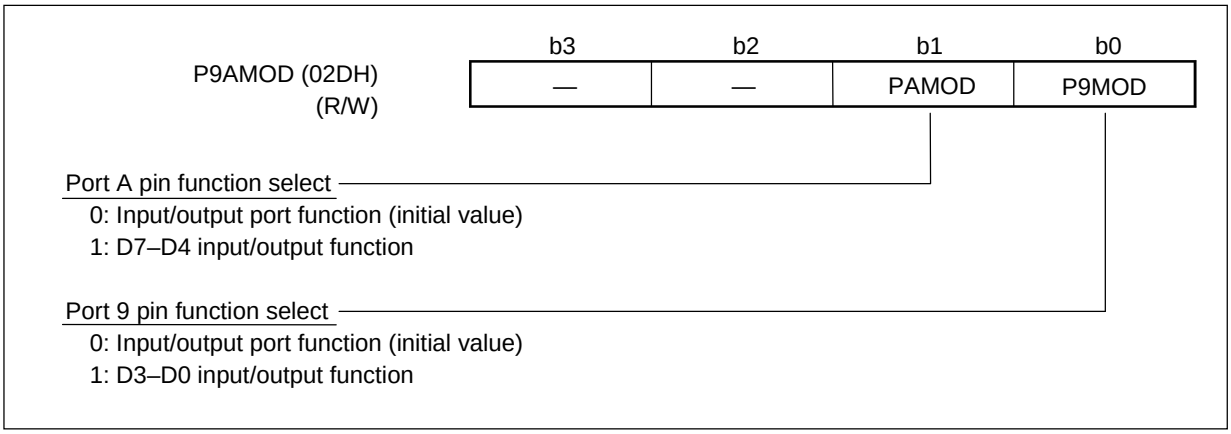
The port secondary functions are indicated in Table 12-2.

Table 12-2 Secondary Port Functions

Port	Secondary function	Content
P8.0	$\overline{RD}$	External memory read signal
P8.1	$\overline{WR}$	External memory write signal
P8.2	—	
P8.3	INIT4	External 4 interrupt
P9.0	D0	External memory data bus
P9.1	D1	
P9.2	D2	
P9.3	D3	
PA.0	D4	
PA.1	D5	
PA.2	D6	
PA.3	D7	

At system reset P8MOD and P9AMOD are reset to "0", and ports are used as normal ports.





If each bit of P9AMOD is set to "1" and the MOVXB instruction is executed, P9 through PA perform data signaling for external memory.

Input or output is based on the contents of the MOVXB instruction. If the MOVXB instruction is not executed, P9 through PA perform the normal input/output port function.

12.6.3 External interrupt function of port 8.3 (External 4 interrupt)

Port 8.3 is allocated an external 4 interrupt as its secondary function.

Port 8.3 external interrupt generation is triggered at the falling edge of the 128 Hz or 4 kHz time base counter, which is the sampling clock.

After the port level changes, the interrupt request signal XI4INT is output, and the interrupt request flag QXI4 is set. The maximum delay for this sequence is one cycle of the sampling clock (128 Hz or 4 kHz).

The interrupt vector address for the external 4 interrupt is 001CH.

Figure 12-10 shows the equivalent circuit for external 4 interrupt control.

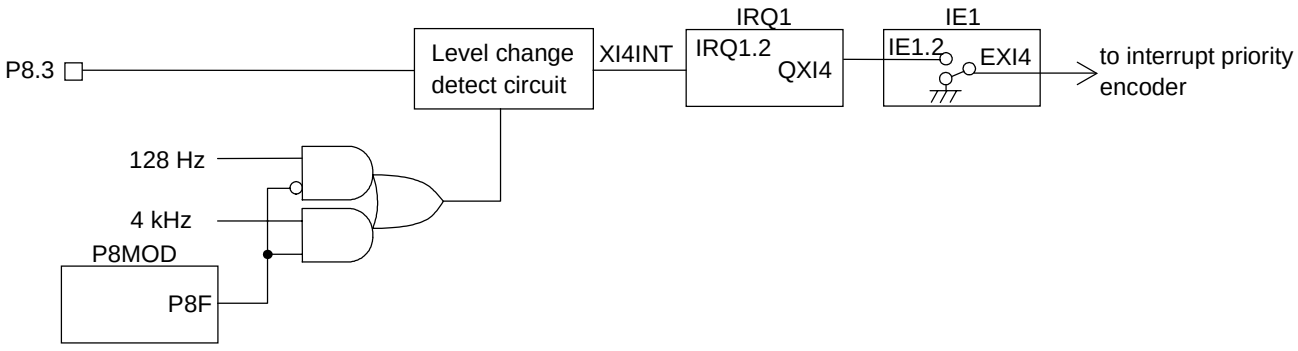


Figure 12-10 External 4 Interrupt Control Equivalent Circuit

Figure 12-11 shows the external 4 interrupt generation timing.

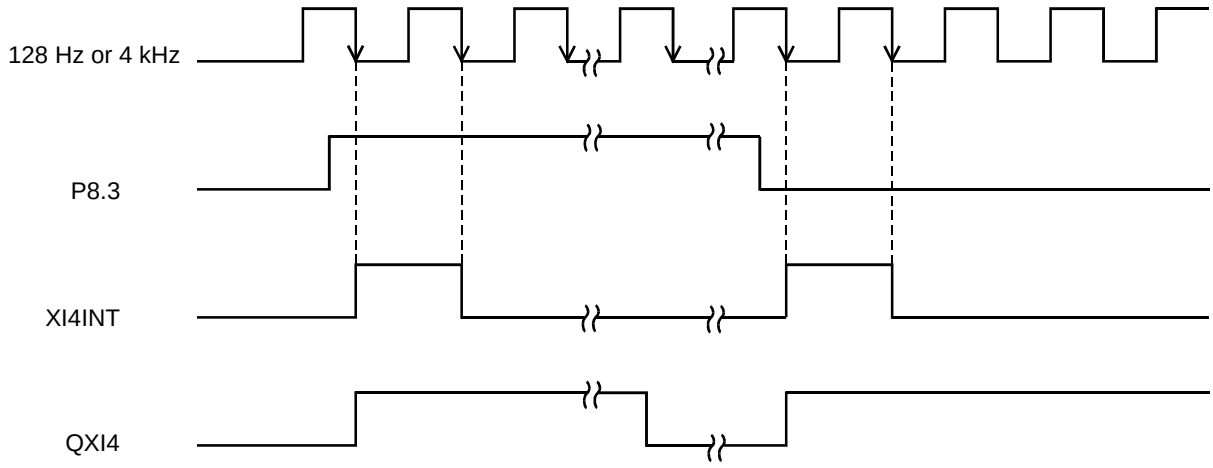


Figure 12-11 External 4 Interrupt Generation Timing

12.7 Port B (PB.0–PB.3)

12.7.1 Port B configuration

The MSM63188A has Port B, a 4-bit input/output port.

The circuit configuration for port B is shown in Figure 12-12.

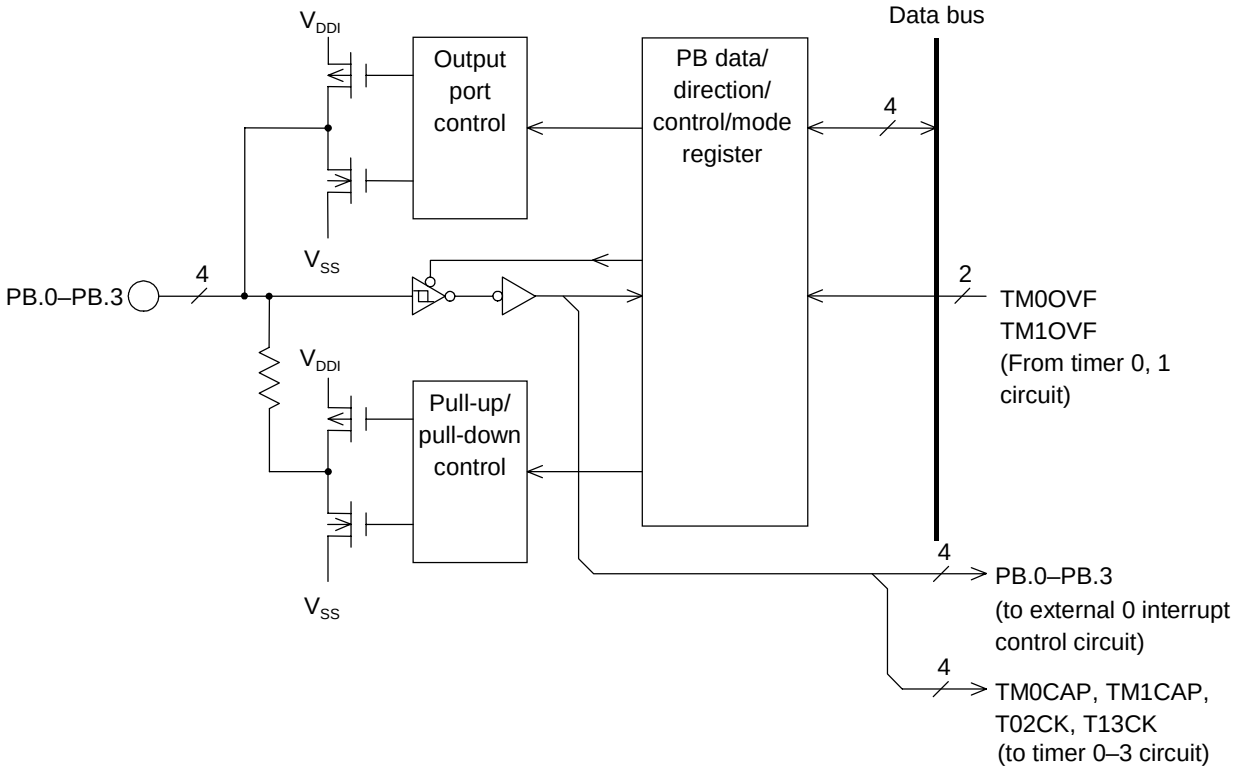


Figure 12-12 Port B Configuration

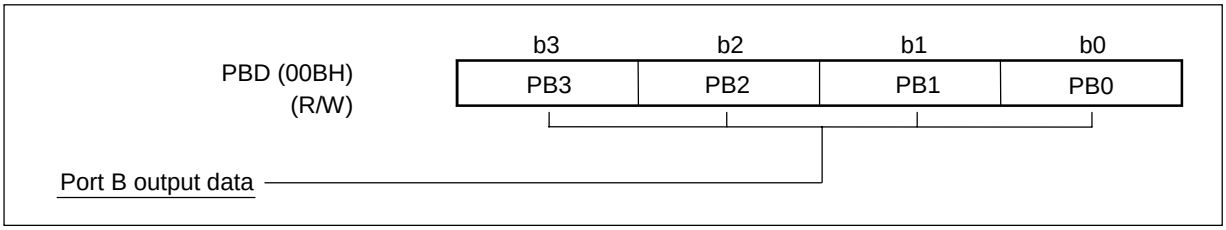
12.7.2 Port B registers

(1) Port B data register (PBD)

PBD is a 4-bit special function register used to set the output values for port B.

When the port B direction register (PBDIR) is set to "1" and the output mode is selected, the content of PBD is output to port B.

If the PBDIR bits are reset to "0" and the input mode is selected and PBD is read, the port B pin level is read.



At system reset PBD is reset to "0". When data is written to PBD, the actual pin change timing is at the rising edge of the system clock for state 2 (S2) of the write instruction.

Figure 12-13 indicates port change timing.

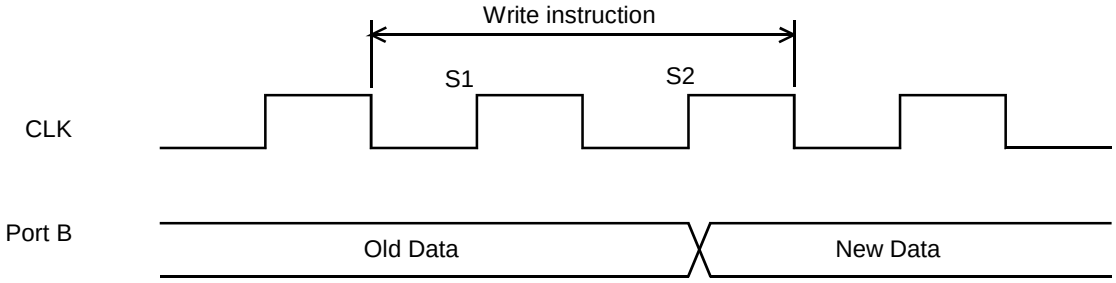
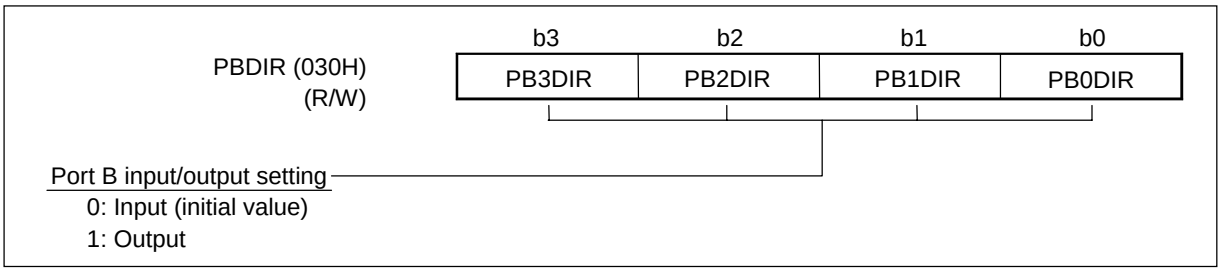


Figure 12-13 Port B Change Timing

(2) Port B direction register (PBDIR)

PBDIR is a 4-bit special function register (SFR) which specifies the port input/output direction in bit units. Pins corresponding to port direction register bits "0" are input, and those corresponding to bits set to "1" are output.

At system reset PBDIR is reset to "0", and port B is initialized to input mode.



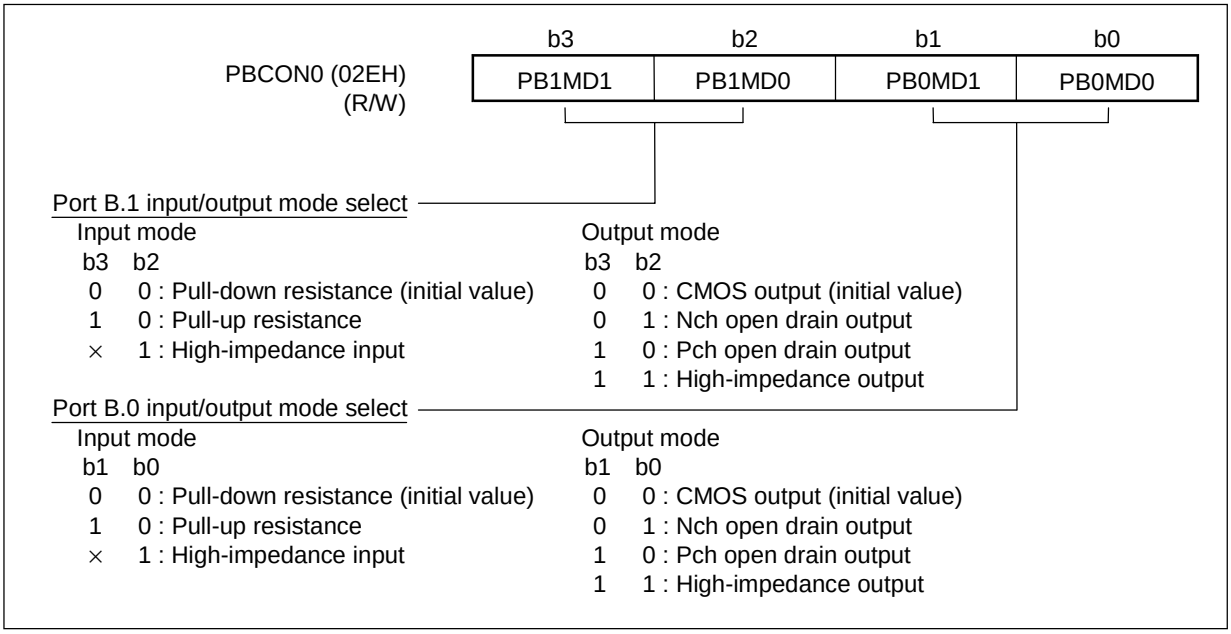
(3) Port B control registers 0/1 (PBCON0, PBCON1)

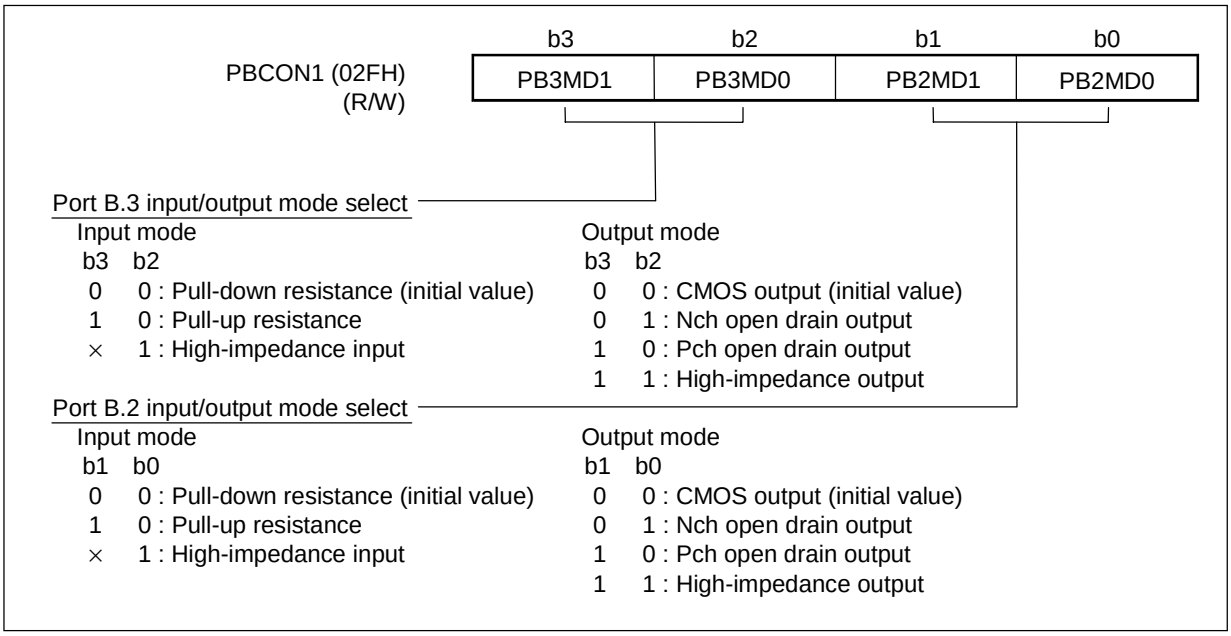
PBCON0 and PBCON1 are 4-bit special function registers (SFRs) used to select port input/output mode.

The input mode can be pull-down resistance input, pull-up resistance input or high-impedance input.

The output mode can be CMOS output, Nch open drain output, Pch open drain output or high-impedance output.

At system reset PBCON0 and PBCON1 are reset to "0", and port B is initialized to pull-down resistance input mode and CMOS output mode.





(4) Port B mode register (PBMOD)

PBMOD is a 4-bit special function register (SFR) used to select the sampling frequency when port B is used for external interrupt, and to select secondary functions other than external interrupt.

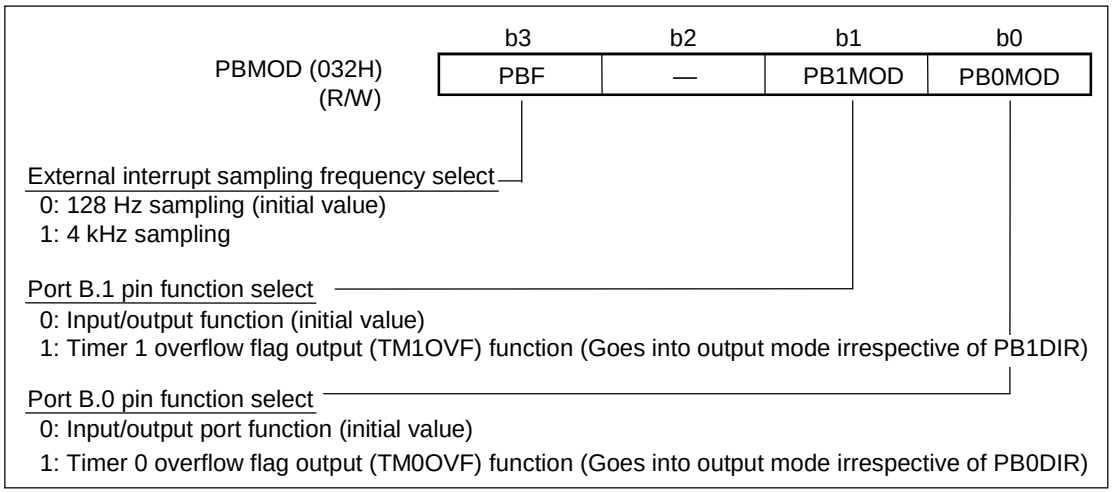
The external interrupt sampling frequency is either 128 Hz or 4 kHz.

At system reset PBMOD is reset to "0".

Port secondary functions are indicated in Table 12-3.

Table 12-3 Secondary Port Functions

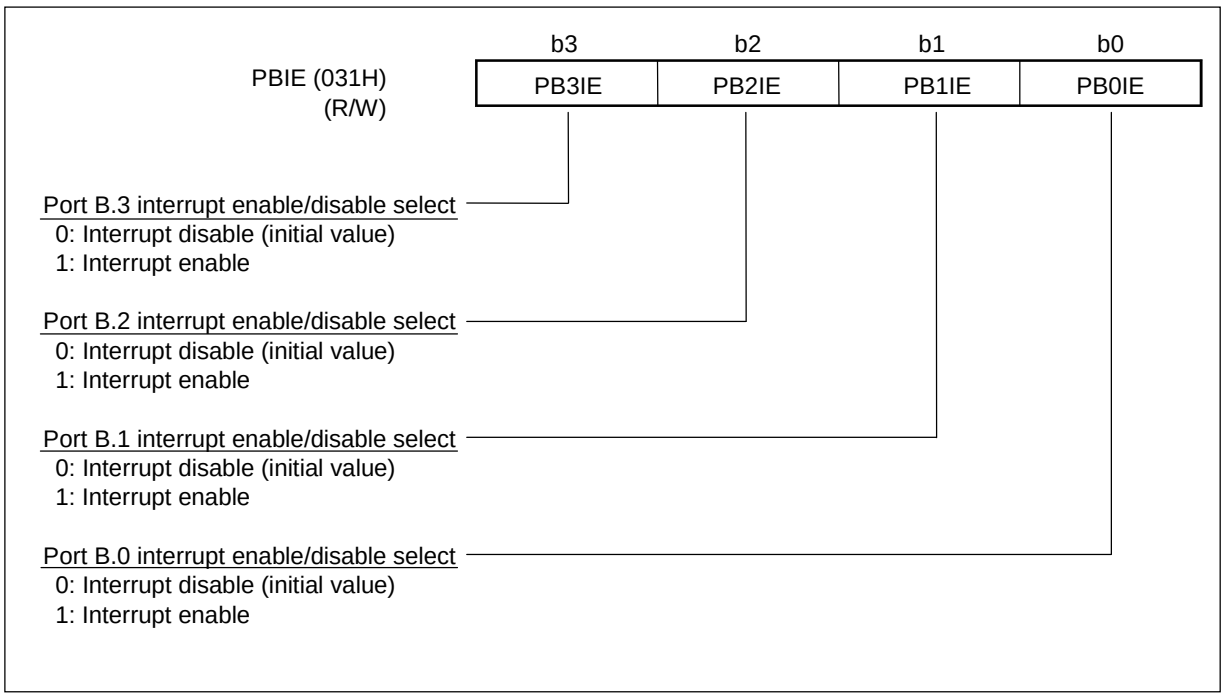
Port	Secondary function	Content
PB.0	TM0CAP	Timer 0 capture input
PB.1	TM1CAP	Timer 1 capture input
PB.2	T02CK	Timer 0, Timer 2 external clock input
PB.3	T13CK	Timer 1, Timer 3 external clock input
PB.0	TM0OVF	Timer 0 overflow flag output
PB.1	TM1OVF	Timer 1 overflow flag output
PB.0	INT0	External 0 interrupt
PB.1		
PB.2		
PB.3		



(5) Port B interrupt enable register (PBIE)

PBIE is a 4-bit special function register (SFR) used to enable/disable individual bits when port B is used for external interrupt input.

At system reset PBIE is reset to "0", and port B is initialized to the interrupt disable state.



12.7.3 External interrupt function of port B (External 0 interrupt)

The port B has external 0 interrupt allocated as secondary function. Individual bits of port B can be enabled/disabled.

External interrupt generation for port B is triggered by the falling edge of the 128 Hz or 4 kHz time base counter, which is the sampling clock.

After the port level changes, the interrupt request signal (XI0INT) is output, and the interrupt request flag (QXI0) is set. The maximum delay for this sequence is one cycle of the sampling clock (128 Hz or 4 kHz).

External interrupts for port B are set when a level change at any of port B inputs occurs, so each bit of the port must be read to determine which bit of the port has generated the interrupt.

The interrupt start address for external 0 interrupt is 0014H.

Figure 12-14 shows the equivalent circuit for external 0 interrupt control.

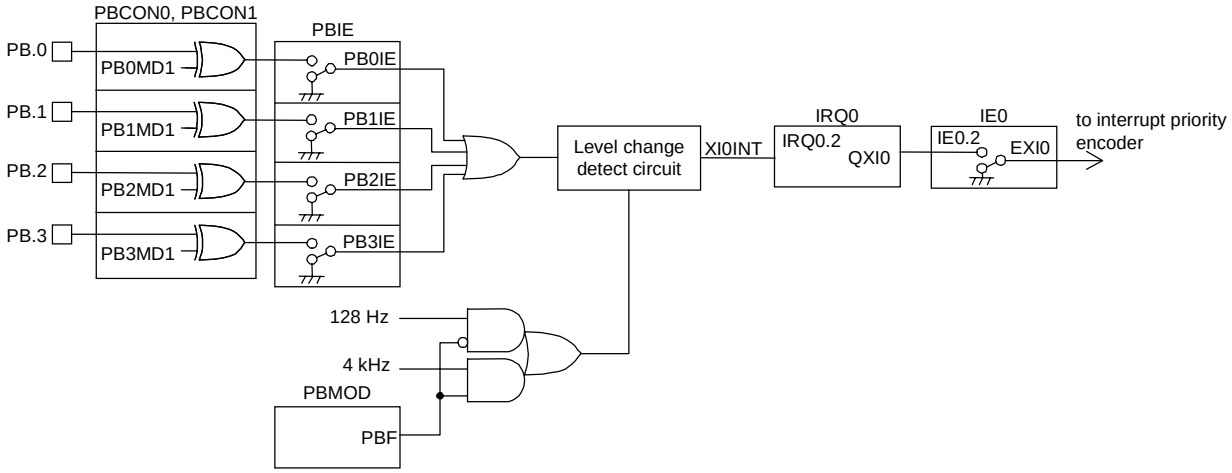


Figure 12-14 External 0 Interrupt Control Equivalent Circuit

Figure 12-15 shows the external 0 interrupt generation timing.

(a) PB0MD1 to PB3MD1 = "0" (initial value: inputs with pull-down resistors or high impedance input) setting

- When all PB.0 to PB.3 inputs are at a "L" level
  External 0 interrupt is generated when any port B input changes to a "H" level.
- When any of PB.0 to PB.3 inputs is at a "H" level
  External 0 interrupt is generated when all the port B inputs change to a "L" level.

(b) PB0MD1 and PB1MD1 = "0" and PB2MD1 and PB3MD1 = "1" (PB.0 and PB.1 selected as inputs with pull-down resistors or high impedance input; PB.2 and PB.3 selected as inputs with pull-up resistors or high impedance input) setting

- When both PB.0 and PB.1 inputs are at a "L" level AND both PB.2 and PB.3 inputs are at a "H" level
  External 0 interrupt is generated when either PB.0 or PB.1 input changes to a "H" level (alternatively, when either PB.2 or PB.3 input changes to a "L" level).
- When either PB.0 or PB.1 input is at a "H" level OR either PB.2 or PB.3 input is at a "L" level
  External 0 interrupt is generated when both PB.0 and PB.1 inputs change to a "L" level AND both PB.2 and PB.3 inputs change to a "H" level.

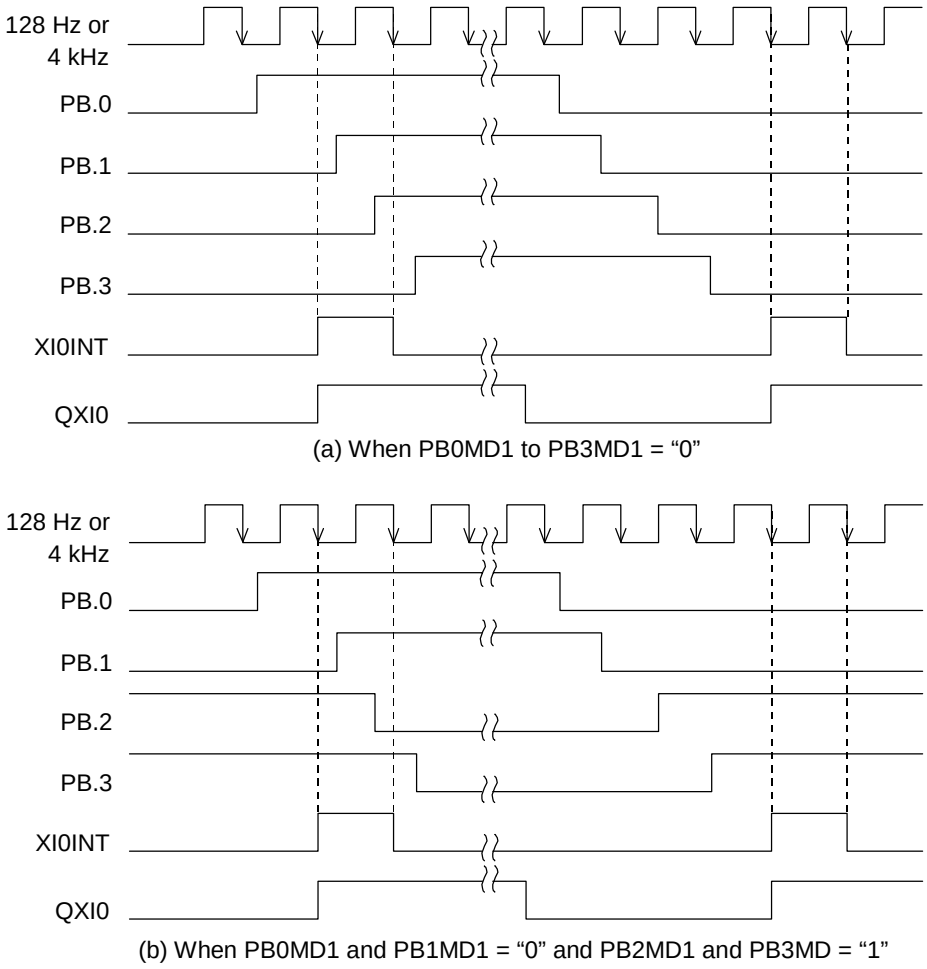


Figure 12-15 Interrupt Generation Timing of External 0 Interrupt

12.8 Port C (PC.0–PC.3)

12.8.1 Port C configuration

The MSM63188A has Port C, a 4-bit input/output port.

The circuit configuration for port C is shown in Figure 12-16.

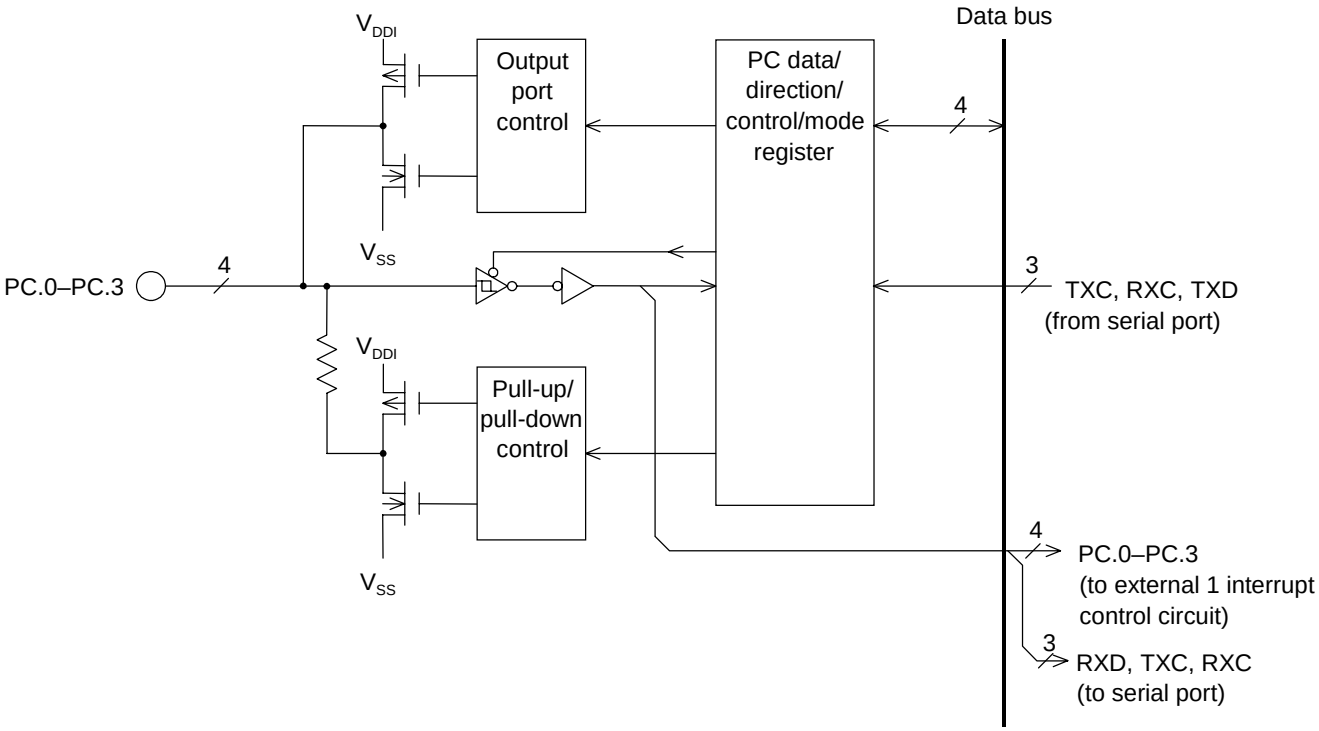


Figure 12-16 Port C Configuration

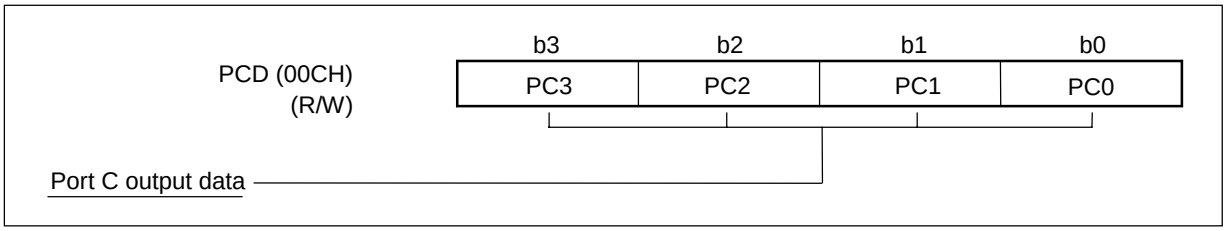
12.8.2 Port C registers

(1) Port C data register (PCD)

PCD is a 4-bit special function register used to set the output values for port C.

When the port C direction register (PCDIR) is set to "1" and the output mode is selected, the content of PCD is output to port C.

If the PCDIR bits are reset to "0" and the input mode is selected and PCD is read, the port C pin level is read.



At system reset PCD is reset to "0". When data is written to PCD, the actual pin change timing is at the rising edge of the system clock for state 2 (S2) of the write instruction.

Figure 12-17 indicates port change timing.

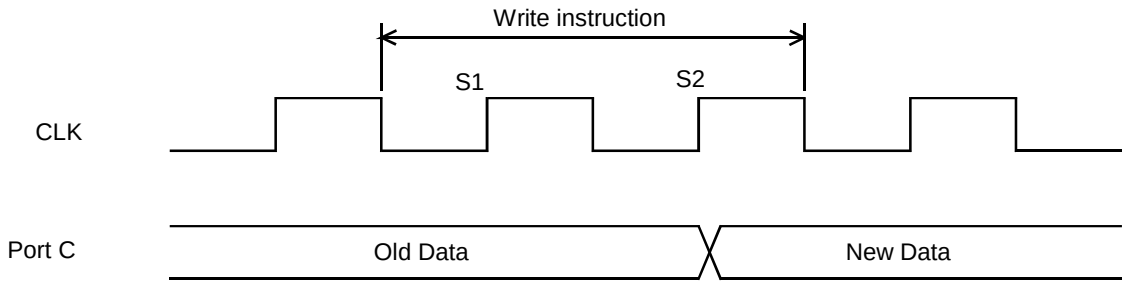
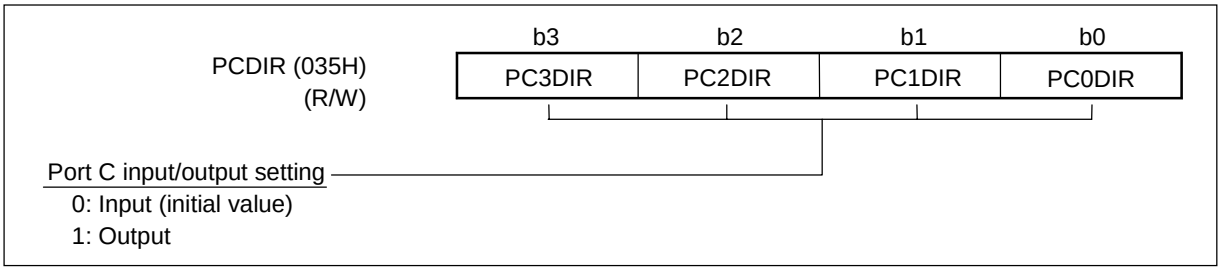


Figure 12-17 Port C Change Timing

(2) Port C direction register (PCDIR)

PCDIR is a 4-bit special function register (SFR) which specifies the port input/output direction in bit units. Pins corresponding to port direction register bits 0 are input, and those corresponding to bits set to "1" are output.

At system reset PCDIR is reset to "0", and port C is initialized to input mode.



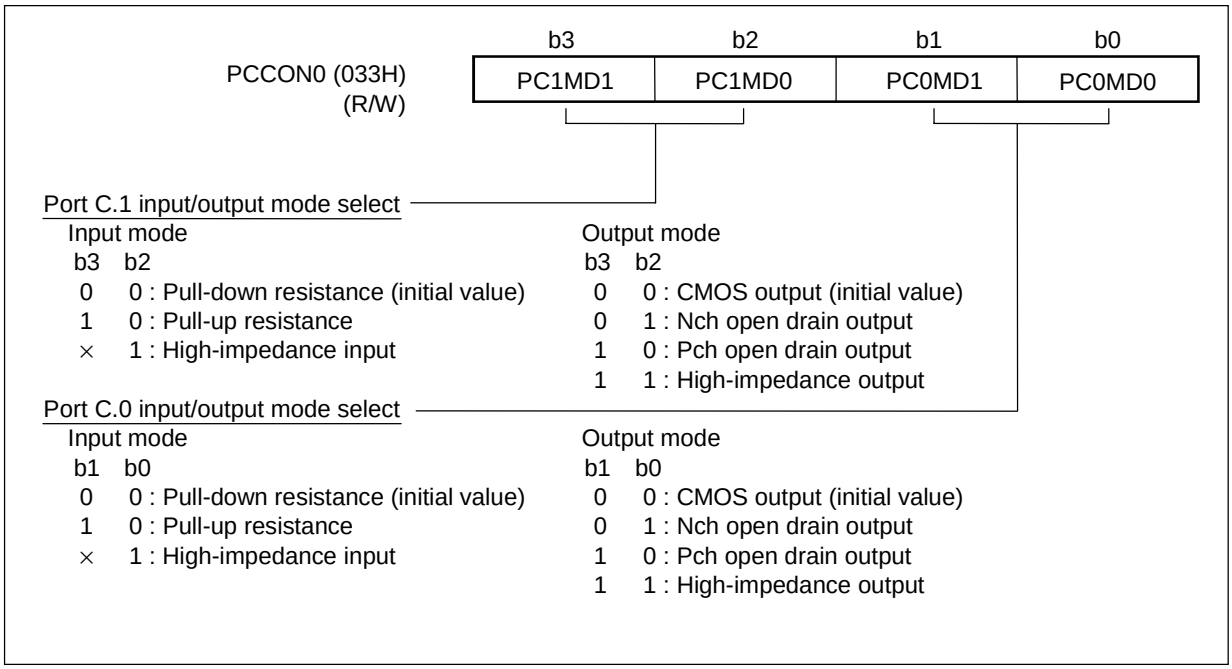
(3) Port C control registers 0/1 (PCCON0, PCCON1)

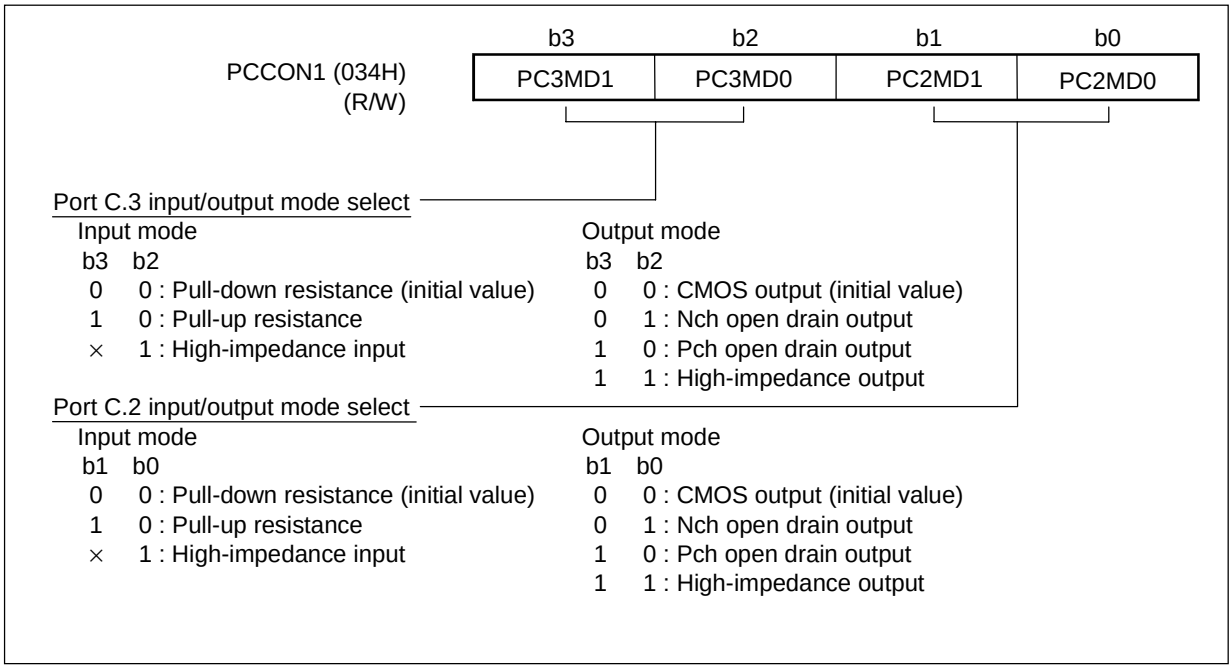
PCCON0 and PCCON1 are 4-bit special function registers (SFRs) used to select port input/output mode.

The input mode can be pull-down resistance input, pull-up resistance input or high-impedance input.

The output mode can be CMOS output, Nch open drain output, Pch open drain output or high-impedance output.

At system reset PCCON0 and PCCON1 are reset to "0", and port C is initialized to pull-down resistance input mode and CMOS output mode.





(4) Port C mode registers 0/1 (PCMOD0, PCMOD1)

PCMOD0 and PCMOD1 are 4-bit special function registers (SFRs) used to select the sampling frequency when port C is used for external interrupt, and to select secondary functions other than external interrupt.

The external interrupt sampling frequency is either 128 Hz or 4 kHz.

At system reset PCMOD0 and PCMOD1 are reset to "0".

Port secondary functions are indicated in Table 12-4.

Table 12-4 Secondary Port Functions

Port	Secondary function	Content
PC.0	RXD	Serial port receive data input
PC.1	TXC	Serial port send clock I/O
PC.2	RXC	Serial port receive clock I/O
PC.3	TXD	Serial port send data output
PC.0	INT1	External 1 interrupt
PC.1		
PC.2		
PC.3		

PCMOD0 (037H) (R/W)

b3	b2	b1	b0
—	—	—	PCF

External interrupt sampling frequency select
0: 128 Hz sampling (initial value)
1: 4 kHz sampling

PCMOD1 (038H) (R/W)

b3	b2	b1	b0
PC3MOD	PC2MOD	PC1MOD	PC0MOD

Port C.3 pin function select
0: Input/output port function (initial value)
1: Serial port transmit data output (TXD) function (Goes into output mode irrespective of PC3DIR)

Port C.2 pin function select
0: Input/output port function (initial value)
1: Serial port receive clock input/output (RXC) function (Switching of input/output mode depends on SRCLK bit of serial port receive control register SRCON1. It is performed irrespective of PC2DIR)

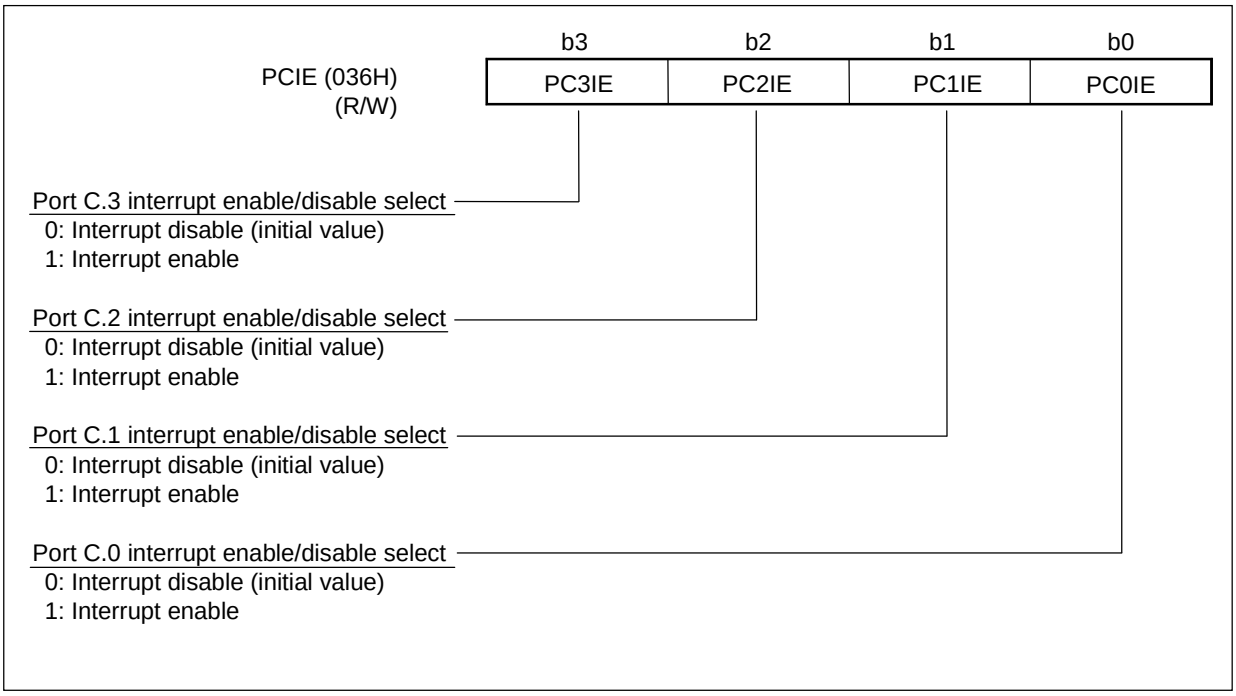
Port C.1 pin function select
0: Input/output port function (initial value)
1: Serial port transmit clock input/output (TXC) function (Switching of input/output mode depends on STCLK bit of serial port transmit control register STCON1. It is performed irrespective of PC1DIR)

Port C.0 pin function select
0: Input/output port function (initial value)
1: Serial port receive data input (RXD) function (Goes into input mode irrespective of PC0DIR)

(5) Port C interrupt enable register (PCIE)

PCIE is a 4-bit special function register (SFR) used to enable/disable individual bits when port C is used for external interrupt input.

At system reset the port C interrupt enable register is reset to "0", and port C is initialized to the interrupt disable state.



12.8.3 External interrupt function of port C (External 1 interrupt)

The port C has external 1 interrupt allocated as secondary function. Individual bits of port C can be enabled/disabled.

External interrupt generation for port C is triggered by the falling edge of the 128 Hz or 4 kHz time base counter, which is the sampling clock.

After the port level changes, the interrupt request signal (XI1INT) is output, and the interrupt request flag (QXI1) is set. The maximum delay for this sequence is one cycle of the sampling clock (128 Hz or 4 kHz).

External interrupts for port C are set when a level change at any of port C inputs occurs, so each bit of the port must be read to determine which bit of port C has generated the interrupt.

The interrupt start address for external 1 interrupt is 0016H.

Figure 12-18 shows the equivalent circuit for external 1 interrupt control.

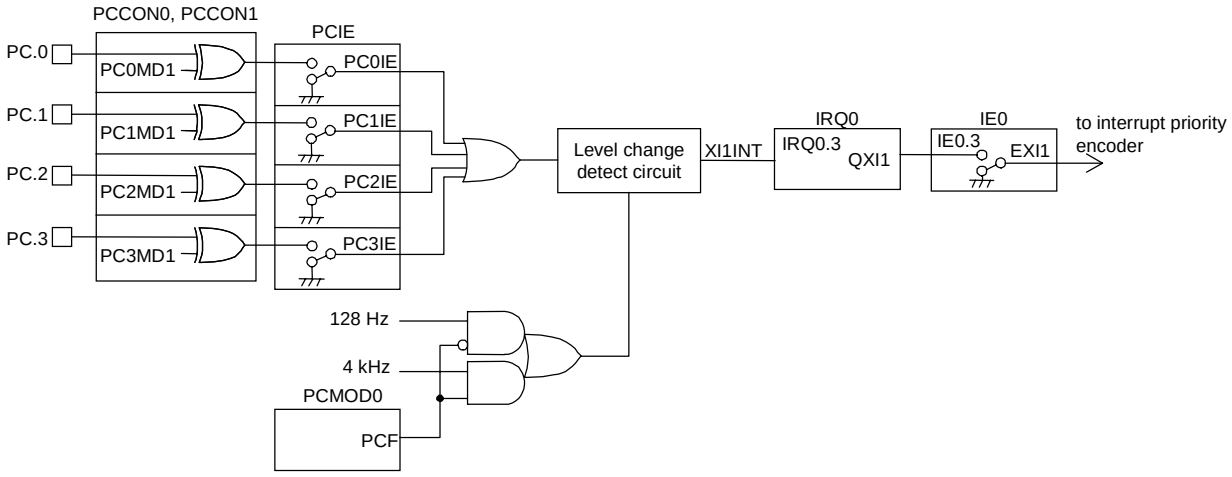


Figure 12-18 External 1 Interrupt Control Equivalent Circuit

Figure 12-19 shows the external 1 interrupt generation timing.

(a) PC0MD1 to PC3MD1 = "0" (initial value: inputs with pull-down resistors or high impedance input) setting

- When all PC.0 to PC.3 inputs are at a "L" level
  External 1 interrupt is generated when any port C input changes to a "H" level.

- When any of PC.0 to PC.3 inputs is at a "H" level
  External 1 interrupt is generated when all the port B inputs change to a "L" level.

(b) PC0MD1 and PC1MD1 = "0" and PC2MD1 and PC3MD1 = "1" (PC.0 and PC.1 selected as inputs with pull-down resistors or high impedance input; PC.2 and PC.3 selected as inputs with pull-up resistors or high impedance input) setting

- When both PC.0 and PC.1 inputs are at a "L" level AND both PC.2 and PC.3 inputs are at a "H" level
  External 1 interrupt is generated when either PC.0 or PC.1 input changes to a "H" level (alternatively, when either PC.2 or PC.3 input changes to a "L" level).

- When either PC.0 or PC.1 input is at a "H" level OR either PC.2 or PC.3 input is at a "L" level External 1 interrupt is generated when both PC.0 and PC.1 inputs change to a "L" level AND both PC.2 and PC.3 inputs change to a "H" level.

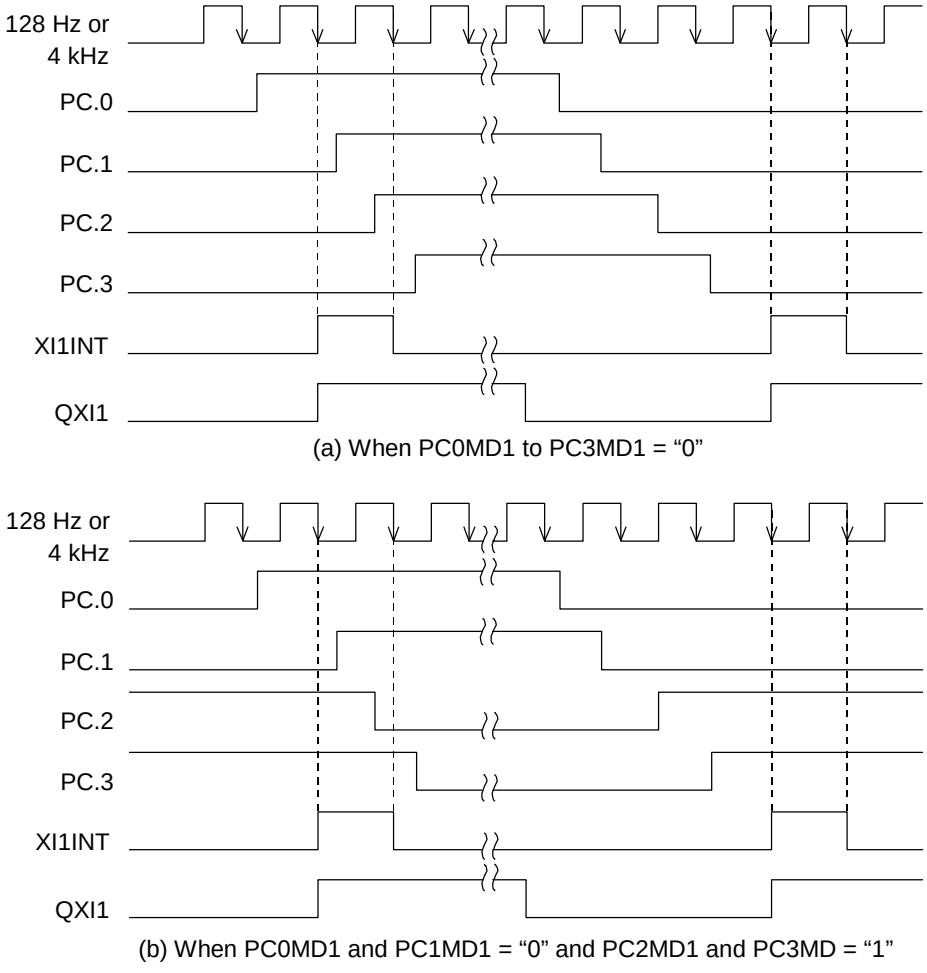


Figure 12-19 Interrupt Generation Timing of External 1 Interrupt

12.9 Port D (PD.0–PD.3)

12.9.1 Port D configuration

The MSM63184A and MSM63188A have Port D, a 4-bit input/output port.

The circuit configuration for port D is shown in Figure 12-20.

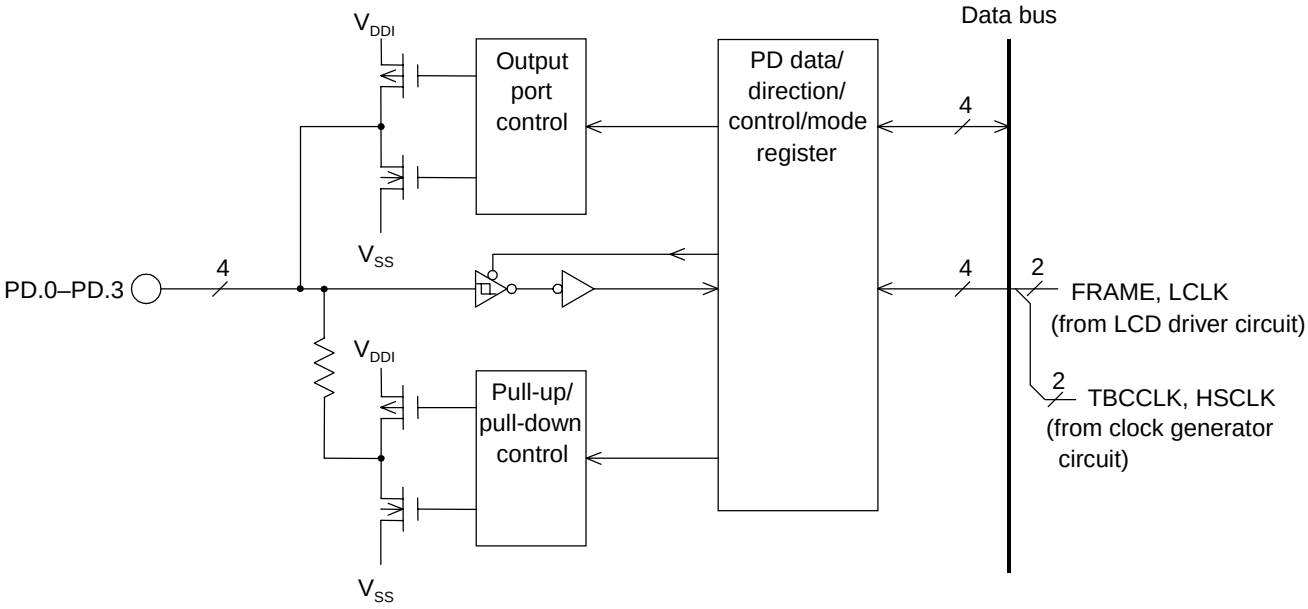


Figure 12-20 Port D Configuration

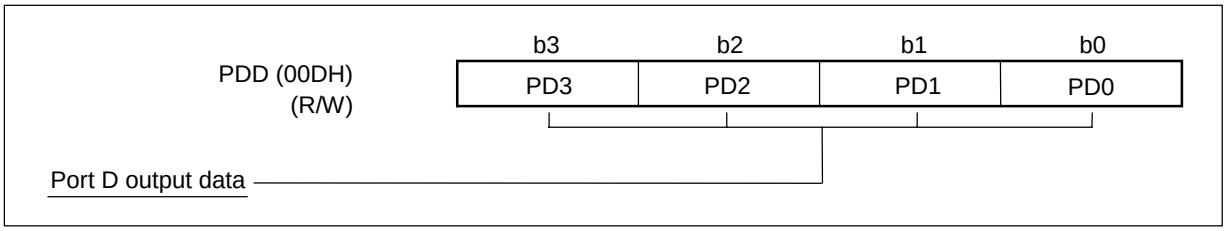
12.9.2 Port D registers

(1) Port D data register (PDD)

PDD is a 4-bit special function register used to set the output values for port D.

When the port D direction register (PDDIR) is set to 1 and the output mode is selected, the content of PDD is output to port D.

If the PDDIR bits are reset to 0 and the input mode is selected and PDD is read, the port D pin level is read.



At system reset PDD is reset to "0". When data is written to PDD, the actual pin change timing is at the rising edge of the system clock for state 2 (S2) of the write instruction.

Figure 12-21 indicates port change timing.

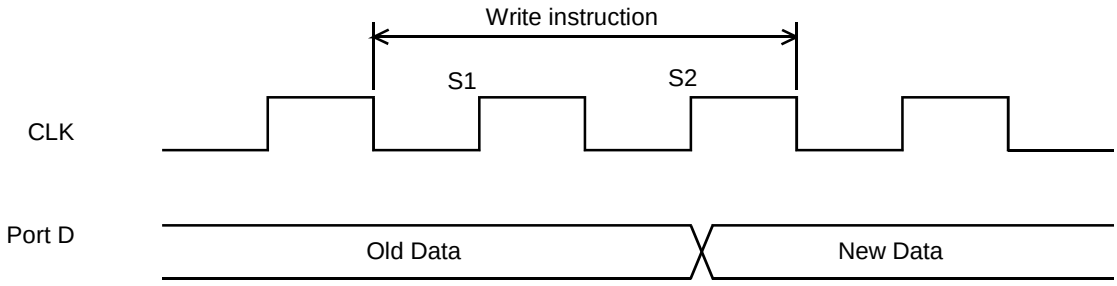
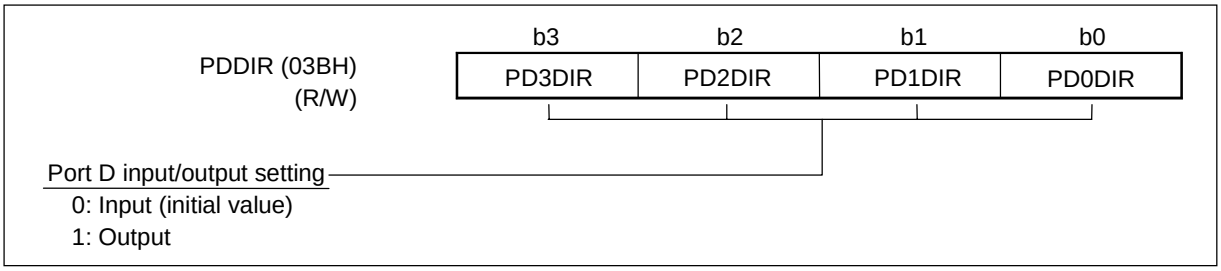


Figure 12-21 Port D Change Timing

(2) Port D direction register (PDDIR)

PDDIR is a 4-bit special function register (SFR) which specifies the port input/output direction in bit units. Pins corresponding to port direction register bits "0" are input, and those corresponding to bits set to "1" are output.

At system reset PDDIR is reset to 0, and port D is initialized to input mode.



(3) Port D control registers 0/1 (PDCON0, PDCON1)

PDCON0 and PDCON1 are 4-bit special function registers (SFRs) used to select port input/output mode.

The input mode can be pull-down resistance input, pull-up resistance input or high-impedance input.

The output mode can be CMOS output, Nch open drain output, Pch open drain output or high-impedance output.

At system reset PDCON0 and PDCON1 are reset to "0", and port D is initialized to pull-down resistance input mode and CMOS output mode.

PDCON0 (039H) (R/W)

b3	b2	b1	b0
PD1MD1	PD1MD0	PD0MD1	PD0MD0

Port D.1 input/output mode select

Input mode

b3	b2	
0	0	Pull-down resistance (initial value)
1	0	Pull-up resistance
×	1	High-impedance input

Output mode

b3	b2	
0	0	CMOS output (initial value)
0	1	Nch open drain output
1	0	Pch open drain output
1	1	High-impedance output

Port D.0 input/output mode select

Input mode

b1	b0	
0	0	Pull-down resistance (initial value)
1	0	Pull-up resistance
×	1	High-impedance input

Output mode

b1	b0	
0	0	CMOS output (initial value)
0	1	Nch open drain output
1	0	Pch open drain output
1	1	High-impedance output

PDCON1 (03AH) (R/W)

b3	b2	b1	b0
PD3MD1	PD3MD0	PD2MD1	PD2MD0

Port D.3 input/output mode select

Input mode

b3	b2	
0	0	Pull-down resistance (initial value)
1	0	Pull-up resistance
×	1	High-impedance input

Output mode

b3	b2	
0	0	CMOS output (initial value)
0	1	Nch open drain output
1	0	Pch open drain output
1	1	High-impedance output

Port D.2 input/output mode select

Input mode

b1	b0	
0	0	Pull-down resistance (initial value)
1	0	Pull-up resistance
×	1	High-impedance input

Output mode

b1	b0	
0	0	CMOS output (initial value)
0	1	Nch open drain output
1	0	Pch open drain output
1	1	High-impedance output

(4) Port D mode register (PDMOD)

PDMOD is a 4-bit special function register (SFR) used to select the sampling frequency when port D is used for external interrupt, and to select secondary functions other than external interrupt.

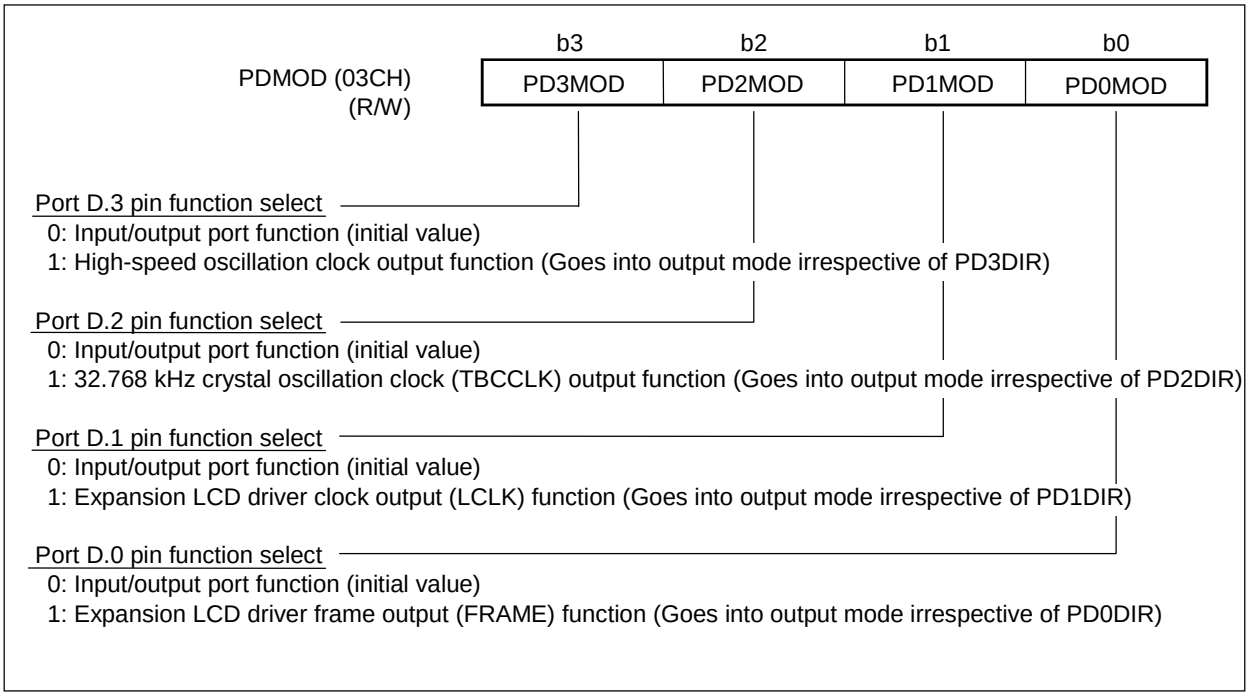
The external interrupt sampling frequency is either 128 Hz or 4 kHz.

At system reset PDMOD is reset to "0".

Port secondary functions are indicated in Table 12-5.

Table 12-5 Secondary Port Functions

Port	Secondary function	Content
PD.0	FRAME	Expansion LCD driver frame output
PD.1	LCLK	Expansion LCD driver clock output
PD.2	TBCCLK	32.768 kHz crystal oscillation clock output
PD.3	HSCLK	High-speed oscillation clock output



12.10 Port E (PE.0–PE.3)

12.10.1 Port E configuration

The MSM63184A has Port E, a 4-bit input/output port.

The circuit configuration for port E is shown in Figure 12-22.

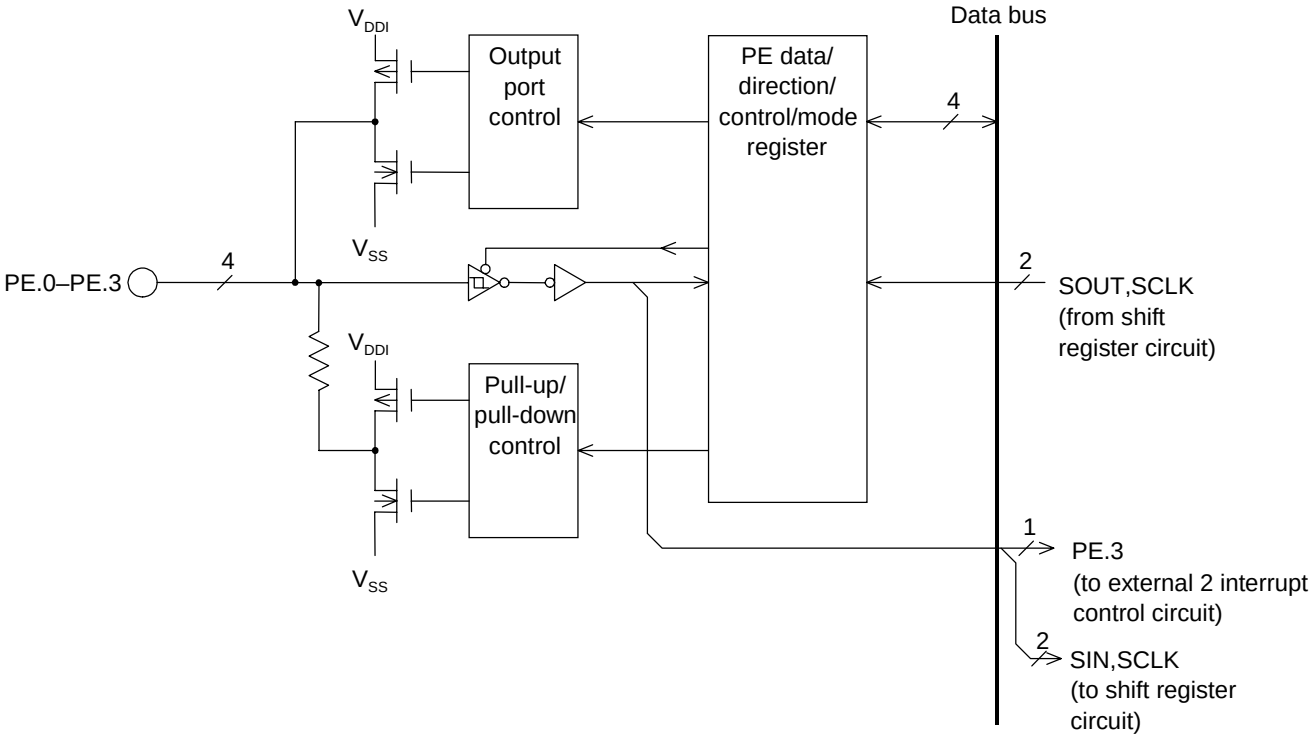


Figure 12-22 Port E Configuration

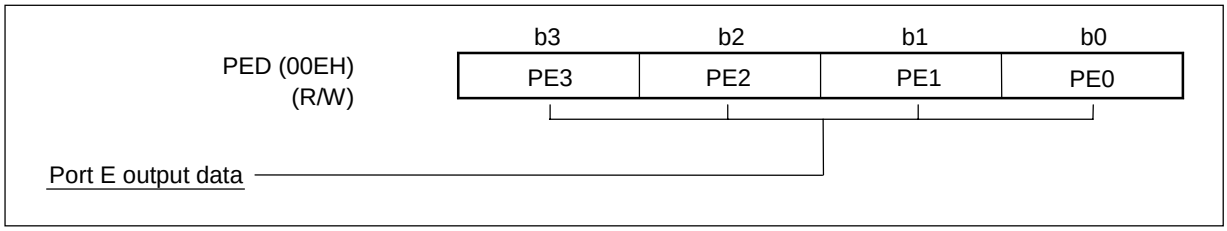
12.10.2 Port E registers

(1) Port E data register (PED)

PED is a 4-bit special function register used to set the output values for port E.

When the port E direction register (PEDIR) is set to "1" and the output mode is selected, the content of PED is output to port E.

If the PEDIR bits are reset to "0" and the input mode is selected and PED is read, the port E pin level is read.



At system reset PED is reset to "0". When data is written to PED, the actual pin change timing is at the rising edge of the system clock for state 2 (S2) of the write instruction.

Figure 12-23 indicates port change timing.

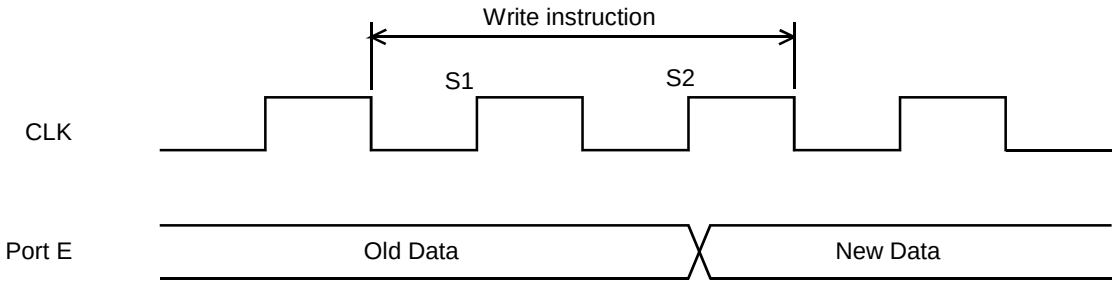
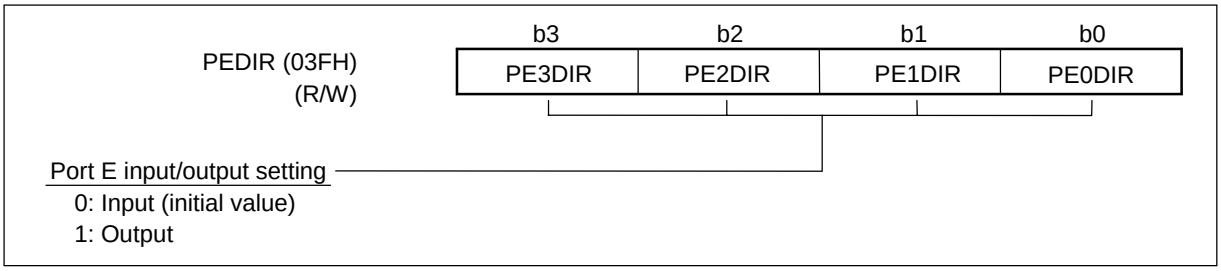


Figure 12-23 Port E Change Timing

(2) Port E direction register (PEDIR)

PEDIR is a 4-bit special function register (SFR) which specifies the port input/output direction in bit units. Pins corresponding to port direction register bits "0" are input, and those corresponding to bits set to "1" are output.

At system reset PEDIR is reset to "0", and port E is initialized to input mode.



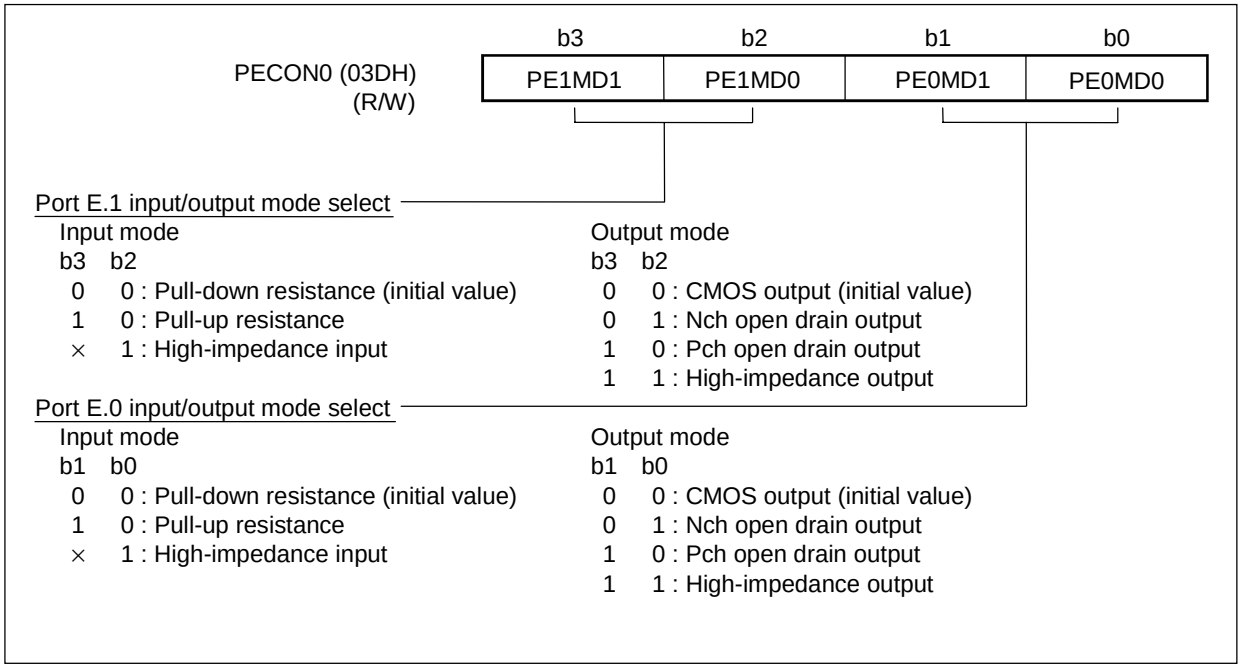
(3) Port E control registers 0/1 (PECON0, PECON1)

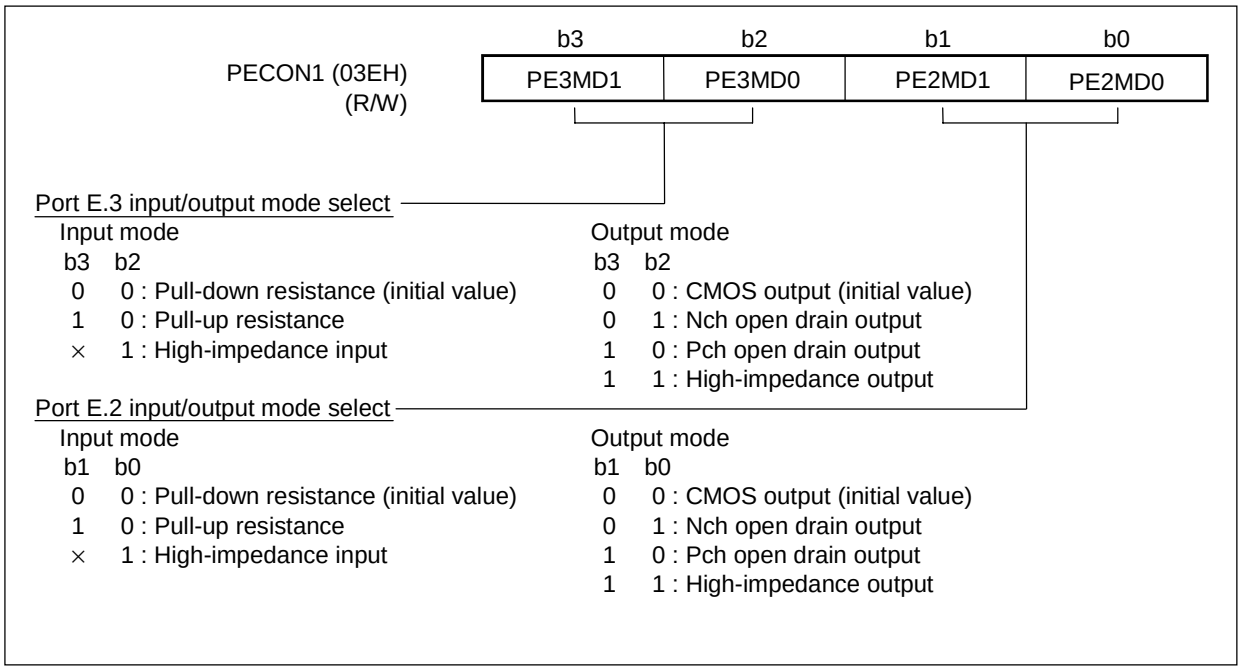
PECON0 and PECON1 are 4-bit special function registers (SFRs) used to select port input/output mode.

The input mode can be pull-down resistance input, pull-up resistance input or high-impedance input.

The output mode can be CMOS output, Nch open drain output, Pch open drain output or high-impedance output.

At system reset PECON0 and PECON1 are reset to "0", and port E is initialized to pull-down resistance input mode and CMOS output mode.





(4) Port E mode register (PEMOD)

PEMOD is a 4-bit special function register (SFR) used to select the sampling frequency when port E is used for external interrupt, and to select secondary functions other than external interrupt.

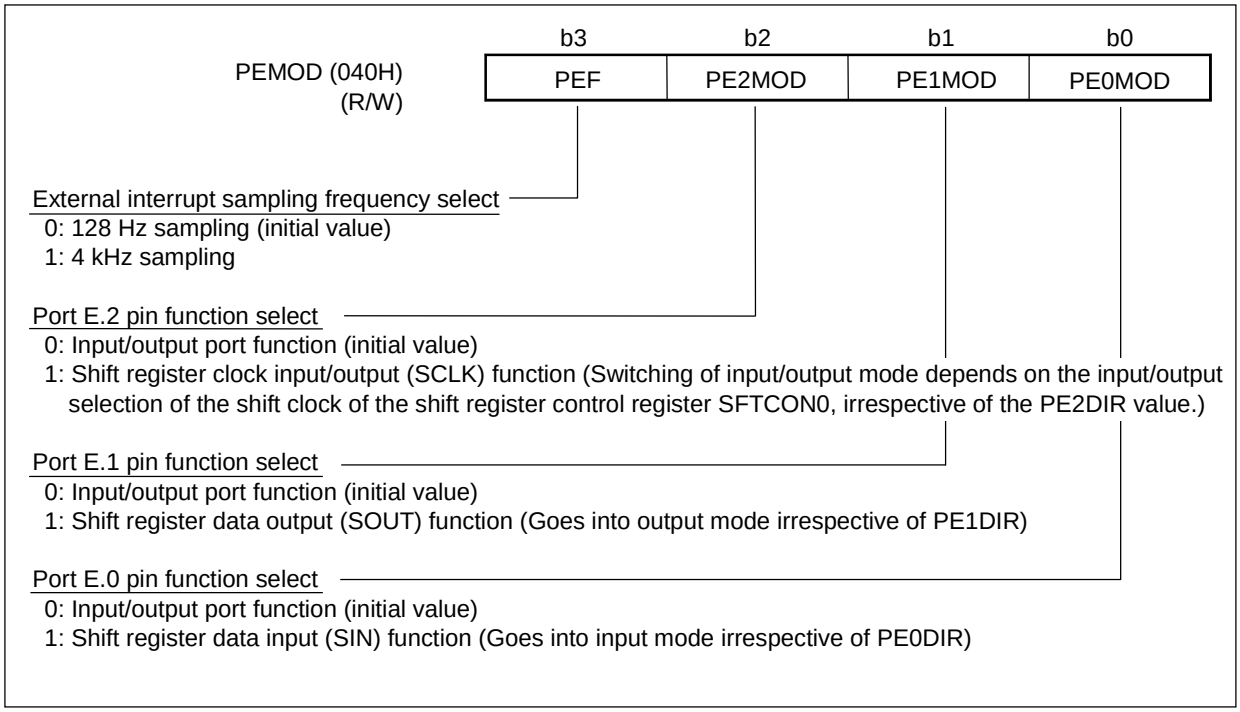
The external interrupt sampling frequency is either 128 Hz or 4 kHz.

At system reset PEMOD is reset to "0".

Port secondary functions are indicated in Table 12-6.

Table 12-6 Secondary Port Functions

Port	Secondary function	Content
PE.0	SIN	Shift register data input
PE.1	SOUT	Shift register data output
PE.2	SCLK	Shift register clock input/output
PE.3	INT2	External 2 interrupt



12.10.3 External interrupt function of port E.3 (External 2 interrupt)

Port E.3 has external 2 interrupt allocated as secondary function.

External interrupt generation for port E.3 is triggered by the falling edge of the 128 Hz or 4 kHz time base counter, which is the sampling clock.

After the port level changes, the interrupt request signal (XI2INT) is output, and the interrupt request flag (QXI2) is set. The maximum delay for this sequence is one cycle of the sampling clock (128 Hz or 4 kHz).

The interrupt start address for external 2 interrupt is 0018H.

Figure 12-24 shows the equivalent circuit for external 2 interrupt control

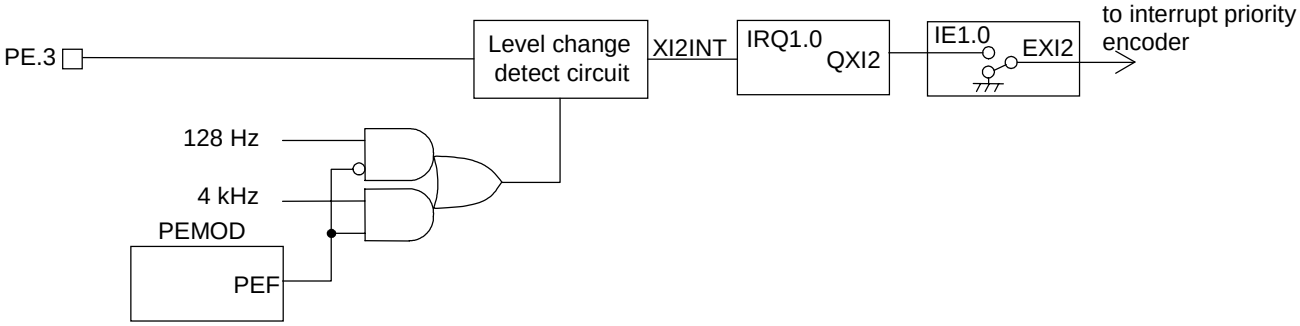


Figure 12-24 External 2 Interrupt Control Equivalent Circuit

Figure 12-25 shows the external 2 interrupt generation timing.

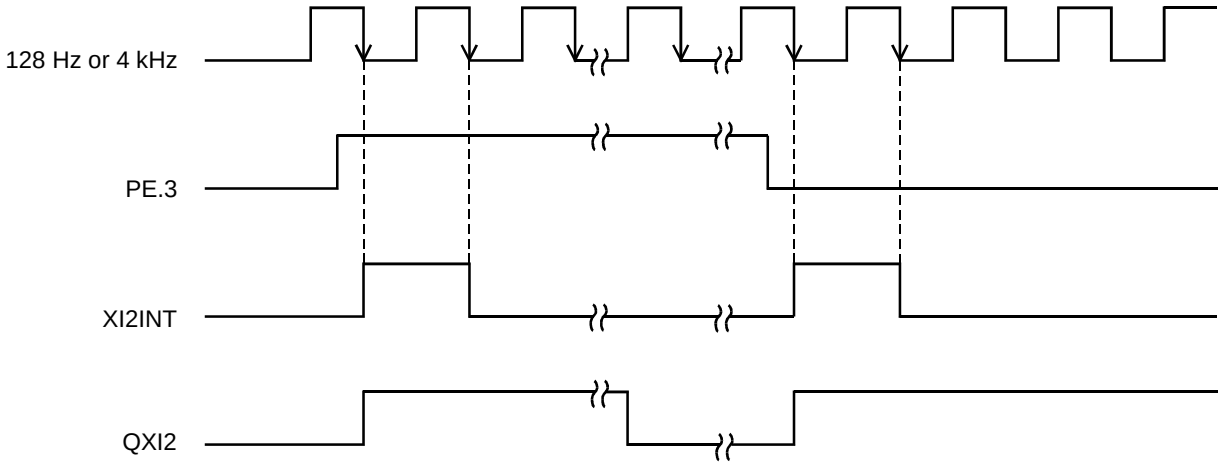


Figure 12-25 External 2 Interrupt Generation Timing

Chapter 13

External Memory Interface (EXTMEM)

Chapter 13 External Memory Interface (EXTMEM)

13.1 Overview

The MSM63180 family products use port secondary functions to facilitate the interface with external memory. The external memory transfer instructions are used to transfer data efficiently.

Table 13-1 indicates the port secondary functions for the external memory interface.

Figure 13-1 shows the connection diagram for external memory.

Refer to Chapter 12 for information on port secondary function settings.

Table 13-1 Port Secondary Functions

Pin name	I/O	Function
P4.0/A0	O	P4, P5, P6, P7 secondary functions: Address bus signals for external memory access
P4.1/A1		
P4.2/A2		
P4.3/A3		
P5.0/A4		
P5.1/A5		
P5.2/A6		
P5.3/A7		
P6.0/A8		
P6.1/A9		
P6.2/A10		
P6.3/A11		
P7.0/A12		
P7.1/A13		
P7.2/A14		
P7.3/A15		
P9.0/D0	I/O	P9, PA secondary functions: Data bus signals for external memory access
P9.1/D1		
P9.2/D2		
P9.3/D3		
PA.0/D4		
PA.1/D5		
PA.2/D6		
PA.3/D7		
P8.0/$\overline{RD}$	O	P8.0 secondary functions: read signal (negative logic) for external memory access
P8.1/$\overline{WR}$	O	P8.1 secondary functions: write signal (negative logic) for external memory access

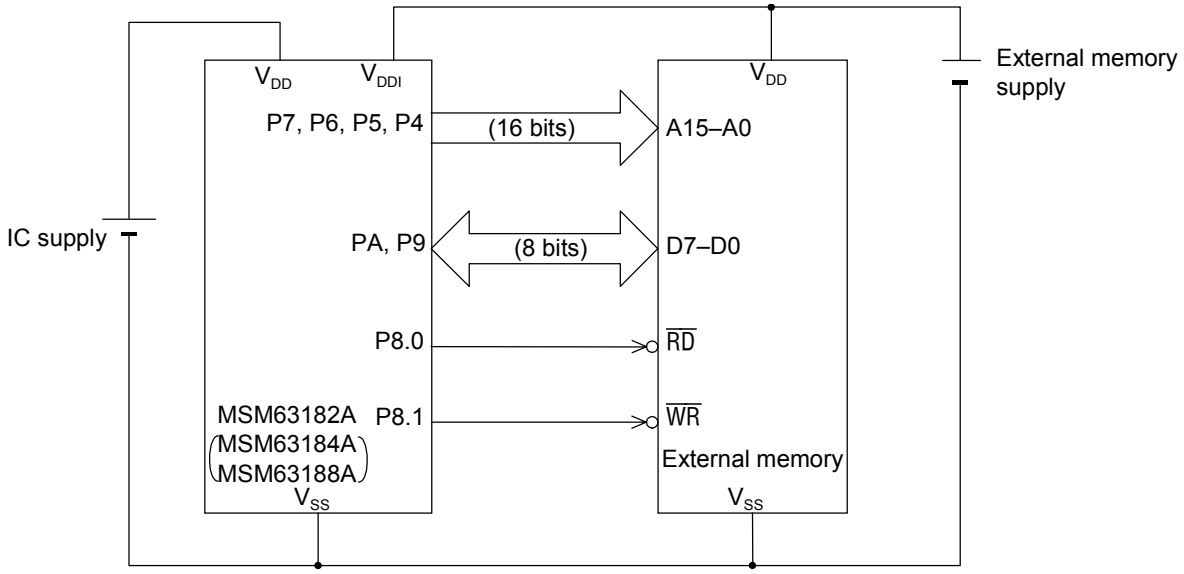


Figure 13-1 Connection to External Memory

13.2 External Memory Address Space

A maximum of 16 address lines can be selected as port secondary functions, allowing access to 64 Kbytes of external memory.

Chip select (CS) can be used for ports other than those set for secondary functions to expand the external memory space above 64 Kbytes. For example (Figure 13-2), if port 3 (P3.3–P3.0) is used for chip select, the external memory space will be

64 Kbytes × 4 = 256 Kbytes.

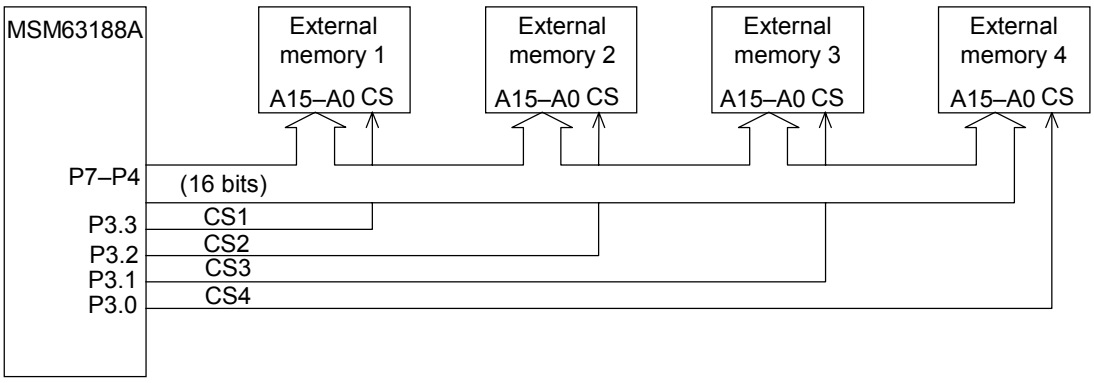


Figure 13-2 Example of Memory Expansion with Chip Select (CS)

13.3 Setting Port Secondary Functions

Port secondary functions are set to access external memory. Refer to Chapter 11 for information on the required registers.

Unless an external memory transfer instruction is executed, P7–P4, PA and P9 will be as specified in the port control register (that is, normal output and I/O port).

When P8.0 and P8.1 are set for secondary functions they are immediately allocated to read signal ($\overline{RD}$) and write signal ($\overline{WR}$).

13.4 Write to External Memory

The following external memory transfer instructions are executed to write to external memory.

MOVXB [RA], obj
or
MOVXB xadr16, obj

Figure 13-3 shows the timing for external memory write.

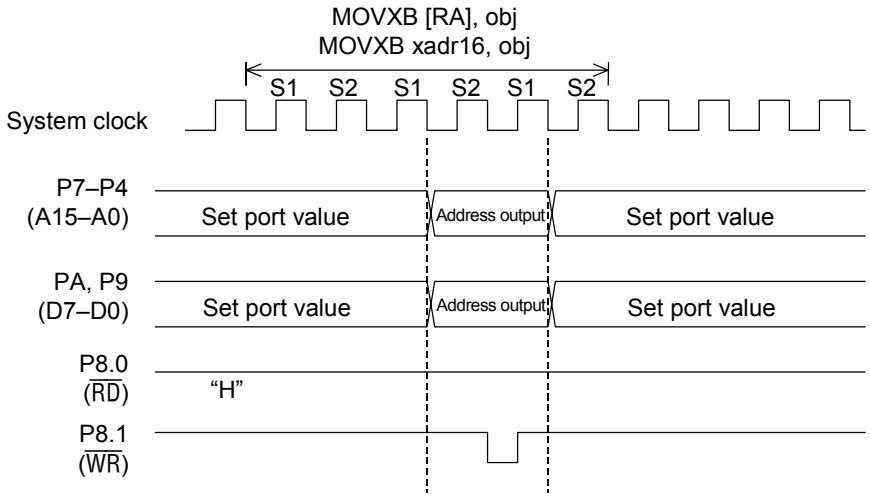


Figure 13-3 Timing for External Memory Write

13.5 Read from External Memory

The following external memory transfer instructions are executed to read from external memory.

MOVXB obj, [RA]
or
MOVXB obj, xadr16

Figure 13-4 shows the timing for external memory read.

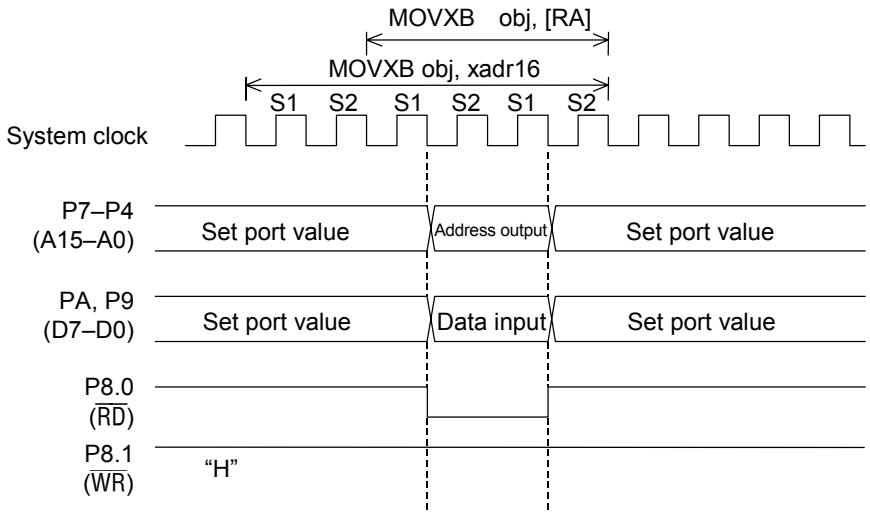


Figure 13-4 External Memory Read Timing

Chapter 14

Melody Driver (MELODY)

Chapter 14 Melody Driver (MELODY)

14.1 Overview

The MSM63188A has an internal melody circuit and buzzer circuit.

While automatically reading melody data in ROM (program memory) as specified by an MSA instruction, the melody circuit outputs a melody signal via the MD and MDB pins.

The melody circuit can select 29 different tones, 63 different tone lengths, and 15 different tempos.

The buzzer circuit has four different buzzer output modes at a frequency of 4 kHz. The buzzer driver signal is output via the MD and MDB pins.

Melody output is a higher priority operation than buzzer output.

14.2 Melody Driver Configuration

The melody driver configuration is shown in Figure 14-1.

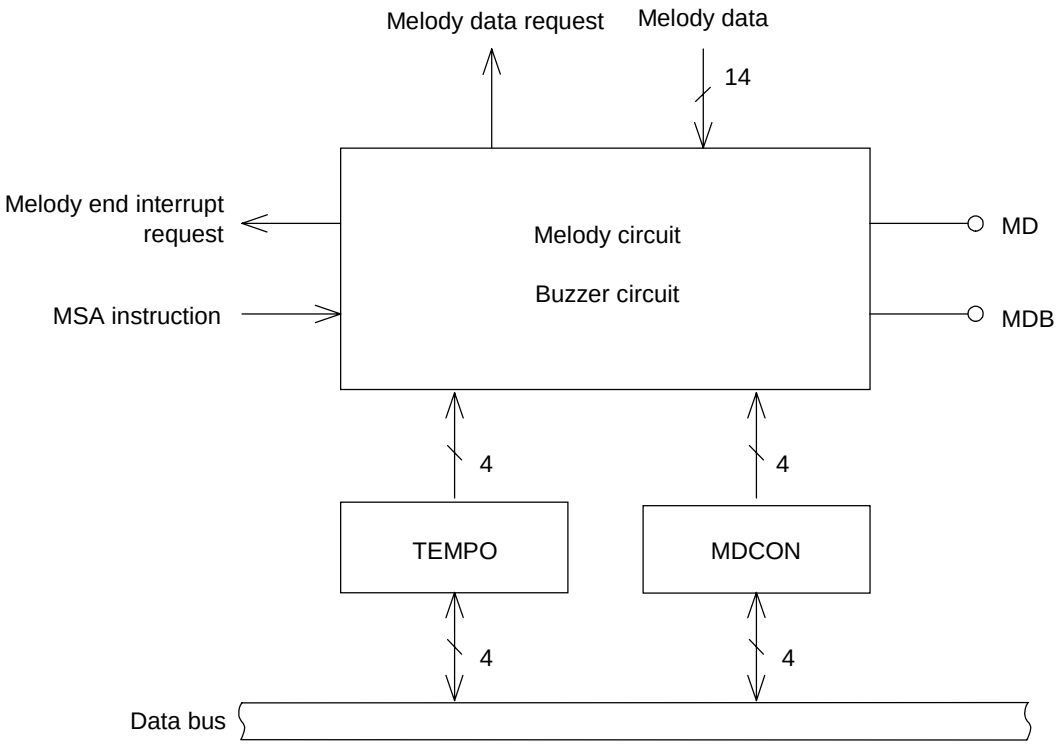


Figure 14-1 Melody Driver Configuration

14.3 Melody Circuit Operation

After the melody tempo is set in the tempo register (TEMP), execution of an MSA instruction will start operation of the melody circuit.

The melody circuit output melody data while automatically reading melody data in ROM (program memory) as specified by an MSA instruction. When the last melody data is read (END bit is "1"), the melody circuit generates a melody end interrupt request. At this time, if an MSA instruction is executed, after the last melody data is output, melody output will continue from the melody data specified by the MSA instruction. If an MSA instruction is not executed, the melody output will stop after the last melody data is output.

MSF (bit 3 of MDCON) is a flag indicating the melody output status. When MSF is "1", the melody is being output, and when "0", the melody is stopped. Setting MSF to "0" during melody output will forcibly stop the melody output. If it is required to stop melody output forcibly, describe the program according to the "Note" on page 14-11. If forcibly stopped, the melody output cannot be restarted at the address at which it was stopped.

14.3.1 Tempo data

Tempo data is set in the tempo register (TEMPO). Tempo data defines the basic tone length.

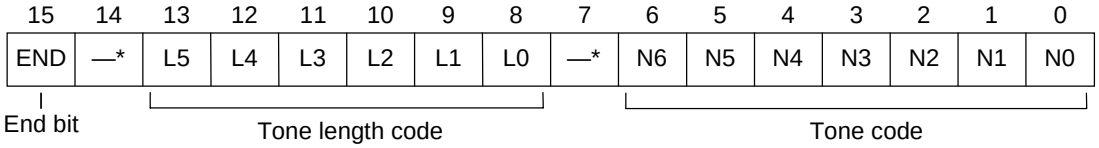
The tempos (number of counts per minute) set by TEMPO are shown in Table 14-1.

Table 14-1 Melody Tempo

TEMPO					Tempo
TP3–0	TP3	TP2	TP1	TP0	
0H	0	0	0	0	♩ = 480
1H	0	0	0	1	♩ = 480
2H	0	0	1	0	♩ = 320
3H	0	0	1	1	♩ = 240
4H	0	1	0	0	♩ = 192
5H	0	1	0	1	♩ = 160
6H	0	1	1	0	♩ ≅ 137
7H	0	1	1	1	♩ = 120
8H	1	0	0	0	♩ ≅ 107
9H	1	0	0	1	♩ = 96
AH	1	0	1	0	♩ ≅ 87
BH	1	0	1	1	♩ = 80
CH	1	1	0	0	♩ ≅ 74
DH	1	1	0	1	♩ ≅ 69
EH	1	1	1	0	♩ = 64
FH	1	1	1	1	♩ = 60

14.3.2 Melody data

Melody data is 14-bit format data in the program ROM defining tone, tone length and end tone. The melody data format is indicated in Figure 14-2.



* Bits 14 and 7 may be either "0" or "1".

Figure 14-2 Melody Data Format

(1) Tone code

The tone code is set in bits 6 through 0 of the melody data. The frequencies that can be output by the melody circuit are defined as:

$$\frac{65536}{(N + 2)} \text{ Hz (where N is an integer from 4 to 127)}$$

The relation between N and tone code bits is:

$$N = 2^6N6 + 2^5N5 + 2^4N4 + 2^3N3 + 2^2N2 + 2^1N1 + 2^0N0$$

If N6 through N2 are all set to "0", there is no melody output for the time specified by the tone length code. Values for N1 and N0 are irrelevant.

Table 14-2 indicates the relations between tones and tone codes.

Table 14-2 Tone and Tone Code Correspondence

Tone	Frequency (Hz)	Tone code							
		N6	N5	N4	N3	N2	N1	N0	N6–N0
C^1	529	1	1	1	1	0	1	1	7BH
Cis^1	560	1	1	1	0	0	1	1	73H
D^1	590	1	1	0	1	1	0	1	6DH
Dis^1	624	1	1	0	0	1	1	1	67H
E^1	662	1	1	0	0	0	0	1	61H
F^1	705	1	0	1	1	0	1	1	5BH
Fis^1	745	1	0	1	0	1	1	0	56H
G^1	790	1	0	1	0	0	0	1	51H
Gis^1	840	1	0	0	1	1	0	0	4CH
A^1	886	1	0	0	1	0	0	0	48H
Ais^1	936	1	0	0	0	1	0	0	44H
B^1	993	1	0	0	0	0	0	0	40H
C^2	1057	0	1	1	1	1	0	0	3CH
Cis^2	1111	0	1	1	1	0	0	1	39H
D^2	1192	0	1	1	0	1	0	1	35H

Tone	Frequency (Hz)	Tone code							
		N6	N5	N4	N3	N2	N1	N0	N6–N0
Dis^2	1260	0	1	1	0	0	1	0	32H
E^2	1338	0	1	0	1	1	1	1	2FH
F^2	1394	0	1	0	1	1	0	1	2DH
Fis^2	1490	0	1	0	1	0	1	0	2AH
G^2	1560	0	1	0	1	0	0	0	28H
Gis^2	1680	0	1	0	0	1	0	1	25H
A^2	1771	0	1	0	0	0	1	1	23H
Ais^2	1872	0	1	0	0	0	0	1	21H
B^2	1986	0	0	1	1	1	1	1	1FH
C^3	2114	0	0	1	1	1	0	1	1DH
D^3	2341	0	0	1	1	0	1	0	1AH
Dis^3	2521	0	0	1	1	0	0	0	18H
E^3	2621	0	0	1	0	1	1	1	17H
Fis^3	2979	0	0	1	0	1	0	0	14H

(2) Tone length code

The tone length code is set in melody data bits 13 through 8. Table 14-3 indicates the relation between tone length and tone length code (L5 to L0). The tone length that is set during execution of the MSA instruction is shorter by approximately 3 msec. When all bits are "0", the tone length is the minimum tone length (the same as setting only L0 to "1".)

Table 14-3 Tone and Tone Length Code Correspondence

Tone length	Tone length code						
	L5	L4	L3	L2	L1	L0	L5–0
	1	1	1	1	1	1	3FH
	1	0	1	1	1	1	2FH
	0	1	1	1	1	1	1FH
	0	1	0	1	1	1	17H
	0	0	1	1	1	1	0FH
	0	0	1	0	1	1	0BH
	0	0	0	1	1	1	07H
	0	0	0	1	0	1	05H
	0	0	0	0	1	1	03H
	0	0	0	0	1	0	02H
	0	0	0	0	0	1	01H

Tone lengths for data specified by the tone length code and the tempo data are expressed by the following:

$1.953125 \times (TP + 1) \times (L + 1)$ msec (where TP is an integer from 1 to 15, and L is an integer from 1 to 63)

TP is a value set in the tempo register (TEMPO), and has the following bit correspondence:

$TP = 2^3TP3 + 2^2TP2 + 2^1TP1 + 2^0TP0$

L is set by the tone length code, and has a bit correspondence with the tone length code as:

$L = 2^5L5 + 2^4L4 + 2^3L3 + 2^2L2 + 2^1L1 + 2^0L0$

(3) End bit

The end bit is set in bit 15 of the melody data. If the end bit is set to "1" in an end melody data when output is started, the melody circuit generates a melody end interrupt request, and stops the melody after the end melody data is output.

14.3.3 Melody circuit application example

An example melody is shown in Figure 14-3.

Table 14-4 lists the note codes for the melody shown in Figure 14-3.

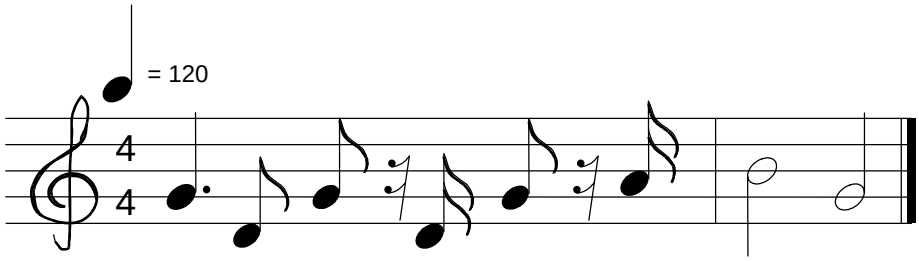


Figure 14-3 Example Melody

Table 14-4 Note Code Table

Note	Note code																Hex
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	END	—*	L5	L4	L3	L2	L1	L0	—*	N6	N5	N4	N3	N2	N1	N0	
G^2	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0	2F28H
D^2	0	0	0	0	1	1	1	1	0	0	1	1	0	1	0	1	0F35H
G^2	0	0	0	0	1	1	1	1	0	0	1	0	1	0	0	0	0F28H
—	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0700H
D^2	0	0	0	0	0	1	1	1	0	0	1	1	0	1	0	1	0735H
G^2	0	0	0	0	1	1	1	1	0	0	1	0	1	0	0	0	0F28H
—	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	1	0700H
A^2	0	0	0	0	0	1	1	1	0	0	1	0	0	0	1	1	0723H
B^2	0	0	1	1	1	1	1	1	0	0	0	1	1	1	1	1	3F1FH
G^2	1	0	1	1	1	1	1	1	0	0	1	0	1	0	0	0	BF28H

* Bits 14 and 7 may be "0" or "1", but in this example they are shown as "0".

14.4 Buzzer Circuit Operation

When EMBD (bit 2 of MDCON) is set to "1", a buzzer driver signal is sent to the melody driver output pins (MD, MDB).

Four buzzer output modes can be selected by MBM1 (bit 1 of MDCON) and MBM0 (bit 0 of MDCON): two types of intermittent tones, a single tone, or a continuous tone output. The buzzer output frequency is 4 kHz and has a 50% duty ratio.

In the intermittent tone 1 mode, a waveform synchronized to the 8 Hz output of the time base counter is output.
In the intermittent tone 2 mode, a waveform synchronized to the logical AND of 8 Hz signal output and a "L" level of 1 Hz signal of the time base counter is output.

In the single tone mode, output starts in synchronization with the rising edge of EMBD. At the second falling edge of the 32 Hz output of the time base counter, EMBD is cleared to "0" and output is stopped.
In the continuous tone mode, output is continued while EMBD is "1".

While the melody is being output (MSF (bit 3 of MDCON) = "1"), the buzzer output is turned OFF. If melody output is started during buzzer output, EMBD is cleared to "0", the buzzer output is stopped, and melody output is given priority.

Figure 14-4 shows the output waveforms of each mode. Shaded sections indicate the 4 kHz output frequency.

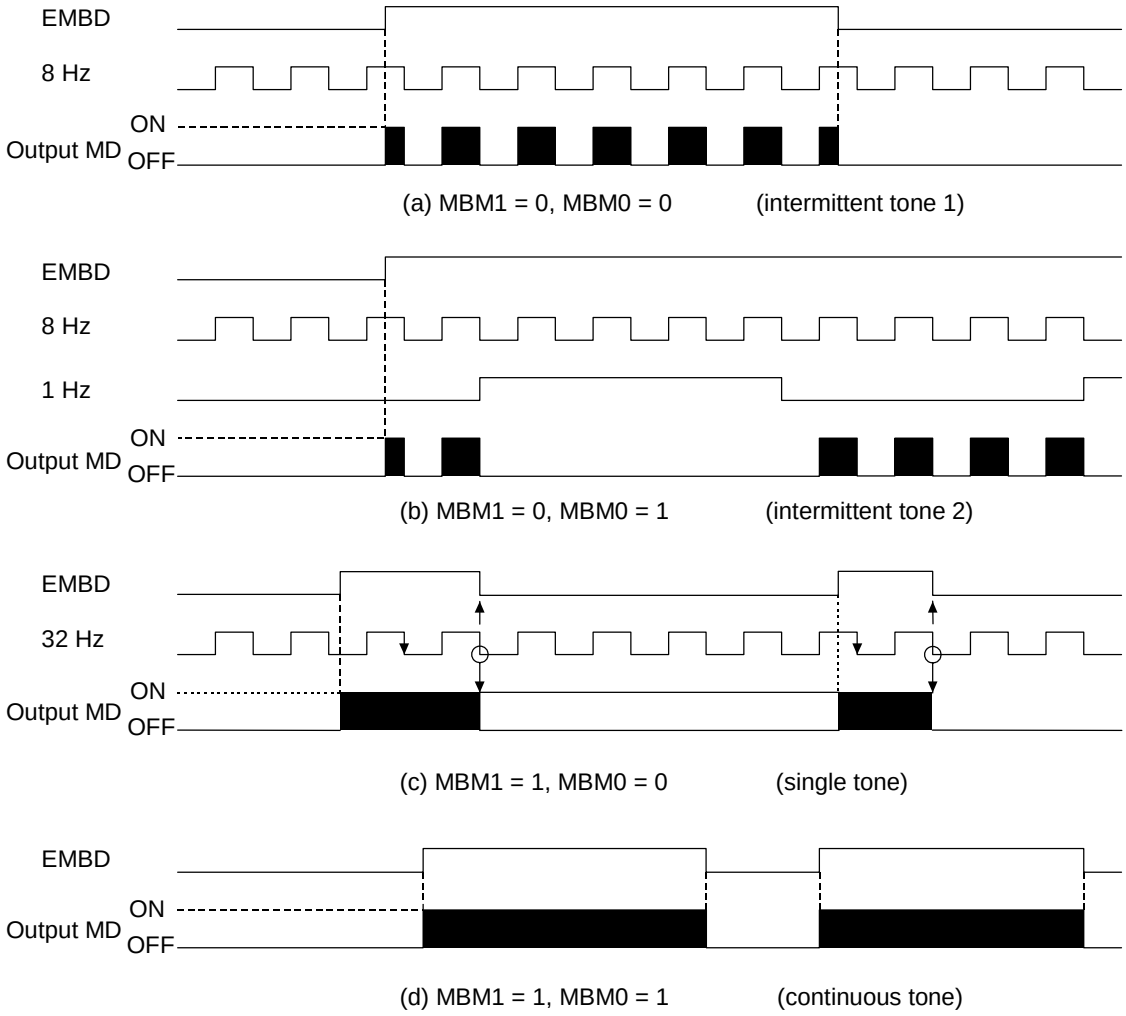


Figure 14-4 Buzzer Driver Output Waveforms in Each Output Mode

14.5 Melody Driver Registers

(1) Tempo register (TEMPO)

TEMPO is a 4-bit special function register (SFR) that sets the melody driver register.

TEMPO (096H) (R/W)

b3	b2	b1	b0
TMP3	TMP2	TMP1	TMP0

Melody tempo select

b3	b2	b1	b0	
0	0	0	0	♩ = 480 (initial value)
0	0	0	1	♩ = 480
0	0	1	0	♩ = 320
0	0	1	1	♩ = 240
0	1	0	0	♩ = 192
0	1	0	1	♩ = 160
0	1	1	0	♩ ≅ 137
0	1	1	1	♩ = 120
1	0	0	0	♩ ≅ 107
1	0	0	1	♩ = 96
1	0	1	0	♩ ≅ 87
1	0	1	1	♩ = 80
1	1	0	0	♩ ≅ 74
1	1	0	1	♩ ≅ 69
1	1	1	0	♩ = 64
1	1	1	1	♩ = 60

(2) Melody driver control register (MDCON)

MDCON is a 4-bit special function register (SFR) that controls the melody driver output.

MDCON (097H) (R/W)

b3	b2	b1	b0
MSF	EMBD	MBM1	MBM0

Melody status flag
0 : Melody stopped (initial value)
1 : Melody output

Buzzer output ON/OFF select
0 : Buzzer output OFF (initial value)
1 : Buzzer output ON

Buzzer mode select

b1	b0	
0	0	: Intermittent tone 1 (initial value)
0	1	: Intermittent tone 2
1	0	: Single tone
1	1	: Continuous tone

Bit 3: MSF

This flag indicates the melody output status.

When an MSA instruction starts the melody, MSF is set to "1". After output of the last melody data (END bit is "1"), MSF is cleared to "0".

Setting MSF to "0" during melody output will forcibly stop the melody output. If forcibly stopped, the melody output cannot be restarted at the address at which it was stopped.

At system reset, MSF is cleared to "0".

Note:

If MSF (bit 3 of MDCON) is set to "0" to stop melody output forcibly, it is required to set the stop address on the ROM table to the end-data address (8000H). In this case, set MSF to "0" after writing the melody end data that consists of two words of melody (silence with the END bit being "1") data. If this programming is not executed, melody output may not be stopped even if MSF is set to "0". Example programming is shown below.

```
;*Program part***********
      DI                    ; 0. Disable master interrupt (MIE).
      MSA  MDSTOP_DATA      ; 1. Write melody end data to the melody circuit.
      MOV  A,#0             ; 2. Set the MSF to "0".
      MOV  MDCON,A          ;
      MOV  A,#1101b         ; 3. Clear melody end interrupt request (QMD).
      AND  IRQ0,A           ;
      EI                    ; 4. Enable master interrupt (MIE).
;*ROM table data part****
;*Provide two words of melody data so that a melody will always be terminated even if a melody
;*request is issued twice.
MDSTOP_DATA:
      DW   8000H            ; Silence data 1
      DW   8000H            ; Silence data 2
;************************
```

In the EASE63180 Emulator, melody output will be stopped only by setting MSF to "0"; writing melody end data is not needed.

Bit 2: EMBD

This bit turns the buzzer output ON or OFF.

At system reset, EMBD is cleared to "0" and buzzer output is turned OFF.

In the single tone output mode, setting EMBD to "1" turns ON the buzzer output. After the second falling edge of the 32 Hz output, EMBD is cleared to "0" and buzzer output is turned OFF.

If melody output is started during buzzer output, EMBD is cleared to "0" and the buzzer output is turned OFF.

Bit 1, 0: MBM1, MBM0

These bits select the buzzer output mode.

Output of two types of intermittent tones, a single tone or a continuous tone can be selected.

At system reset, MBM1 and MBM0 are cleared to "0", selecting output of intermittent tone 1.

Buzzer output mode	Waveform
Intermittent tone 1	Intermittent tone waveform synchronized to 8 Hz output of time base counter
Intermittent tone 2	Intermittent tone waveform synchronized to the logical AND of 8 Hz signal output and a "L" level of 1 Hz signal output of the time base counter
Single tone	Single tone waveform beginning when EMBD is set to "1" until second falling edge of 32 Hz output of time base counter
Continuous tone	Continuous tone waveform that is constant while EMBD is "1"

Figure 14-5 shows the output waveforms of the melody driver output pins.

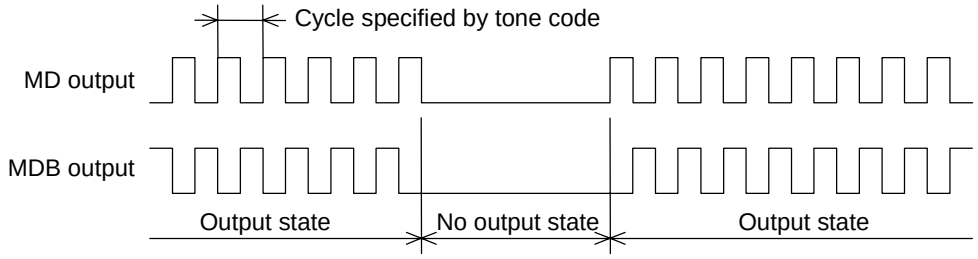


Figure 14-5 Output Waveforms of Melody Driver Output Pins

Chapter 15

Buzzer Driver (BUZZER)

Chapter 15 Buzzer Driver (BUZZER)

15.1 Overview

The MSM63182A and MSM63184A have an internal buzzer driver supporting 15 buzzer output waveforms and four buzzer output modes. Buzzer output is controlled by the buzzer driver control register (BDCON) and the buzzer frequency control register (BFCON).

15.2 Buzzer Driver Configuration

The buzzer driver configuration is shown in Figure 15-1.

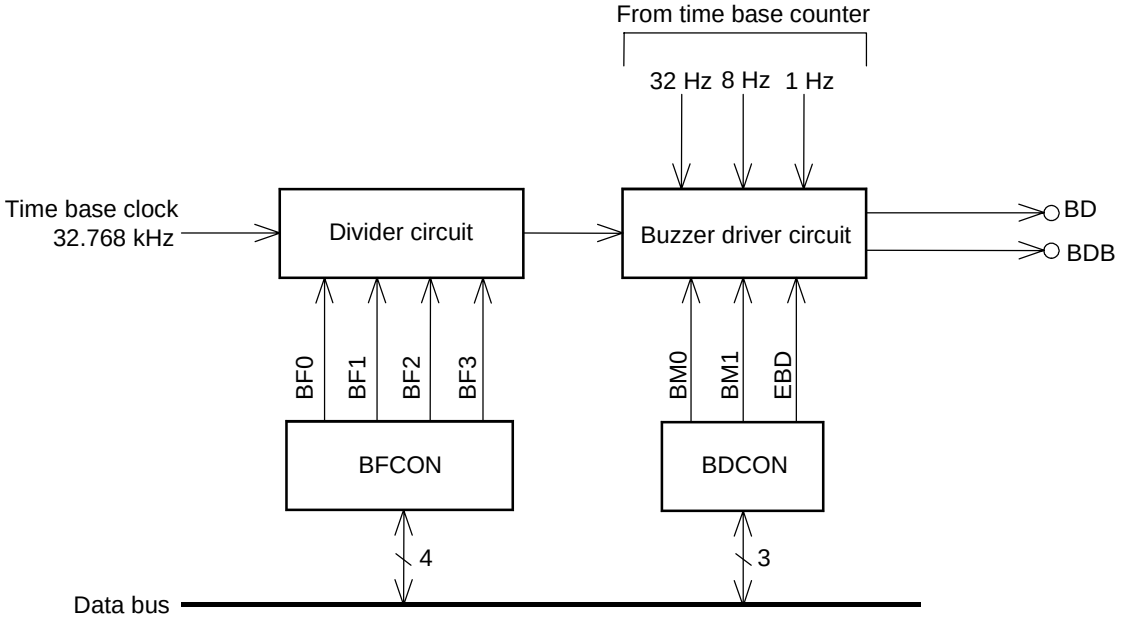


Figure 15-1 Buzzer Driver Configuration

15.3 Buzzer Driver Operation

When bit 2 (EBD) of the buzzer driver control register (BDCON) is set to "1", the buzzer drive signal is output to the buzzer driver pin. The buzzer output frequency is one of 15 set by the buzzer frequency control register (BFCON). The buzzer output mode can be set to any of four choices (intermittent 1, intermittent 2, single tone or continuous) by bits 1 and 0 (BM1, BM0) of the buzzer driver control register (BDCON). The buzzer output frequency signal duty ratio is 50%.

Intermittent tone mode 1 is output as a waveform synchronized to the 8 Hz time base counter. Intermittent tone mode 2 is output as a waveform to the logical product of the 8 Hz and a "L" level of 1 Hz signal of the time base counter. The single tone mode begins output synchronized to the rising edge of EBD, with EBD reset to "0" at the second 32 Hz falling edge of the time base counter to stop output. In continuous tone mode output is continued as long as EBD is set to "1".

Figure 15-2 shows the output waveforms for each mode. The shaded portions show the buzzer output frequency signals.

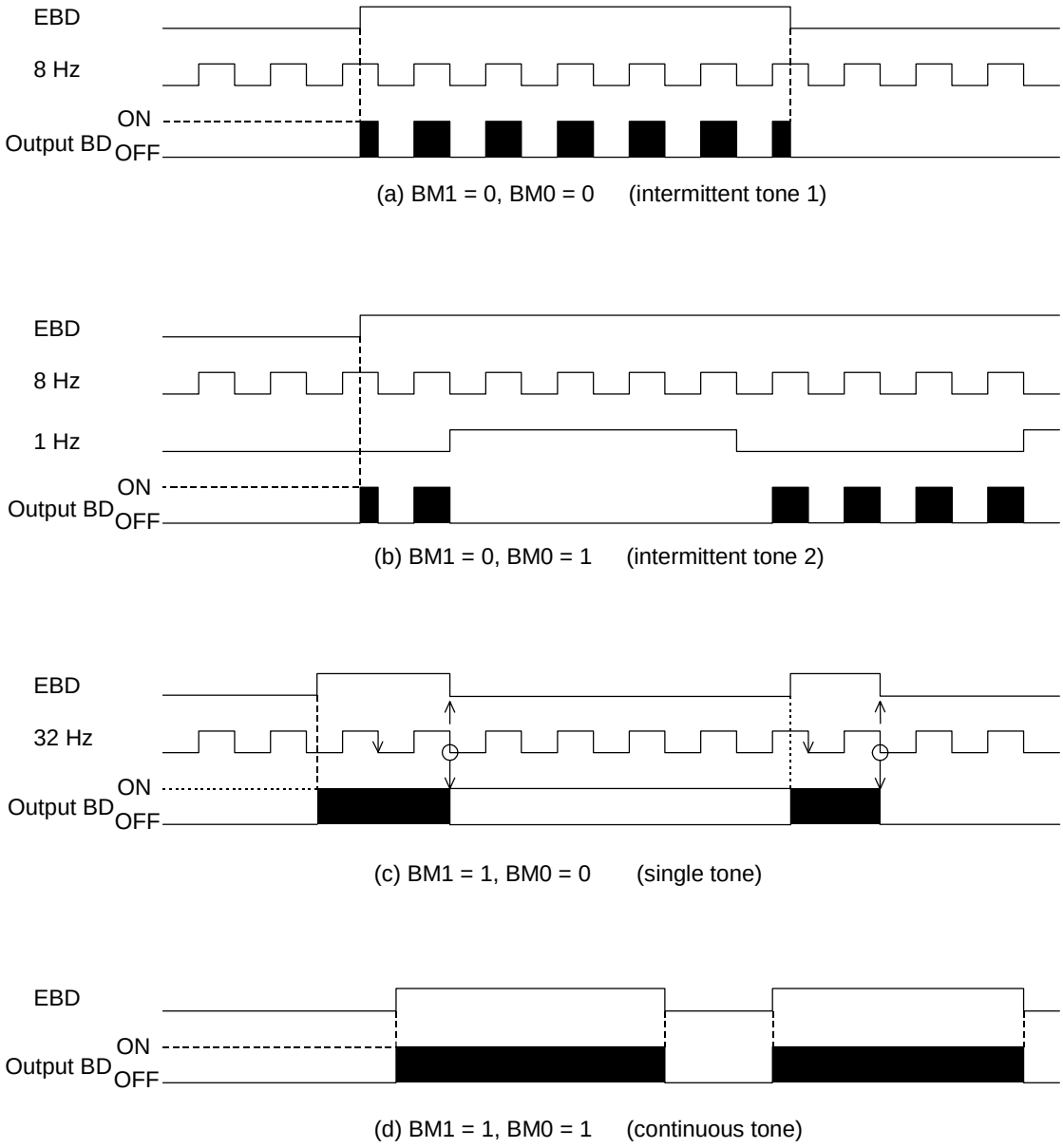
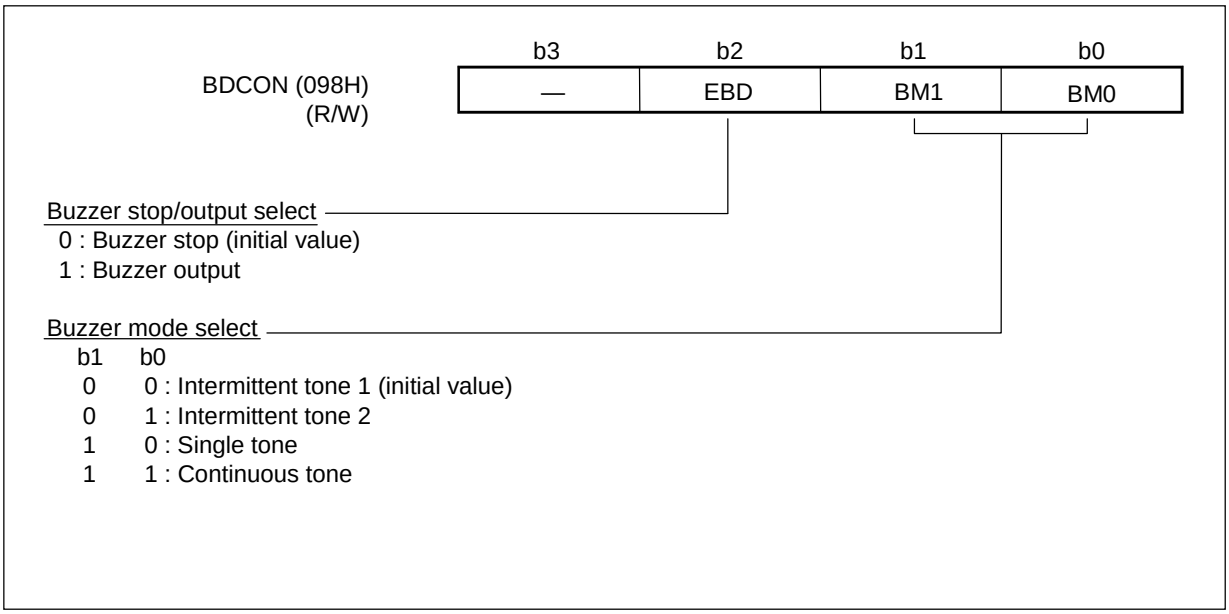


Figure 15-2 Buzzer Driver Output Waveforms in Each Output Mode

15.4 Buzzer Driver Registers

(1) Buzzer driver control register (BDCON)

BDCON is a 4-bit special function register (SFR) controlling the four buzzer output modes and buzzer output/stop.



Bit 2: EBD

This bit selects buzzer output/stop. At system reset it is reset to "0", turning off the buzzer output. In the single-tone output mode, when EBD is set to "1", buzzer output is started with EBD reset to "0" at the second 32 Hz falling edge to stop output.

Bit 1, 0: BM1, BM0

These bits select the buzzer driver output mode, to intermittent 1, intermittent 2, single tone or continuous output. At system reset both BM1 and BM0 are reset to "0", selecting intermittent tone 1.

(2) Buzzer frequency control register (BFCON)

BFCON is a 4-bit special function register (SFR) controlling the buzzer output frequency.

BFCON (099H) (R/W)

b3	b2	b1	b0
BF3	BF2	BF1	BF0

Buzzer output frequency select

b3	b2	b1	b0	
0	0	0	0	: Output stop (initial value)
0	0	0	1	: 5.461 kHz
0	0	1	0	: 4.096 kHz
0	0	1	1	: 3.277 kHz
0	1	0	0	: 2.730 kHz
0	1	0	1	: 2.341 kHz
0	1	1	0	: 2.048 kHz
0	1	1	1	: 1.820 kHz
1	0	0	0	: 1.638 kHz
1	0	0	1	: 1.489 kHz
1	0	1	0	: 1.365 kHz
1	0	1	1	: 1.260 kHz
1	1	0	0	: 1.170 kHz
1	1	0	1	: 1.092 kHz
1	1	1	0	: 1.024 kHz
1	1	1	1	: 0.964 kHz

Bits 3–0: BF3–0

These bits select the buzzer output frequency. At system reset all are reset to "0", stopping output. The output frequency duty ratio is 50%.

Figure 15-3 shows the output waveforms for the buzzer driver output pins.

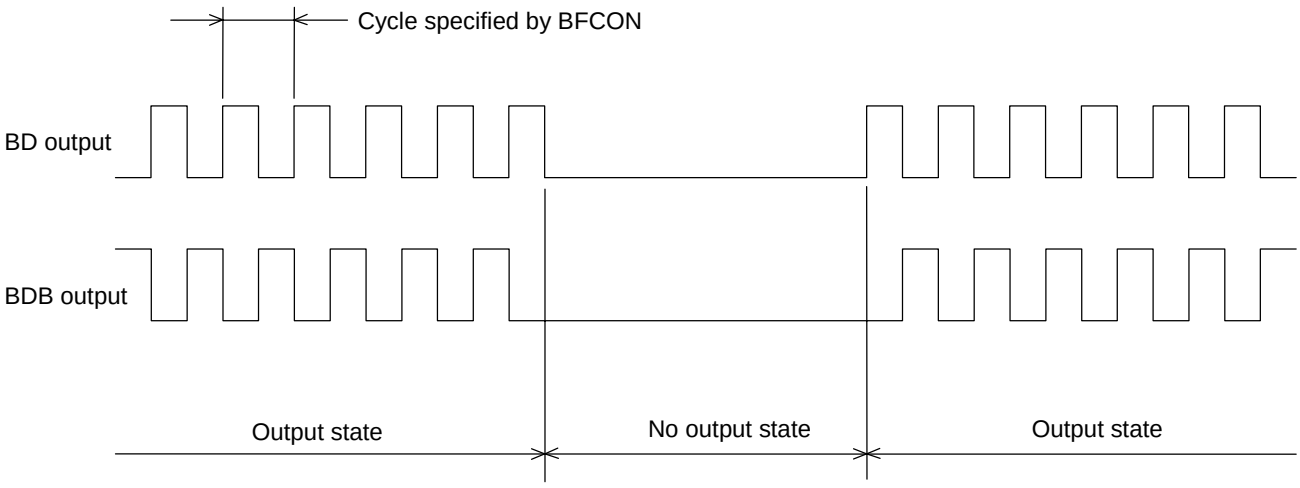


Figure 15-3 Output Waveforms for BD and BDB Pins

Chapter 16

Serial Port (SIO)

Chapter 16 Serial Port (SIO)

16.1 Overview

The serial port (SIO) is a serial communication port for which either synchronous or asynchronous communication can be selected.

The serial port implements the send and receive circuits in independent circuits, making it possible to send and receive simultaneously.

The send and receive modes can be UART mode (asynchronous communication mode) or synchronous mode (synchronous communication mode).

In synchronous mode an internal clock mode generates the shift clock internally, and an external clock mode receives an external shift clock.

Table 16-1 shows the serial port modes.

Table 16-1 Serial Port Modes

		Mode		Baud rate
Serial port	Send side	UART mode		Can be set to a user-specified value with timers 2 and 3 (TM2, 3)
		Synchronous mode	Internal clock mode	Crystal oscillation frequency
			External clock mode	From external clock
	Receive side	UART mode		1. 9600 bps 2. 4800 bps 3. 2400 bps 4. 1200 bps
		Synchronous mode	Internal clock mode	Crystal oscillation frequency
			External clock mode	From external clock

16.2 Serial Port Configuration

Figure 16-1 indicates the serial port configuration.

The serial port consists of the send/receive clock generator circuits, the send/receive control registers, the buffer registers to store send/receive data, send/receive data transfer shift registers, and the send/receive status registers.

PC.0/PXD is the send serial data input pin, PC.3/TXD is the send serial data output pin, PC.1/TXC is the serial send clock I/O pin, and PC.2/RXC is the serial receive clock I/O pin. Set I/O and secondary functions with the port control registers as needed for each communication mode.

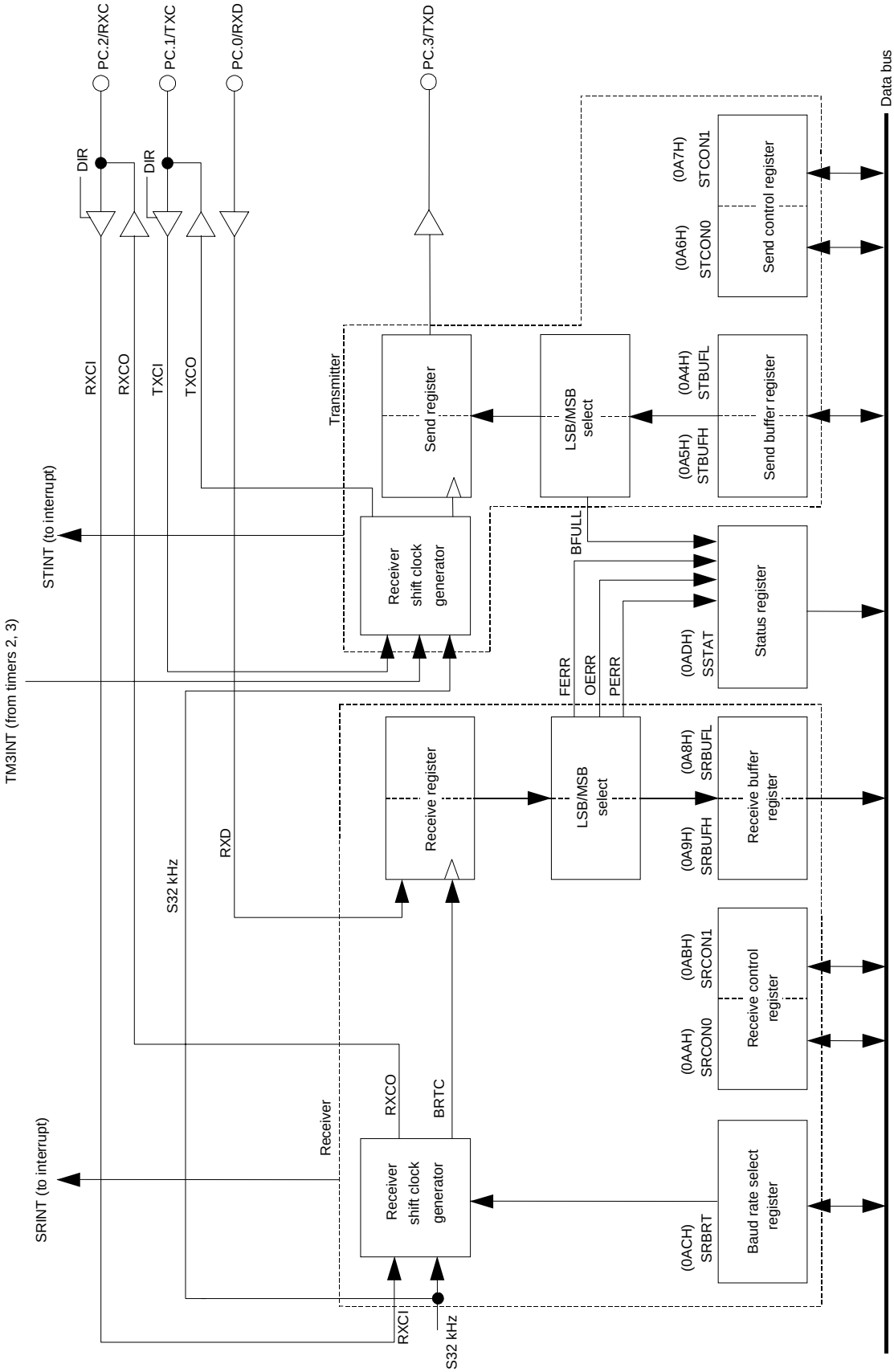
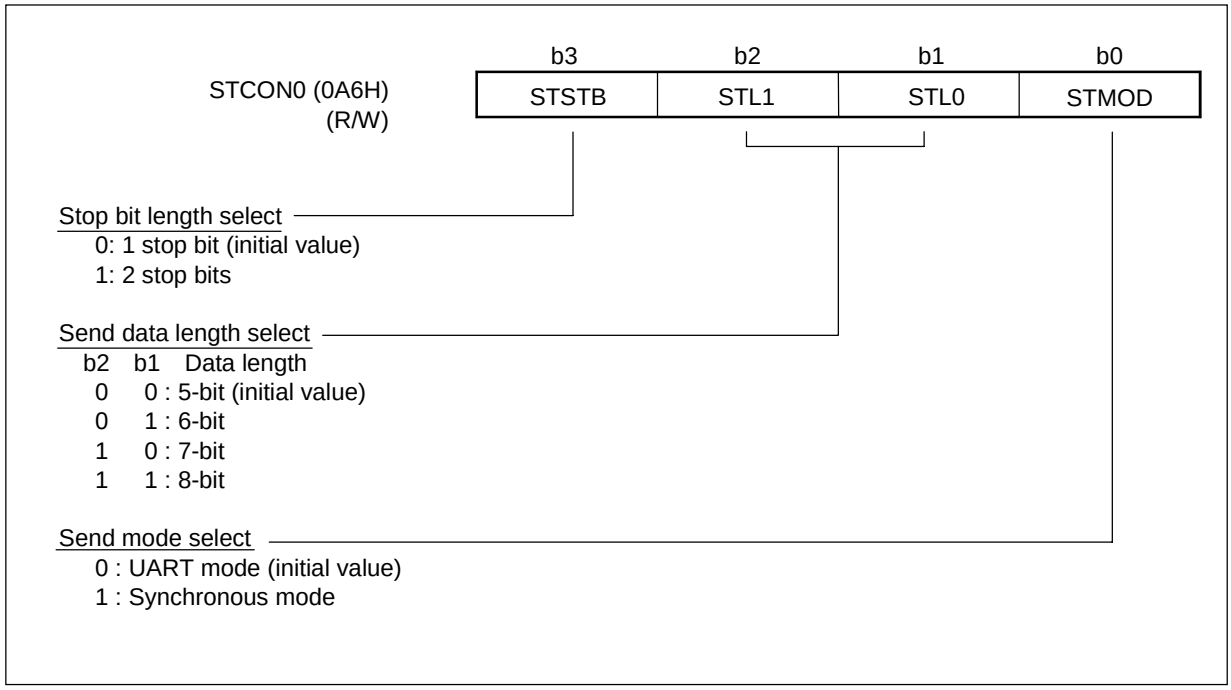


Figure 16-1 Serial Port Configuration

16.3 Serial Port Registers

(1) Send control registers 0/1 (STCON0, STCON1)

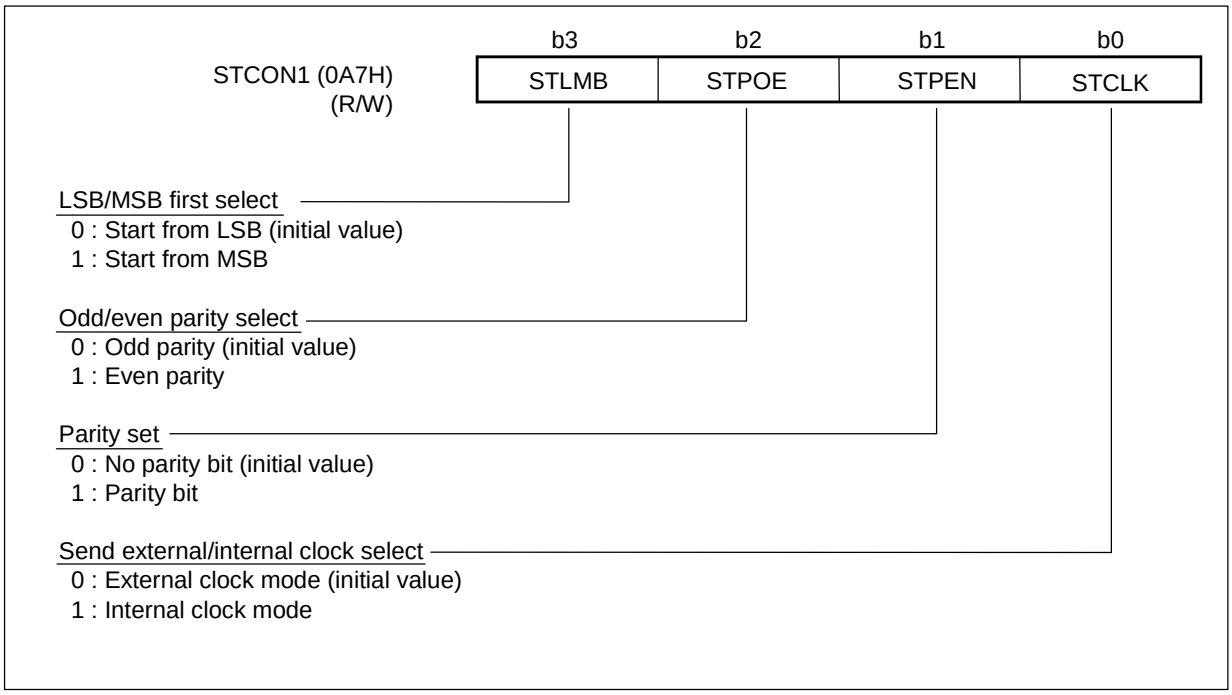
STCON0 and STCON1 are 4-bit special function registers (SFRs) to control the serial port send operation. STCON0 and STCON1 are initialized to "0" at system reset.



Bit 3: STSTB
This bit specifies stop bit length. Valid only when bit 0 is "0" (UART mode).

Bit 2, 1: STL0, STL1
These bits specify the send data length.

Bit 0: STMOD
This bit specifies the serial mode send operation mode.



Bit 3: STLMB

This bit specifies whether the LSB or MSB is sent first.

Bit 2: STPOE

This bit specifies whether the parity bit is even or odd. Valid only when bit 1 is "1" (parity bit).

Bit 1: STPEN

This bit specifies whether or not a parity bit is added.

Bit 0: STCLK

This bit specifies the external/internal send clock for synchronous mode. Valid only when STMOD (bit 0 of STCON0) is "1" (synchronous mode).

(2) Send buffer register (STBUFL, STBUFH)

	b3	b2	b1	b0
STBUFL (0A4H) (R/W)	TB3	TB2	TB1	TB0
STBUFH (0A5H) (R/W)	TB7	TB6	TB5	TB4

STBUFL and STBUFH are 4-bit special function registers (SFRs) that set send data for serial port send operation.

LSB/MSB selection (see below) allows the data send direction (LSB or MSB first) to be specified. Both STBUFL and STBUFH are initialized to "0" at system reset.

Send operation begins when send data is set to STBUFH. Be sure to set send data to STBUFL before setting data to STBUFH.

Also set the baud rate and send mode before beginning send operation.

If send operation is already under way when send data is set to STBUFH, send for the new data begins when the prior send has ended, and at the same time an interrupt request signal (STINT) is generated. In the STINT interrupt routine the program should first write the send data to STBUFL and STBUFH to assure no pauses in the send sequence.

(3) Send register

The send register is a shift register that handles the shift operation in send. At system reset it is cleared to 00H. The send register cannot be directly accessed from the CPU.

The hardware send flow is indicated in Figure 16-2, to explain the timing for transfer of data from STBUFL/H to the send register.

First set the send mode and baud rate. When send data is set to STBUFH, the status (SSTAT) buffer full flag (BFULL) is set to "1", and unless, send operation is already under way the content of STBUFL/H is transferred to the send register and send operation begins. When send operation begins the BFULL flag is reset to "0", and the next send data can be set to STBUFL/H.

If prior data and operation is not complete, the send data is held in STBUFL/H until send is completed. In this case BFULL remains set to "1". When the prior send operation is complete the send data will be transferred from STBUFL/H to the send register, and send begins.

Note:

When BFULL is "1" it is possible to set data to STBUFL/H, but prior data set to STBUFL/H that is being held there is overwritten and lost. Always set data after verifying that the BFULL flag is "0".

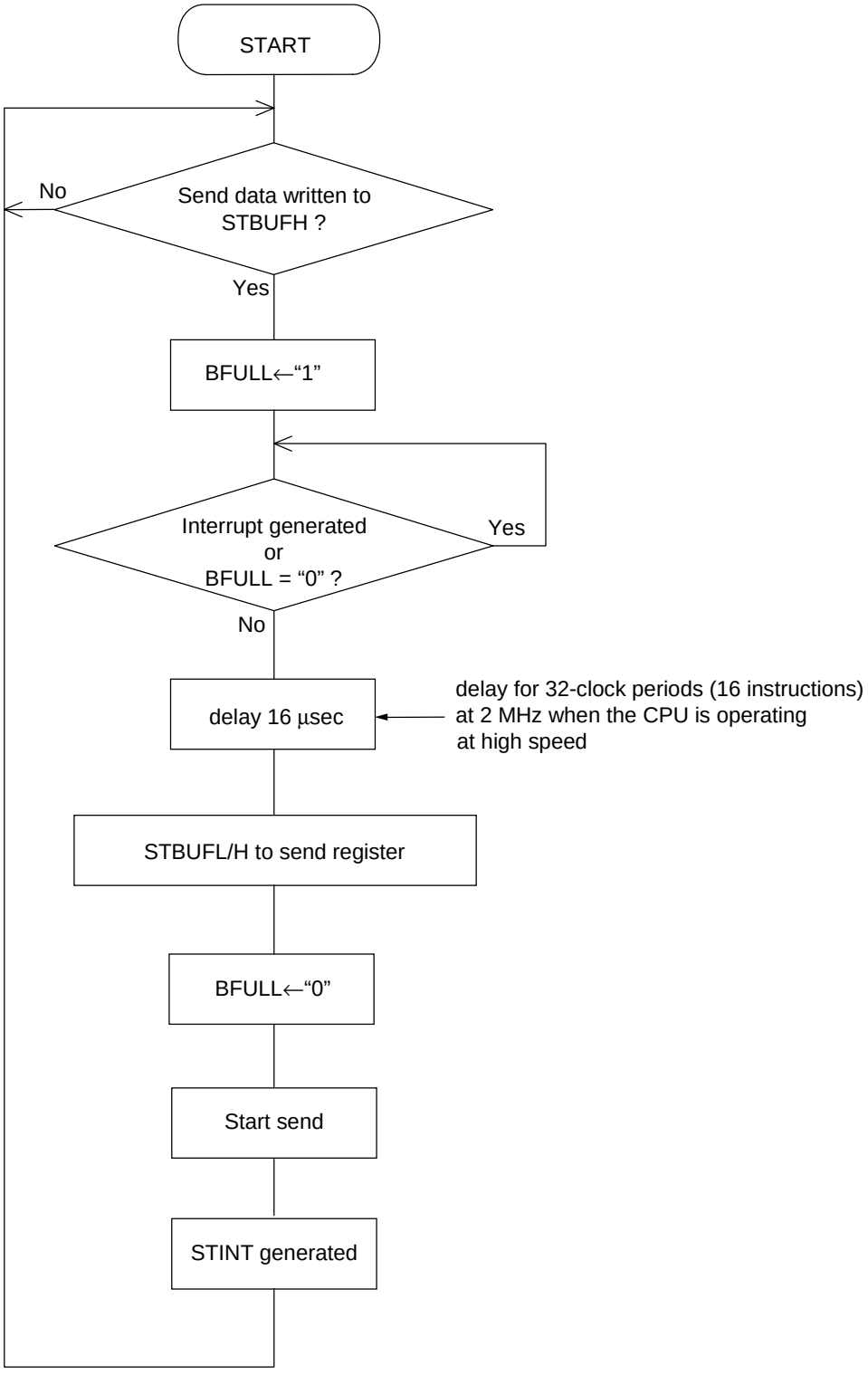
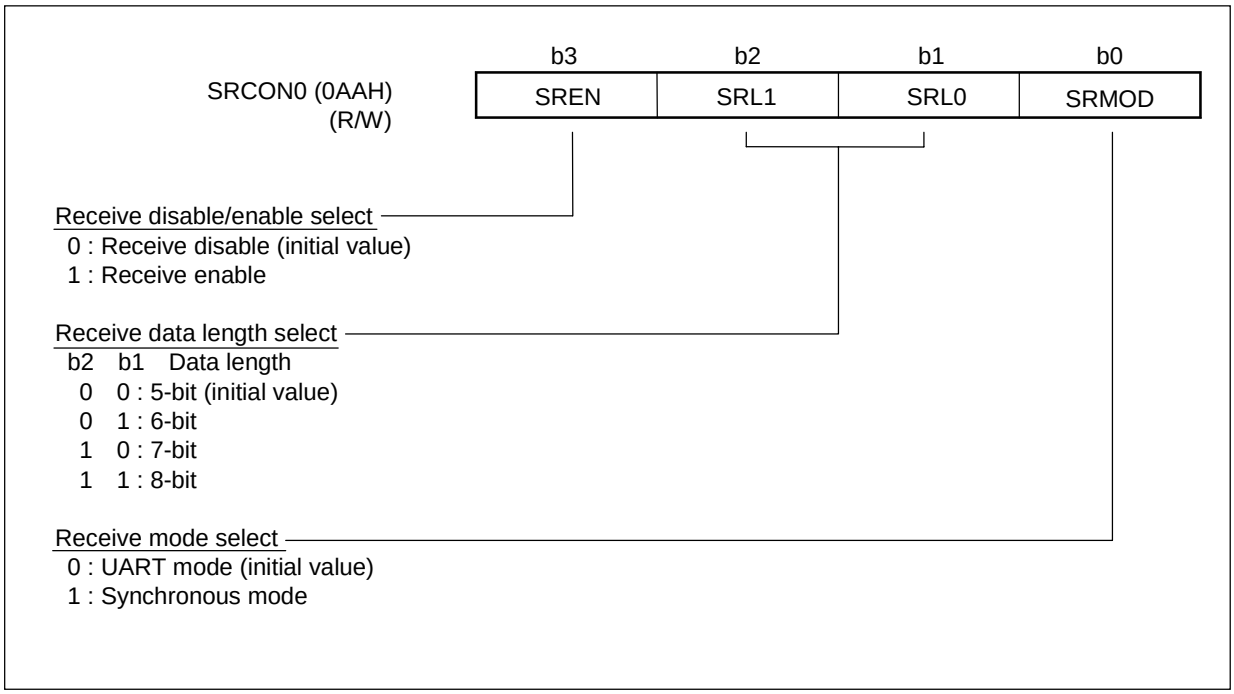


Figure 16-2 Hardware Send Operation Flow

(4) Receive control registers 0/1 (SRCON0, SRCON1)

SRCON0 and SRCON1 are 4-bit special function registers (SFRs) controlling serial port receive operation.

SRCON0 and SRCON1 are initialized to "0" at system reset.



Bit 3: SREN

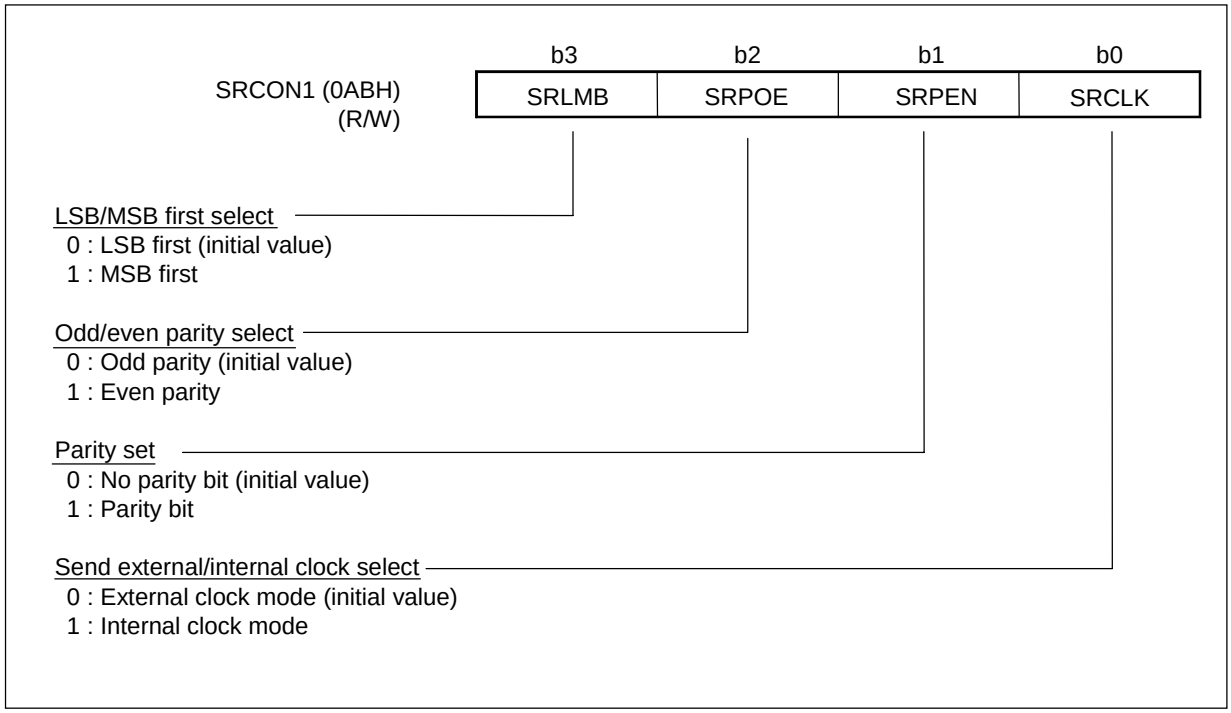
This bit specifies receive operation disable/enable. After receive is enabled in the synchronous mode, this bit is reset to "0" after receiving one frame of data. In the UART mode it does not change.

Bit 2, 1: SRL0, SRL1

These bits specify the receive data length.

Bit 0: SRMOD

This bit specifies the serial port receive operation mode.



Bit 3: SRLMB

This bit specifies whether LSB or MSB is received first.

Bit 2: SRPOE

This bit specifies whether the parity bit is even or odd. Valid only when bit 1 is "1" (parity bit).

Bit 1: SRPEN

This bit specifies whether or not a parity bit is added.

Bit 0: SRCLK

This bit specifies the external/internal receive clock for synchronous mode. Valid only when SRMOD (bit 0 of SRCON0) is "1" (synchronous mode).

(5) Receive register

The receive register is the shift register that handles shift operation at receive. It is initialized to 00H at system reset. It cannot be directly accessed by the CPU. When a receive operation is complete, the data read into the receive register is transferred to SRBUFL/H, and at the same time the receive interrupt request signal (SRINT) is generated.

(6) Receive buffer register (SRBUFL, SRBUFH)

SRBUFL (0A8H) (R)

b3	b2	b1	b0
RB3	RB2	RB1	RB0

SRBUFH (0A9H) (R)

b3	b2	b1	b0
RB7	RB6	RB5	RB4

SRBUFL and SRBUFH are 4-bit special function registers (SFRs) used to hold the received data in serial port reception. SRBUFL and SRBUFH are initialized to "0" at system reset.

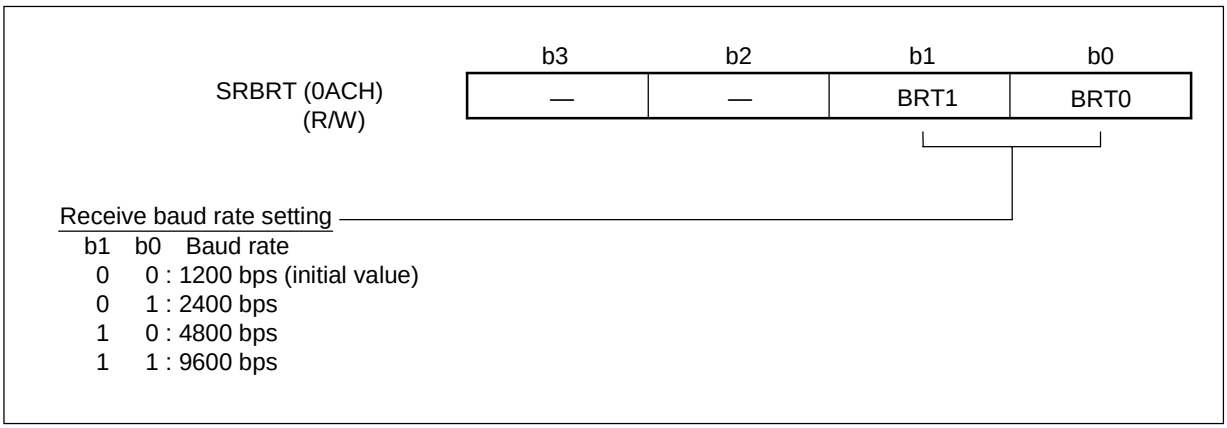
When receive operation is completed the contents of the receive register are sent to SRBUFL/H, and the receive interrupt request (SRINT) is generated. The contents of SRBUFL/H are held until the next receive operation is completed.

If data from a prior receive operation is in SRBUFL/H and new data is received, an overrun error will result. When an overrun error is generated, new received data cannot be loaded into SRBUFL/H.

(7) Receive baud rate setting register (SRBRT)

SRBRT is a 4-bit special function register (SFR) used to set the receive baud rate for serial port receive operation in UART mode.

SRBRT is initialized to 0CH at system reset.



Bit 1, 0: BRT0, BRT1

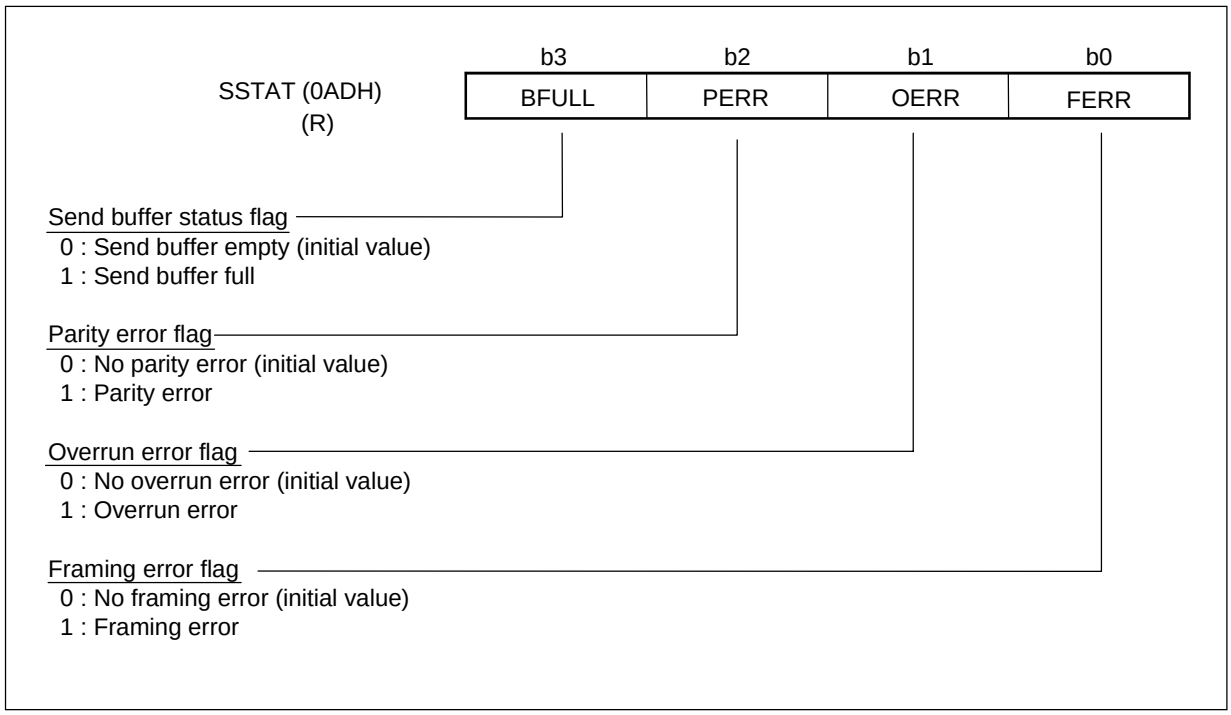
These bits set the receive baud rate.

(8) Serial port status register (SSTAT)

SSTAT is a 4-bit special function register (SFR) used to indicate the status of serial port send/receive.

SSTAT is initialized to "0" at system reset.

SSTAT is a read-only register, and the content is reset every time it is read.



Bit 3: BFULL (send buffer status flag)

This bit is enabled in both UART and synchronous modes, and is set to "1" when send data is set to STBUFL/H in the send mode, and reset to "0" when the send data is transferred to the send register.
When BFULL is set to "1" and send data is set (written) to STBUFL/H, the previous data set to those registers is overwritten and lost. Always set data only after verifying that the BFULL flag is "0".

Bit 2: PERR (parity error flag)

This bit is enabled in both UART and synchronous modes, and is set to "1" when the parity for the received data does not match the parity bit attached to the data.

Bit 1: OERR (overrun error flag)

This bit is enabled in both UART and synchronous modes, and is set to "1" when data reception is completed and the data received the previous time has still not been transferred to the CPU. In this case, the new data cannot be transferred to SRBUFL/H.

Bit 0: FERR (framing error flag)

This is only enabled in the UART mode and is set to "1" in the following instances.
(1) When a "1" is detected in start bit sampling
(2) When a "0" is detected in stop bit sampling
In either case a receive interrupt request signal (SRINT) is generated.

16.4 Serial Port Operation Description

16.4.1 Data format

(1) UART mode

The data format for the UART mode is shown in Figure 16-3.

SRCON0/1 and STCON0/1 can be set to specify a data bit length of 5 to 8 bits. The parity bit can be enabled/disabled. If enabled it can be set to even or odd. Stop bit length can be set to 1 or 2 bits.

The combination of these parameters gives a range of from 7 to 12 bits for send/receive data frames.

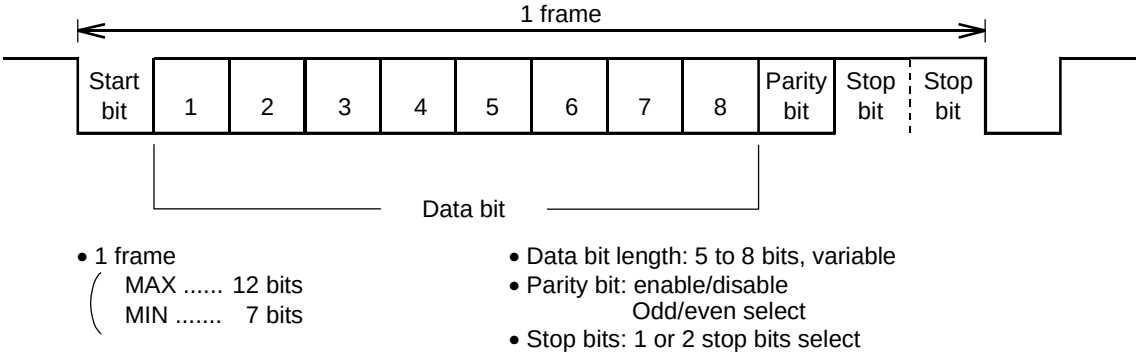


Figure 16-3 UART Mode Data Format

(2) Synchronous mode

The data format for the UART mode is shown in Figure 16-4.

SRCON0/1 and STCON0/1 can be set to specify a data bit length of 5 to 8 bits. The parity bit can be enabled/disabled, and if enabled can be set to even or odd.

The combination of these parameters gives a range of from 5 to 9 bits for send/receive data frames.

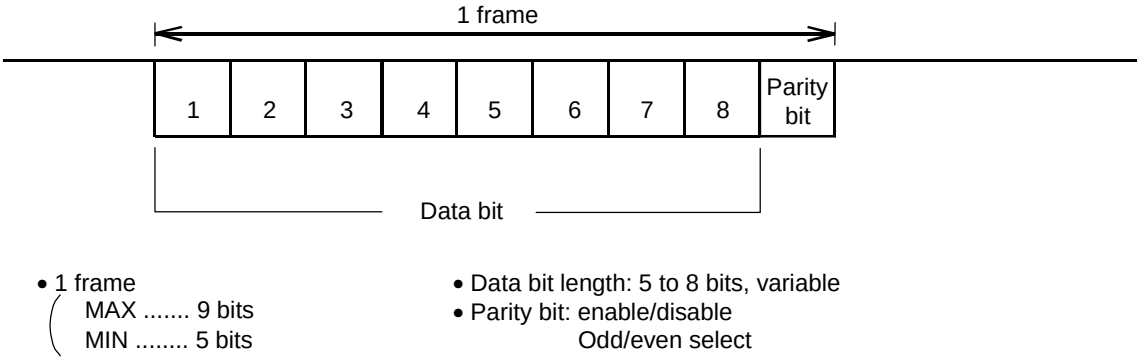


Figure 16-4 Synchronous Mode Data Format

16.4.2 Send operation description

The serial port send circuit has a two-stage configuration. This consists of the send register and the send buffer register (STBUFL/H), so it is possible to set send data to STBUFL/H while sending the previous data. When the BFULL flag of the serial port status register (SSTAT) is 1, however, it indicates that STBUFL/H send data has not yet been transferred to the send register. Always verify that the BFULL flag is 0 before transferring data.

(1) UART mode

The UART mode is specified by setting STMOD (bit 0 of STCON0) to "0". Figure 16-5 is the UART mode send timing chart. The UART mode send procedure is described below. The send baud rate is set first, then the timer, and then the send format (data bit length, parity bit, etc.) in STCON0 and STCON1. The TM3INT signal supplied from timers 2 and 3 is the baud rate clock.

① Set send data to STBUFL/H.

② The send data is transferred from STBUFL/H to the send register, and send operation begins. At the same time the serial port send interrupt request (STINT) is generated.

③ Verify that BFULL = "0", then after a delay of 16 μsec, set the next send data to STBUFL/H.

④ When send operation is complete, the send data set to STBUFL/H is transferred to the send register, and send operation begins. At the same time the serial port send interrupt request (STINT) is generated.

Repeat operation ③ the required number of times.

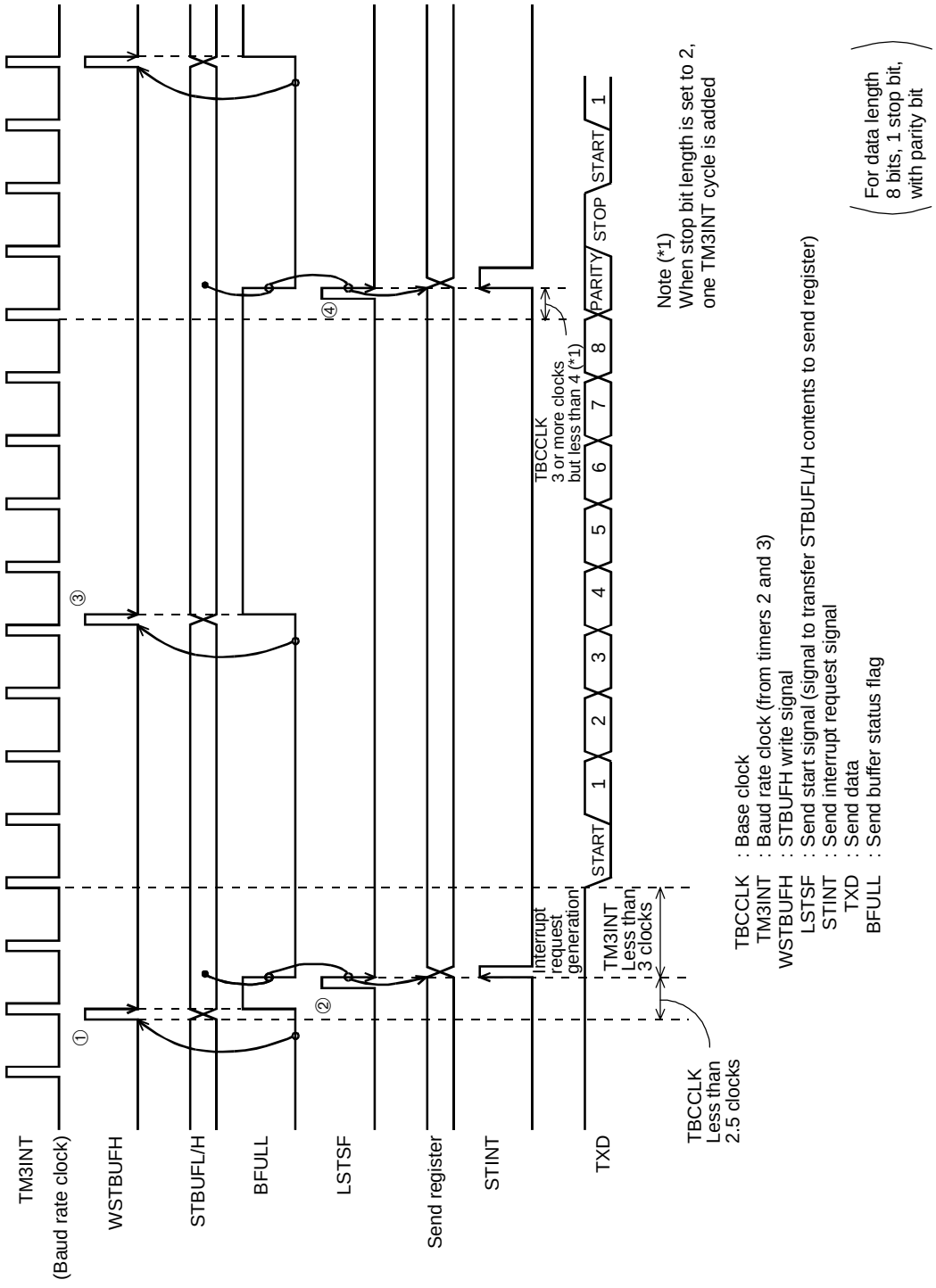


Figure 16-5 UART Mode Send Timing Chart

(2) Synchronous internal clock mode

The synchronous internal clock mode is selected by setting STMOD (bit 0 of STCON0) to "1", and STCLK (bit 0 of STCON1) to "1".

Figure 16-6 is the send timing chart for the synchronous internal clock mode.

The synchronous internal clock send procedure is described below.

First the send format (data bit length, parity bit, etc.) is set to STCON0 and STCON1.

① Set send data to STBUFL/H.

② The send data is transferred from STBUFL/H to the send register, and send operation begins. At the same time the interrupt request signal (STINT) is generated.

③ Check that BFULL = "0", then set the next send data to STBUFL/H.

④ When the send operation is complete, the send data set to STBUFL/H is transferred to the send register, and the send operation begins. At the same time, the serial port send interrupt signal (STINT) is generated.

Repeat step ③ the required number of times.

In the synchronous internal clock mode the send baud rate is fixed at the crystal oscillation frequency, that is, the frequency (32.768 kHz) of the time base clock (TBCCLK).

After data is set to STBUFH, the send clock (TXCO) is generated between 2 and 3.5 clocks of the TBCCLK source, and a send operation starts.

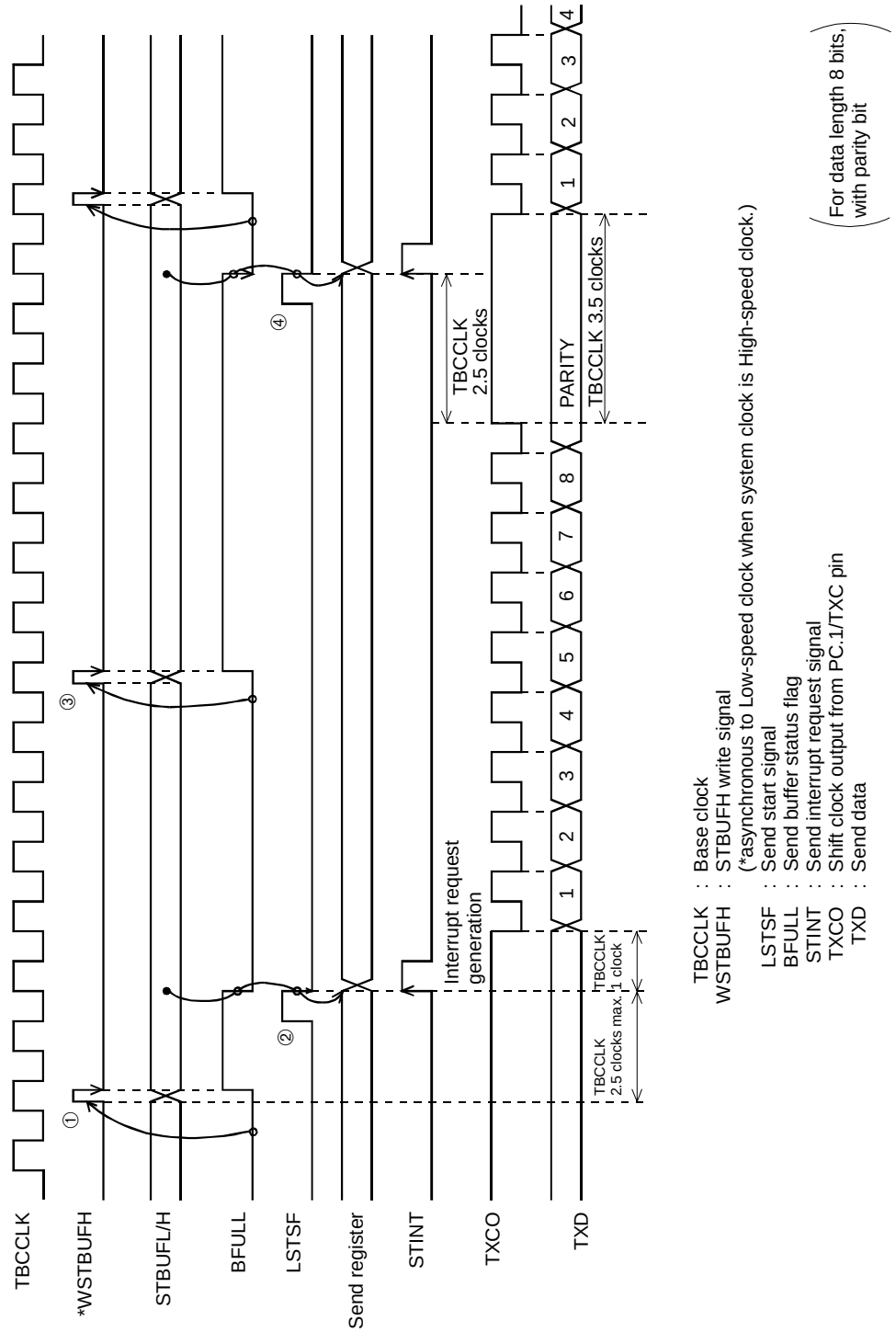


Figure 16-6 Send Timing Chart for Synchronous Internal Clock Mode

(3) Synchronous external clock mode

The synchronous external clock mode is selected by setting STMOD (bit 0 of STCON0) to "1", and STCLK (bit 0 of STCON1) to "0".

Figure 16-7 is the send timing chart for the synchronous external clock mode.

The synchronous external clock send procedure is described below.

First set the send format (data bit length, parity bit, etc.) to STCON0 and STCON1.

① Set send data to STBUFL/H.

② The send data is transferred from STBUFL/H to the send register, and at the same time the interrupt request signal (STINT) is generated.

③ Send operation is started by the send shift clock (TXCI).

④ Check that BFULL = "0", then set the next send data to STBUFL/H.

⑤ When the send operation is complete, the send data set to STBUFL/H is transferred to the send register. At the same time, the serial port send interrupt signal (STINT) is generated.

Repeat step ④ the required number of times.

In the synchronous external clock mode the send baud rate is determined by the input shift clock (TXCI).
To send data continuously, keep an interval of at least 3.5 clocks (approx. 107 µs) of TBCCLK for one frame of clocked (TXCI) send data.

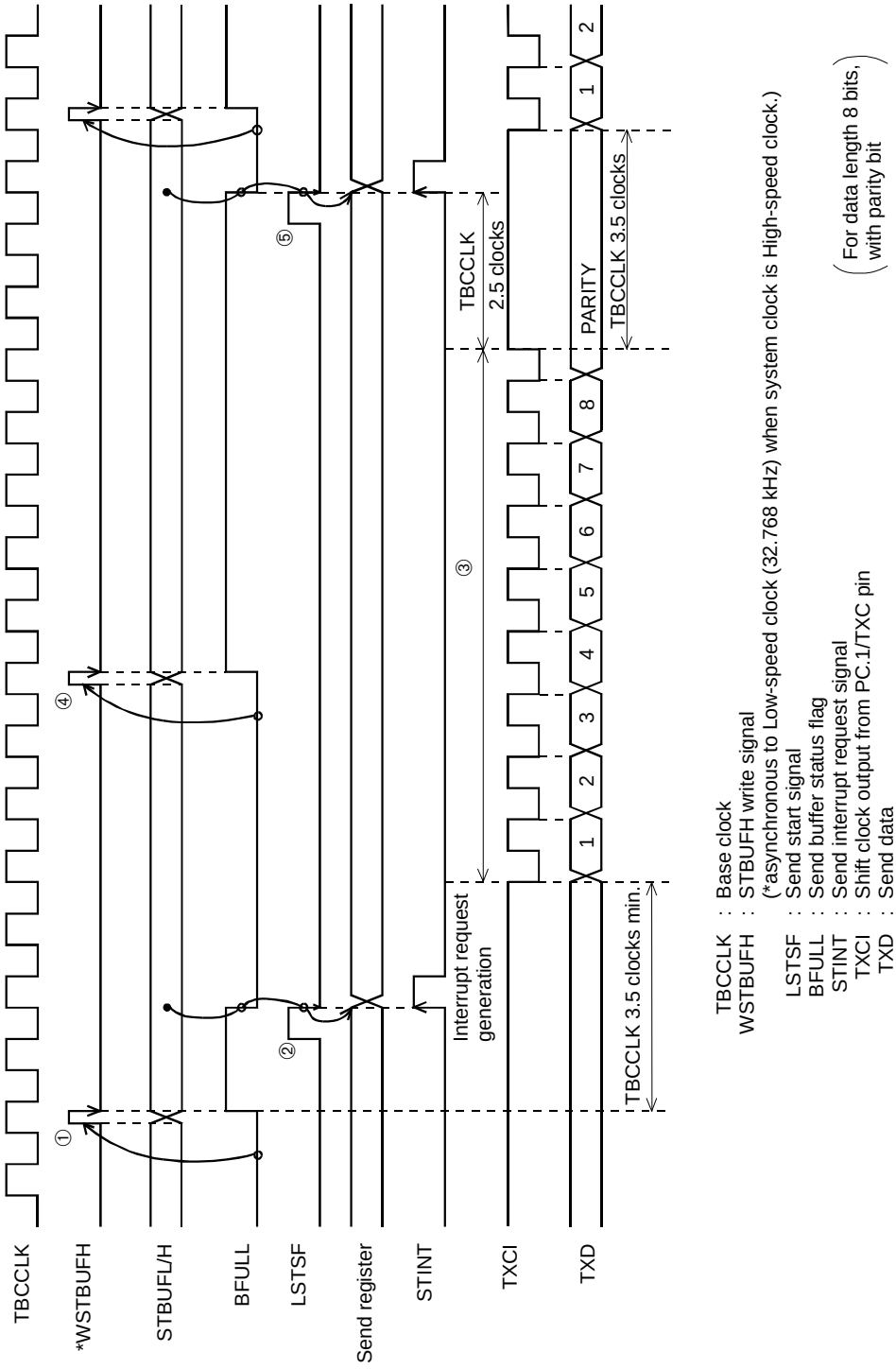


Figure 16-7 Send Timing Chart for Synchronous External Clock Mode

16.4.3 Receive operation description

(1) UART mode

The UART mode is specified by setting SRMOD (bit 0 of SRCON0) to "0". Figure 16-8 is the UART mode receive timing chart. The UART mode receive procedure is described below.

First set the receive baud rate in the receive baud rate setting register (SRBRT). Supported baud rates for UART mode receive are 1200, 2400, 4800, and 9600 bps.

Set the receive format (data bit length, parity bit, etc.) in SRCON0 and SRCON1.

① Set SREN (bit 3 of SRCON0) to "1" to enable receive.

② At the negative edge of the receive data (RXD) start bit, receive operation will start.

③ Receive operation ends.

If a framing or overrun error occurs the FERR or OERR flag of the status register (SSTAT) will be set to "1".

④ Received data is transferred to SRBUFL/H.

If a parity error occurs, the PERR flag of the status register (SSTAT) is set to "1".

⑤ The serial port receive interrupt request (SRINT) is generated.

Receive data is received until receive is disabled (SREN = "0"). When receive is ended, reset the receive enable/disable flag (SREN) to "0".

The receive data sampling clock (SRSMPL) is generated based on the TBCCLK supply, not on the high-speed clock. This allows receive operations to be executed while in the energy-saving mode.

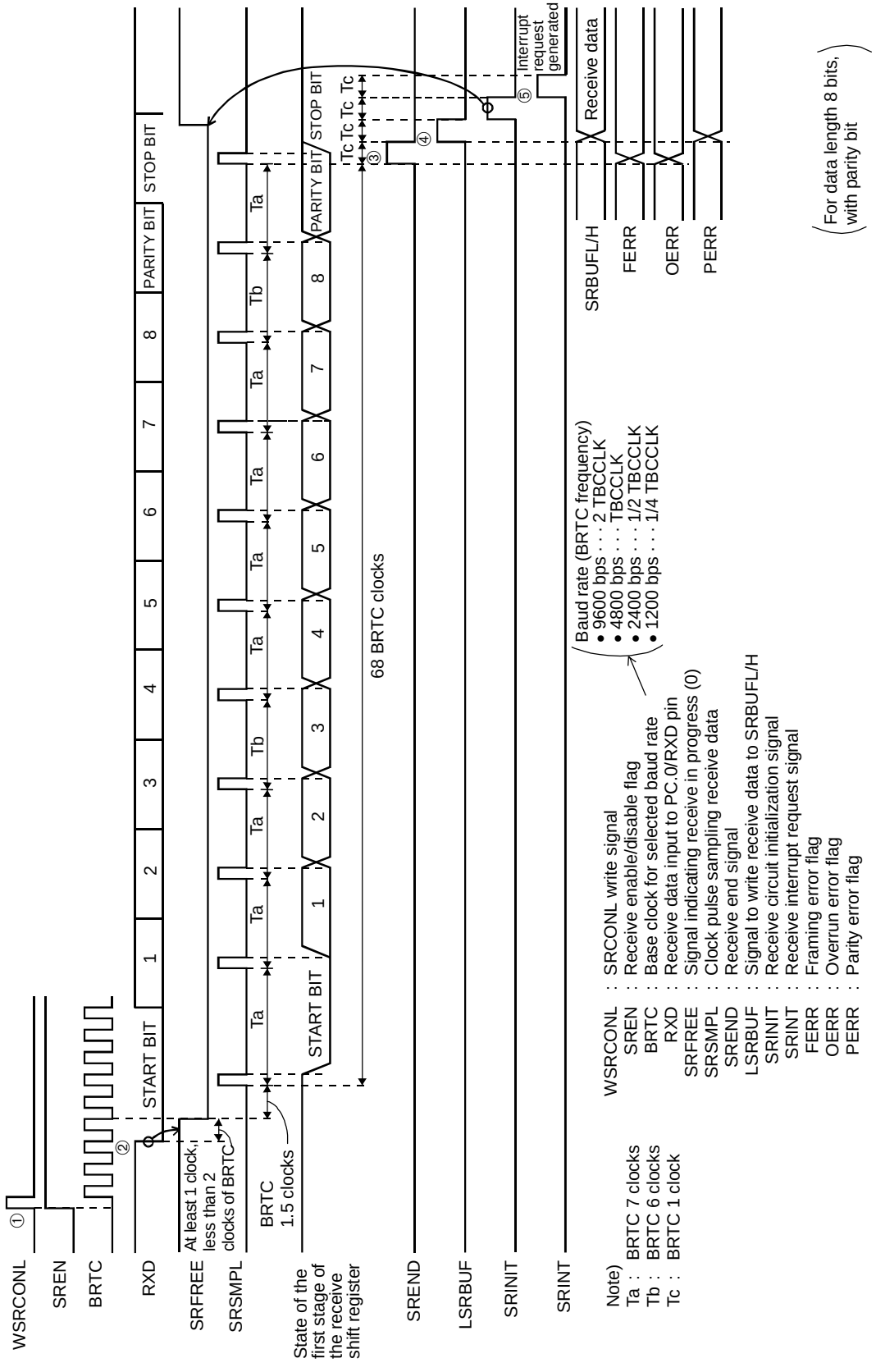


Figure 16-8 UART Mode Receive Timing Chart

(2) Synchronous internal clock mode

The synchronous internal clock mode is selected by setting SRMOD (bit 0 of SRCON0) to "1" and SRCLK (bit 0 of SRCON1) to "1".

Figure 16-9 is the receive timing chart for the synchronous internal clock mode.

The synchronous internal clock receive procedure is indicated below.

First set the receive format (data bit length, parity bit, etc.) in SRCON1 and SRCON0.

① Set SREN (bit 3 of SRCON0) to "1" (receive enable).

② 3 to 4 BRTC clock cycles later the receive shift clock (RXCO) is generated, and the receive operation starts.

(The shift clock is supplied from the PC.2/RXC pin.)

③ At the positive edge of RXCO the data received from the PC.0/RXD pin is written to the receive register.

④ Receive operation ends.

If an overrun error occurs the OERR flag in status register (SSTAT) is set to "1".

⑤ Received data is transferred to SRBUFL/H.

If a parity error occurs, the PERR flag of status register (SSTAT) is set to "1".

⑥ The serial port receive interrupt request signal (SRINT) is generated.

⑦ At the negative edge of SRINT, SREN is reset to "0".

Repeat step ① the required number of times. In the synchronous internal clock mode the receive baud rate is fixed to TBCCLK.

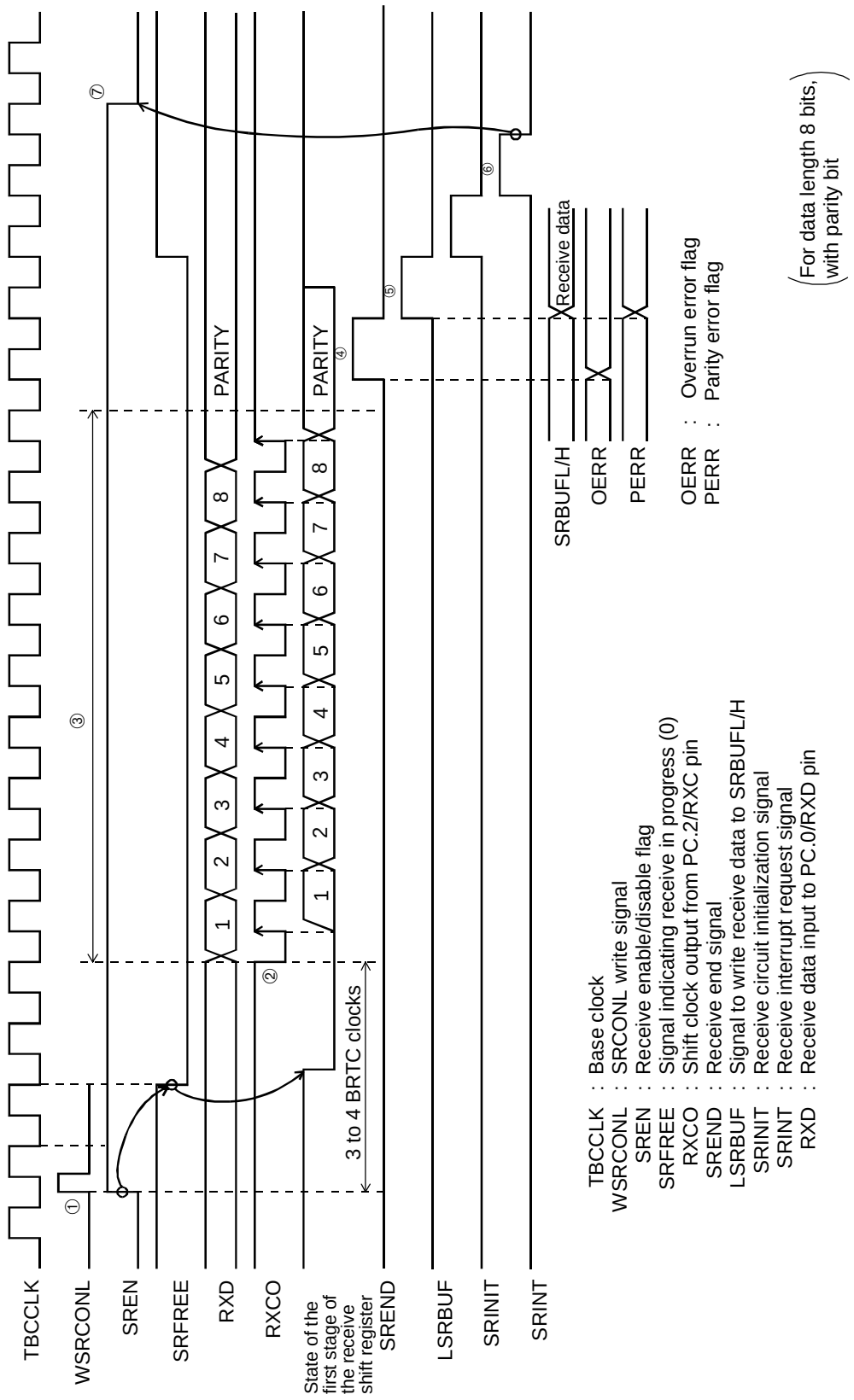


Figure 16-9 Synchronous Internal Clock Mode Receive Timing Chart

(3) Synchronous external clock mode

The synchronous external clock mode is selected by setting SRMOD (bit 0 of SRCON0) to "1" and SRCLK (bit 0 of SRCON1) to "0".

Figure 16-10 is the receive timing chart for the synchronous external clock mode.

The synchronous external clock receive procedure is indicated below.

First set the receive format (data bit length, parity bit, etc.) in SRCON1 and SRCON0.

① Set SREN (bit 3 of SRCON0) to "1" (receive enable).

② At the positive edge of the receive shift clock input through PC.2/RXC pin, the receive data from PC.0/RXD pin is written to the receive register.

③ Receive operation ends.

If an overrun error occurs the OERR flag in status register (SSTAT) is set to "1".

④ Received data is transferred to SRBUFL/H.

If a parity error occurs, the PERR flag of status register (SSTAT) is set to "1".

⑤ The serial port receive interrupt request signal (SRINT) is generated.

⑥ At the negative edge of SRINT, SREN is reset to "0".

Repeat step ① the required number of times.

In the synchronous external clock mode the receive baud rate is determined by the external clock (RXCI). Allow at least five clocks (approx. 153 µs) of TBCCLK between the time the receive is enabled (SREN = "1") and the time the external clock (RXCI) is input.

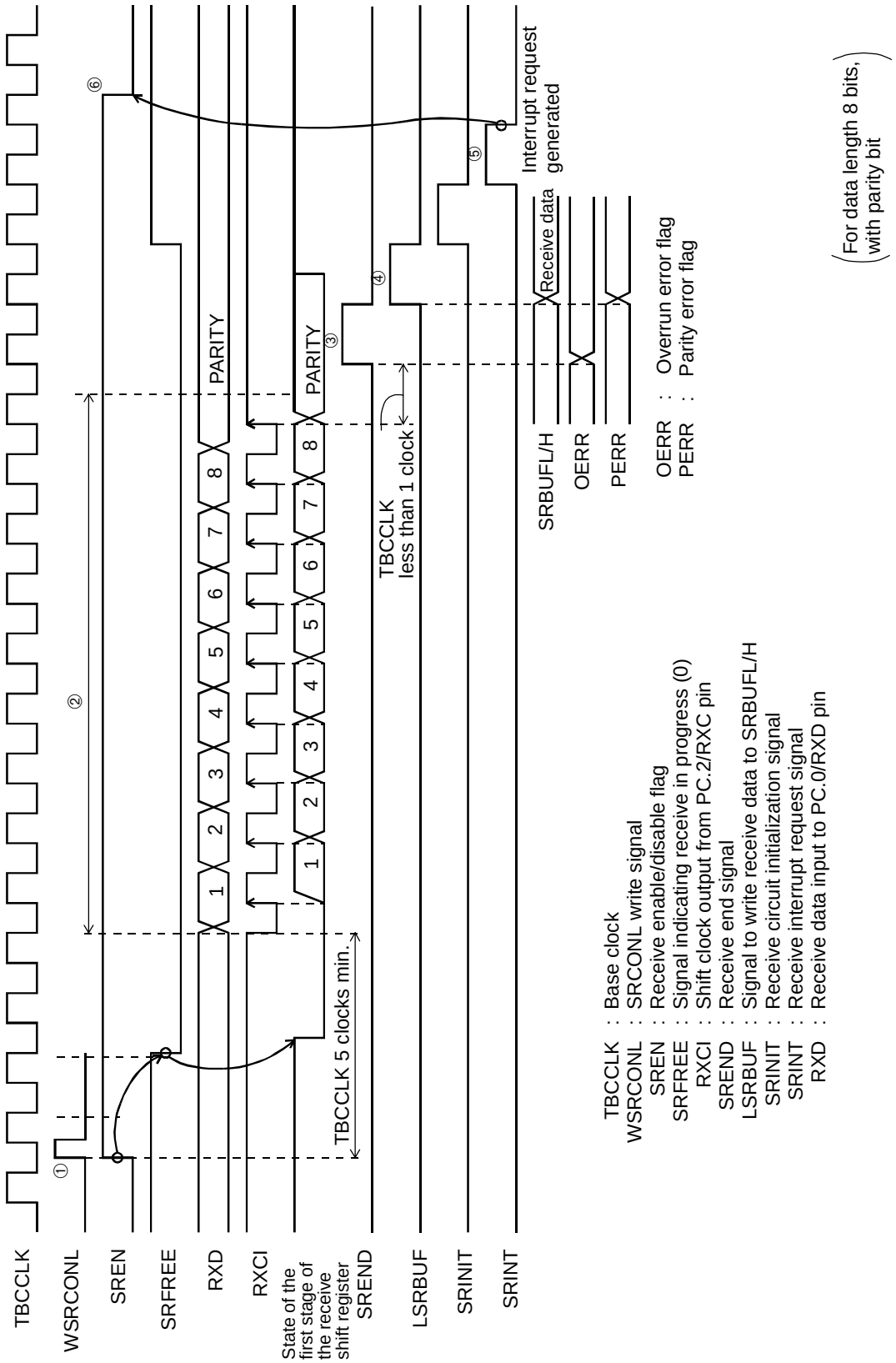


Figure 16-10 Synchronous External Clock Mode Receive Timing Chart

16.5 Send/Receive Data LSB/MSB First Select

Either LSB first or MSB first can be selected for send data by setting STLMB (bit 3 of STCON1).

Either LSB first or MSB first can be selected for receive data by setting SRLMB (bit 3 of SRCON1).

16.5.1 Selecting send data LSB/MSB first

Set STLMB (bit 3 of STCON1) to "0" to select LSB first for send.

The correspondence between LSB first send data and the send buffer register bit is shown in Figure 16-11. In this case, the LSB is TB0 (bit 0 of STBUFL).

Set STLMB to "1" to send the MSB first.

The correspondence between MSB first send data and the send buffer register bit is shown in Figure 16-12. In this case, the MSB is TB7 (bit 3 of STBUFH).

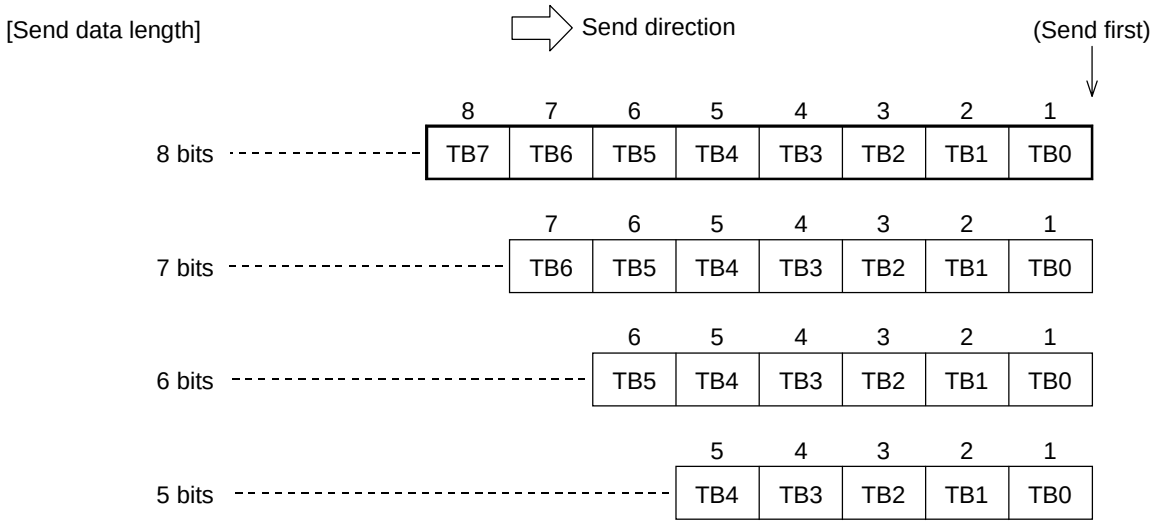


Figure 16-11 Correspondence Between LSB First Send Data and Send Buffer Register

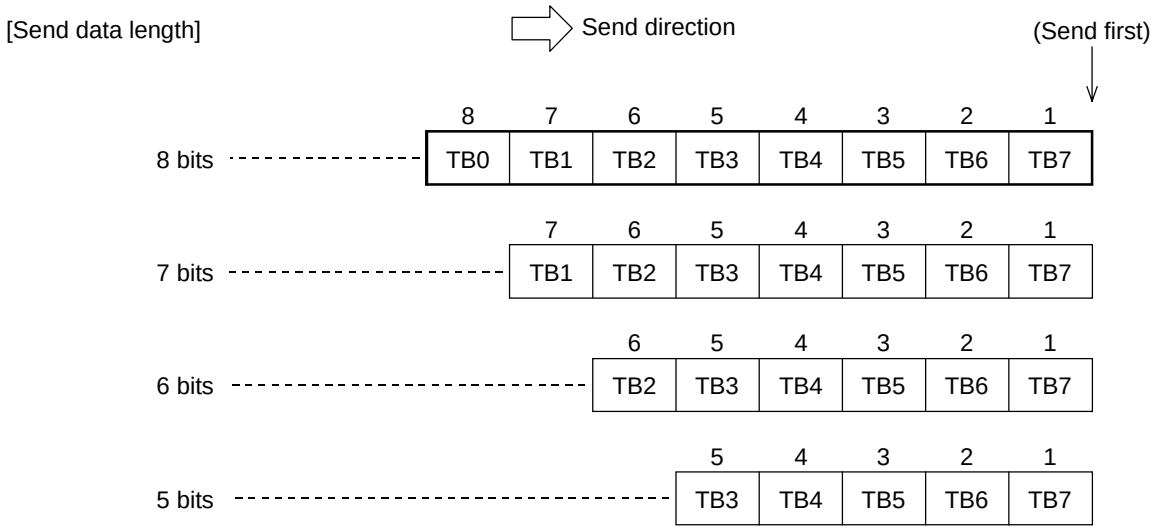


Figure 16-12 Correspondence Between MSB First Send Data and Send Buffer Register

16.5.2 Selecting receive data LSB/MSB first

When the LSB is first in receive data, set SRLMB (bit 3 of SRCON1) to "0".

If the MSB is first, set SRLMB to "1".

The correspondence between receive data and SRBUFL/H bits for LSB first receive is shown in Figure 16-13, and for MSB first receive in Figure 16-14.

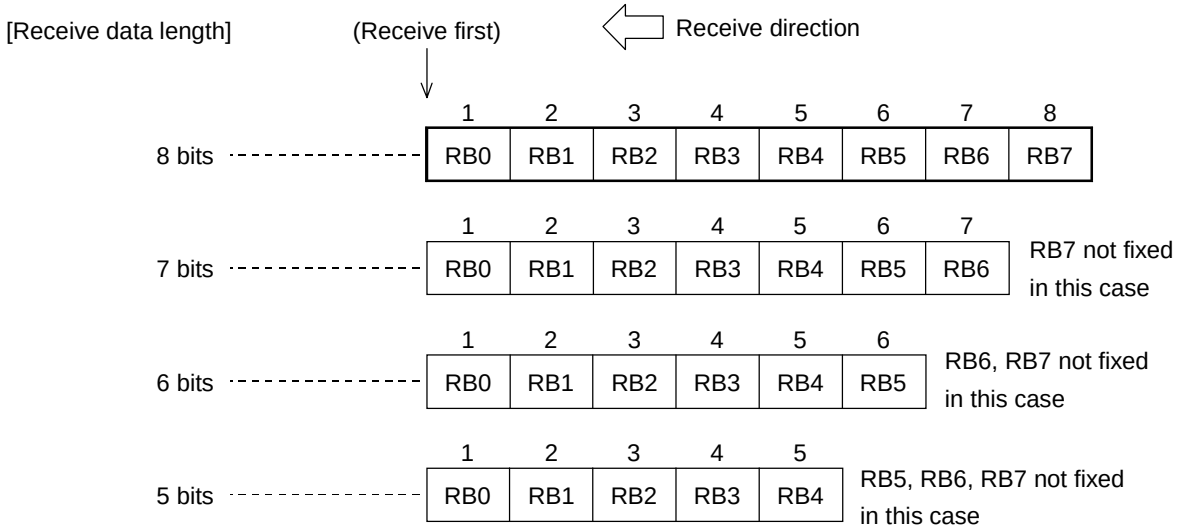


Figure 16-13 Correspondence Between LSB First Receive Data and Receive Buffer Register

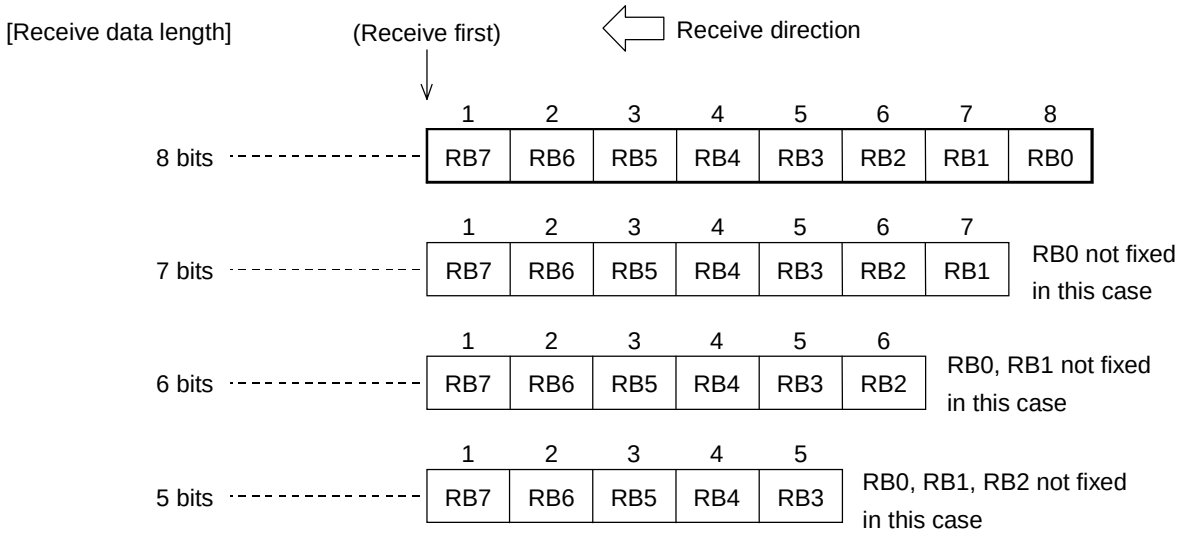


Figure 16-14 Correspondence Between MSB First Receive Data and Receive Buffer Register

Chapter 17

Shift Register (SFT)

Chapter 17 Shift Register (SFT)

17.1 Overview

The MSM63184A has one internal 8-bit shift register channel for clock synchronous communication.

The shift register is synchronized with the clock specified by the shift register control register 0 (SFTCON0), and can handle 8-bit data send and receive simultaneously. When 8-bit data transfer is completed, a shift register interrupt is requested.

17.2 Shift Register Configuration

The shift register configuration is shown in Figure 17-1.

PE.0/SIN, PE.1/SOUT and PE.2/SCLK are the shift data input pin, the shift data output pin and the shift clock input/output pin respectively. Set the secondary function by using port control register.

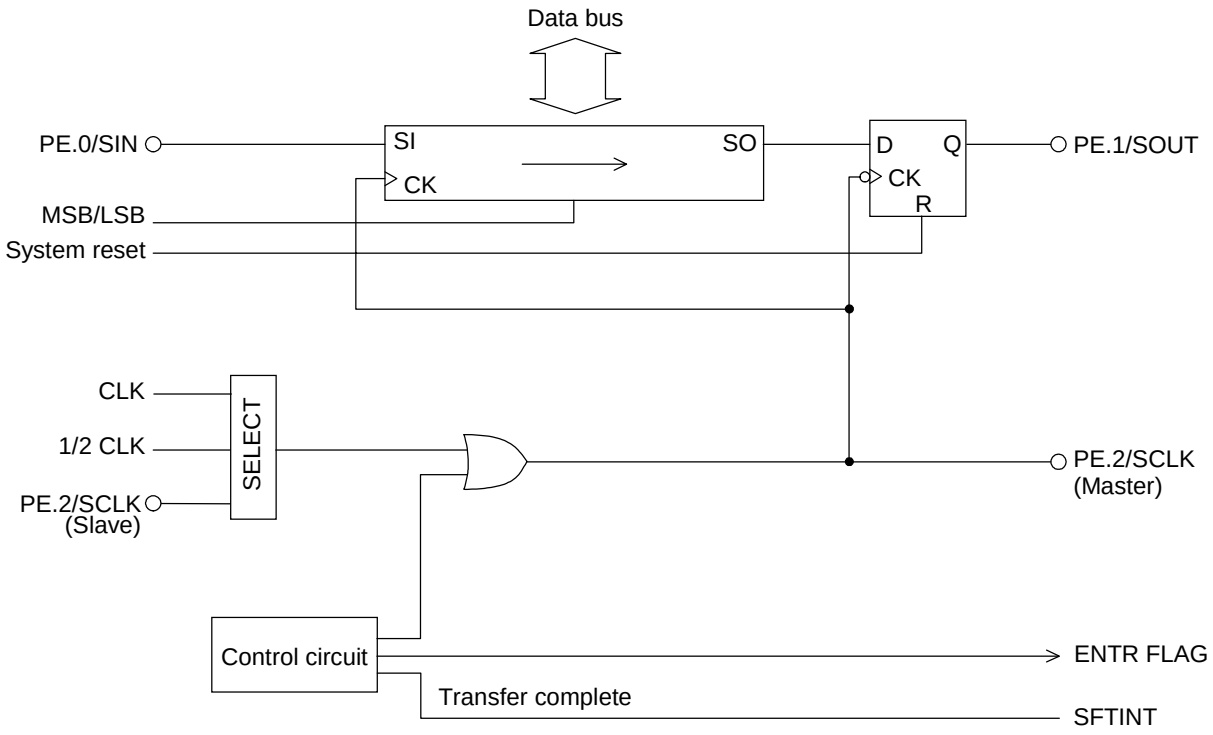


Figure 17-1 Shift Register Configuration

17.3 Shift Register Operation

The shift register can be set to master or slave mode, and to MSB first or LSB first. The send data is written to the shift register (SFTRL, SFTRH), and transfer is started by setting bit 0 (ENTR) of the shift control register 1 (SFTCON1) to "1". After 8-bit data transfer (send/receive), operation ends.

Bits 1 and 0 (SELCK1, SELCK0) of the shift control register 0 (SFTCON0) can set the shift clock to CLK or 1/2 CLK. This operation is master mode and the shift clock is output to the PE.2/SCLK pin.

When the shift clock is set to external clock, the system operates in slave mode, and operation is to the clock input through the PE.2/SCLK pin. If 9 or more clocks are input consecutively, the ninth and following clocks are ignored.

In both master and slave modes, the shift register is synchronized to the shift clock falling edge, and shift out data is output from the first bit through the PE.1/SOUT pin. In synchronization with the shift clock rising edge, shift in data is input from the first bit through the PE.0/SIN pin.

For external devices, shift in data changes on the falling edge of the shift clock, and shift out data changes on the rising edge of the shift clock.

When 8-bit data transfer is complete, bit 0 (ENTR) of SFTCON1 is reset to "0". When transfer is completed, the interrupt request signal (SFTINT) is generated (see Figure 17-2).

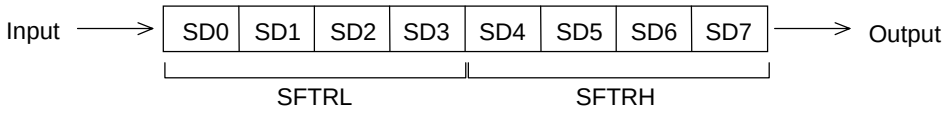
At system reset and between transfers (from the end of one 8-bit transfer until the next transfer starts), the output pin state is as indicated in Table 17-1 (when set to the output secondary function).

Table 17-1 Output Pin States

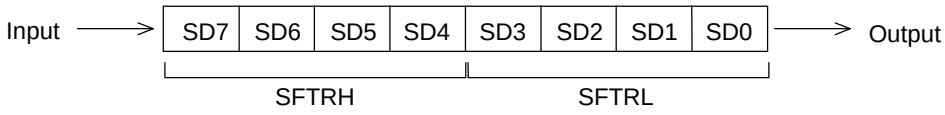
Pin name	At system reset	Between transfers
PE.2/SCLK	"H"	"H"
PE.1/SOUT	"L"	Last transfer data for first transfer

MSB/LSB first is set by bit 2 (SDIR) of SFTCON0.

- SDIR = 0 : MSB first mode



- SDIR = 1 : LSB first mode



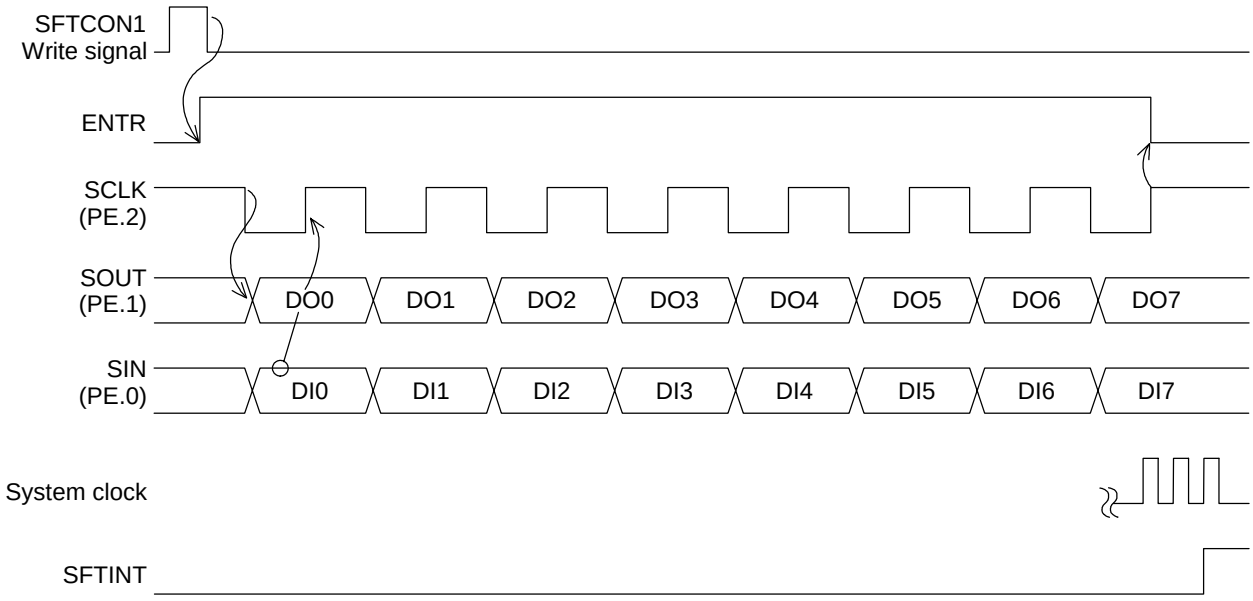


Figure 17-2 Shift Register Operation Timing

Note:

In the slave mode the ENTR bit setting should be done when the PE.2/SCLK pin is high.
If SFTRL/SFTRH are written during transfer, the transfer data (send and receive) is overwritten. In this case, terminate the transfer and start over.
Even when receiving only, transfer begins with setting the ENTR bit.

17.4 Registers

(1) Shift register L/H (SFTRL, SFTRH)

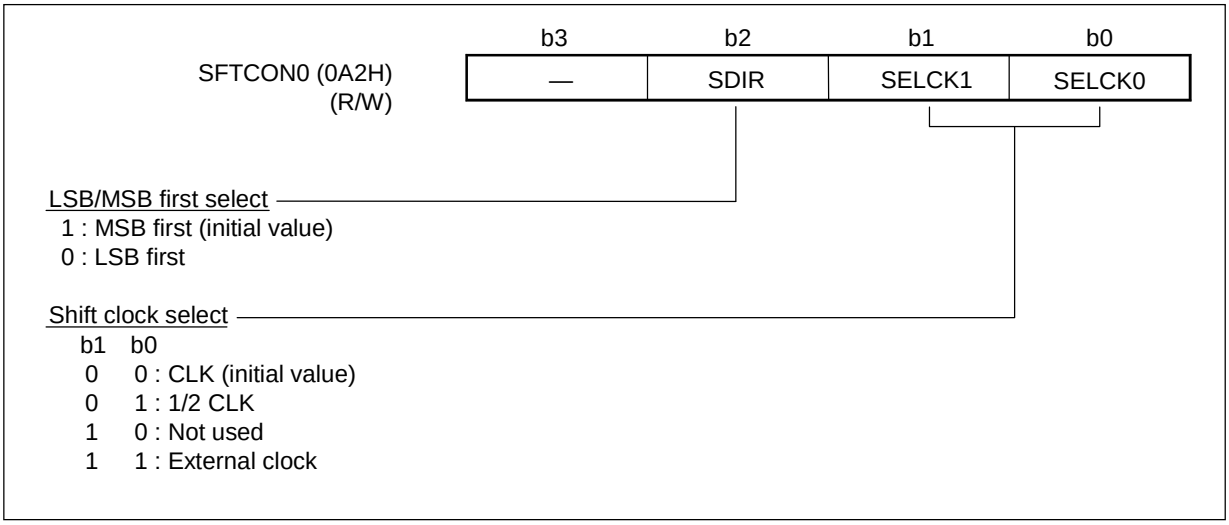
SFTRL and SFTRH are 4-bit special function registers (SFRs) used to write shift register send data and read receive data.

	b3	b2	b1	b0
SFTRL (0A0H) (R/W)	SD3	SD2	SD1	SD0
SFTRH (0A1H) (R/W)	SD7	SD6	SD5	SD4

SFTRL and SFTRH are reset to "0" at system reset.

(2) Shift register control registers (SFTCON0, SFTCON1)

SFTCON0 and SFTCON1 are 4-bit special function registers (SFRs) that control shift register operation. At system reset both are initialized to 0.

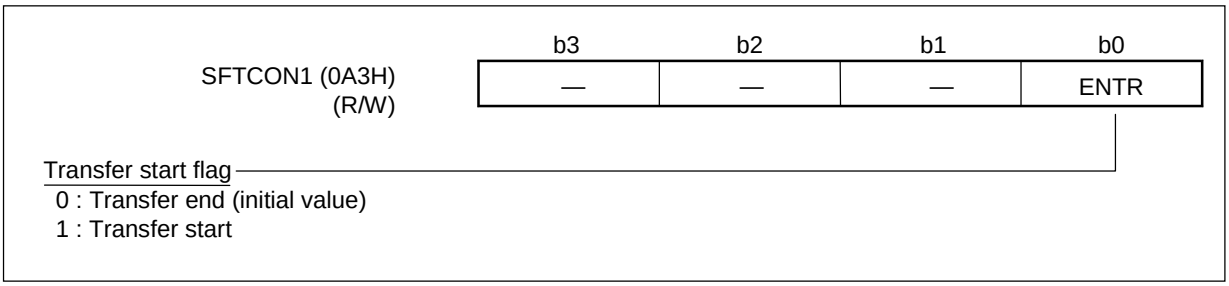


Bits 1, 0: SELCK1, SELCK0

These bits select the shift clock. If set to CLK or 1/2 CLK the system operates in master mode. If set to external clock the system operates in slave mode.

Bit 2: SDIR

This bit selects the transfer order for 8-bit send/receive data. When the SDIR bit is "0" it means MSB first, and when "1", LSB first.



Bit 0: ENTR

When ENTR is set to "1", transfer starts, and when 8-bit transfer ends, it is automatically reset.

17.5 Shift Register Application Example

An example of shift register set for clock synchronous communication is described below.

(1) Set the supported port modes (secondary function).

Port control register	Master mode	
PEMOD	Bit 2 = "1"	(PE.2/SCLK)
	Bit 1 = "1"	(PE.1/SOUT)
	Bit 0 = "1"	(PE.0/SIN)

(2) Select the shift clock with SFTCON0 bits 1 and 0 (SELCK1, SELCK0).

(3) Select MSB/LSB first with SFTCON0 bit 2 (SDIR). ("1" for MSB first, "0" for LSB first).

(4) Set the interrupt enable register 3 (IE3) bit 2 (ESFT) to "1".

(5) Set the master interrupt enable flag (MIE) to "1", and enable all interrupts.

(6) Write send data to the shift register L/H (SFTRL, SFTRH).

(7) Set bit 0 (ENTR) of SFTCON1 to "1", and begin the transfer.

With the above settings the shift register begins to operate, and the CPU receives the shift register interrupt. When 8-bit transfer is complete, checks can be made by the interrupt and by monitoring the ENTR bit.

Chapter 18

LCD Driver (LCD)

Chapter 18 LCD Driver (LCD)

18.1 Overview

The MSM63180 family products have an internal dot matrix LCD driver with 16 common outputs. The MSM63182A has 32 segment outputs and can drive up to 512 (32 × 16) dots. The MSM63184A has 40 segment outputs and can drive up to 640 (40 × 16) dots. The MSM63188A has 64 segment outputs and can drive up to 1024 (64 × 16) dots. This LCD driver can be software-selected to all off, all on or power down mode. The driver provides 1/4 or 1/5 bias, selectable duty from 1/1 to 1/16, and adjustable (16-tone) contrast.

18.2 LCD Driver Configuration

The MSM63188A LCD driver configuration is shown in Figure 18-1.

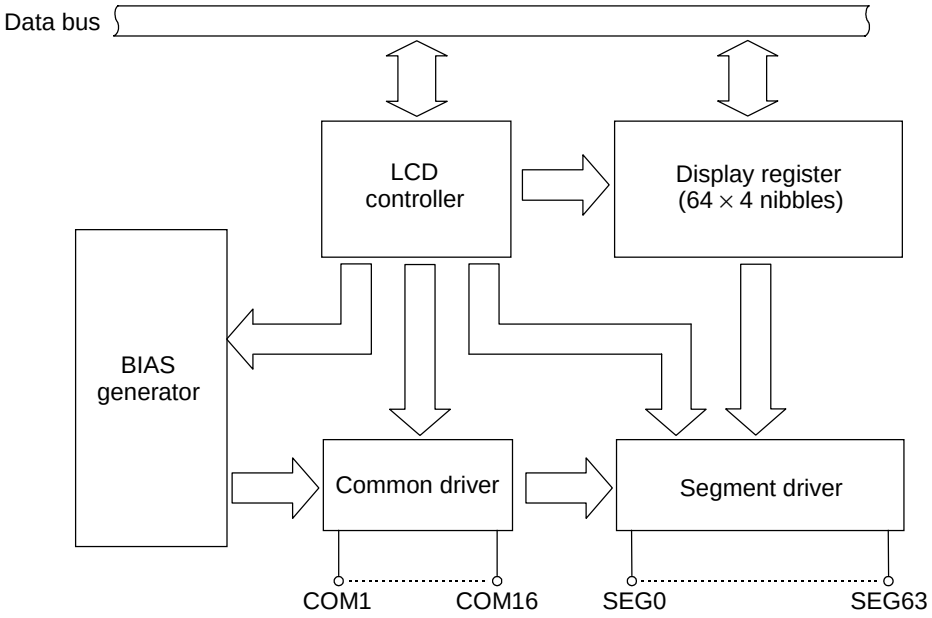


Figure 18-1 MSM63188A LCD Driver Configuration

18.3 LCD Driver Operation

The display control register 1 (DSPCON1) selects the duty from 1/1 to 1/16. The frame frequency for each duty ratio is indicated in Table 18-1. Depending on the duty selected, the common signal (COM1–COM16) is generated, and data written in synchronization with that common signal to the display registers (DSPR0–255) is output to the segment driver. The segment driver uses bits 0 and 1 (LCDON, ALLON) of the display control register 0 (DSPCON0) to control all off or all on modes.

When bit 2 (PDWN) of the display control register 0 (DSPCON0) is set to "1", the power down mode is enabled. In this mode the bias generation circuit operation stops, and COM1–16 and SEG0–63 pins are all output at the V_{SS} level to reduce supply current.

BISEL (bit 3 of DSPCON0) selects 1/4 or 1/5 bias.

DSPCNT controls the LCD contrast of 16 tones (V_{DDH} = 2.4 V or more).

When the LCD driver is not used, select the power-down mode and reset all the bits of the display control register (DSPCNT) to "0" to decrease supply current.

Table 18-1 Frame Frequency for Each Duty

DSPCON1					Duty	Frame frequency
DT3–0	DT3	DT2	DT1	DTO		
0H	0	0	0	0	1/16	64 Hz
1H	0	0	0	1	1/1	1024 Hz
2H	0	0	1	0	1/2	512 Hz
3H	0	0	1	1	1/3	About 341 Hz
4H	0	1	0	0	1/4	256 Hz
5H	0	1	0	1	1/5	About 205 Hz
6H	0	1	1	0	1/6	About 171 Hz
7H	0	1	1	1	1/7	About 146 Hz
8H	1	0	0	0	1/8	128 Hz
9H	1	0	0	1	1/9	About 114 Hz
0AH	1	0	1	0	1/10	About 102 Hz
0BH	1	0	1	1	1/11	About 93 Hz
0CH	1	1	0	0	1/12	About 85 Hz
0DH	1	1	0	1	1/13	About 79 Hz
0EH	1	1	1	0	1/14	About 73 Hz
0FH	1	1	1	1	1/15	About 68 Hz

18.4 Bias Generator (BIAS)

The bias generator lowers the voltage (V_{DD2}) generated in the voltage regulator circuit with an external capacitor connected to pins C1 and C2 to generate V_{DD1} to V_{DD5} bias voltages for the LCD driver.

The power down mode stops the voltage lowering/raising operation of the bias generation circuit in order to reduce supply current.

Figure 18-2 shows the bias generator configuration for 1/5 bias, and Figure 18-3 shows the configuration for 1/4 bias. For details of the backup circuit and the voltage regulator circuit, see Chapter 21, "Backup Circuit".

Tables 18-2 and 18-3 show the table of display contrast adjusting voltages.

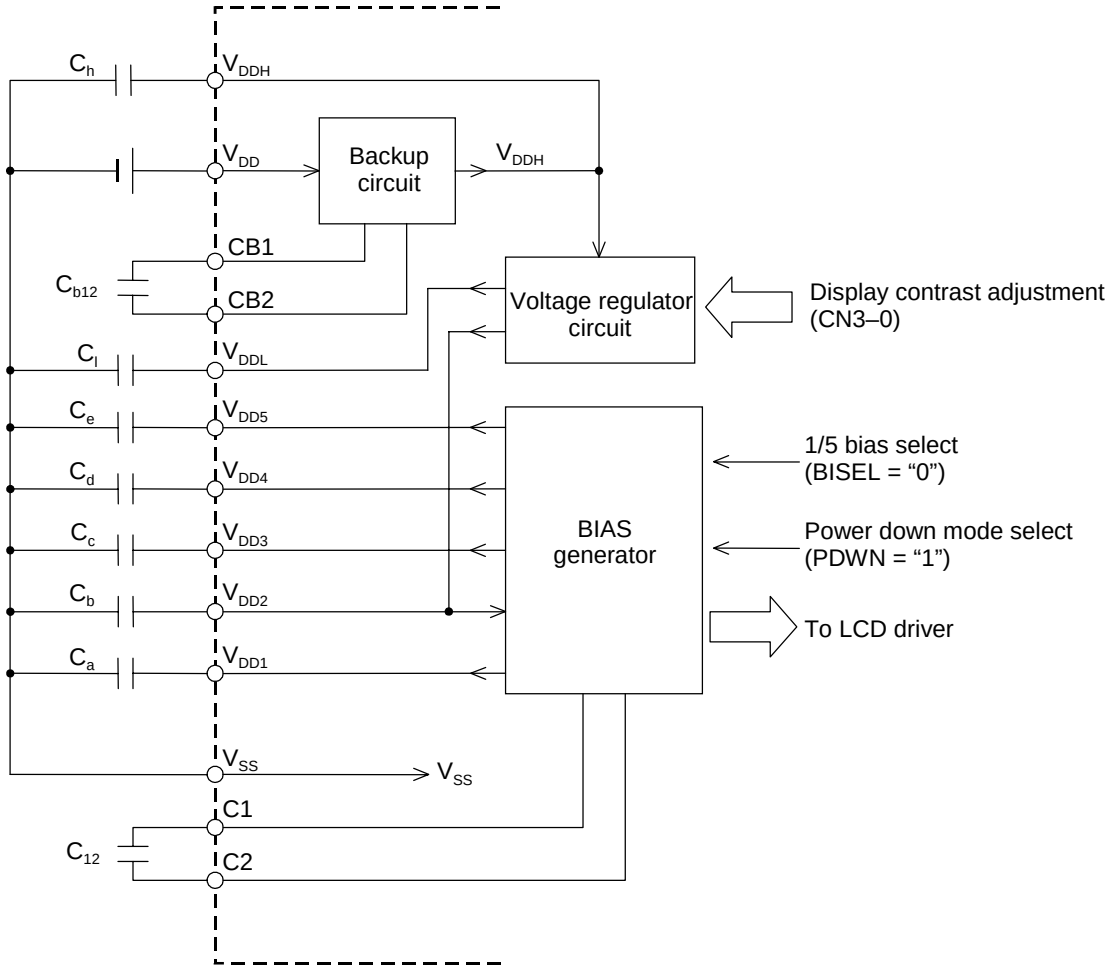


Figure 18-2 Bias Generator Configuration for 1/5 Bias

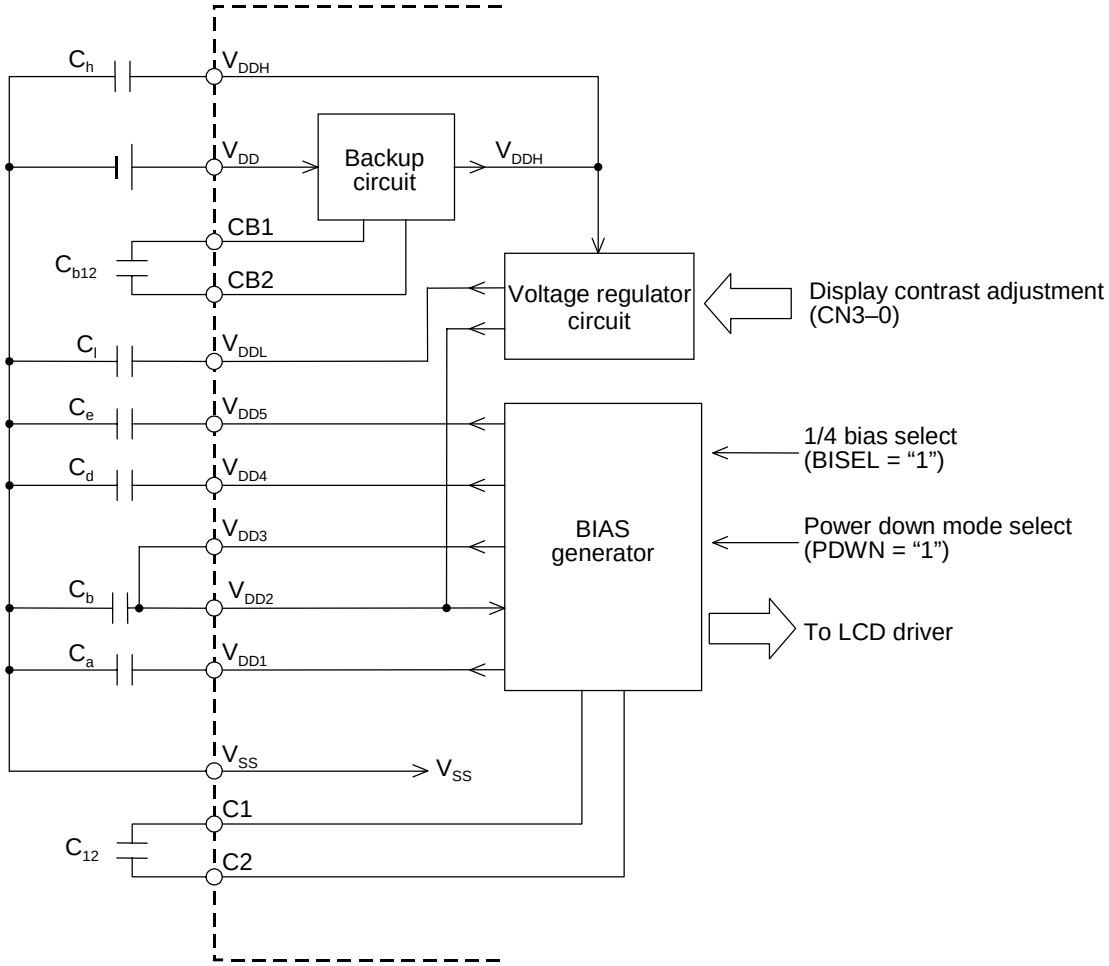


Figure 18-3 Bias Generator Configuration for 1/4 Bias

Table 18-2 Display Contrast Adjusting Voltages (V_{DD2})

(Ta = 25°C, V_{SS} = 0 V)

DSPCNT					V_{DD2} Voltage (V)			Contrast
CN3–0	CN3	CN2	CN1	CN0	Min.	Typ.	Max.	
0H	0	0	0	0	1.60	1.80	2.00	Light
1H	0	0	0	1	1.64	1.84	2.04	
2H	0	0	1	0	1.68	1.88	2.08	
3H	0	0	1	1	1.72	1.92	2.12	
4H	0	1	0	0	1.76	1.96	2.16	
5H	0	1	0	1	1.80	2.00	2.20	
6H	0	1	1	0	1.84	2.04	2.24	
7H	0	1	1	1	1.88	2.08	2.28	
8H	1	0	0	0	1.92	2.12	2.32	
9H	1	0	0	1	1.96	2.16	2.36	
0AH	1	0	1	0	2.00	2.20	2.40	
0BH	1	0	1	1	2.04	2.24	2.44	
0CH	1	1	0	0	2.08	2.28	2.48	
0DH	1	1	0	1	2.12	2.32	2.52	
0EH	1	1	1	0	2.16	2.36	2.56	
0FH	1	1	1	1	2.20	2.40	2.60	Dark

Table 18-3 Display Contrast Adjusting Voltages (V_{DD1}, V_{DD3}, V_{DD4}, and V_{DD5})

(V_{SS} = 0 V)

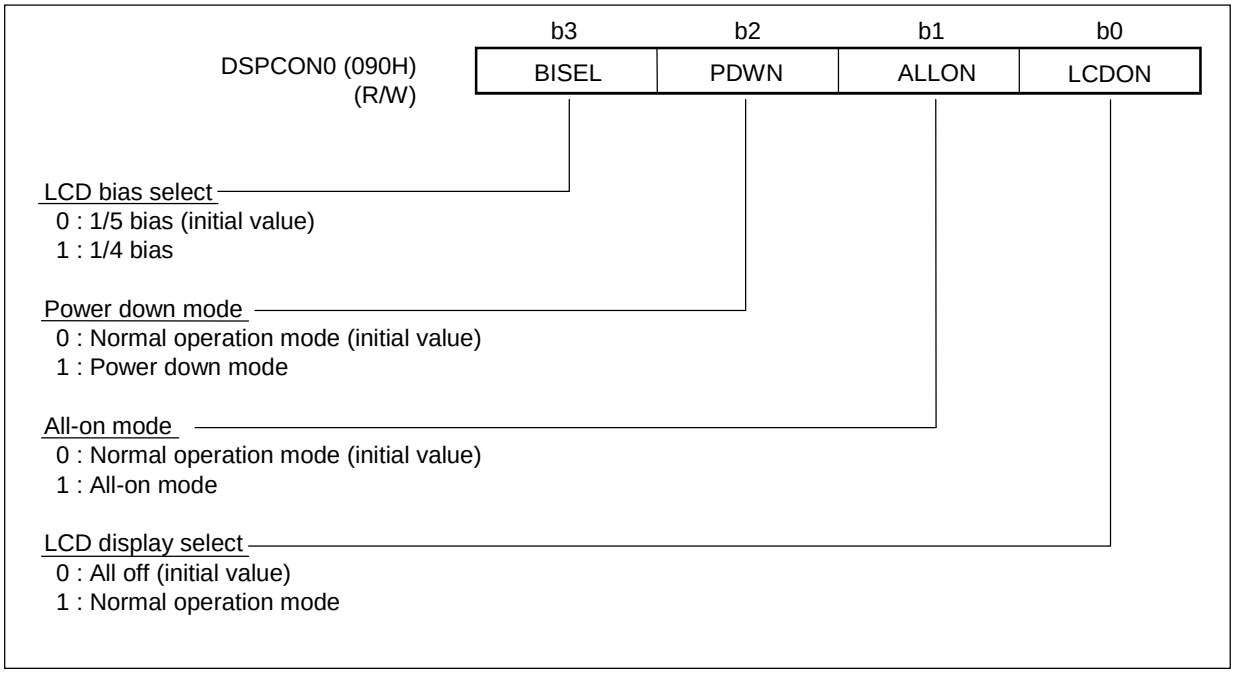
BISEL	Mode	Power supply name	Voltage (V)		
			Min.	Typ.	Max.
0	1/5 bias	V_{DD1}	Typ. – 0.2	$1/2 \times V_{DD2}$*	Typ. + 0.2
		V_{DD3}	Typ. – 0.3	$3/2 \times V_{DD2}$*	Typ. + 0.3
		V_{DD4}	Typ. – 0.4	$2 \times V_{DD2}$*	Typ. + 0.4
		V_{DD5}	Typ. – 0.5	$5/2 \times V_{DD2}$*	Typ. + 0.5
1	1/4 bias	V_{DD1}	Typ. – 0.2	$1/2 \times V_{DD2}$*	Typ. + 0.2
		V_{DD3}	Typ. – 0.2	V_{DD2}*	Typ. + 0.2
		V_{DD4}	Typ. – 0.3	$3/2 \times V_{DD2}$*	Typ. + 0.3
		V_{DD5}	Typ. – 0.4	$2 \times V_{DD2}$*	Typ. + 0.3

V_{DD2}*: Typical V_{DD2} value in Table 18-2

18.5 LCD Driver Registers

(1) Display control register 0 (DSPCON0)

DSPCON0 is a 4-bit special function register controlling LCD driver operation.



Bit 3: BISEL

This bit selects 1/4 or 1/5 bias. At system reset it is "0", selecting 1/5 bias.

Bit 2: PDWN

This bit selects the power down mode. When this bit is set to "1", the bias generation circuit stops its voltage lowering/raising operation and pins COM1–16 and SEG0–63 are all set to the V_{SS} level, reducing supply current. At system reset it is cleared to "0".

Bit 1: ALLON

When ALLON is set to "1" all segment drivers are turned on. The ALLON bit has priority over the LCDON bit. At system reset it is cleared to "0".

Bit 0: LCDON

When the LCDON bit is set to "1", the display data in the display register is output to the segment drivers. At system reset it is cleared to "0", and all segment drivers are turned off.

(2) Display control register 1 (DSPCON1)

DSPCON1 is a 4-bit special function register (SFR) used to select the LCD driver duty. At system reset, each bit of DSPCON1 is initialized to "0".

DSPCON1 (091H) (R/W)

b3	b2	b1	b0
DT3	DT2	DT1	DT0

Duty select

b3	b2	b1	b0	
0	0	0	0	: 1/16 duty (initial value)
0	0	0	1	: 1/1 duty
0	0	1	0	: 1/2 duty
0	0	1	1	: 1/3 duty
0	1	0	0	: 1/4 duty
0	1	0	1	: 1/5 duty
0	1	1	0	: 1/6 duty
0	1	1	1	: 1/7 duty
1	0	0	0	: 1/8 duty
1	0	0	1	: 1/9 duty
1	0	1	0	: 1/10 duty
1	0	1	1	: 1/11 duty
1	1	0	0	: 1/12 duty
1	1	0	1	: 1/13 duty
1	1	1	0	: 1/14 duty
1	1	1	1	: 1/15 duty

(3) Display contrast register (DSPCNT)

DSPCNT is a 4-bit special function register (SFR) used to adjust display contrast. At system reset, each bit of DSPCNT is initialized to "0".

DSPCNT (092H) (R/W)

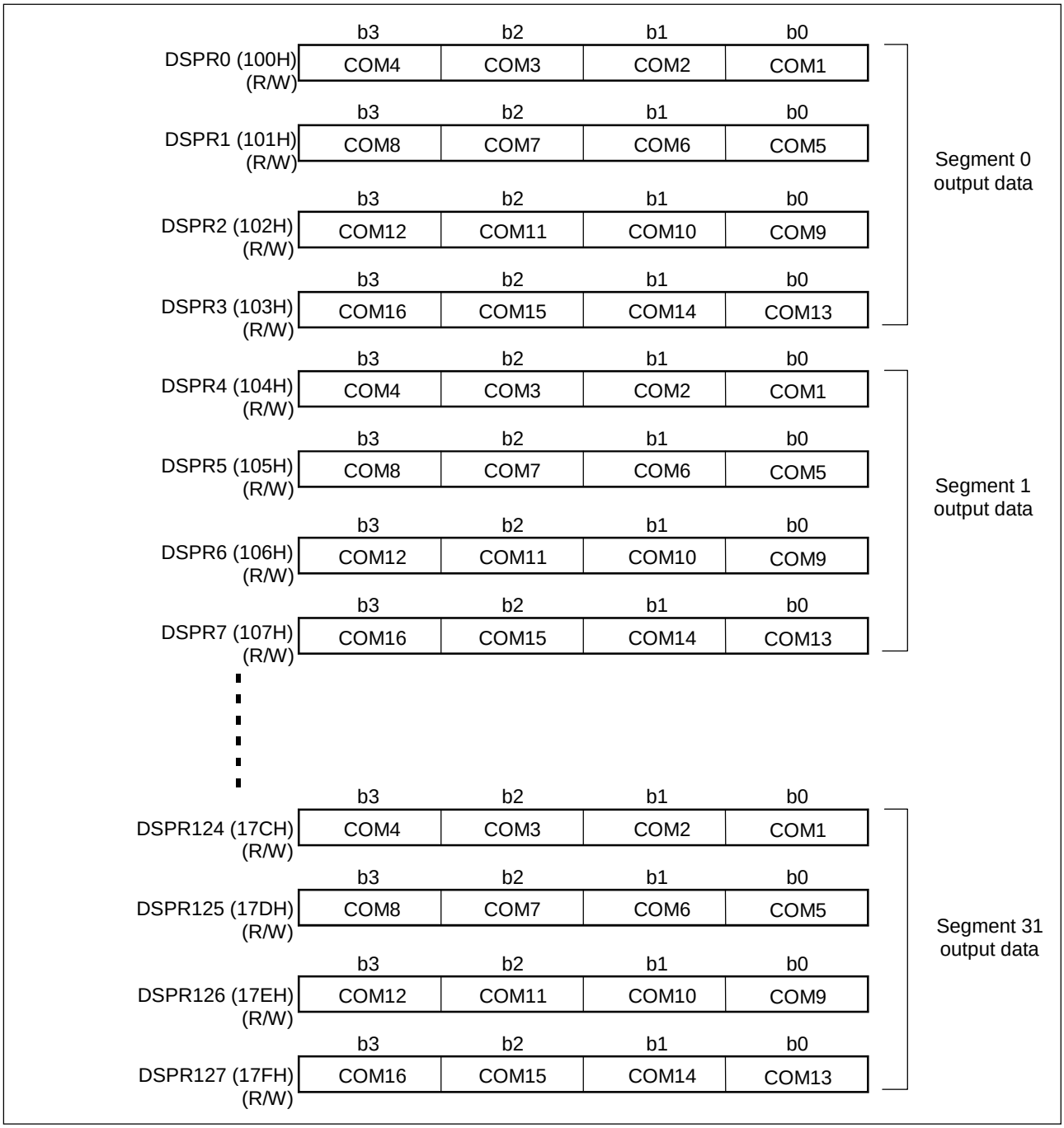
b3	b2	b1	b0
CN3	CN2	CN1	CN0

Contrast select

b3	b2	b1	b0	
0	0	0	0	: Light (initial value)
0	0	0	1	:
0	0	1	0	:
0	0	1	1	:
0	1	0	0	:
0	1	0	1	:
0	1	1	0	:
0	1	1	1	:
1	0	0	0	:
1	0	0	1	:
1	0	1	0	:
1	0	1	1	:
1	1	0	0	:
1	1	0	1	:
1	1	1	0	:
1	1	1	1	: Dark

(4) MSM63182A Display register (DSPR0–127)

DSPR0–127 are segment output data registers for the dot matrix LCD driver allocated to BANK 1. The correspondence between display registers and segment outputs is shown below.

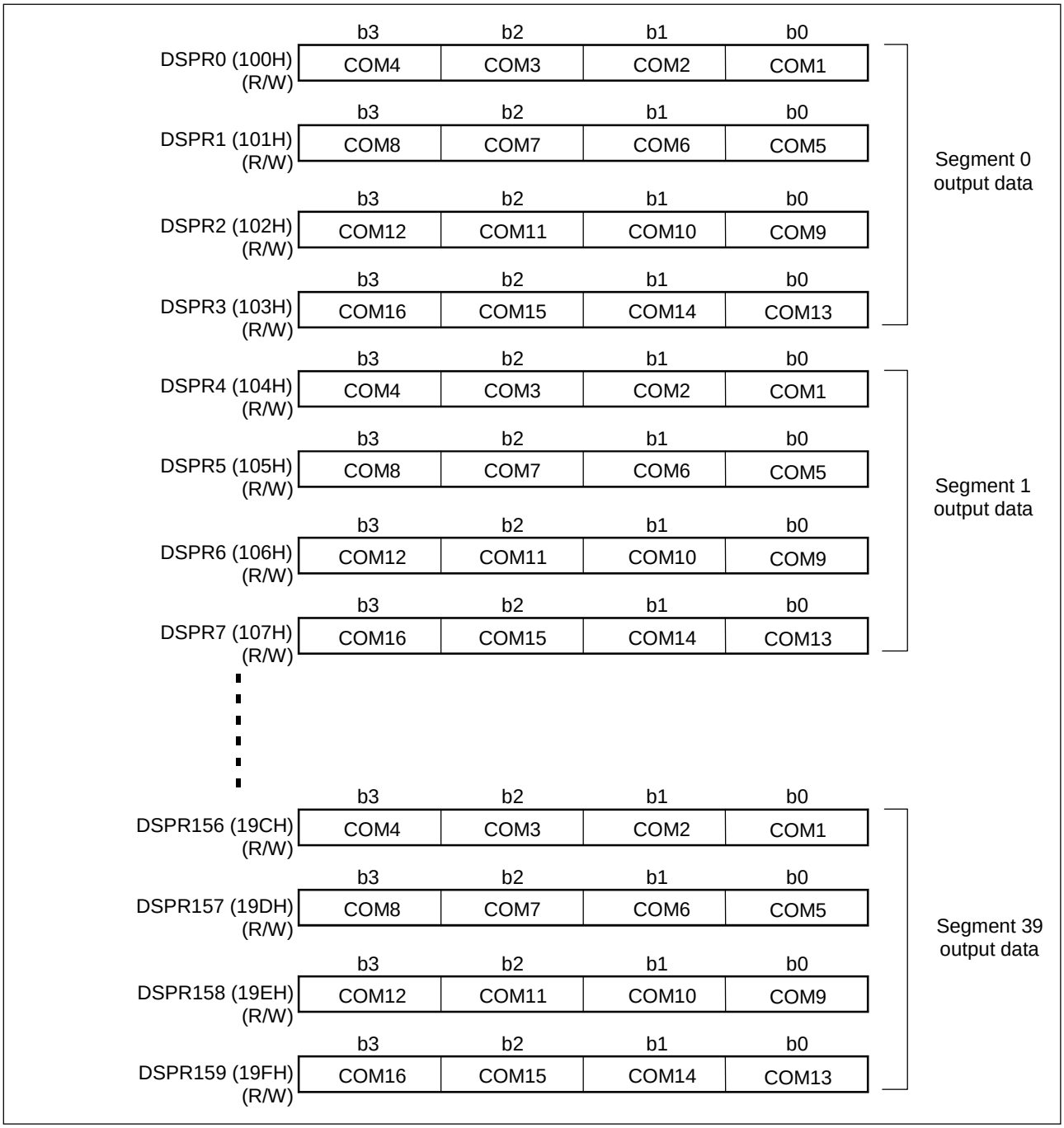


Notes:

- When a display register bit is set to "1", the corresponding LCD dot lights. When reset to "0" it goes off.
- To keep stable display state, each individual LCD dot should be set to ON/OFF with bit operation instructions.
- At system reset the display registers (DSPR0 to DSPR127) are undefined and should be initialized.

(5) MSM63184 Display register (DSPR0–159)

DSPR0–159 are segment output data registers for the dot matrix LCD driver allocated to BANK 1. The correspondence between display registers and segment outputs is shown below.

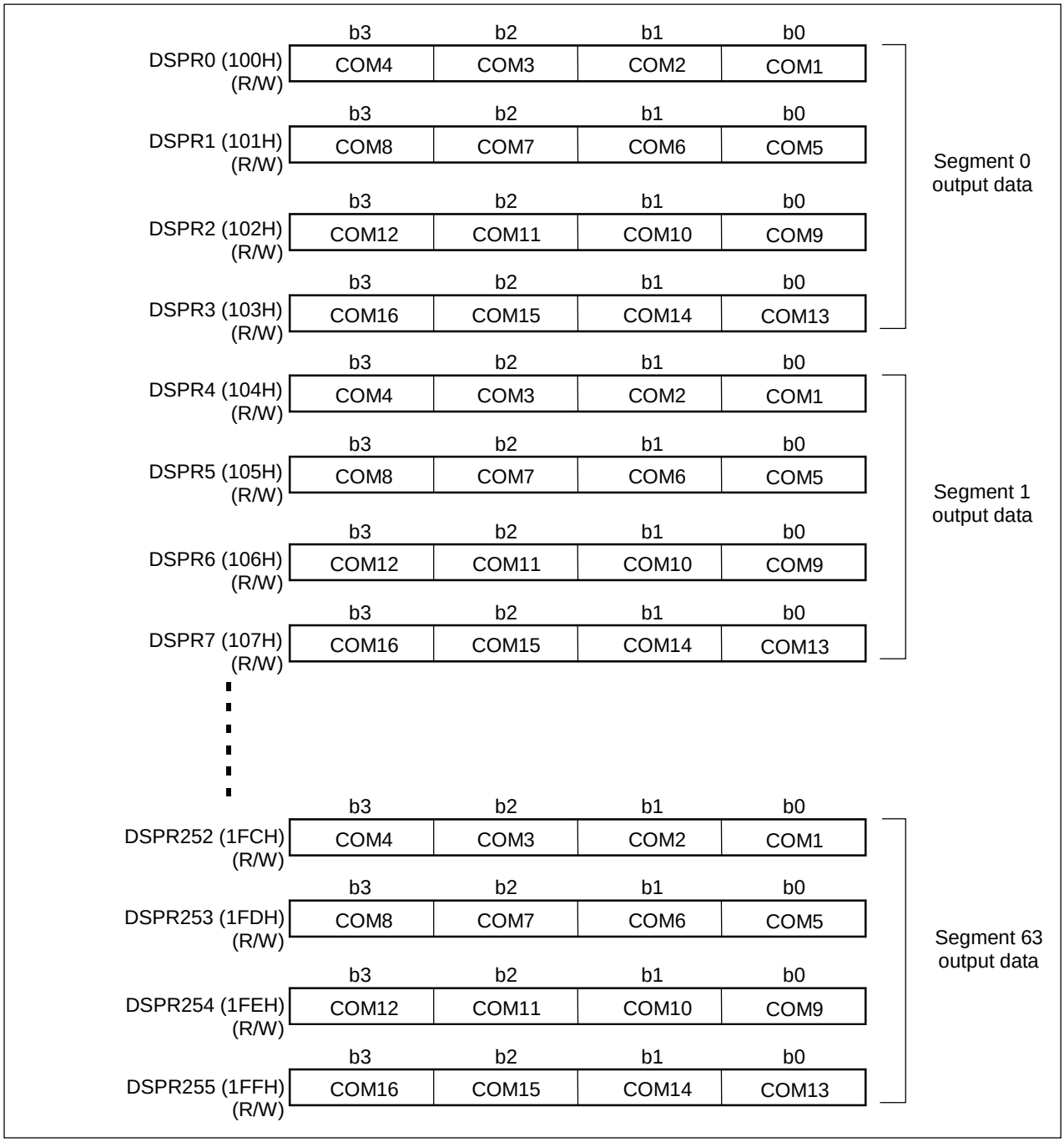


Notes:

- When a display register bit is set to "1", the corresponding LCD dot lights. When reset to "0" it goes off.
- To keep stable display state, each individual LCD dot should be set to ON/OFF with bit operation instructions.
- At system reset the display registers (DSPR0 to DSPR159) are undefined and should be initialized.

(6) MSM63188A Display register (DSPR0–255)

DSPR0–255 are segment output data registers for the dot matrix LCD driver allocated to BANK 1. The correspondence between display registers and segment outputs is shown below.



Notes:

- When a display register bit is set to "1", the corresponding LCD dot lights. When reset to "0" it goes off.
- To keep stable display state, each individual LCD dot should be set to ON/OFF with bit operation instructions.
- At system reset the display registers (DSPR0 to DSPR255) are undefined and should be initialized.

18.6 LCD Driver Output Waveform

Figures 18-4 (a) and 18-4 (b) show the output waveforms for 1/16 duty and 1/5 bias, and Figures 18-5 (a) and 18-5 (b) show the output waveforms for 1/8 duty and 1/4 bias.

The frames and clock waveforms are output waveforms for expanded LCD drivers as a secondary function of the port D.

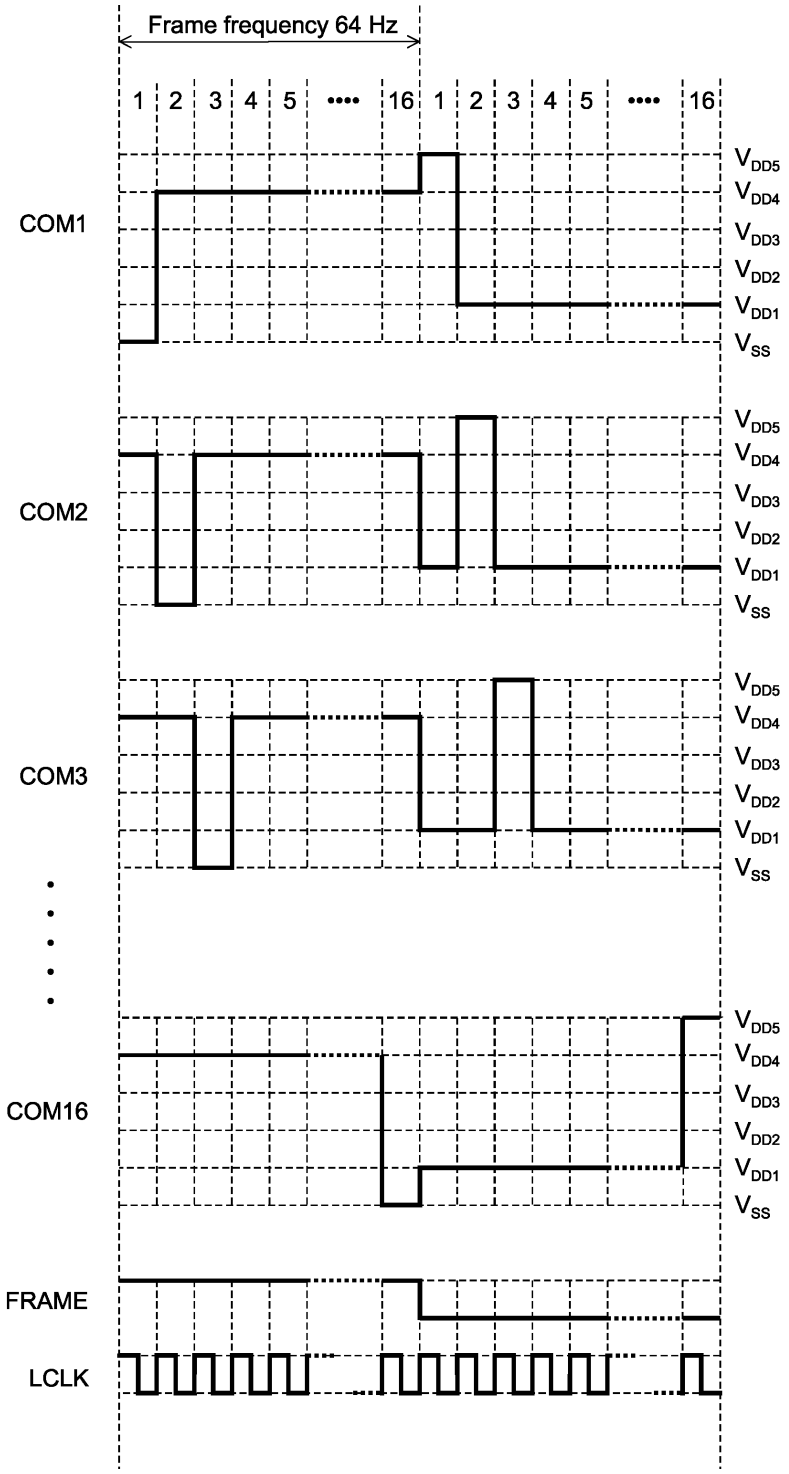


Figure 18-4 (a) 1/16 Duty, 1/5 Bias Common Output Waveform

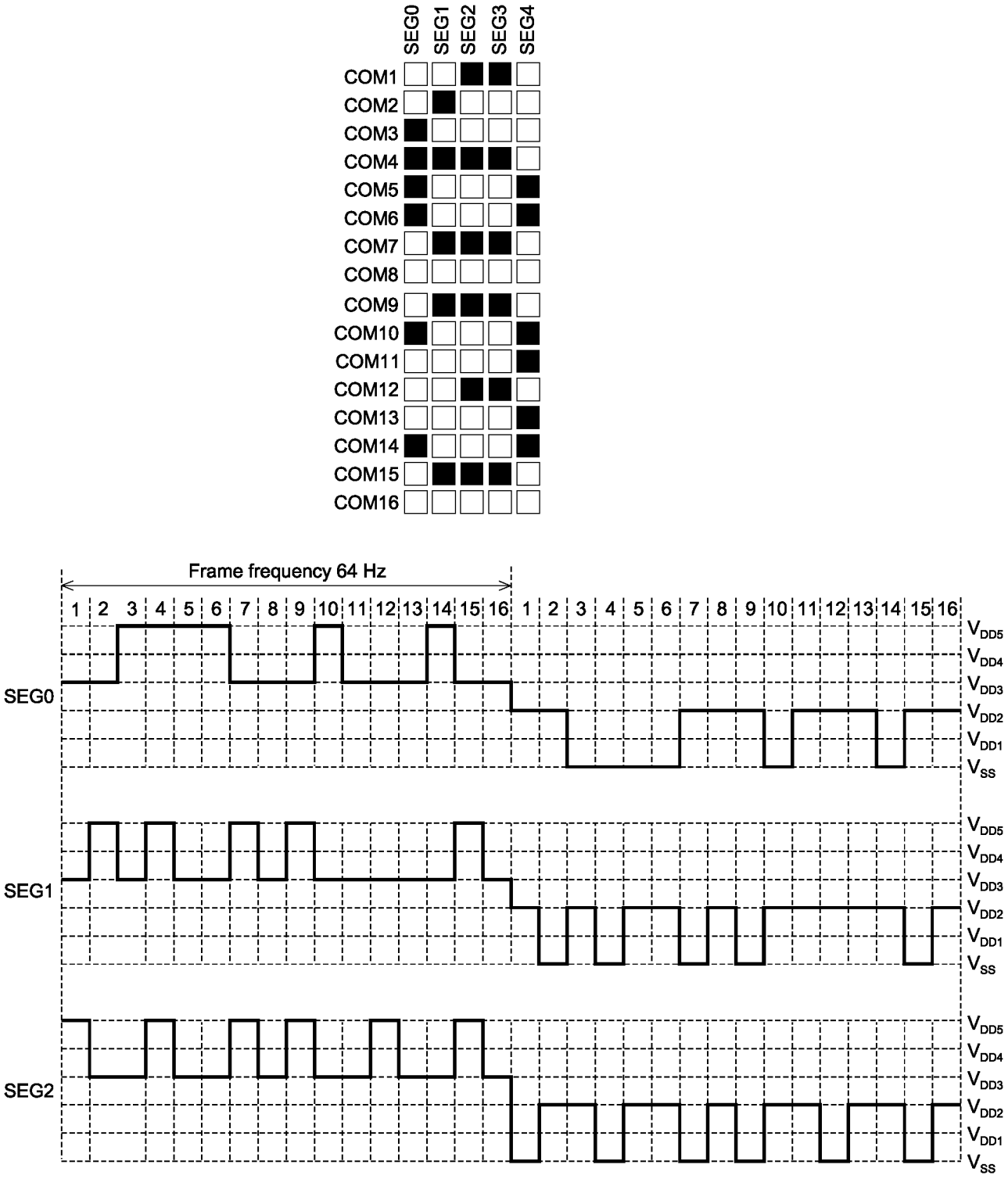


Figure 18-4 (b) 1/16 Duty, 1/5 Bias Segment Output Waveform

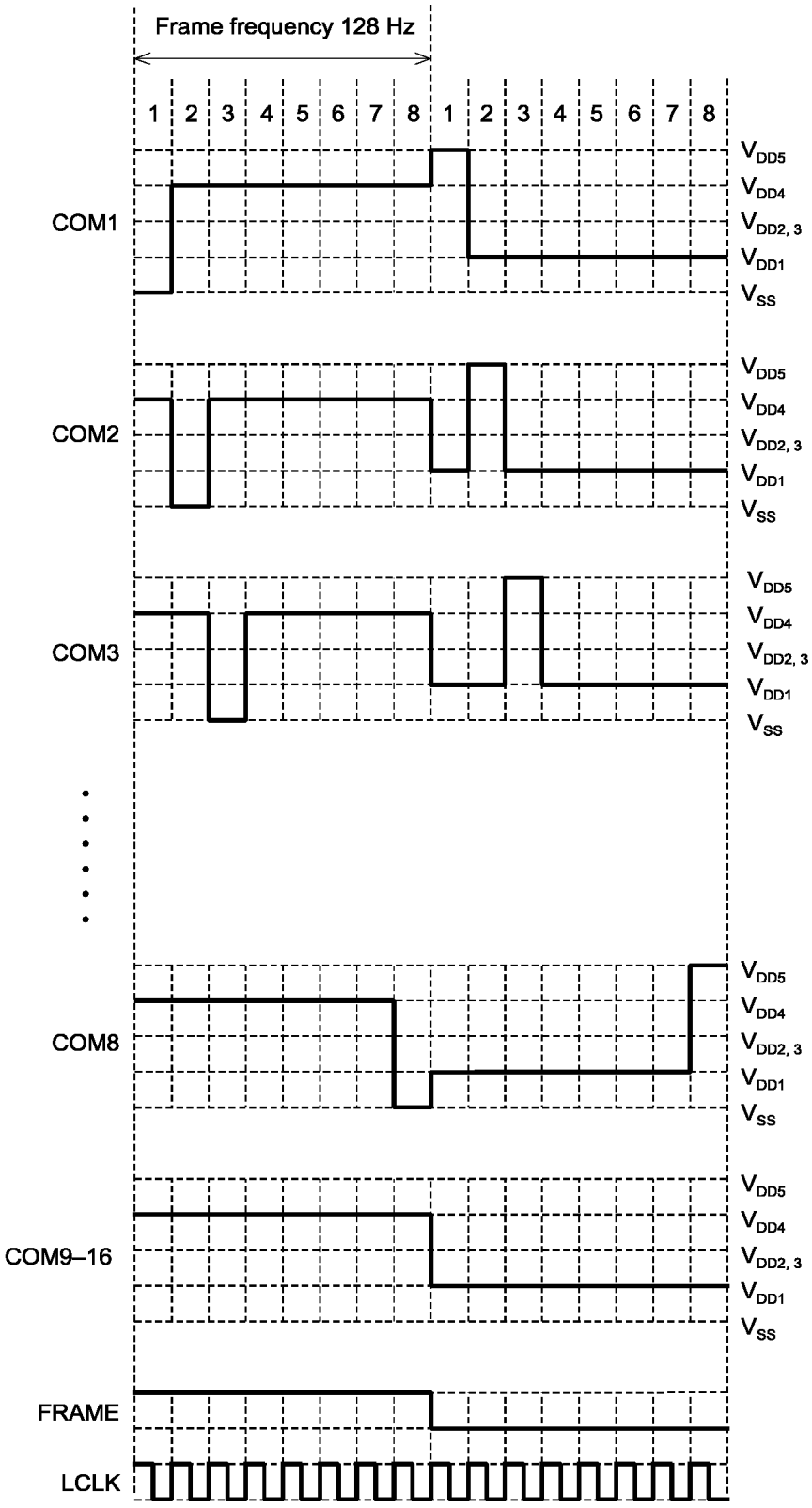


Figure 18-5 (a) 1/8 Duty, 1/4 Bias Common Output Waveform

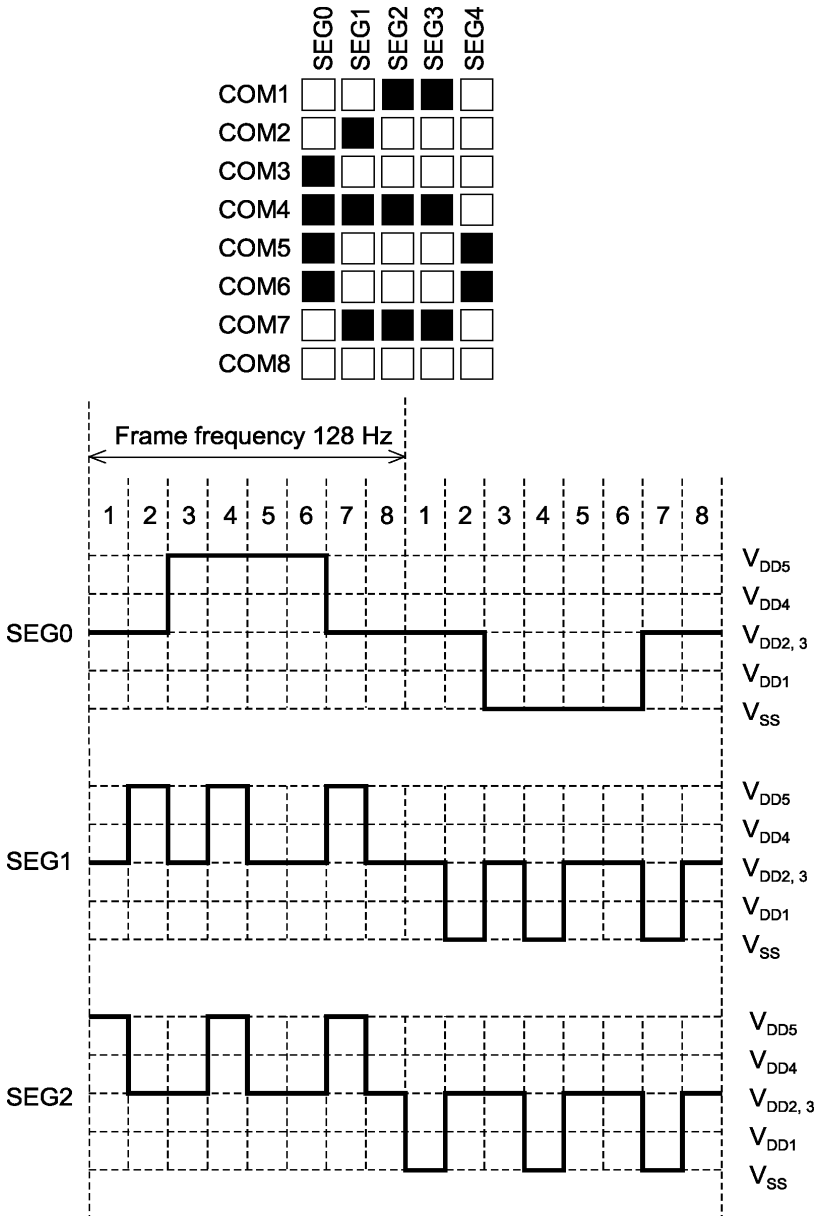


Figure 18-5 (b) 1/8 Duty, 1/4 Bias Segment Output Waveform

Chapter 19

Multiplication/Division Circuit (MULDIV)

Chapter 19 Multiplication/Division Circuit (MULDIV)

19.1 Overview

The MSM63188A has an 8-bit × 8-bit = 16-bit multiplication (MUL) and a 16-bit/8-bit = 16-bit division (DIV), implemented with an internal circuit.

The registers used are shown in Table 19-1.

All calculation registers are not stacked when interrupts occur.

Table 19-1 Registers Used in Multiplication and Division Circuit

Register name	Symbol	Address	b3	b2	b1	b0	R/W	Value at system reset
Multiplication/division condition register	MDCR	086H	OV	EF	DIVS	MULS	R/W	0H
C register L	CRL	087H	CR3	CR2	CR1	CR0	R/W	0H
C register H	CRH	088H	CR7	CR6	CR5	CR4	R/W	0H
D register L	DRL	089H	DR3	DR2	DR1	DR0	R/W	0H
D register H	DRH	08AH	DR7	DR6	DR5	DR4	R/W	0H
E register L	ERL	08BH	ER3	ER2	ER1	ER0	R/W	0H
E register H	ERH	08CH	ER7	ER6	ER5	ER4	R/W	0H
F register L	FRL	08DH	FR3	FR2	FR1	FR0	R/W	0H
F register H	FRH	08EH	FR7	FR6	FR5	FR4	R/W	0H

For multiplication the C register is multiplied by the E register. The result is stored in the DC register (D: high-order 8 bits, C: low-order 8 bits) after 5 machine cycles.

For division the D register is divided by the E register. The result is stored in the DC register (dividend) and F register (remainder) after 10 machine cycles.

19.2 Multiplication and Division Registers

19.2.1 Calculation registers

The multiplication and division calculation registers (CRL, CRH, DRL, DRH, ERL, ERH, FRL, FRH) are 4-bit special function registers (SFRs), used to set and store multiplicand, divisor, dividend and results.

	b3	b2	b1	b0
CRL (087H) (R/W)	CR3	CR2	CR1	CR0
CRH (088H) (R/W)	CR7	CR6	CR5	CR4

	b3	b2	b1	b0
DRL (089H) (R/W)	DR3	DR2	DR1	DR0
DRH (08AH) (R/W)	DR7	DR6	DR5	DR4

	b3	b2	b1	b0
ERL (08BH) (R/W)	ER3	ER2	ER1	ER0
ERH (08CH) (R/W)	ER7	ER6	ER5	ER4

	b3	b2	b1	b0
FRL (08DH) (R/W)	FR3	FR2	FR1	FR0
FRH (08EH) (R/W)	FR7	FR6	FR5	FR4

The following registers are used for multiplication and division.

[Multiplication]

DR•CR←CR × ER

CR (CRH, CRL): Holds the multiplicand. After multiplication, holds the low-order 8 bits of the result.

ER (ERH, ERL): Holds the multiplier. After multiplication, holds data.

DR (DRH, DRL): After execution, the high-order 8 bits of the result are stored.

If the result of multiplication cannot be stored in the low-order 8 bits (DR is not 0), the multiplication/division condition register (MDCR) OV flag is set to "1". When bit 0 (MULS) of MDCR is set to "1", multiplication starts, and the result is output to the appropriate registers five machine cycles later.

[Division]

DR•CR←DR•CR/ER

FR←DR•CR mod ER

DR (DRH, DRL): The high-order 8 bits of the number being divided are set here. After execution, this register holds the high-order 8 bits of the result.

CR (CRH, CRL): The low-order 8 bits of the number being divided are set here. After execution, this register holds the low-order 8 bits of the result.

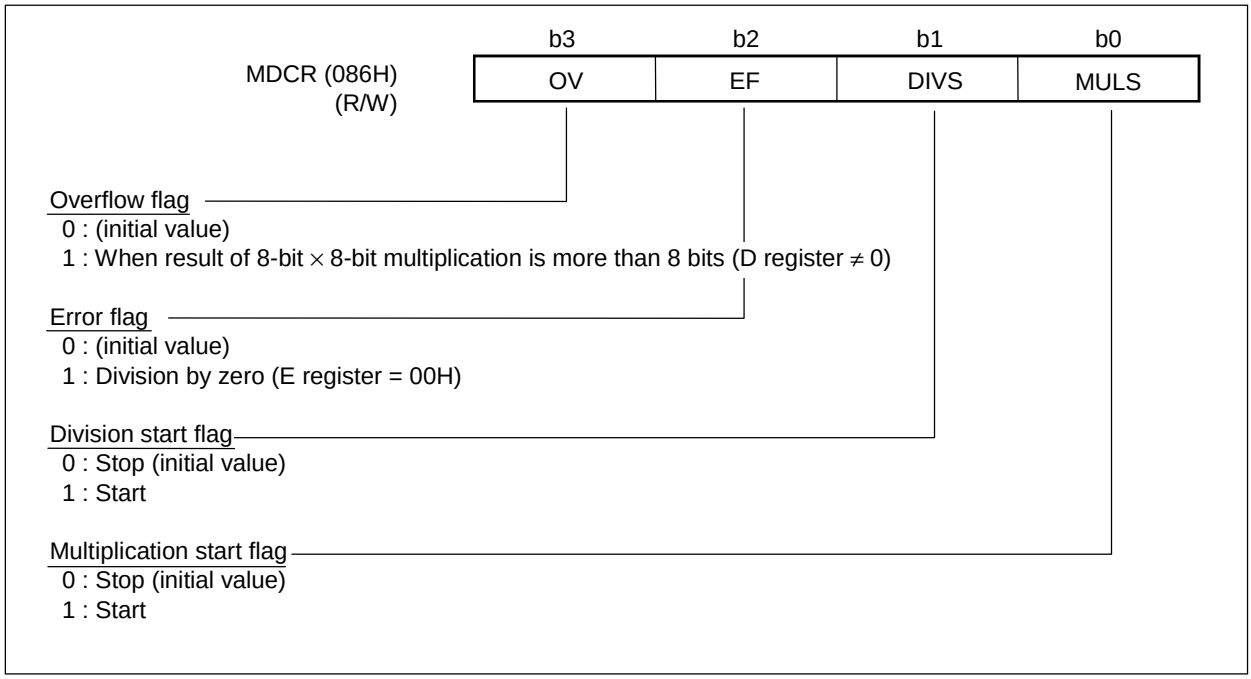
ER (ERH, ERL): The divisor is set here. After execution, this register holds data.

DR (DRH, DRL): After execution, this register holds the remainder.

If division is executed with ER = 00H (division by zero), the MDCR EF flag is set to "1". After division by zero the DC register value is 0FFFFH, and the pre-execution value from the C register is set to the F register. When bit 1 (DIVS) of MDCR is set to "1", division begins and the result is output to the appropriate registers ten machine cycles later.

19.2.2 Multiplication/division condition register (MDCR)

MDCR is a 4-bit special function register (SFR) with a multiplication/division start flag and a status flag indicating the status of the operation when finished.



Bit 3: OV (overflow flag)

Set to "1" when there is a carry (D register other than 00H) to the high-order 8 bits in multiplication, and otherwise cleared to "0". This bit is initialized to "0" at system reset.

Bit 2: EF (error flag)

Set to "1" when the E register is "0" in division, and otherwise cleared to "0". This bit is initialized to "0" at system reset.

Bit 1: DIVS (DIV start)

Division is started when this bit is set to "1", and is completed in ten machine cycles. When division is complete DIVS is reset to "0". This bit initializes to "0" at system reset.

Bit 0: MULS (MUL start)

This flag starts multiplication when set to "1", and multiplication is completed in five machine cycles. MULS is cleared to "0" when multiplication is complete. This bit is reset to "0" at system reset.

19.3 Multiplication/Division Execution

Multiplication and division execution is handled in the following sequences:

[Multiplication]

1. Multiplicand set to C register (CRH, CRL).
2. Multiplier set to E register (ERH, ERL).
3. MDCR MULS flag set to "1".

[Division]

1. High-order 8 bits of number being divided set to D register (DRH, DRL), and low-order 8 bits to C register (CRH, CRL).
2. Divisor set to E register (ERH, ERL).
3. MDCR DIVS flag set to "1".

Chapter 20

Battery Low Detect Circuit (BLD)

Chapter 20 Battery Low Detect Circuit (BLD)

20.1 Overview

The MSM63182A, MSM63184A, and MSM63188A have an internal battery low detect circuit (BLD).

The battery low detect circuit detects when the battery voltage (supply voltage V_{DD}) falls below the judgment voltage value. Four levels of judgment voltage can be selected by the BLDCON bits.

Judgment voltage values (Ta = 25°C): 1.05 ±0.10 V, 1.30 ±0.15 V, 2.20 ±0.20 V, 2.80 ±0.30 V

20.2 Battery Low Detect Circuit Configuration

The battery low detect circuit consists of the judgment circuit and the judgment voltage select circuit.

The circuit configuration is shown in Figure 20-1.

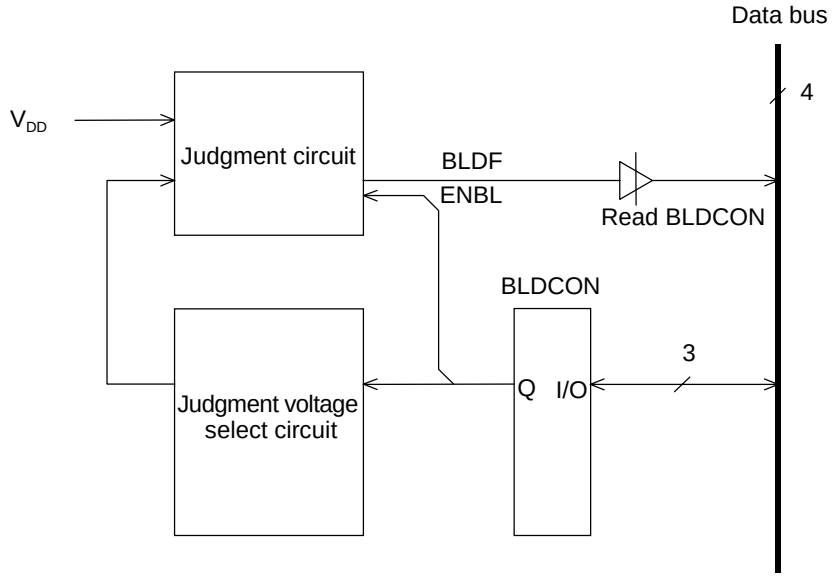


Figure 20-1 Battery Low Detect Circuit

20.3 Battery Low Detect Circuit Operation

The battery low detect circuit is controlled by the enable bit (ENBL) allocated to the battery low detect control register (BLDCON). The judgment results are sent to the CPU through the judgment result flag (BLDF).

ENBL is the battery low detect circuit enable control bit, and when this bit is set to "1", BLD operates. When ENBL is reset to "0" BLD operation stops, and the supply current for this circuit drops to zero.

BLDF is the judgment result flag. When BLDF is "1" it indicates that the voltage is less than the set threshold voltage. When BLD is "0" it indicates that the voltage is higher. This flag is enabled when ENBL is "1".

Figure 20-2 indicates a representative operation time chart example.

The judgment circuit of the battery low detect circuit takes time to be stable. Accordingly, read the BLDF flag 10 ms or more after setting the ENBL to "1". No load should be applied to the supply voltage during this detection.

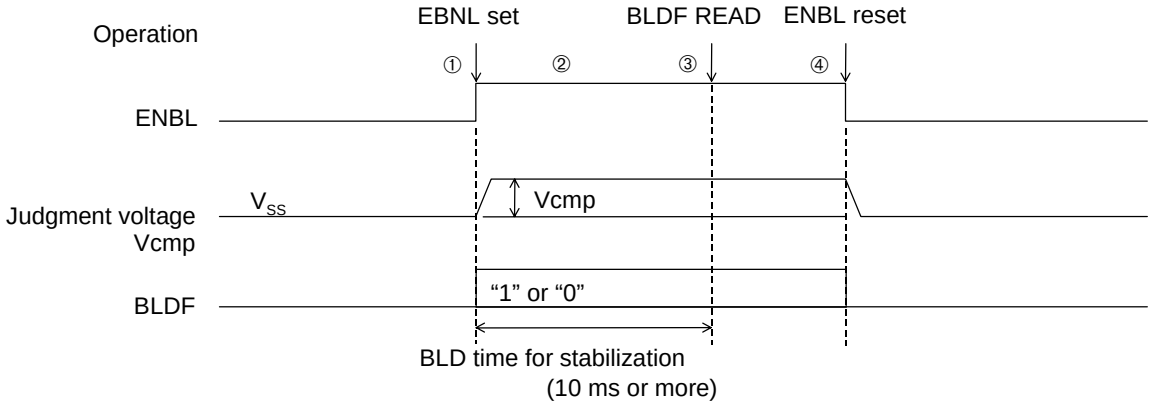


Figure 20-2 Operation Time Chart Example

The operation of Figure 20-2 is as follows.

① ENBL is set to "1" to activate BLD.

② No load should be applied to the supply voltage until the BLD becomes stable (10 ms or more).

③ The judgment result flag is read.

④ ENBL is cleared to "0".

20.4 Judgment Voltage

One of four judgment voltages is selected by bits LD1 and LD0 allocated to battery low detect control register BLDCON. The voltages are shown in Table 20-1.

Table 20-1 Judgment Voltage

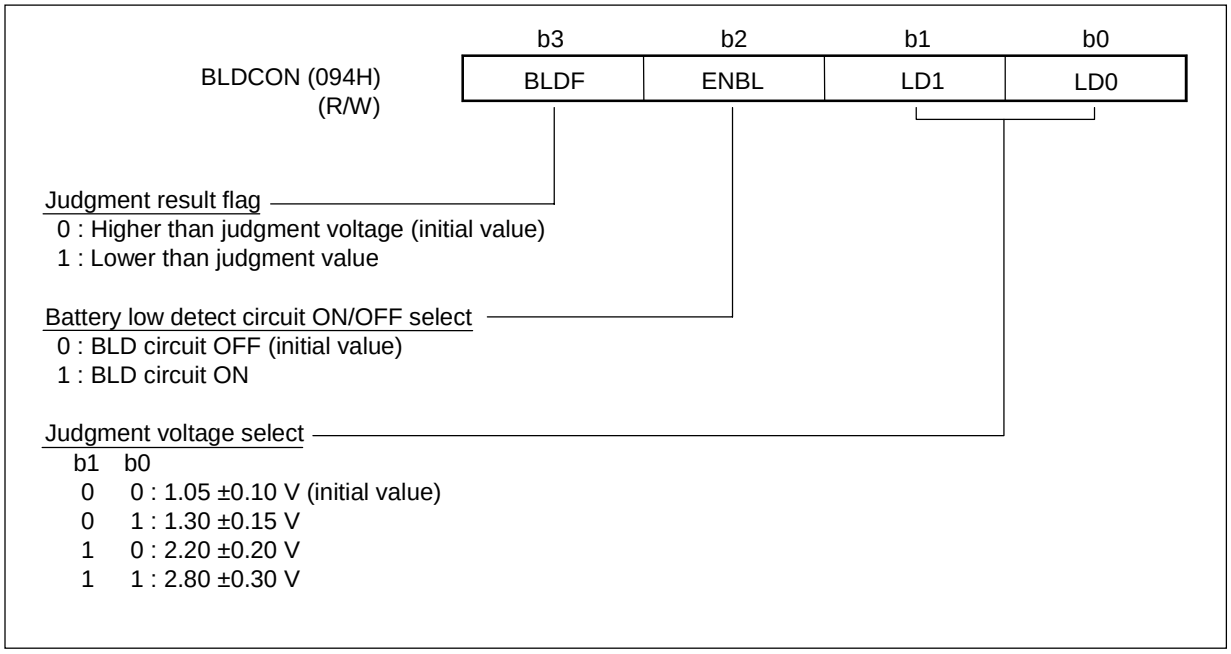
LD1	LD0	Judgment voltage	Notes
0	0	1.05 ±0.10	BLDF = 1 when V_{DD} ≤ Judgment voltage
0	1	1.30 ±0.15	BLDF = 1 when V_{DD} ≤ Judgment voltage
1	0	2.20 ±0.20	BLDF = 1 when V_{DD} ≤ Judgment voltage
1	1	2.80 ±0.30	BLDF = 1 when V_{DD} ≤ Judgment voltage

The judgment voltage is set to 1.05 V at system reset.

When supply voltage V_{DD} is less than or equal to the judgment voltage, BLDF is "1", and when higher BLDF is "0".

20.5 Battery Low Detect Circuit Register

The battery low detect circuit is controlled by the battery low detect control register (BLDCON).



Bit 3: BLDF

This bit indicates the judgement result of the battery low detect circuit.
This bit is set to "1" when V_{DD} is lower than the judgement voltage selected by bits 0 and 1.
This bit is set to "0" when V_{DD} is higher.
This bit is set to "0" when the BLD circuit stops operation.
This bit is a read-only bit and writing to this bit is disabled.

Bit 2: ENBL

This bit turns the battery low detect circuit ON or OFF.
When ENBL is set to "1", the battery low detect circuit is ON. When ENBL is set to "0", the battery low detect circuit is OFF.
At system reset, this bit is cleared to "0".

Bit 1, 0: LD1, LD0

These bits select a judgment voltage. At reset, these bits are reset to "0" to select 1.05 V.

Chapter 21

Backup Circuit (BACKUP)

Chapter 21 Backup Circuit (BACKUP)

21.1 Overview

The MSM63180 family products contain a backup circuit that generates V_{DDH} to be supplied to the voltage regulator circuit that outputs the internal logic voltage (V_{DDL}) and the bias reference voltage (V_{DD2}), and the high-speed oscillation circuit.

The V_{DD} doubled by an external capacitor is output to V_{DDH}.

The backup circuit enables a low voltage operation.

When V_{DD} alone is used without using a backup function, it is possible to release a backup function and inhibit the operation of the backup circuit.

The V_{DD} ranges from 0.9 to 2.7 V when a backup function is used and from 1.8 to 5.5 V when the function is not used.

21.2 Power Supply Circuit Configuration

21.2.1 When the backup function is used

Figure 21-1 shows the power supply circuit configuration when the backup function is used. The external capacitor C_{b12} for CB1 and CB2 raises V_{DD} and generates V_{DDH}. The capacitor C_h should be inserted berween V_{DDH} and V_{SS}. The backup function is turned ON or OFF according to bit 0 (BACKUP) of the backup control register (BUPCON).

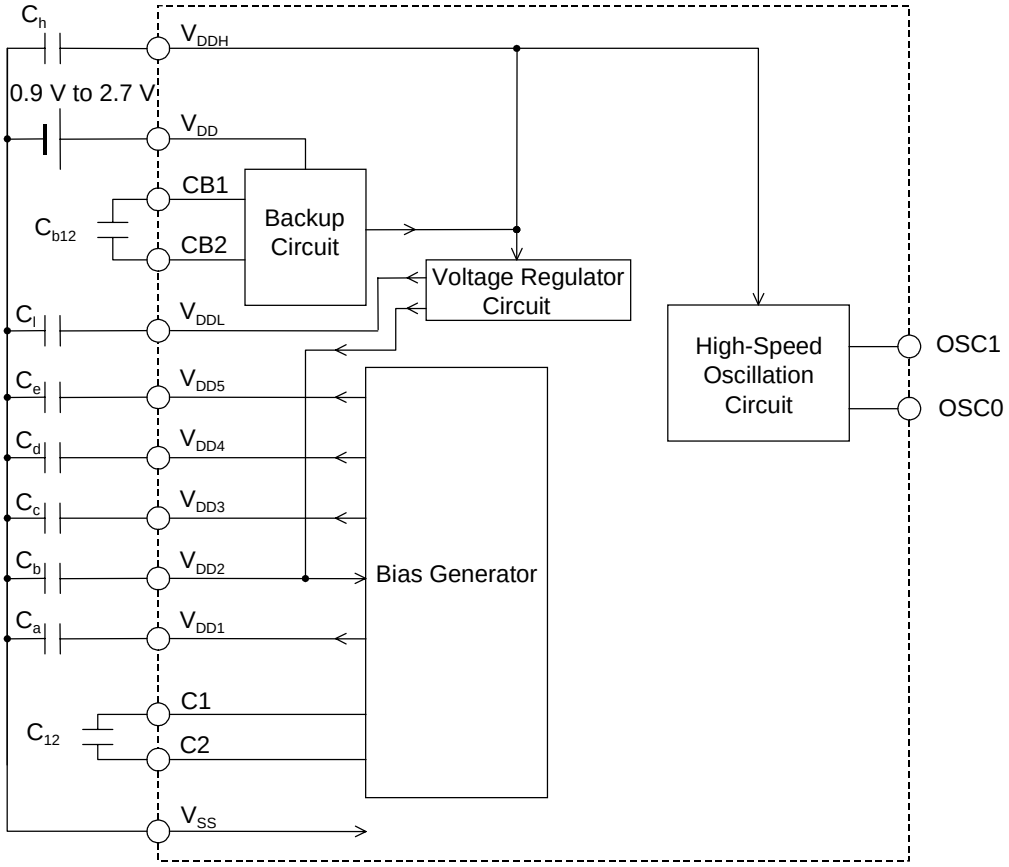


Figure 21-1 Power Supply Circuit Configuration When Backup is Used

Notes:

- In systems that use the backup circuit, connect an external capacitor (C_{b12}) between the CB1 and CB2 pins.
- The backup circuit cannot be switched ON/OFF once operation has begun.
  Design peripheral circuits such as external capacitor C_{b12} to meet the ON/OFF specification of the backup circuit.

21.2.2 When the backup function is not used

Figure 21-2 shows the power supply circuit configuration when the backup function is not used. In this configuration, the backup function can not be used and it is necessary to reset the backup select bit (BACKUP) to "0" to release the backup mode at the beginning of the program. Otherwise, the backup circuit operates, resulting in an increase in supply current.

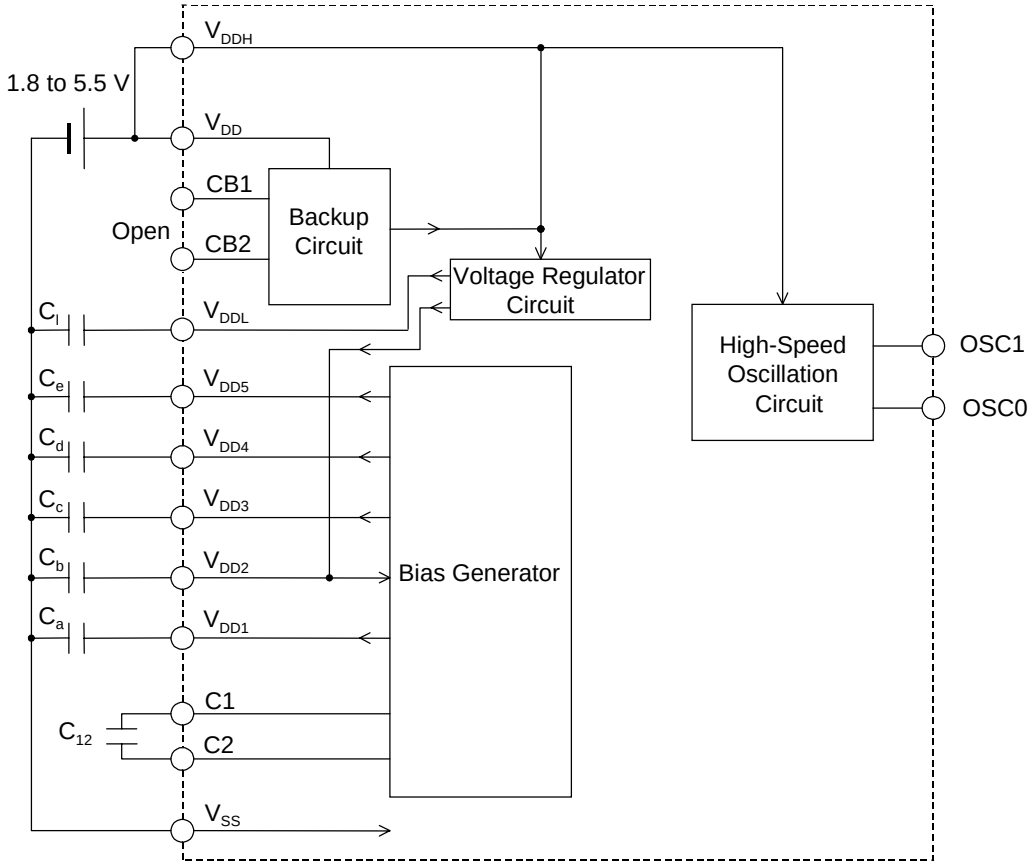


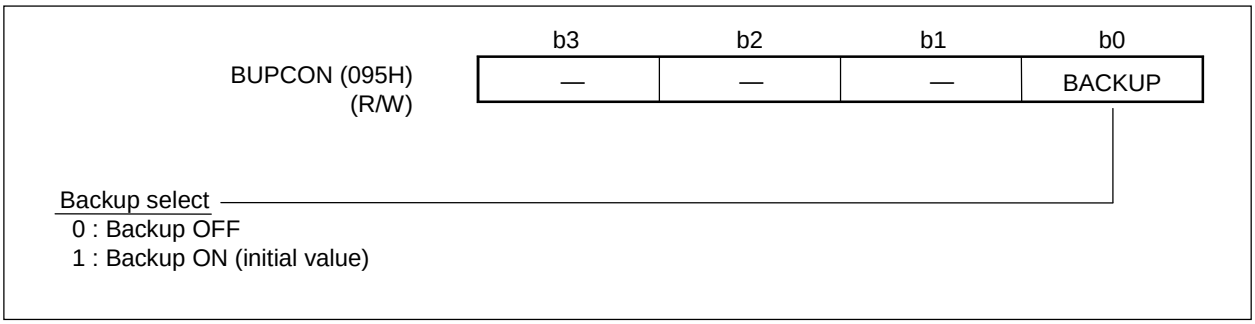
Figure 21-2 Power Supply Circuit Configuration When Backup Function is not Used

Note:

- The backup circuit cannot be switched ON/OFF once operation has begun.
  Design peripheral circuits such as external capacitor C_{b12} to meet the ON/OFF specification of the backup circuit.

21.3 Backup Control Register (BUPCON)

BUPCON is a 4-bit special function register (SFR) to control the backup circuit.



Bit 0: BACKUP

Upon reset, the BACKUP bit is set to "1" to enter the backup state.

To release the backup state, the BACKUP bit should be reset to "0" to stop the switching operation for raising the voltage.

21.4 Power Supply Circuit Operation

When the backup function is used, the level of the V_{DDH} output is forcibly switched to the V_{DD} level (supply voltage) while the time base counter is reset (RESET0 = "1"). About 62.5 ms after the reset is cancelled, the backup function is enabled and the level of the V_{DDH} becomes equal to twice the V_{DD}. When the backup function is disabled, the V_{DDH} output immediately returns to the V_{DD} level.

When the backup function is not used, the V_{DDH} output should be short-circuited to V_{DD} externally.

The V_{DDL} output of the power supply for internal logic is forcibly switched to the V_{DD} level when the time base counter is reset and switched to about 1.3 V immediately after the reset is cancelled. When the high-speed start/stop bit (ENOSC) of the frequency control register (FCON) is set to "1", the V_{DDL} output is switched to the V_{DDH} level. When the ENOSC bit is reset to "0", the V_{DDL} output returns to about 1.3 V.

The V_{DD2} output (bias reference voltage) is forcibly switched to the V_{DD} level when the time base counter is reset, and returns to a voltage (1.8 to 2.4 V) which is set by the display contrast register (DSPCONT) after the reset is cancelled.

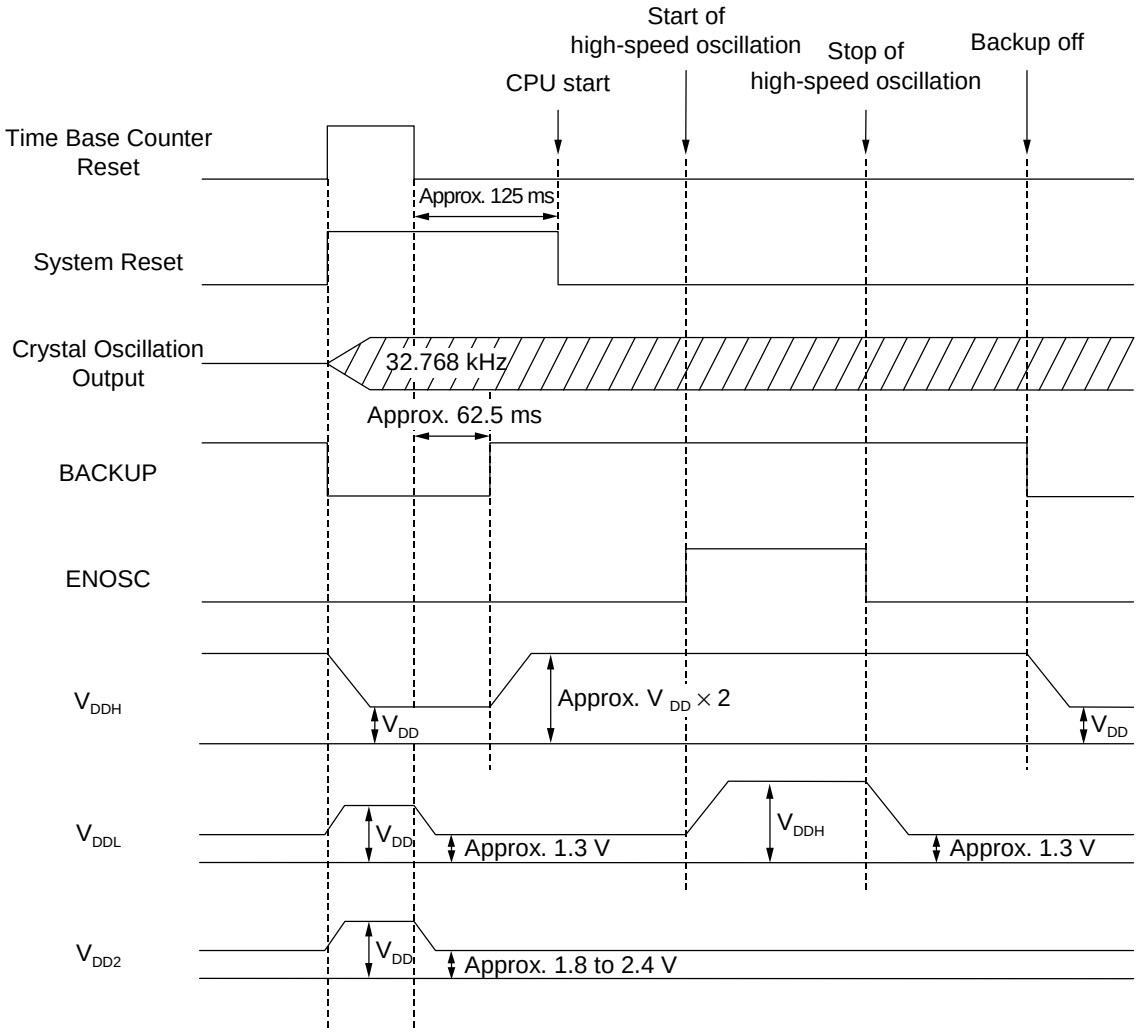


Figure 21-3 Power Supply Circuit Waveforms

Appendixes

Appendix A List of Special Function Registers

The solid black circles (●) indicate that the device is provided with the particular register.

Register name	Symbol	Address	b3	b2	b1	b0	R/W	Initial value at system reset	MSM 63182A	MSM 63184A	MSM 63188A
Port 0 data register	P0D	000H	P03	P02	P01	P00	R	Undefined	●	●	●
Port 1 data register	P1D	001H	P13	P12	P11	P10	R	Undefined			
Port 2 data register	P2D	002H	P23	P22	P21	P20	R/W	0H			●
Port 3 data register	P3D	003H	P33	P32	P31	P30	R/W	0H			
Port 4 data register	P4D	004H	P43	P42	P41	P40	R/W	0H	●	●	●
Port 5 data register	P5D	005H	P53	P52	P51	P50	R/W	0H			
Port 6 data register	P6D	006H	P63	P62	P61	P60	R/W	0H			
Port 7 data register	P7D	007H	P73	P72	P71	P70	R/W	0H			
Port 8 data register	P8D	008H	P83	P82	P81	P80	R/W	0H			
Port 9 data register	P9D	009H	P93	P92	P91	P90	R/W	0H			
Port A data register	PAD	00AH	PA3	PA2	PA1	PA0	R/W	0H			
Port B data register	PBD	00BH	PB3	PB2	PB1	PB0	R/W	0H			●
Port C data register	PCD	00CH	PC3	PC2	PC1	PC0	R/W	0H			
Port D data register	PDD	00DH	PD3	PD2	PD1	PD0	R/W	0H		●	●
Port E data register	PED	00EH	PE3	PE2	PE1	PE0	R/W	0H		●	
Reserved		00FH									
Port 0 control register 0	P0CON0	010H	P03MD	P02MD	P01MD	P00MD	R/W	0H	●	●	●
Port 0 control register 1	P0CON1	011H	—	—	P0PUD	P0F	R/W	0CH			
Port 0 interrupt enable register	P0IE	012H	P03IE	P02IE	P01IE	P00IE	R/W	0H			
Port 1 control register 0	P1CON0	013H	P13MD	P12MD	P11MD	P10MD	R/W	0H			
Port 1 control register 1	P1CON1	014H	—	—	P1PUD	P1F	R/W	0CH			
Port 1 interrupt enable register	P1IE	015H	P13IE	P12IE	P11IE	P10IE	R/W	0H			
Port 2 control register 0	P2CON0	016H	P21MD1	P21MD0	P20MD1	P20MD0	R/W	0H			●
Port 2 control register 1	P2CON1	017H	P23MD1	P23MD0	P22MD1	P22MD0	R/W	0H			
Port 3 control register 0	P3CON0	018H	P31MD1	P31MD0	P30MD1	P30MD0	R/W	0H			
Port 3 control register 1	P3CON1	019H	P33MD1	P33MD0	P32MD1	P32MD0	R/W	0H			
Port 4 control register 0	P4CON0	01AH	P41MD1	P41MD0	P40MD1	P40MD0	R/W	0H	●	●	●
Port 4 control register 1	P4CON1	01BH	P43MD1	P43MD0	P42MD1	P42MD0	R/W	0H			
Port 5 control register 0	P5CON0	01CH	P51MD1	P51MD0	P50MD1	P50MD0	R/W	0H			
Port 5 control register 1	P5CON1	01DH	P53MD1	P53MD0	P52MD1	P52MD0	R/W	0H			
Port 6 control register 0	P6CON0	01EH	P61MD1	P61MD0	P60MD1	P60MD0	R/W	0H			
Port 6 control register 1	P6CON1	01FH	P63MD1	P63MD0	P62MD1	P62MD0	R/W	0H			

Register name	Symbol	Address	b3	b2	b1	b0	R/W	Initial value at system reset	MSM 63182A	MSM 63184A	MSM 63188A
Port 7 control register 0	P7CON0	020H	P71MD1	P71MD0	P70MD1	P70MD0	R/W	0H			
Port 7 control register 1	P7CON1	021H	P73MD1	P73MD0	P72MD1	P72MD0	R/W	0H			
Port 47 mode register	P47MOD	022H	P7MOD	P6MOD	P5MOD	P4MOD	R/W	0H			
Port 8 control register 0	P8CON0	023H	P81MD1	P81MD0	P80MD1	P80MD0	R/W	0H			
Port 8 control register 1	P8CON1	024H	P83MD1	P83MD0	P82MD1	P82MD0	R/W	0H			
Port 8 direction register	P8DIR	025H	P83DIR	P82DIR	P81DIR	P80DIR	R/W	0H			
Port 8 mode register	P8MOD	026H	P8F	—	P81MOD	P80MOD	R/W	4H			
Port 9 control register 0	P9CON0	027H	P91MD1	P91MD0	P90MD1	P90MD0	R/W	0H	●	●	●
Port 9 control register 1	P9CON1	028H	P93MD1	P93MD0	P92MD1	P92MD0	R/W	0H			
Port 9 direction register	P9DIR	029H	P93DIR	P92DIR	P91DIR	P90DIR	R/W	0H			
Port A control register 0	PACON0	02AH	PA1MD1	PA1MD0	PA0MD1	PA0MD0	R/W	0H			
Port A control register 1	PACON1	02BH	PA3MD1	PA3MD0	PA2MD1	PA2MD0	R/W	0H			
Port A direction register	PADIR	02CH	PA3DIR	PA2DIR	PA1DIR	PA0DIR	R/W	0H			
Port 9A mode register	P9AMOD	02DH	—	—	PAMOD	P9MOD	R/W	0CH			
Port B control register 0	PBCON0	02EH	PB1MD1	PB1MD0	PB0MD1	PB0MD0	R/W	0H			
Port B control register 1	PBCON1	02FH	PB3MD1	PB3MD0	PB2MD1	PB2MD0	R/W	0H			
Port B direction register	PBDIR	030H	PB3DIR	PB2DIR	PB1DIR	PB0DIR	R/W	0H			
Port B interrupt enable register	PBIE	031H	PB3IE	PB2IE	PB1IE	PB0IE	R/W	0H			
Port B mode register	PBMOD	032H	PBF	—	PB1MOD	PB0MOD	R/W	4H			
Port C control register 0	PCCON0	033H	PC1MD1	PC1MD0	PC0MD1	PC0MD0	R/W	0H			●
Port C control register 1	PCCON1	034H	PC3MD1	PC3MD0	PC2MD1	PC2MD0	R/W	0H			
Port C direction register	PCDIR	035H	PC3DIR	PC2DIR	PC1DIR	PC0DIR	R/W	0H			
Port C interrupt enable register	PCIE	036H	PC3IE	PC2IE	PC1IE	PC0IE	R/W	0H			
Port C mode register 0	PCMOD0	037H	—	—	—	PCF	R/W	0EH			
Port C mode register 1	PCMOD1	038H	PC3MOD	PC2MOD	PC1MOD	PC0MOD	R/W	0H			
Port D control register 0	PDCON0	039H	PD1MD1	PD1MD0	PD0MD1	PD0MD0	R/W	0H			
Port D control register 1	PDCON1	03AH	PD3MD1	PD3MD0	PD2MD1	PD2MD0	R/W	0H			
Port D direction register	PDDIR	03BH	PD3DIR	PD2DIR	PD1DIR	PD0DIR	R/W	0H		●	●
Port D mode register	PDMOD	03CH	PD3MOD	PD2MOD	PD1MOD	PD0MOD	R/W	0H			
Port E control register 0	PECON0	03DH	PE1MD1	PE1MD0	PE0MD1	PE0MD0	R/W	0H			
Port E control register 1	PECON1	03EH	PE3MD1	PE3MD0	PE2MD1	PE2MD0	R/W	0H		●	
Port E direction register	PEDIR	03FH	PE3DIR	PE2DIR	PE1DIR	PE0DIR	R/W	0H			

Register name	Symbol	Address	b3	b2	b1	b0	R/W	Initial value at system reset	MSM 63182A	MSM 63184A	MSM 63188A
Port E mode register	PEMOD	040H	PEF	PE2MOD	PE1MOD	PE0MOD	R/W	0H		●	
Reserved		041H									
Reserved		042H									
Reserved		043H									
Reserved		044H									
Reserved		045H									
Reserved		046H									
Reserved		047H									
Reserved		048H									
Reserved		049H									
Reserved		04AH									
Reserved		04BH									
Reserved		04CH									
Reserved		04DH									
Reserved		04EH									
Reserved		04FH									
Reserved		050H							●	●	
Interrupt enable register 0	IE0		EXI1	EXI0	EMD	—	R/W	1H			●
Interrupt enable register 1	IE1	051 H	EXI5	EXI4	—	—	R/W	3H	●		●
			EXI5	EXI4	—	EXI2		2H		●	
Reserved		052H							●	●	
Interrupt enable register 2	IE2		ETM3	ETM2	ETM1	ETM0	R/W	0H			●
Interrupt enable register 3	IE3	053H	E10Hz	—	—	—	R/W	7H	●		
			E10Hz	ESFT	—	—		3H		●	
			E10Hz	—	EST	ESR		4H			●
Interrupt enable register 4	IE4	054H	E2Hz	E4Hz	E16Hz	E32Hz	R/W	0H	●	●	●
Interrupt request register 0	IRQ0	055H	—	—	—	QWDT	R/W	0EH	●	●	
			QXI1	QXI0	QMD	QWDT		0H			●
Interrupt request register 1	IRQ1	056H	QXI5	QXI4	—	—	R/W	3H	●		●
			QXI5	QXI4	—	QXI2		2H		●	
Reserved		057H							●	●	
Interrupt request register 2	IRQ2		QTM3	QTM2	QTM1	QTM0	R/W	0H			●
Interrupt request register 3	IRQ3	058H	Q10Hz	—	—	—	R/W	7H	●		
			Q10Hz	QSFT	—	—		3H		●	
			Q10Hz	—	QST	QSR		4H			●
Interrupt request register 4	IRQ4	059H	Q2Hz	Q4Hz	Q16Hz	Q32Hz	R/W	0H	●	●	●
Reserved		05AH									
Reserved		05BH									
Reserved		05CH									
Reserved		05DH									
Reserved		05EH									
Reserved		05FH									

Register name	Symbol	Address	b3	b2	b1	b0	R/W	Initial value at system reset	MSM 63182A	MSM 63184A	MSM 63188A
Time base counter register 0	TBCR0	060H	16Hz	32Hz	64Hz	128Hz	R/W	0H	●	●	●
Time base counter register 1	TBCR1	061H	1Hz	2Hz	4Hz	8Hz	R/W	0H			
Frequency control register	FCON	062H	—	OSCSEL	ENOSC	CPUCLK	R/W	8H			
Reserved		063H									
100 Hz counter register	T100CR	064H	100C3	100C2	100C1	100C0	R/W	Undefined	●	●	●
10 Hz counter register	T10CR	065H	10C3	10C2	10C1	10C0	R/W	0H			
100 Hz timer counter control register	T100CON	066H	—	—	—	ECNT	R/W	0EH			
Reserved		067H									
Timer 0 data register L	TM0DL	068H	T0D3	T0D2	T0D1	T0D0	R/W	0H			●
Timer 0 data register H	TM0DH	069H	T0D7	T0D6	T0D5	T0D4	R/W	0H			
Timer 1 data register L	TM1DL	06AH	T1D3	T1D2	T1D1	T1D0	R/W	0H			
Timer 1 data register H	TM1DH	06BH	T1D7	T1D6	T1D5	T1D4	R/W	0H			
Timer 0 counter register L	TM0CL	06CH	T0C3	T0C2	T0C1	T0C0	R/W	0H			
Timer 0 counter register H	TM0CH	06DH	T0C7	T0C6	T0C5	T0C4	R/W	0H			
Timer 1 counter register L	TM1CL	06EH	T1C3	T1C2	T1C1	T1C0	R/W	0H			
Timer 1 counter register H	TM1CH	06FH	T1C7	T1C6	T1C5	T1C4	R/W	0H			
Timer 0 control register 0	TM0CON0	070H	—	FMEAS0	TM0ECAP	TM0RUN	R/W	8H			
Timer 0 control register 1	TM0CON1	071H	—	—	TM0CL1	TM0CL0	R/W	0CH			
Timer 1 control register 0	TM1CON0	072H	—	—	TM1ECAP	TM1RUN	R/W	0CH			
Timer 1 control register 1	TM1CON1	073H	—	—	TM1CL1	TM1CL0	R/W	0CH			
Timer 0 status register	TM0STAT	074H	—	—	TM0CAP	TM0OVF	R	0CH			
Timer 1 status register	TM1STAT	075H	—	—	TM1CAP	TM1OVF	R	0CH			
Timer 2 data register L	TM2DL	076H	T2D3	T2D2	T2D1	T2D0	R/W	0H			
Timer 2 data register H	TM2DH	077H	T2D7	T2D6	T2D5	T2D4	R/W	0H			
Timer 3 data register L	TM3DL	078H	T3D3	T3D2	T3D1	T3D0	R/W	0H			
Timer 3 data register H	TM3DH	079H	T3D7	T3D6	T3D5	T3D4	R/W	0H			
Timer 2 counter register L	TM2CL	07AH	T2C3	T2C2	T2C1	T2C0	R/W	0H			
Timer 2 counter register H	TM2CH	07BH	T2C7	T2C6	T2C5	T2C4	R/W	0H			
Timer 3 counter register L	TM3CL	07CH	T3C3	T3C2	T3C1	T3C0	R/W	0H			
Timer 3 counter register H	TM3CH	07DH	T3C7	T3C6	T3C5	T3C4	R/W	0H			
Timer 2 control register 0	TM2CON0	07EH	—	FMEAS2	—	TM2RUN	R/W	0AH			
Timer 2 control register 1	TM2CON1	07FH	—	—	TM2CL1	TM2CL0	R/W	0CH			

Register name	Symbol	Address	b3	b2	b1	b0	R/W	Initial value at system reset	MSM 63182A	MSM 63184A	MSM 63188A
Timer 3 control register 0	TM3CON0	080H	—	—	—	TM3RUN	R/W	0EH			
Timer 3 control register 1	TM3CON1	081H	—	—	TM3CL1	TM3CL0	R/W	0CH			●
Timer 2 status register	TM2STAT	082H	—	—	—	TM2OVF	R	0EH			
Timer 3 status register	TM3STAT	083H	—	—	—	TM3OVF	R	0EH			
Reserved		084H									
Reserved		085H									
Multiplication/division condition register	MDCR	086H	OV	EF	DIVS	MULS	R/W	0H			
C register L	CRL	087H	CR3	CR2	CR1	CR0	R/W	0H			
C register H	CRH	088H	CR7	CR6	CR5	CR4	R/W	0H			
D register L	DRL	089H	DR3	DR2	DR1	DR0	R/W	0H			
D register H	DRH	08AH	DR7	DR6	DR5	DR4	R/W	0H			●
E register L	ERL	08BH	ER3	ER2	ER1	ER0	R/W	0H			
E register H	ERH	08CH	ER7	ER6	ER5	ER4	R/W	0H			
F register L	FRL	08DH	FR3	FR2	FR1	FR0	R/W	0H			
F register H	FRH	08EH	FR7	FR6	FR5	FR4	R/W	0H			
Reserved		08FH									
Display control register 0	DSPCON0	090H	BISEL	PDWN	ALLON	LCDON	R/W	0H			
Display control register 1	DSPCON1	091H	DT3	DT2	DT1	DT0	R/W	0H	●	●	●
Display contrast register	DSPCNT	092H	CN3	CN2	CN1	CN0	R/W	0H			
Reserved		093H									
Low-voltage battery detect control register	BLDCON	094H	BLDF	ENBL	LD1	LD0	R/W	0H	●	●	●
Back-up control register	BUPCON	095H	—	—	—	BACKUP	R/W	0FH	●	●	●
Tempo register	TEMPO	096H	TMP3	TMP2	TMP1	TMP0	R/W	0H			
Melody driver control register	MDCON	097H	MSF	EMBD	MBM1	MBM0	R/W	0H			●
Buzzer driver control register	BDCON	098H	—	EBD	BM1	BM0	R/W	8H			
Buzzer frequency control register	BFCON	099H	BF3	BF2	BF1	BF0	R/W	0H	●	●	
Reserved		09AH									
Reserved		09BH									
Reserved		09CH									
Reserved		09DH									
Reserved		09EH									
Watchdog timer control register	WDTCON	09FH	d3	d2	d1	d0	W	—	●	●	●

Register name	Symbol	Address	b3	b2	b1	b0	R/W	Initial value at system reset	MSM 63182A	MSM 63184A	MSM 63188A
Shift register L	SFTRL	0A0H	SD3	SD2	SD1	SD0	R/W	0H			
Shift register H	SFTRH	0A1H	SD7	SD6	SD5	SD4	R/W	0H			
Shift register control register 0	SFTCON0	0A2H	—	SDIR	SELCK1	SELCK0	R/W	8H		●	
Shift register control register 1	SFTCON1	0A3H	—	—	—	ENTR	R/W	0EH			
Serial port send buffer L	STBUFL	0A4H	TB3	TB2	TB1	TB0	R/W	0H			
Serial port send buffer H	STBUFH	0A5H	TB7	TB6	TB5	TB4	R/W	0H			
Serial port send control register 0	STCON0	0A6H	STSTB	STL1	STL0	STMOD	R/W	0H			
Serial port send control register 1	STCON1	0A7H	STLMB	STPOE	STPEN	STCLK	R/W	0H			
Serial port receive buffer L	SRBUFL	0A8H	RB3	RB2	RB1	RB0	R	0H			
Serial port receive buffer H	SRBUFH	0A9H	RB7	RB6	RB5	RB4	R	0H			●
Serial port receive control register 0	SRCON0	0AAH	SREN	SRL1	SRL0	SRMOD	R/W	0H			
Serial port receive control register 1	SRCON1	0ABH	SRLMB	SRPOE	SRPEN	SRCLK	R/W	0H			
Serial port receive baud rate setting register	SRBAT	0ACH	—	—	BRT1	BRT0	R/W	0CH			
Serial port status register	SSTAT	0ADH	BFULL	PERR	OERR	FERR	R	0H			
Reserved		0AEH to 0F1H									
RA register 0	RA0	0F2H	a3	a2	a1	a0	R/W	0H			
RA register 1	RA1	0F3H	a7	a6	a5	a4	R/W	0H			
RA register 2	RA2	0F4H	a11	a10	a9	a8	R/W	0H	●	●	●
RA register 3	RA3	0F5H	a15	a14	a13	a12	R/W	0H			
Register stack pointer	RSP	0F6H	rsp3	rsp2	rsp1	rsp0	R/W	0H			
Stack pointer	SP	0F7H	sp3	sp2	sp1	sp0	R	0H			
Reserved		0F8H									
Y register	Y	0F9H	y3	y2	y1	y0	R/W	0H			
X register	X	0FAH	x3	x2	x1	x0	R/W	0H			
L register	L	0FBH	l3	l2	l1	l0	R/W	0H			
H register	H	0FCH	h3	h2	h1	h0	R/W	0H	●	●	●
Current bank register	CBR	0FDH	c3	c2	c1	c0	R/W	0H			
Extra bank register	EBR	0FEH	e3	e2	e1	e0	R/W	0H			
Master interrupt enable register	MIEF	0FFH	—	—	—	MIE	R	0EH			

Register name	Symbol	Address	Seg-ment	b3	b2	b1	b0	R/W	Initial value at system reset	MSM 63182A	MSM 63184A	MSM 63188A
Display register 0	DSPR0	100H	0	COM4	COM3	COM2	COM1	R/W	Undefined	●	●	●
Display register 1	DSPR1	101H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 2	DSPR2	102H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 3	DSPR3	103H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 4	DSPR4	104H	1	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 5	DSPR5	105H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 6	DSPR6	106H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 7	DSPR7	107H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 8	DSPR8	108H	2	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 9	DSPR9	109H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 10	DSPR10	10AH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 11	DSPR11	10BH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 12	DSPR12	10CH	3	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 13	DSPR13	10DH		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 14	DSPR14	10EH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 15	DSPR15	10FH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 16	DSPR16	110H	4	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 17	DSPR17	111H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 18	DSPR18	112H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 19	DSPR19	113H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 20	DSPR20	114H	5	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 21	DSPR21	115H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 22	DSPR22	116H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 23	DSPR23	117H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 24	DSPR24	118H	6	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 25	DSPR25	119H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 26	DSPR26	11AH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 27	DSPR27	11BH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 28	DSPR28	11CH	7	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 29	DSPR29	11DH		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 30	DSPR30	11EH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 31	DSPR31	11FH		COM16	COM15	COM14	COM13	R/W	Undefined			

Register name	Symbol	Address	Seg-ment	b3	b2	b1	b0	R/W	Initial value at system reset	MSM 63182A	MSM 63184A	MSM 63188A
Display register 32	DSPR32	120H	8	COM4	COM3	COM2	COM1	R/W	Undefined	●	●	●
Display register 33	DSPR33	121H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 34	DSPR34	122H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 35	DSPR35	123H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 36	DSPR36	124H	9	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 37	DSPR37	125H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 38	DSPR38	126H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 39	DSPR39	127H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 40	DSPR40	128H	10	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 41	DSPR41	129H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 42	DSPR42	12AH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 43	DSPR43	12BH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 44	DSPR44	12CH	11	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 45	DSPR45	12DH		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 46	DSPR46	12EH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 47	DSPR47	12FH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 48	DSPR48	130H	12	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 49	DSPR49	131H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 50	DSPR50	132H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 51	DSPR51	133H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 52	DSPR52	134H	13	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 53	DSPR53	135H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 54	DSPR54	136H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 55	DSPR55	137H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 56	DSPR56	138H	14	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 57	DSPR57	139H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 58	DSPR58	13AH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 59	DSPR59	13BH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 60	DSPR60	13CH	15	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 61	DSPR61	13DH		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 62	DSPR62	13EH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 63	DSPR63	13FH		COM16	COM15	COM14	COM13	R/W	Undefined			

Register name	Symbol	Address	Seg-ment	b3	b2	b1	b0	R/W	Initial value at system reset	MSM 63182A	MSM 63184A	MSM 63188A
Display register 64	DSPR64	140H	16	COM4	COM3	COM2	COM1	R/W	Undefined	●	●	●
Display register 65	DSPR65	141H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 66	DSPR66	142H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 67	DSPR67	143H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 68	DSPR68	144H	17	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 69	DSPR69	145H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 70	DSPR70	146H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 71	DSPR71	147H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 72	DSPR72	148H	18	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 73	DSPR73	149H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 74	DSPR74	14AH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 75	DSPR75	14BH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 76	DSPR76	14CH	19	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 77	DSPR77	14DH		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 78	DSPR78	14EH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 79	DSPR79	14FH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 80	DSPR80	150H	20	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 81	DSPR81	151H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 82	DSPR82	152H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 83	DSPR83	153H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 84	DSPR84	154H	21	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 85	DSPR85	155H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 86	DSPR86	156H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 87	DSPR87	157H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 88	DSPR88	158H	22	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 89	DSPR89	159H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 90	DSPR90	15AH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 91	DSPR91	15BH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 92	DSPR92	15CH	23	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 93	DSPR93	15DH		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 94	DSPR94	15EH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 95	DSPR95	15FH		COM16	COM15	COM14	COM13	R/W	Undefined			

Register name	Symbol	Address	Segment	b3	b2	b1	b0	R/W	Initial value at system reset	MSM 63182A	MSM 63184A	MSM 63188A
Display register 96	DSPR96	160H	24	COM4	COM3	COM2	COM1	R/W	Undefined	●	●	●
Display register 97	DSPR97	161H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 98	DSPR98	162H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 99	DSPR99	163H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 100	DSPR100	164H	25	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 101	DSPR101	165H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 102	DSPR102	166H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 103	DSPR103	167H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 104	DSPR104	168H	26	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 105	DSPR105	169H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 106	DSPR106	16AH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 107	DSPR107	16BH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 108	DSPR108	16CH	27	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 109	DSPR109	16DH		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 110	DSPR110	16EH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 111	DSPR111	16FH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 112	DSPR112	170H	28	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 113	DSPR113	171H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 114	DSPR114	172H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 115	DSPR115	173H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 116	DSPR116	174H	29	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 117	DSPR117	175H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 118	DSPR118	176H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 119	DSPR119	177H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 120	DSPR120	178H	30	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 121	DSPR121	179H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 122	DSPR122	17AH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 123	DSPR123	17BH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 124	DSPR124	17CH	31	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 125	DSPR125	17DH		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 126	DSPR126	17EH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 127	DSPR127	17FH		COM16	COM15	COM14	COM13	R/W	Undefined			

Register name	Symbol	Address	Seg-ment	b3	b2	b1	b0	R/W	Initial value at system reset	MSM 63182A	MSM 63184A	MSM 63188A
Display register 128	DSPR128	180H	32	COM4	COM3	COM2	COM1	R/W	Undefined		●	●
Display register 129	DSPR129	181H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 130	DSPR130	182H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 131	DSPR131	183H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 132	DSPR132	184H	33	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 133	DSPR133	185H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 134	DSPR134	186H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 135	DSPR135	187H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 136	DSPR136	188H	34	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 137	DSPR137	189H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 138	DSPR138	18AH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 139	DSPR139	18BH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 140	DSPR140	18CH	35	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 141	DSPR141	18DH		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 142	DSPR142	18EH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 143	DSPR143	18FH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 144	DSPR144	190H	36	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 145	DSPR145	191H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 146	DSPR146	192H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 147	DSPR147	193H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 148	DSPR148	194H	37	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 149	DSPR149	195H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 150	DSPR150	196H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 151	DSPR151	197H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 152	DSPR152	198H	38	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 153	DSPR153	199H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 154	DSPR154	19AH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 155	DSPR155	19BH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 156	DSPR156	19CH	39	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 157	DSPR157	19DH		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 158	DSPR158	19EH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 159	DSPR159	19FH		COM16	COM15	COM14	COM13	R/W	Undefined			

Register name	Symbol	Address	Segment	b3	b2	b1	b0	R/W	Initial value at system reset	MSM 63182A	MSM 63184A	MSM 63188A
Display register 160	DSPR160	1A0H	40	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 161	DSPR161	1A1H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 162	DSPR162	1A2H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 163	DSPR163	1A3H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 164	DSPR164	1A4H	41	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 165	DSPR165	1A5H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 166	DSPR166	1A6H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 167	DSPR167	1A7H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 168	DSPR168	1A8H	42	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 169	DSPR169	1A9H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 170	DSPR170	1AAH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 171	DSPR171	1ABH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 172	DSPR172	1ACH	43	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 173	DSPR173	1ADH		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 174	DSPR174	1AEH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 175	DSPR175	1AFH		COM16	COM15	COM14	COM13	R/W	Undefined			●
Display register 176	DSPR176	1B0H	44	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 177	DSPR177	1B1H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 178	DSPR178	1B2H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 179	DSPR179	1B3H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 180	DSPR180	1B4H	45	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 181	DSPR181	1B5H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 182	DSPR182	1B6H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 183	DSPR183	1B7H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 184	DSPR184	1B8H	46	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 185	DSPR185	1B9H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 186	DSPR186	1BAH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 187	DSPR187	1BBH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 188	DSPR188	1BCH	47	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 189	DSPR189	1BDH		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 190	DSPR190	1BEH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 191	DSPR191	1BFH		COM16	COM15	COM14	COM13	R/W	Undefined			

Register name	Symbol	Address	Segment	b3	b2	b1	b0	R/W	Initial value at system reset	MSM 63182A	MSM 63184A	MSM 63188A
Display register 192	DSPR192	1C0H	48	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 193	DSPR193	1C1H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 194	DSPR194	1C2H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 195	DSPR195	1C3H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 196	DSPR196	1C4H	49	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 197	DSPR197	1C5H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 198	DSPR198	1C6H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 199	DSPR199	1C7H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 200	DSPR200	1C8H	50	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 201	DSPR201	1C9H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 202	DSPR202	1CAH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 203	DSPR203	1CBH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 204	DSPR204	1CCH	51	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 205	DSPR205	1CDH		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 206	DSPR206	1CEH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 207	DSPR207	1CFH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 208	DSPR208	1D0H	52	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 209	DSPR209	1D1H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 210	DSPR210	1D2H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 211	DSPR211	1D3H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 212	DSPR212	1D4H	53	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 213	DSPR213	1D5H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 214	DSPR214	1D6H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 215	DSPR215	1D7H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 216	DSPR216	1D8H	54	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 217	DSPR217	1D9H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 218	DSPR218	1DAH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 219	DSPR219	1DBH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 220	DSPR220	1DCH	55	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 221	DSPR221	1DDH		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 222	DSPR222	1DEH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 223	DSPR223	1DFH		COM16	COM15	COM14	COM13	R/W	Undefined			

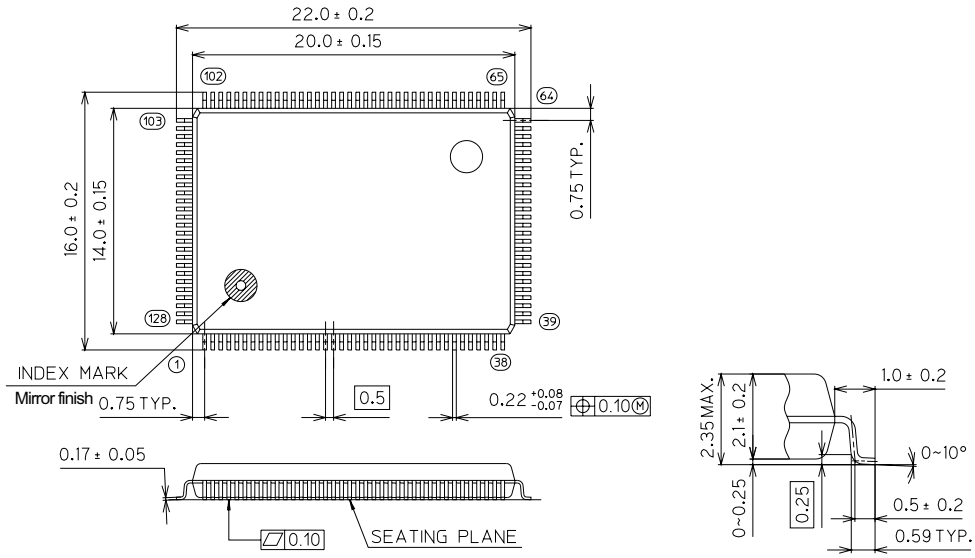
Register name	Symbol	Address	Segment	b3	b2	b1	b0	R/W	Initial value at system reset	MSM 63182A	MSM 63184A	MSM 63188A
Display register 224	DSPR224	1E0H	56	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 225	DSPR225	1E1H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 226	DSPR226	1E2H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 227	DSPR227	1E3H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 228	DSPR228	1E4H	57	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 229	DSPR229	1E5H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 230	DSPR230	1E6H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 231	DSPR231	1E7H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 232	DSPR232	1E8H	58	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 233	DSPR233	1E9H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 234	DSPR234	1EAH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 235	DSPR235	1EBH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 236	DSPR236	1ECH	59	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 237	DSPR237	1EDH		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 238	DSPR238	1EEH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 239	DSPR239	1EFH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 240	DSPR240	1F0H	60	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 241	DSPR241	1F1H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 242	DSPR242	1F2H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 243	DSPR243	1F3H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 244	DSPR244	1F4H	61	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 245	DSPR245	1F5H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 246	DSPR246	1F6H		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 247	DSPR247	1F7H		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 248	DSPR248	1F8H	62	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 249	DSPR249	1F9H		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 250	DSPR250	1FAH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 251	DSPR251	1FBH		COM16	COM15	COM14	COM13	R/W	Undefined			
Display register 252	DSPR252	1FCH	63	COM4	COM3	COM2	COM1	R/W	Undefined			
Display register 253	DSPR253	1FDH		COM8	COM7	COM6	COM5	R/W	Undefined			
Display register 254	DSPR254	1FEH		COM12	COM11	COM10	COM9	R/W	Undefined			
Display register 255	DSPR255	1FFH		COM16	COM15	COM14	COM13	R/W	Undefined			

Appendix B Package Dimensions

MSM63182A-xxxGS-K
MSM63184A-xxxGS-K

(Unit: mm)

QFP128-P-1420-0.50-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5µm)
Package weight (g)	1.19 TYP.
Rev. No./Last Revised	4/Nov. 28, 1996

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

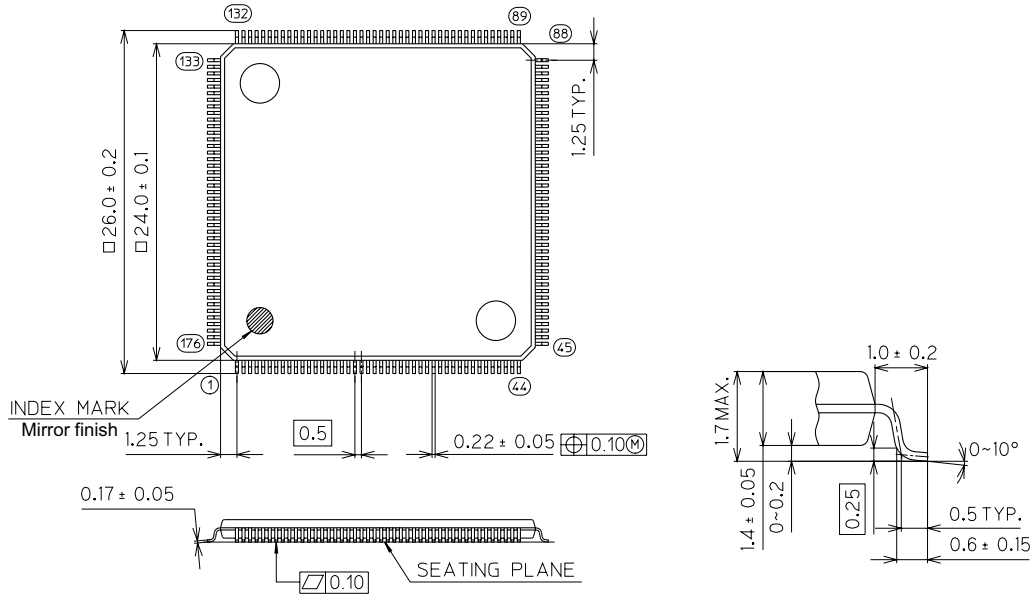
The SOP, QFP, TSOP, TQFP, LQFP, SOJ, QFJ (PLCC), SHP, and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.

Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature, and times).

MSM63188A-xxxGS-BK

(Unit: mm)

LQFP176-P-2424-0.50-BK



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5μm)
Package weight (g)	1.87 TYP.
Rev. No./Last Revised	3/Nov. 28, 1996

Oki Electric Industry Co., Ltd.

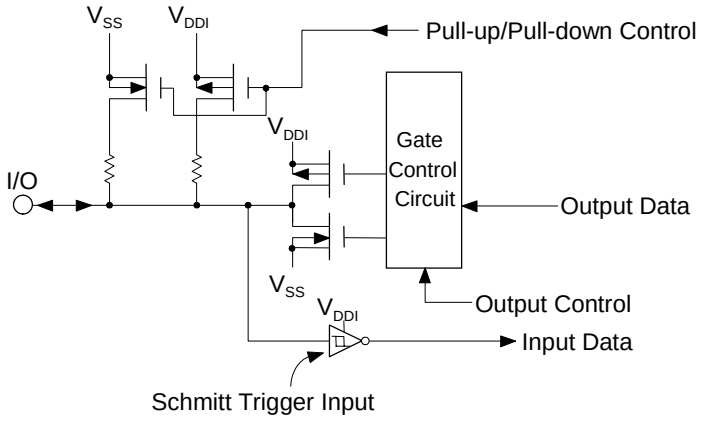
Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, TQFP, LQFP, SOJ, QFJ (PLCC), SHP, and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.

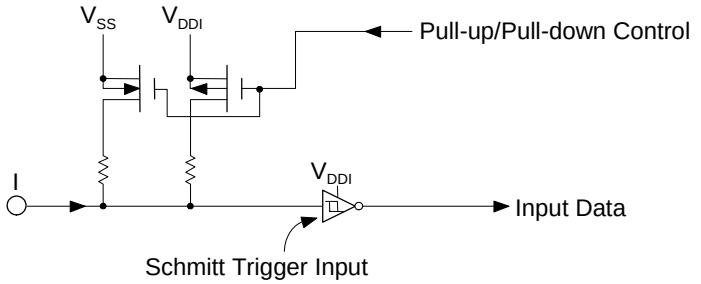
Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature, and times).

Appendix C Input/Output Circuit Configuration

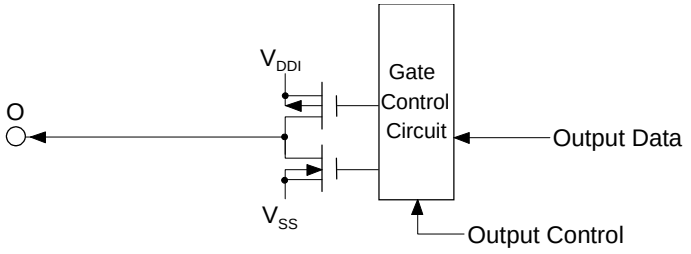
A. I/O Port (P8.0–P8.3, P9.0–P9.3, PA.0–PA.3, PB.0–PB.3, PC.0–PC.3, PD.0–PD.3, PE.0–PE.3)



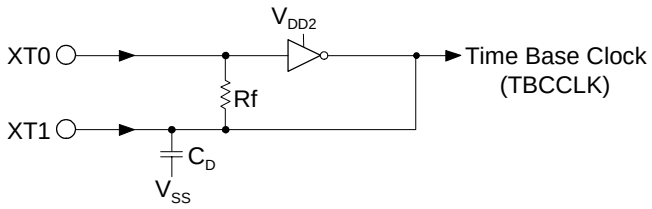
B. Input Port (P0.0–P0.3, P1.0–P1.3)



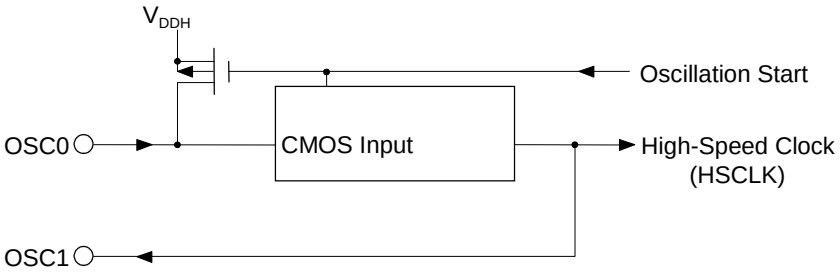
C. Output Port (P2.0–P2.3, P3.0–P3.3, P4.0–P4.3, P5.0–P5.3, P6.0–P6.3, P7.0–P7.3)



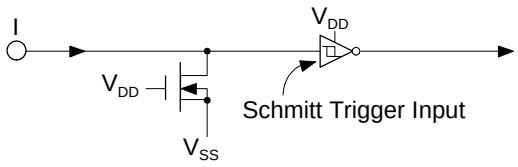
D. Crystal Oscillation Circuit



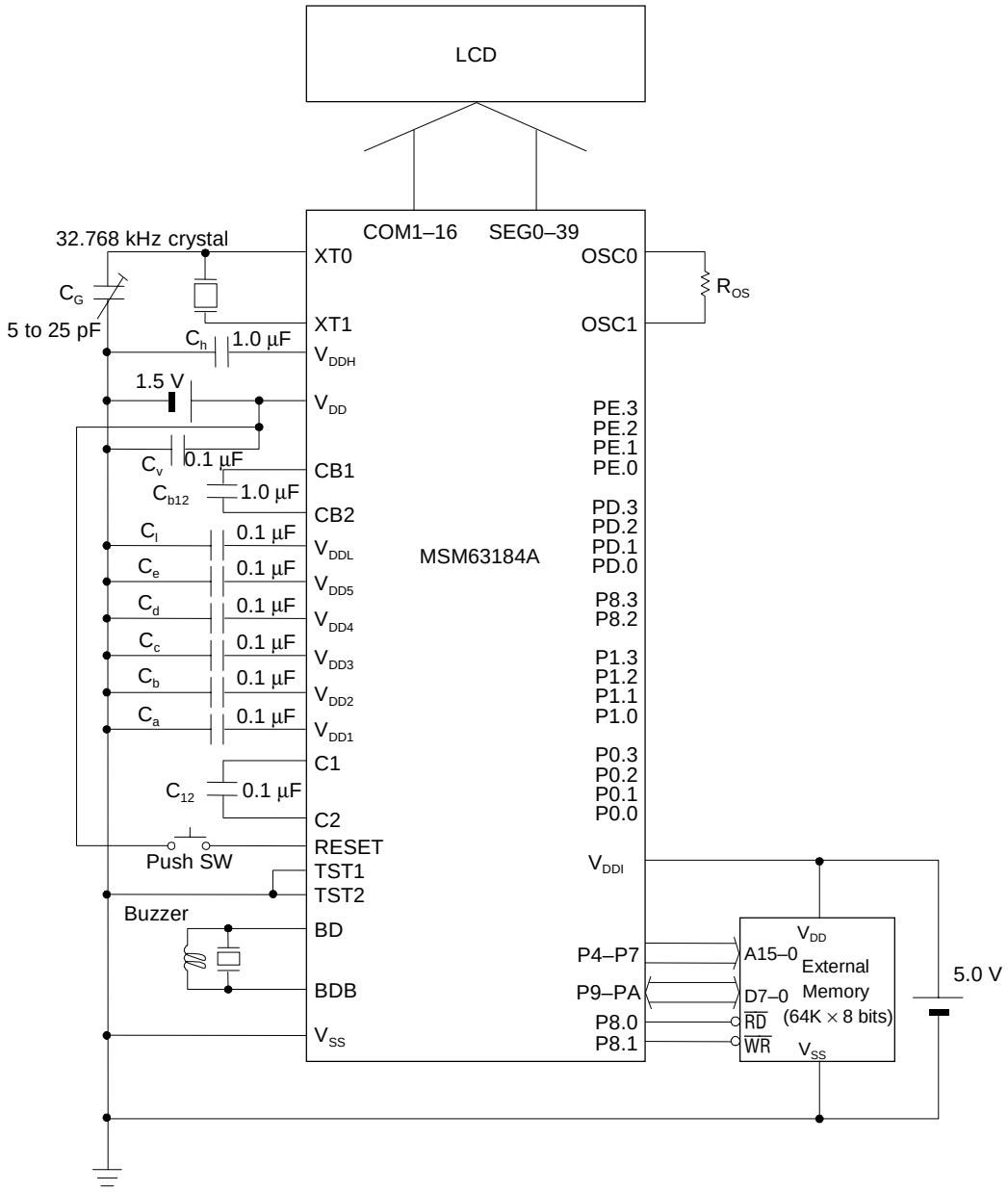
E. High-Speed Oscillation Circuit



F. RESET, TST1, and TST2 Inputs



Appendix D Application Circuit Examples

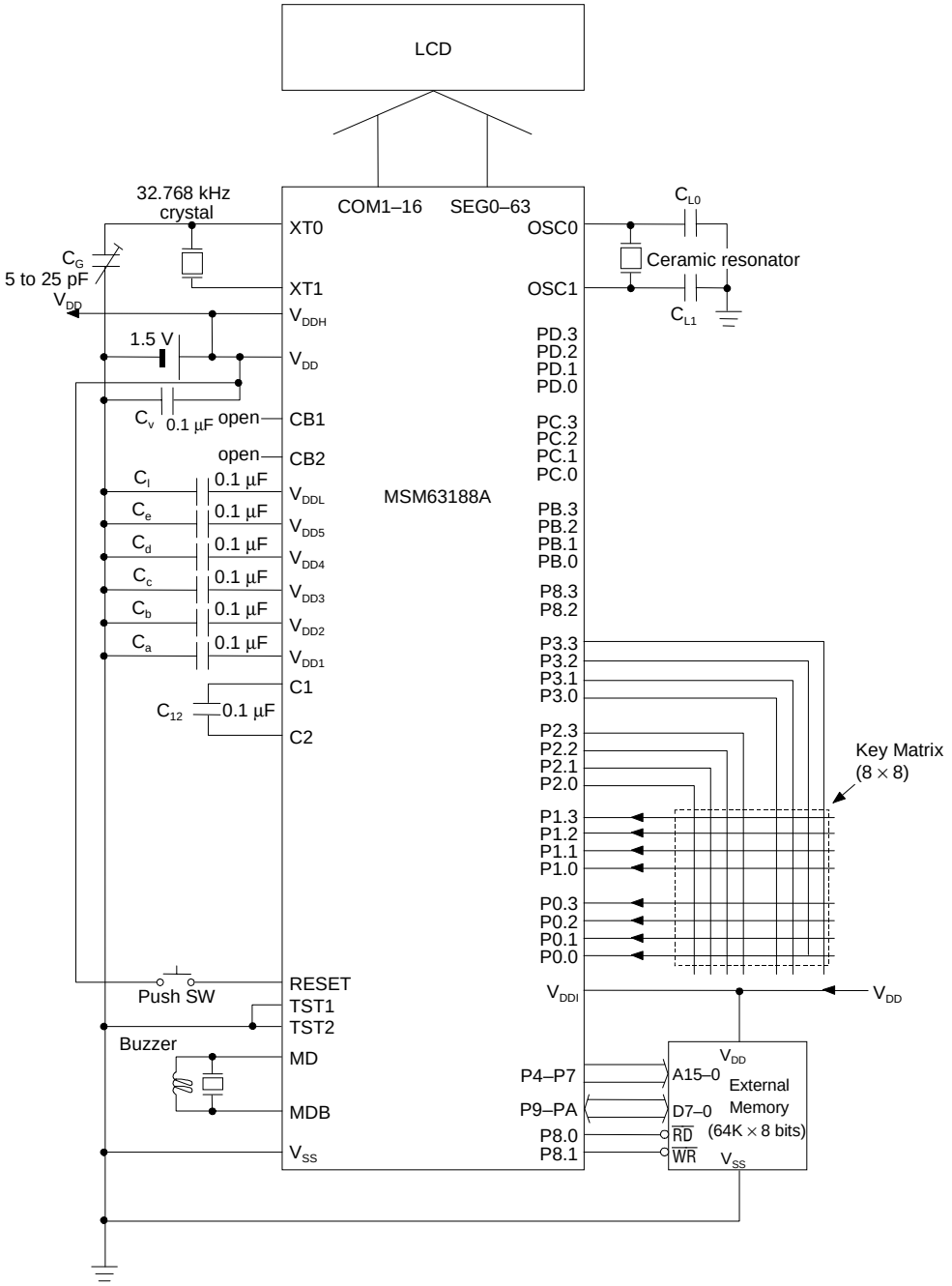


- RC oscillation is selected for high-speed oscillation.
- The power supply for the ports is shared with V_{DD}.
- C_V is an IC power supply bypass capacitor.
- Capacitance values for C_a, C_b, C_c, C_d, C_e, C_l, C_{b12}, C_{12}, C_h, and C_G are only for reference.

Figure D-1 Application Circuit Example with Power Supply Backup

Note:

V_{DDI} is the power supply pin for input, output, and I/O ports.
V_{DDI} must be connected to the positive power supply pin (V_{DD}) of the chip or the power supply pin of the external equipment.



- Ceramic oscillation is selected for high-speed oscillation.
- The power supply for the ports is shared with V_{DD}.
- C_V is an IC power supply bypass capacitor.
- Capacitance values for C_a, C_b, C_c, C_d, C_e, C_l, C_V, C_G, and C_{12} are only for reference.

Figure D-2 Application Circuit Example with No Backup

Note:

V_{DDI} is the power supply pin for input and I/O ports.
V_{DDI} must be connected to the positive power supply pin (V_{DD}) of the chip or the power supply pin of the external equipment.

Appendix E Electrical Characteristics

Absolute Maximum Ratings

(V_{SS} = 0 V)

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage 1	V_{DD1}	Ta = 25°C	–0.3 to +1.6	V
Supply Voltage 2	V_{DD2}	Ta = 25°C	–0.3 to +2.9	V
Supply Voltage 3	V_{DD3}	Ta = 25°C	–0.3 to +4.2	V
Supply Voltage 4	V_{DD4}	Ta = 25°C	–0.3 to +5.5	V
Supply Voltage 5	V_{DD5}	Ta = 25°C	–0.3 to +6.8	V
Supply Voltage 6	V_{DD}	Ta = 25°C	–0.3 to +6.0	V
Supply Voltage 7	V_{DDI}	Ta = 25°C	–0.3 to +6.0	V
Supply Voltage 8	V_{DDH}	Ta = 25°C	–0.3 to +6.0	V
Supply Voltage 9	V_{DDL}	Ta = 25°C	–0.3 to +6.0	V
Input Voltage 1	V_{IN1}	V_{DD} input, Ta = 25°C	–0.3 to V_{DD} + 0.3	V
Input Voltage 2	V_{IN2}	V_{DDI} input, Ta = 25°C	–0.3 to V_{DDI} + 0.3	V
Output Voltage 1	V_{OUT1}	V_{DD1} output, Ta = 25°C	–0.3 to V_{DD1} + 0.3	V
Output Voltage 2	V_{OUT2}	V_{DD2} output, Ta = 25°C	–0.3 to V_{DD2} + 0.3	V
Output Voltage 3	V_{OUT3}	V_{DD3} output, Ta = 25°C	–0.3 to V_{DD3} + 0.3	V
Output Voltage 4	V_{OUT4}	V_{DD4} output, Ta = 25°C	–0.3 to V_{DD4} + 0.3	V
Output Voltage 5	V_{OUT5}	V_{DD5} output, Ta = 25°C	–0.3 to V_{DD5} + 0.3	V
Output Voltage 6	V_{OUT6}	V_{DD} output, Ta = 25°C	–0.3 to V_{DD} + 0.3	V
Output Voltage 7	V_{OUT7}	V_{DDI} output, Ta = 25°C	–0.3 to V_{DDI} + 0.3	V
Output Voltage 8	V_{OUT8}	V_{DDH} output, Ta = 25°C	–0.3 to V_{DDH} + 0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

Recommended Operating Conditions

- When backup is used

(V_{SS} = 0 V)

Parameter	Symbol	Condition	Range	Unit
Operating Temperature	T_{OP}	—	–20 to +70	°C
Operating Voltage	V_{DD}	—	0.9 to 2 7	V
	V_{DDI}	—	0.9 to 5.5	V
Crystal Oscillation Frequency	f_{XT}	—	30 to 35	kHz
Ceramic Oscillation Frequency	f_{CM}	V_{DD} = 0.9 to 1.2 V	—	Hz
		V_{DD} = 1.2 to 2.7 V	300k to 500k	
		V_{DD} = 1.5 to 2.7 V	200k to 1M	
External RC Oscillator Resistance	R_{OS}	V_{DD} = 0.9 to 1.2 V	—	kΩ
		V_{DD} = 1.2 to 2.7 V	100 to 300	
		V_{DD} = 1.5 to 2.7 V	50 to 300	

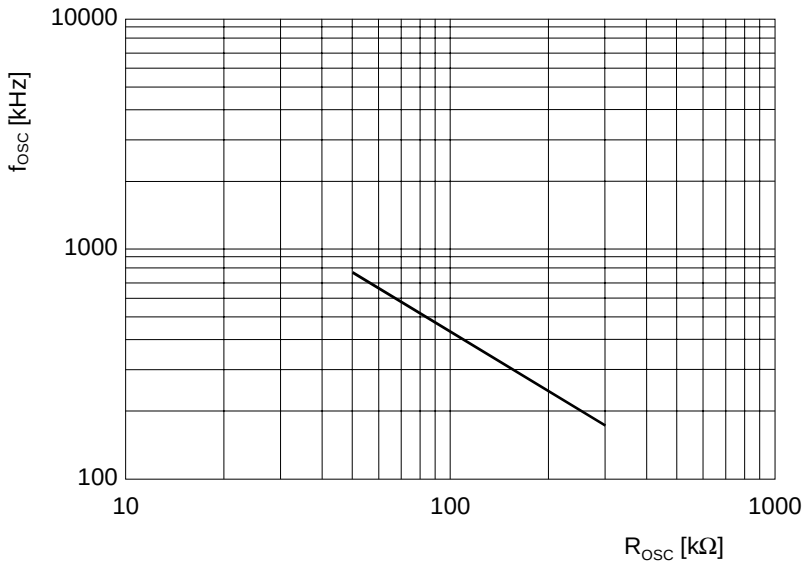
- When backup is not used

(V_{SS} = 0 V)

Parameter	Symbol	Condition	Range	Unit
Operating Temperature	T_{OP}	—	–20 to +70	°C
Operating Voltage	V_{DD}	—	1.8 to 5.5	V
	V_{DDI}	—	1.8 to 5.5	V
Crystal Oscillation Frequency	f_{XT}	—	30 to 35	kHz
Ceramic Oscillation Frequency	f_{CM}	V_{DD} = 1.8 to 5.5 V	300k to 500k	Hz
		V_{DD} = 2.2 to 5.5 V	300k to 1M	
		V_{DD} = 2.7 to 5.5 V	200k to 2M	
External RC Oscillator Resistance	R_{OS}	V_{DD} = 1.8 to 5.5 V	100 to 300	kΩ
		V_{DD} = 2.2 to 5.5 V	50 to 300	
		V_{DD} = 2.7 to 5.5 V	30 to 300	

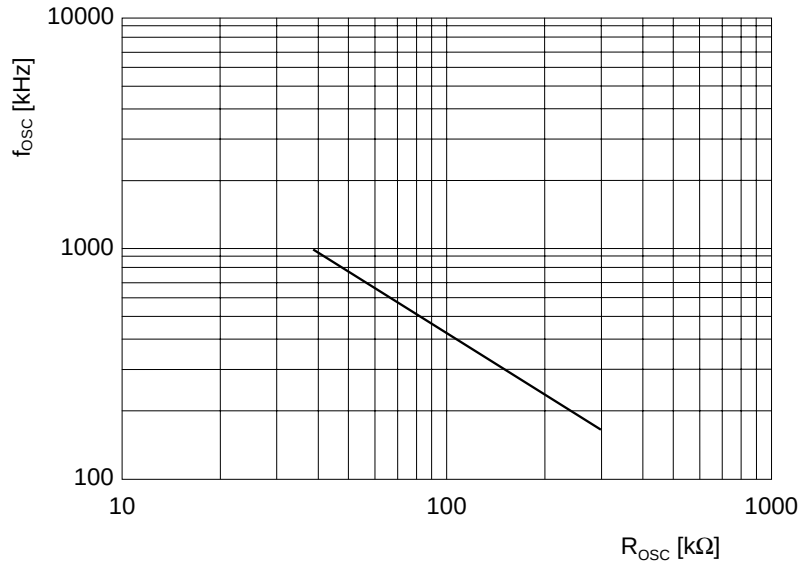
- Typical characteristics of high-speed RC oscillation
  When backup is used (V_{DD} = V_{DDI} = 1.5 V)

[Reference data]



- Typical characteristics of high-speed RC oscillation
  When backup is not used (V_{DD} = V_{DDI} = 3.0 V)

[Reference data]



DC Characteristics

(V_{DD} = V_{DDI} = 0.9 to 5.5 V, V_{SS} = 0 V, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
V_{DD2} Voltage	V_{DD2}	1/5 bias, 1/4 bias (Ta = 25°C)	1.7	1.8	1.9	V	
V_{DD2} Voltage Temperature Deviation	ΔV_{DD2}	—	—	–4	—	mV/°C	
V_{DD1} Voltage	V_{DD1}	1/5 bias, 1/4 bias	Typ. – 0.1	1/2 × V_{DD2}	Typ. + 0.1	V	
V_{DD3} Voltage	V_{DD3}	1/5 bias	Typ. – 0.3	3/2 × V_{DD2}	Typ. + 0.3	V	
		1/4 bias (short-circuit to V_{DD2})	Typ. – 0.2	V_{DD2}	Typ. + 0.2		
V_{DD4} Voltage	V_{DD4}	1/5 bias	Typ. – 0.4	2 × V_{DD2}	Typ. + 0.4	V	
		1/4 bias	Typ. – 0.3	3/2 × V_{DD2}	Typ. + 0.3		
V_{DD5} Voltage	V_{DD5}	1/5 bias	Typ. – 0.5	5/2 × V_{DD2}	Typ. + 0.5	V	
		1/4 bias	Typ. – 0.4	2 × V_{DD2}	Typ. + 0.4		
V_{DDH} Voltage (With backup)	V_{DDH}	V_{DD} = 1.5 V High speed clock: stopped	2.8	—	3.0	V	
		V_{DD} = 1.5 V High speed clock: oscillating (Ceramic oscillation 1 MHz)	2.0	—	2.7	V	
V_{DDL} Voltage	V_{DDL}	High speed clock: stopped	0.8	1.3	1.8	V	
		High speed clock: oscillating (V_{DD} = 1.2 to 5.5 V)	1.2	—	5.5	V	
Crystal Oscillation Start Voltage	V_{STA}	Oscillation start time: within 5 seconds	1.0	—	—	V	1
Crystal Oscillation Hold Voltage	V_{HOLD}	With backup	0.9	—	—	V	
		With no backup	1.7	—	—	V	
Crystal Oscillation Stop Detect Time	T_{STOP}	—	0.1	—	5.0	ms	
External Crystal Oscillator Capacitance	C_G	—	5	—	25	pF	
Internal Crystal Oscillator Capacitance	C_D	—	20	25	30	pF	
External Ceramic Oscillator Capacitance	C_{L0}, C_{L1}	CSA2.00MG (Murata MFG.-make) used V_{DD} = 3.0 V	—	30	—	pF	
Internal RC Oscillator Capacitance	C_{OS}	—	8	12	16	pF	
POR Voltage	V_{POR1}	V_{DD} = 1.5 V	0	—	0.4	V	
		V_{DD} = 3.0 V	0	—	0.7	V	
Non-POR Voltage	V_{POR2}	V_{DD} = 1.5 V	1.2	—	1.5	V	
		V_{DD} = 3.0 V	2.0	—	3.0	V	

Notes:

1. "V_{DD2}" changes in the range from 1.8 to 2.4 V according to the value of Display Contrast register (DSPCNT).
2. "T_{STOP}" means that if XTOSC stops over 5 ms, the system is reset.
3. "POR" denotes Power ON Reset.
4. "V_{POR1}" indicates that POR occurs when V_{DD} falls from V_{DD} to V_{POR1} and again rises up to V_{DD}.
5. "V_{POR2}" indicates that POR does not occur when V_{DD} falls from V_{DD} to V_{POR2} and again rises up to V_{DD}.

DC Characteristics (MSM63182A only)

- When backup is used

(V_{DD} = V_{DDI} = 1.5 V, V_{SS} = 0 V, 1/5 bias, DSPCNT = 0H, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring Circuit
Supply Current 1	I_{DD1}	CPU is in HALT state. (High-speed clock oscillation stopped)	Ta = –20 to +50°C	—	5.1	6.5	µA	1
			Ta = –20 to +70°C	—	5.1	7.0		
Supply Current 2	I_{DD2}	CPU is in HALT state. LCD is in Power Down mode. (High-speed clock oscillation stopped)	Ta = –20 to +50°C	—	3.9	5.0	µA	
			Ta = –20 to +70°C	—	3.9	7.0		
Supply Current 3	I_{DD3}	CPU is in operation at low-speed oscillation. (High-speed clock oscillation stopped)		—	13	17	µA	
Supply Current 4	I_{DD4}	CPU is in operation at high-speed oscillation (RC oscillation, f = approx. 720 kHz, R_{OS} = 51 kΩ)		—	600	800	µA	
Supply Current 5	I_{DD5}	CPU is in operation at high-speed oscillation (Ceramic oscillation, 1 MHz)		—	700	900	µA	

- When backup is not used

(V_{DD} = V_{DDI} = 3.0 V, V_{SS} = 0 V, 1/5 bias, DSPCNT = 0H, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring Circuit
Supply Current 1	I_{DD1}	CPU is in HALT state. (High-speed clock oscillation stopped)	Ta = –20 to +50°C	—	2.4	2.8	µA	1
			Ta = –20 to +70°C	—	2.4	3.0		
Supply Current 2	I_{DD2}	CPU is in HALT state. LCD is in Power Down mode. (High-speed clock oscillation stopped)	Ta = –20 to +50°C	—	1.7	2.2	µA	
			Ta = –20 to +70°C	—	1.7	2.5		
Supply Current 3	I_{DD3}	CPU is in operation at low-speed oscillation. (High-speed clock oscillation stopped)		—	6.3	8.0	µA	
Supply Current 4	I_{DD4}	CPU is in operation at high-speed oscillation (RC oscillation)	f = approx. 800 kHz, R_{OS} = 51 kΩ	—	450	600	µA	
			f = approx. 500 kHz, R_{OS} = 100 kΩ	—	350	450		
Supply Current 5	I_{DD5}	CPU is in operation at high-speed oscillation (Ceramic oscillation, 2 MHz)		—	850	1000	µA	

DC Characteristics (MSM63184A only)

- When backup is used

(V_{DD} = V_{DDI} = 1.5 V, V_{SS} = 0 V, 1/5 bias, DSPCNT = 0H, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring Circuit
Supply Current 1	I_{DD1}	CPU is in HALT state. (High-speed clock oscillation stopped)	Ta = –20 to +50°C	—	5.3	6.5	µA	1
			Ta = –20 to +70°C	—	5.3	8.0		
Supply Current 2	I_{DD2}	CPU is in HALT state. LCD is in Power Down mode. (High-speed clock oscillation stopped)	Ta = –20 to +50°C	—	4.2	5.0	µA	
			Ta = –20 to +70°C	—	4.2	6.5		
Supply Current 3	I_{DD3}	CPU is in operation at low-speed oscillation. (High-speed clock oscillation stopped)		—	15	20	µA	
Supply Current 4	I_{DD4}	CPU is in operation at high-speed oscillation (RC oscillation, f = approx. 720 kHz, R_{OS} = 51 kΩ)		—	600	800	µA	
Supply Current 5	I_{DD5}	CPU is in operation at high-speed oscillation (Ceramic oscillation, 1 MHz)		—	700	900	µA	

- When backup is not used

(V_{DD} = V_{DDI} = 3.0 V, V_{SS} = 0 V, 1/5 bias, DSPCNT = 0H, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring Circuit
Supply Current 1	I_{DD1}	CPU is in HALT state. (High-speed clock oscillation stopped)	Ta = –20 to +50°C	—	2.4	2.9	µA	1
			Ta = –20 to +70°C	—	2.4	3.4		
Supply Current 2	I_{DD2}	CPU is in HALT state. LCD is in Power Down mode. (High-speed clock oscillation stopped)	Ta = –20 to +50°C	—	1.8	2.2	µA	
			Ta = –20 to +70°C	—	1.8	2.8		
Supply Current 3	I_{DD3}	CPU is in operation at low-speed oscillation. (High-speed clock oscillation stopped)		—	7.2	9.0	µA	
Supply Current 4	I_{DD4}	CPU is in operation at high-speed oscillation (RC oscillation)	f = approx. 800 kHz, R_{OS} = 51 kΩ	—	450	600	µA	
			f = approx. 500 kHz, R_{OS} = 100 kΩ	—	350	450		
Supply Current 5	I_{DD5}	CPU is in operation at high-speed oscillation (Ceramic oscillation, 2 MHz)		—	850	1000	µA	

DC Characteristics (MSM63188A only)

- When backup is used

(V_{DD} = V_{DDI} = 1.5 V, V_{SS} = 0 V, 1/5 bias, DSPCNT = 0H, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring Circuit
Supply Current 1	I_{DD1}	CPU is in HALT state. (High-speed clock oscillation stopped)	Ta = –20 to +50°C	—	5.6	7.0	µA	1
			Ta = –20 to +70°C	—	5.6	8.5		
Supply Current 2	I_{DD2}	CPU is in HALT state. LCD is in Power Down mode. (High-speed clock oscillation stopped)	Ta = –20 to +50°C	—	4.5	5.5	µA	
			Ta = –20 to +70°C	—	4.5	7.0		
Supply Current 3	I_{DD3}	CPU is in operation at low-speed oscillation. (High-speed clock oscillation stopped)		—	18	22	µA	
Supply Current 4	I_{DD4}	CPU is in operation at high-speed oscillation (RC oscillation, f = approx. 720 kHz, R_{OS} = 51 kΩ)		—	700	900	µA	
Supply Current 5	I_{DD5}	CPU is in operation at high-speed oscillation (Ceramic oscillation, 1 MHz)		—	800	1000	µA	

- When backup is not used

(V_{DD} = V_{DDI} = 3.0 V, V_{SS} = 0 V, 1/5 bias, DSPCNT = 0H, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring Circuit
Supply Current 1	I_{DD1}	CPU is in HALT state. (High-speed clock oscillation stopped)	Ta = –20 to +50°C	—	2.7	3.0	µA	1
			Ta = –20 to +70°C	—	2.7	3.5		
Supply Current 2	I_{DD2}	CPU is in HALT state. LCD is in Power Down mode. (High-speed clock oscillation stopped)	Ta = –20 to +50°C	—	2.1	2.4	µA	
			Ta = –20 to +70°C	—	2.1	3.0		
Supply Current 3	I_{DD3}	CPU is in operation at low-speed oscillation. (High-speed clock oscillation stopped)		—	8.5	10.5	µA	
Supply Current 4	I_{DD4}	CPU is in operation at high-speed oscillation (RC oscillation)	f = approx. 800 kHz, R_{OS} = 51 kΩ	—	550	800	µA	
			f = approx. 500 kHz, R_{OS} = 100 kΩ	—	390	450		
Supply Current 5	I_{DD5}	CPU is in operation at high-speed oscillation (Ceramic oscillation, 2 MHz)		—	1000	1500	µA	

DC Characteristics

(V_{DD} = V_{DDI} = V_{DDH} = 3.0 V, V_{SS} = 0 V, V_{DD1} = 1.1 V, V_{DD2} = 2.2 V, V_{DD3} = 3.3 V, V_{DD4} = 4.4 V, V_{DD5} = 5.5 V, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring Circuit
Output Current 1 (P2.0–P2.3) (P3.0–P3.3) (P4.0–P4.3) : (PE.0–PE.3)	I_{OH1}	V_{OH1} = V_{DDI} – 0.5 V	V_{DDI} = 1.5 V	–2.0	–1.2	–0.2	mA	
			V_{DDI} = 3.0 V	–5.0	–3.0	–1.0	mA	
			V_{DDI} = 5.0 V	–8.0	–4.0	–1.5	mA	
	I_{OL1}	V_{OL1} = 0.5 V	V_{DDI} = 1.5 V	0.2	1.2	2.0	mA	
			V_{DDI} = 3.0 V	1.0	3.0	5.0	mA	
			V_{DDI} = 5.0 V	1.5	4.0	8.0	mA	
Output Current 2 (BD, BDB) (MD, MDB)	I_{OH2}	V_{OH2} = V_{DD} – 0.7 V	V_{DDI} = 1.5 V	–2.5	–1.3	–0.4	mA	
			V_{DDI} = 3.0 V	–6.0	–4.0	–2.0	mA	
			V_{DD} = V_{DDH} = 5.0 V	–9.0	–5.5	–3.0	mA	
	I_{OL2}	V_{OL2} = 0.7 V	V_{DDI} = 1.5 V	0.4	1.3	2.5	mA	
			V_{DDI} = 3.0 V	2.0	4.0	6.0	mA	
			V_{DD} = V_{DDH} = 5.0 V	3.0	5.5	9.0	mA	
Output Current 3 (SEG0–SEG63) (COM1–COM16)	I_{OH3}	V_{OH3} = V_{DD5} – 0.2 V (V_{DD5} level)		—	—	–4	µA	2
	I_{OHM3}	V_{OHM3} = V_{DD4} + 0.2 V (V_{DD4} level)		4	—	—	µA	
	I_{OHM3S}	V_{OHM3S} = V_{DD4} – 0.2 V (V_{DD4} level)		—	—	–4	µA	
	I_{OMH3}	V_{OMH3} = V_{DD3} + 0.2 V (V_{DD3} level)		4	—	—	µA	
	I_{OMH3S}	V_{OMH3S} = V_{DD3} – 0.2 V (V_{DD3} level)		—	—	–4	µA	
	I_{OML3}	V_{OML3} = V_{DD2} + 0.2 V (V_{DD2} level)		4	—	—	µA	
	I_{OML3S}	V_{OML3S} = V_{DD2} – 0.2 V (V_{DD2} level)		—	—	–4	µA	
	I_{OLM3}	V_{OLM3} = V_{DD1} + 0.2 V (V_{DD1} level)		4	—	—	µA	
	I_{OLM3S}	V_{OLM3S} = V_{DD1} – 0.2 V (V_{DD1} level)		—	—	–4	µA	
	I_{OL3}	V_{OL3} = V_{SS} + 0.2 V (V_{SS} level)		4	—	—	µA	
Output Current 4 (OSC1)	I_{OH4R}	V_{OH4R} = V_{DDH} – 0.5 V (RC OSC mode)	V_{DD} = V_{DDH} = 3.0 V	–2.5	–1.5	–0.75	mA	
			V_{DD} = V_{DDH} = 5.0 V	–3.5	–2.0	–1.0	mA	
	I_{OL4R}	V_{OL4R} = 0.5 V (RC OSC mode)	V_{DD} = V_{DDH} = 3.0 V	0.75	1.5	2.5	mA	
			V_{DD} = V_{DDH} = 5.0 V	1.0	2.0	3.5	mA	
	I_{OH4C}	V_{OH4C} = V_{DDH} – 0.5 V (Ceramic OSC mode)	V_{DD} = V_{DDH} = 3.0 V	–300	–180	–60	µA	
			V_{DD} = V_{DDH} = 5.0 V	–450	–280	–100	µA	
	I_{OL4C}	V_{OL4C} = 0.5 V (Ceramic OSC mode)	V_{DD} = V_{DDH} = 3.0 V	60	180	300	µA	
			V_{DD} = V_{DDH} = 5.0 V	100	280	450	µA	
Output Leakage (P2.0–P2.3) (P3.0–P3.3) (P4.0–P4.3) : (PE.0–PE.3)	I_{OOH}	V_{OH} = V_{DDI}		—	—	0.3	µA	
	I_{OOL}	V_{OL} = V_{SS}		–0.3	—	—	µA	

DC Characteristics

($V_{DD} = V_{DDI} = V_{DDH} = 3.0$ V, $V_{SS} = 0$ V, $V_{DD1} = 1.1$ V, $V_{DD2} = 2.2$ V, $V_{DD3} = 3.3$ V, $V_{DD4} = 4.4$ V, $V_{DD5} = 5.5$ V, Ta = –20 to +70°C unless otherwise specified)

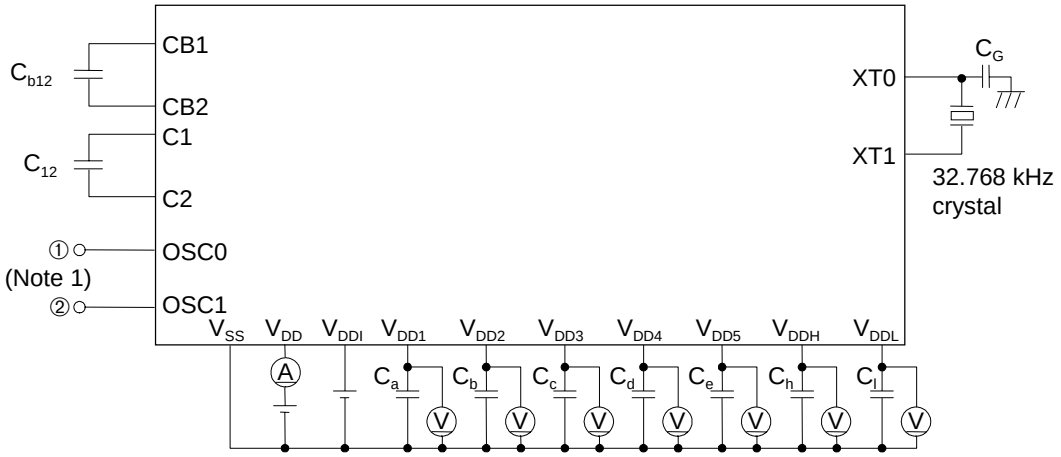
Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring Circuit
Input Current 1 (P0.0–P0.3) (P1.0–P1.3) (P8.0–P8.3) (P9.0–P9.3) : (PE.0–PE.3)	I_{IH1}	$V_{IH1} = V_{DDI}$ (when pulled down)	V_{DDI} = 1.5 V	2	10	30	µA	3
			V_{DDI} = 3.0 V	30	90	180	µA	
			V_{DDI} = 5.0 V	70	250	600	µA	
	I_{IL1}	$V_{IL1} = V_{SS}$ (when pulled up)	V_{DDI} = 1.5 V	–30	–10	–2	µA	
			V_{DDI} = 3.0 V	–180	–90	–30	µA	
			V_{DDI} = 5.0 V	–600	–250	–70	µA	
	I_{IH1Z}	$V_{IH1} = V_{DDI}$ (High impedance)		0	—	1	µA	
	I_{IL1Z}	$V_{IL1} = V_{SS}$ (high impedance)		–1	—	0	µA	
Input Current 2 (OSC0)	I_{IL2}	$V_{IL2} = V_{SS}$ (when pulled up)	$V_{DD} = V_{DDH}$ = 3.0 V	–200	–110	–30	µA	
			$V_{DD} = V_{DDH}$ = 5.0 V	–600	–350	–50	µA	
	I_{IH2R}	$V_{IH2} = V_{DDH}$ (RC OSC mode)		0	—	1	µA	
	I_{IL2R}	$V_{IL2} = V_{SS}$ (RC OSC mode)		–1	—	0	µA	
	I_{IH2C}	$V_{IH2} = V_{DDH}$ (Ceramic OSC mode)	$V_{DD} = V_{DDH}$ = 3.0 V	0.1	0.5	1.0	µA	
			$V_{DD} = V_{DDH}$ = 5.0 V	0.75	1.5	3.0	µA	
	I_{IL2C}	$V_{IL2} = V_{SS}$ (Ceramic OSC mode)	$V_{DD} = V_{DDH}$ = 3.0 V	–1.0	–0.5	–0.1	µA	
			$V_{DD} = V_{DDH}$ = 5.0 V	–3.0	–1.5	–0.75	µA	
Input Current 3 (RESET)	I_{IH3}	$V_{IH3} = V_{DD}$ (when pulled down)	V_{DD} = 1.5 V	10	50	80	µA	
			V_{DD} = 3.0 V	150	350	600	µA	
			$V_{DD} = V_{DDH}$ = 5.0 V	0.5	1.0	2.0	mA	
	I_{IL3}	$V_{IL3} = V_{SS}$		–1	—	0	µA	
Input Current 4 (TST1, TST2)	I_{IH4}	$V_{IH4} = V_{DD}$	V_{DD} = 1.5 V	50	150	300	µA	
			V_{DD} = 3.0 V	0.5	1.0	1.5	mA	
			$V_{DD} = V_{DDH}$ = 5.0 V	1.25	2.5	4.0	mA	
	I_{IL4}	$V_{IL4} = V_{SS}$		–1	—	0	µA	

DC Characteristics

(V_{DD} = V_{DDI} = V_{DDH} = 3.0 V, V_{SS} = 0 V, V_{DD1} = 1.1 V, V_{DD2} = 2.2 V, V_{DD3} = 3.3 V, V_{DD4} = 4.4 V, V_{DD5} = 5.5 V, Ta = –20 to +70°C unless otherwise specified)

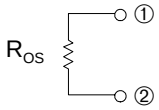
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Input Voltage 1 (P0.0–P0.3) (P1.0–P1.3) (P8.0–P8.3) (P9.0–P9.3) : (PE.0–PE.3)	V_{IH1}	V_{DDI} = 1.5 V	1.2	—	1.5	V	4
		V_{DDI} = 3.0 V	2.4	—	3.0	V	
		V_{DDI} = 5.0 V	4.0	—	5.0	V	
	V_{IL1}	V_{DDI} = 1.5 V	0	—	0.3	V	
		V_{DDI} = 3.0 V	0	—	0.6	V	
		V_{DDI} = 5.0 V	0	—	1.0	V	
Input Voltage 2 (OSC0)	V_{IH2}	V_{DD} = V_{DDH} = 3.0 V	2.4	—	3.0	V	
		V_{DD} = V_{DDH} = 5.0 V	4.0	—	5.0	V	
	V_{IL2}	V_{DD} = V_{DDH} = 3.0 V	0	—	0.6	V	
		V_{DD} = V_{DDH} = 5.0 V	0	—	1.0	V	
Input Voltage 3 (RESET, TST1, TST2)	V_{IH3}	V_{DD} = 1.5 V	1.35	—	1.5	V	
		V_{DD} = 3.0 V	2.4	—	3.0	V	
		V_{DD} = V_{DDH} = 5.0 V	4.0	—	5.0	V	
	V_{IL3}	V_{DD} = 1.5 V	0	—	0.15	V	
		V_{DD} = 3.0 V	0	—	0.6	V	
		V_{DD} = V_{DDH} = 5.0 V	0	—	1.0	V	
Hysteresis Width 1 (P0.0–P0.3) (P1.0–P1.3) (P8.0–P8.3) : (PE.0–PE.3)	ΔV_{T1}	V_{DDI} = 1.5 V	0.05	0.1	0.3	V	
		V_{DDI} = 3.0 V	0.2	0.5	1.0	V	
		V_{DDI} = 5.0 V	0.25	1.0	1.5	V	
Hysteresis Width 2 (RESET, TST1, TST2)	ΔV_{T2}	V_{DD} = 1.5 V	0.05	0.1	0.3	V	
		V_{DD} = 3.0 V	0.2	0.5	1.0	V	
		V_{DD} = V_{DDH} = 5.0 V	0.25	1.0	1.5	V	
Input Pin Capacitance (P0.0–P0.3) (P1.0–P1.3) (P8.0–P8.3) (P9.0–P9.3) : (PE.0–PE.3)	C_{IN}	—	—	—	5	pF	1

Measuring Circuit 1

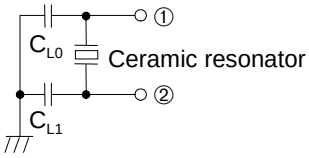


C_a, C_b, C_c, C_d, C_e, C_l, C_{12}	: 0.1 µF
C_h, C_{b12}	: 1 µF
C_G	: 15 pF
C_{L0}	: 30 pF
C_{L1}	: 30 pF
Ceramic resonator	: CSA2.00MG (2 MHz) : CSB1000J (1 MHz) (Murata MFG.-make)

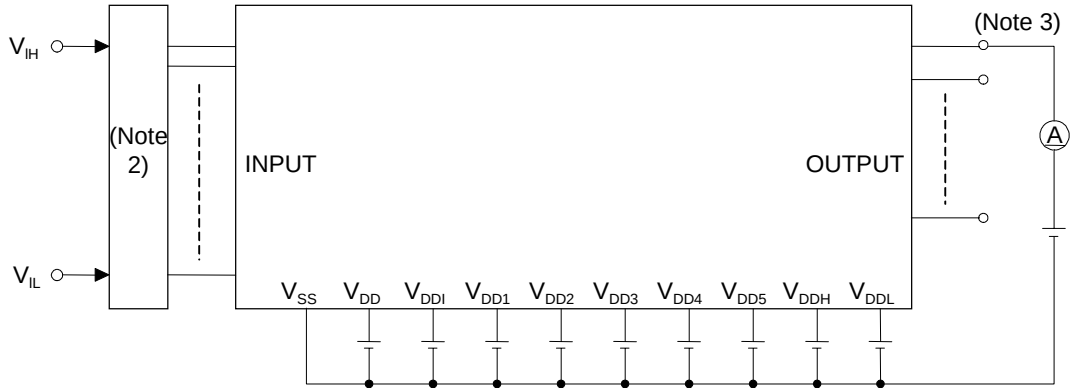
(Note 1) For RC oscillation:



For ceramic oscillation:

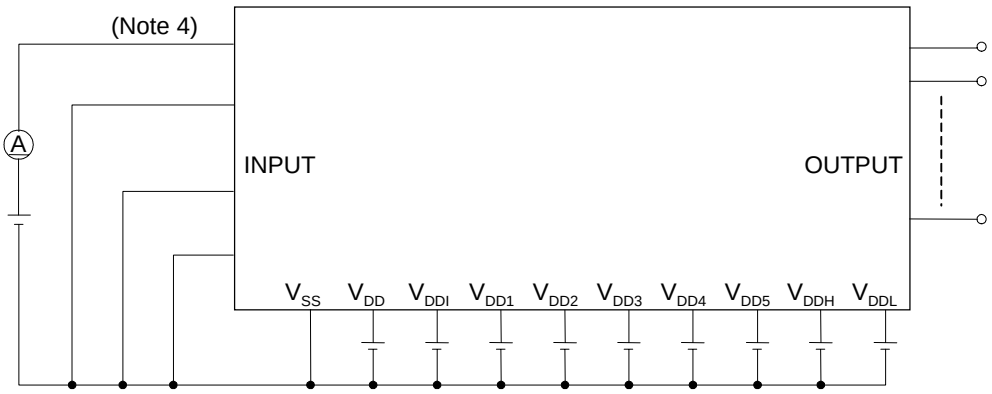


Measuring Circuit 2

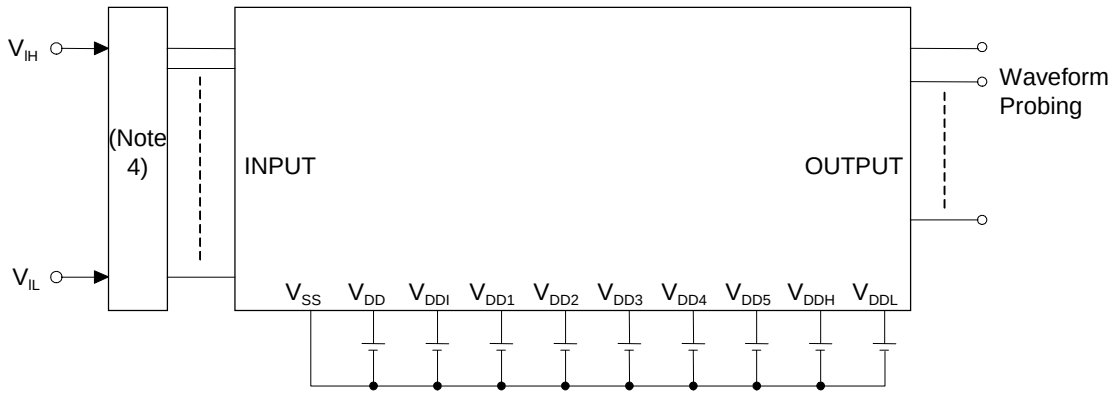


(Note 2) Input logic circuit to determine the specified measuring conditions.
(Note 3) Measured at the specified output pins.

Measuring Circuit 3



Measuring Circuit 4



(Note 4) Measured at the specified input pins.

AC Characteristics (Serial Interface, Serial Port)

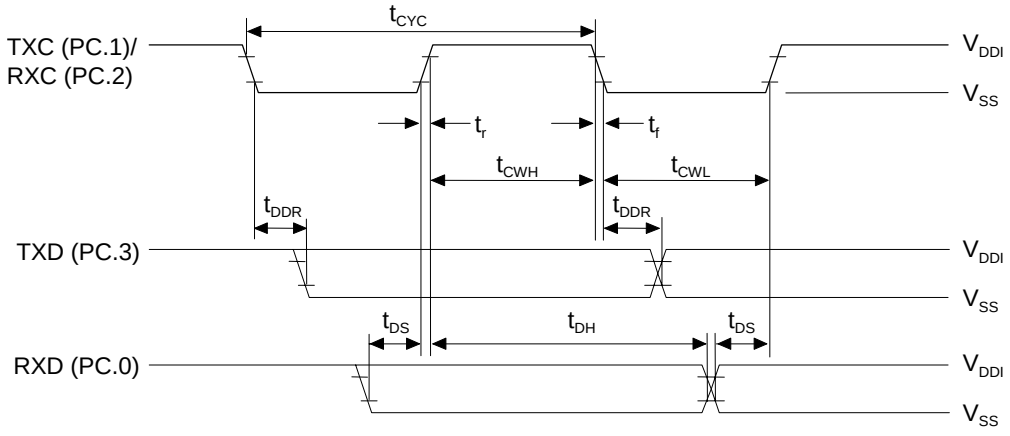
(V_{DD} = 0.9 to 5.5 V, V_{DDH} = 1.8 to 5.5 V, V_{SS} = 0 V, V_{DDI} = 5.0 V, Ta = –20 to +70°C unless otherwise specified)

(1) Synchronous Communication

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
TXC/RXC Input Fall Time	t_f	—	—	—	1.0	µs
TXC/RXC Input Rise Time	t_r	—	—	—	1.0	µs
TXC/RXC Input "L" Level Pulse Width	t_{CWL}	—	0.8	—	—	µs
TXC/RXC Input "H" Level Pulse Width	t_{CWH}	—	0.8	—	—	µs
TXC/RXC Input Cycle Time	t_{CYC}	—	2.0	—	—	µs
TXC/RXC Output Cycle Time	$C_{CYC1(O)}$	CPU in operation at 32 kHz	—	30.5	—	µs
	$C_{CYC2(O)}$	CPU is in operation at 2 MHz V_{DD} = V_{DDH} = 2.7 to 5.5 V	—	0.5	—	µs
TXD Output Delay Time	t_{DDR}	Output load capacitance 10 pF	—	—	0.4	µs
RXD Input Setup Time	t_{DS}	—	0.5	—	—	µs
RXD Input Hold Time	t_{DH}	—	0.8	—	—	µs

Synchronous Communication Timing Waveforms

("H" level = 4.0 V, "L" level = 1.0 V)



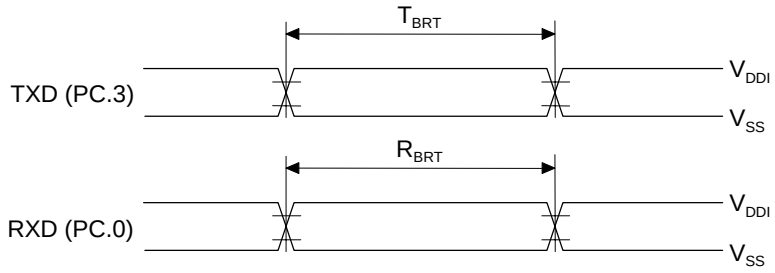
(2) UART Communication

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Transmit Baud Rate	T_{BRT}	$T_{BRT} = 1/f_{BRT}$ $T_{CR} = 1/f_{OSC}$	$T_{BRT} - T_{CR}$	T_{BRT}	$T_{BRT} + T_{CR}$	s
Receive Baud Rate	R_{BRT}	$R_{BRT} = 1/f_{BRT}$	$R_{BRT} \times 0.97$	R_{BRT}	$R_{BRT} \times 1.03$	s

f_{BRT}: Baud rates (1200, 2400, 4800, 9600 bps)

UART Communication Timing Waveforms

("H" level = 4.0 V, "L" level = 1.0 V)



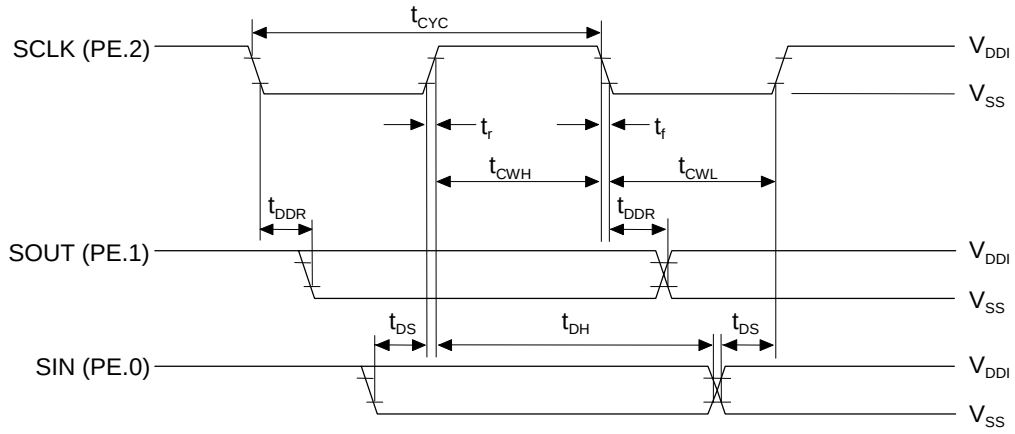
AC Characteristics (Serial Interface, Shift Register)

(V_{DD} = 0.9 to 5.5 V, V_{DDH} = 1.8 to 5.5 V, V_{SS} = 0 V, V_{DDI} = 5.0 V, Ta = –20 to +70°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCLK Input Fall Time	t_f	—	—	—	1.0	µs
SCLK Input Rise Time	t_r	—	—	—	1.0	µs
SCLK Input "L" Level Pulse Width	t_{CWL}	—	0.8	—	—	µs
SCLK Input "H" Level Pulse Width	t_{CWH}	—	0.8	—	—	µs
SCLK Input Cycle Time	t_{CYC}	V_{DDI} = 5 V to V_{DD}	1.8	—	—	µs
SLCK Output Cycle Time	$t_{CYC1(O)}$	CPU in operation at 32 kHz	—	30.5	—	µs
	$t_{CYC2(O)}$	CPU is in operation at 2 MHz V_{DD} = V_{DDH} = 2.7 to 5.5 V	—	0.5	—	µs
SOUT Output Delay Time	t_{DDR}	Output load capacitance 10 pF	—	—	0.4	µs
SIN Input Setup Time	t_{DS}	—	0.5	—	—	µs
SIN Input Hold Time	t_{DH}	—	0.8	—	—	µs

AC Timing Waveforms

("H" level = 4.0 V, "L" level = 1.0 V)



AC Characteristics (External Memory Interface)

(V_{DD} = 0.9 to 5.5 V, V_{DDH} = 1.8 to 5.5 V, V_{SS} = 0 V, V_{DDI} = 5.0 V, Ta = –20 to +70°C unless otherwise specified)

(1) Reading from external memory

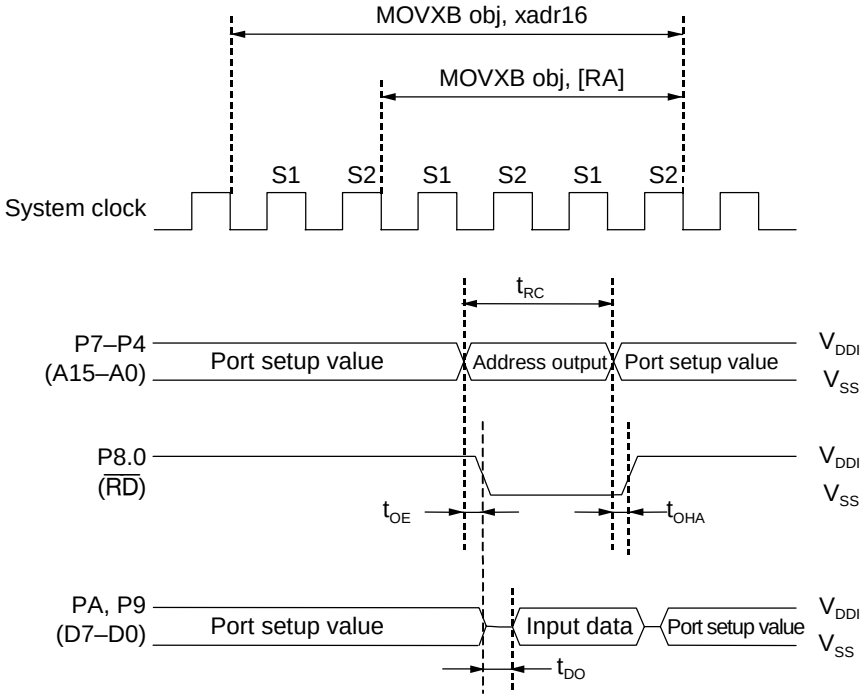
(a) When the CPU operates at 32.768 kHz

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Read Cycle Time	t_{RC}	—	—	61	—	µs
$\overline{RD}$ Output Delay Time	t_{OE}	—	—	—	5	µs
Output Valid Time	t_{OHA}	—	—	—	5	µs
External Memory Output Delay Time	t_{DO}	—	—	—	5	µs

(b) When the CPU operates at 2 MHz (V_{DDH} = 2.7 to 5.5 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Read Cycle Time	t_{RC}	—	1	—	—	µs
$\overline{RD}$ Output Delay Time	t_{OE}	—	—	—	100	ns
Output Valid Time	t_{OHA}	—	—	—	100	ns
External Memory Output Delay Time	t_{DO}	—	—	—	150	ns

AC Characteristics Timing ("H" level = 4.0 V, "L" level = 1.0 V)



(2) Writing to external memory

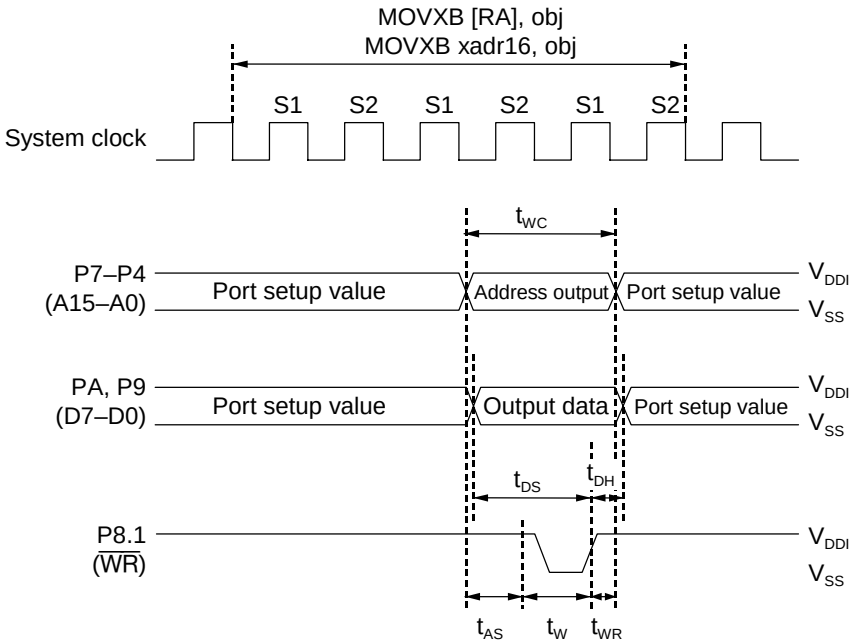
(a) When the CPU operates at 32.768 kHz

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Write Cycle Time	t_{WC}	—	—	61	—	µs
Address Setup Time	t_{AS}	—	—	30.5	—	µs
Write Time	t_{W}	—	—	15.3	—	µs
Write Recovery Time	t_{WR}	—	—	15.3	—	µs
Data Setup Time	t_{DS}	—	—	45.8	—	µs
Data Hold Time	t_{DH}	—	—	15.3	—	µs

(b) When the CPU operates at 2 MHz (V_{DDH} = 2.7 to 5.5 V)

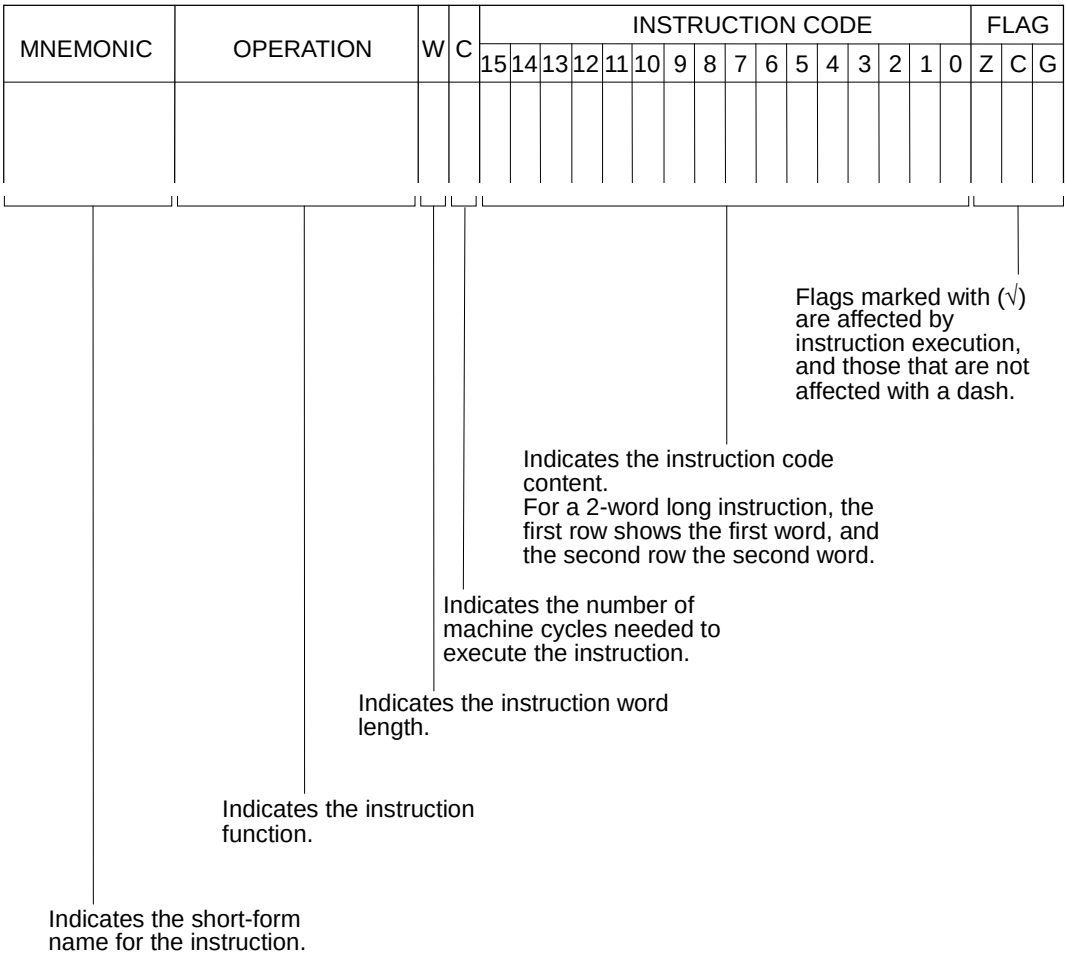
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Write Cycle Time	t_{WC}	—	1	—	—	µs
Address Setup Time	t_{AS}	—	0.4	—	—	µs
Write Time	t_{W}	—	0.2	—	—	µs
Write Recovery Time	t_{WR}	—	0.2	—	—	µs
Data Setup Time	t_{DS}	—	0.7	—	—	µs
Data Hold Time	t_{DH}	—	0.2	—	—	µs

AC Characteristics Timing ("H" level = 4.0 V, "L" level = 1.0 V)



Appendix F Instruction List

The format used in the list of instructions is indicated below.



Transfer Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
MOV direct,A	direct ← A	1	1	1	1	0	0	r_{11}	r_{10}	r_9	r_8	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	—	—	—
MOV [HL],A	[HL] ← A	1	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	—	—	—
MOV [XY],A	[XY] ← A	1	1	0	0	0	0	0	1	0	0	0	0	1	1	0	0	0	0	—	—	—
MOV E:[HL],A	E:[HL] ← A	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	—	—	—
MOV E:[XY],A	E:[XY] ← A	1	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	—	—	—
MOV [HL+],A	[HL] ← A, HL ← HL + 1	1	1	0	0	0	0	0	1	0	0	0	0	1	0	1	0	0	0	—	—	√
MOV [XY+],A	[XY] ← A, XY ← XY + 1	1	1	0	0	0	0	0	1	0	0	0	0	1	1	1	0	0	0	—	—	√
MOV E:[HL+],A	E:[HL] ← A, HL ← HL + 1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	—	—	√
MOV E:[XY+],A	E:[XY] ← A, XY ← XY + 1	1	1	0	0	0	0	0	1	0	0	0	0	0	1	1	0	0	0	—	—	√
MOV \cur,#i4	cur,A ← i4	1	1	0	1	0	0	i_3	i_2	i_1	i_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
MOV [HL],#i4	[HL],A ← i4	1	1	0	0	0	0	0	1	1	0	0	1	1	0	i_3	i_2	i_1	i_0	√	—	—
MOV [XY],#i4	[XY],A ← i4	1	1	0	0	0	0	0	1	1	0	0	1	1	1	i_3	i_2	i_1	i_0	√	—	—
MOV E:[HL],#i4	E:[HL],A ← i4	1	1	0	0	0	0	0	1	1	0	0	1	0	0	i_3	i_2	i_1	i_0	√	—	—
MOV E:[XY],#i4	E:[XY],A ← i4	1	1	0	0	0	0	0	1	1	0	0	1	0	1	i_3	i_2	i_1	i_0	√	—	—
MOV [HL+],#i4	[HL],A ← i4, HL ← HL + 1	1	1	0	0	0	0	0	1	1	1	0	1	1	0	i_3	i_2	i_1	i_0	√	—	√
MOV [XY+],#i4	[XY],A ← i4, XY ← XY + 1	1	1	0	0	0	0	0	1	1	1	0	1	1	1	i_3	i_2	i_1	i_0	√	—	√
MOV E:[HL+],#i4	E:[HL],A ← i4, HL ← HL + 1	1	1	0	0	0	0	0	1	1	1	0	1	0	0	i_3	i_2	i_1	i_0	√	—	√
MOV E:[XY+],#i4	E:[XY],A ← i4, XY ← XY + 1	1	1	0	0	0	0	0	1	1	1	0	1	0	1	i_3	i_2	i_1	i_0	√	—	√
MOV A,#i4	A ← i4	1	1	0	0	0	0	0	0	0	1	1	1	0	0	i_3	i_2	i_1	i_0	√	—	—
MOV A,direct	A ← direct	1	1	1	1	0	1	r_{11}	r_{10}	r_9	r_8	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
MOV A,[HL]	A ← [HL]	1	1	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0	√	—	—
MOV A,[XY]	A ← [XY]	1	1	0	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0	√	—	—
MOV A,E:[HL]	A ← E:[HL]	1	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	√	—	—
MOV A,E:[XY]	A ← E:[XY]	1	1	0	0	0	0	0	0	1	1	0	0	0	1	0	0	0	0	√	—	—
MOV A,[HL+]	A ← [HL], HL ← HL + 1	1	1	0	0	0	0	0	0	1	1	0	0	1	0	1	0	0	0	√	—	√
MOV A,[XY+]	A ← [XY], XY ← XY + 1	1	1	0	0	0	0	0	0	1	1	0	0	1	1	1	0	0	0	√	—	√
MOV A,E:[HL+]	A ← E:[HL], HL ← HL + 1	1	1	0	0	0	0	0	0	1	1	0	0	0	0	1	0	0	0	√	—	√
MOV A,E:[XY+]	A ← E:[XY], XY ← XY + 1	1	1	0	0	0	0	0	0	1	1	0	0	0	1	1	0	0	0	√	—	√
XCH A,sfr	A ↔ sfr	1	1	0	0	1	0	1	1	1	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	—	—	—
XCH A,\cur	A ↔ cur	1	1	0	0	1	1	1	1	1	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	—	—	—
XCH A,[HL]	A ↔ [HL]	1	1	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	1	—	—	—
XCH A,[XY]	A ↔ [XY]	1	1	0	0	0	0	0	0	1	1	0	0	1	1	0	0	0	1	—	—	—
XCH A,E:[HL]	A ↔ E:[HL]	1	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1	—	—	—
XCH A,E:[XY]	A ↔ E:[XY]	1	1	0	0	0	0	0	0	1	1	0	0	0	1	0	0	0	1	—	—	—
XCH A,[HL+]	A ↔ [HL], HL ← HL + 1	1	1	0	0	0	0	0	0	1	1	0	0	1	0	1	0	0	1	—	—	√
XCH A,[XY+]	A ↔ [XY], XY ← XY + 1	1	1	0	0	0	0	0	0	1	1	0	0	1	1	1	0	0	1	—	—	√
XCH A,E:[HL+]	A ↔ E:[HL], HL ← HL + 1	1	1	0	0	0	0	0	0	1	1	0	0	0	0	1	0	0	1	—	—	√
XCH A,E:[XY+]	A ↔ E:[XY], XY ← XY + 1	1	1	0	0	0	0	0	0	1	1	0	0	0	1	1	0	0	1	—	—	√

Rotate Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
ROL sfr	C ← {$_3$sfr$_0$} ← C, A ← sfr	1	1	0	0	1	0	0	0	1	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ROL \cur	C ← {$_3$cur$_0$} ← C, A ← cur	1	1	0	0	1	1	0	0	1	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ROL [HL]	C ← {$_3$[HL]$_0$} ← C, A ← [HL]	1	1	0	0	0	0	0	1	0	0	0	0	1	0	0	1	1	0	√	√	—
ROL [XY]	C ← {$_3$[XY]$_0$} ← C, A ← [XY]	1	1	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	0	√	√	—
ROL E:[HL]	C ← {$_3$E:[HL]$_0$} ← C, A ← E:[HL]	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1	0	√	√	—
ROL E:[XY]	C ← {$_3$E:[XY]$_0$} ← C, A ← E:[XY]	1	1	0	0	0	0	0	1	0	0	0	0	0	1	0	1	1	0	√	√	—
ROL [HL+]	C ← {$_3$[HL]$_0$} ← C, A ← [HL], HL ← HL + 1	1	1	0	0	0	0	0	1	0	0	0	0	1	0	1	1	1	0	√	√	√
ROL [XY+]	C ← {$_3$[XY]$_0$} ← C, A ← [XY], XY ← XY + 1	1	1	0	0	0	0	0	1	0	0	0	0	1	1	1	1	1	0	√	√	√
ROL E:[HL+]	C ← {$_3$E:[HL]$_0$} ← C, A ← E:[HL], HL ← HL + 1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1	1	1	0	√	√	√
ROL E:[XY+]	C ← {$_3$E:[XY]$_0$} ← C, A ← E:[XY], XY ← XY + 1	1	1	0	0	0	0	0	1	0	0	0	0	0	1	1	1	1	0	√	√	√
ROR sfr	C → {$_3$sfr$_0$} → C, A ← sfr	1	1	0	0	1	0	0	0	1	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ROR \cur	C → {$_3$cur$_0$} → C, A ← cur	1	1	0	0	1	1	0	0	1	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ROR [HL]	C → {$_3$[HL]$_0$} → C, A ← [HL]	1	1	0	0	0	0	0	1	0	0	0	0	1	0	0	1	1	1	√	√	—
ROR [XY]	C → {$_3$[XY]$_0$} → C, A ← [XY]	1	1	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1	√	√	—
ROR E:[HL]	C → {$_3$E:[HL]$_0$} → C, A ← E:[HL]	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1	1	√	√	—
ROR E:[XY]	C → {$_3$E:[XY]$_0$} → C, A ← E:[XY]	1	1	0	0	0	0	0	1	0	0	0	0	0	1	0	1	1	1	√	√	—
ROR [HL+]	C → {$_3$[HL]$_0$} → C, A ← [HL], HL ← HL + 1	1	1	0	0	0	0	0	1	0	0	0	0	1	0	1	1	1	1	√	√	√
ROR [XY+]	C → {$_3$[XY]$_0$} → C, A ← [XY], XY ← XY + 1	1	1	0	0	0	0	0	1	0	0	0	0	1	1	1	1	1	1	√	√	√
ROR E:[HL+]	C → {$_3$E:[HL]$_0$} → C, A ← E:[HL], HL ← HL + 1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1	1	1	1	√	√	√
ROR E:[XY+]	C → {$_3$E:[XY]$_0$} → C, A ← E:[XY], XY ← XY + 1	1	1	0	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	√	√	√

Increment/Decrement Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
INC sfr	sfr,A ← sfr + 1	1	1	0	0	1	0	0	0	0	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
INC \cur	cur,A ← cur + 1	1	1	0	0	1	1	0	0	0	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
INC [HL]	[HL],A ← [HL] + 1	1	1	0	0	0	0	0	1	0	1	0	0	1	0	0	0	0	0	√	√	—
INC [XY]	[XY],A ← [XY] + 1	1	1	0	0	0	0	0	1	0	1	0	0	1	1	0	0	0	0	√	√	—
INC E:[HL]	E:[HL],A ← E:[HL] + 1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	√	√	—
INC E:[XY]	E:[XY],A ← E:[XY] + 1	1	1	0	0	0	0	0	1	0	1	0	0	0	1	0	0	0	0	√	√	—
INC [HL+]	[HL],A ← [HL] + 1, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	0	1	0	1	0	0	0	√	√	√
INC [XY+]	[XY],A ← [XY] + 1, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	0	1	1	1	0	0	0	√	√	√
INC E:[HL+]	E:[HL],A ← E:[HL] + 1, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	1	0	0	0	√	√	√
INC E:[XY+]	E:[XY],A ← E:[XY] + 1, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	0	0	1	1	0	0	0	√	√	√
DEC sfr	sfr,A ← sfr – 1	1	1	0	0	1	0	0	0	0	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
DEC \cur	cur,A ← cur – 1	1	1	0	0	1	1	0	0	0	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
DEC [HL]	[HL],A ← [HL] – 1	1	1	0	0	0	0	0	1	0	1	0	0	1	0	0	0	0	1	√	√	—
DEC [XY]	[XY],A ← [XY] – 1	1	1	0	0	0	0	0	1	0	1	0	0	1	1	0	0	0	1	√	√	—
DEC E:[HL]	E:[HL],A ← E:[HL] – 1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	√	√	—
DEC E:[XY]	E:[XY],A ← E:[XY] – 1	1	1	0	0	0	0	0	1	0	1	0	0	0	1	0	0	0	1	√	√	—
DEC [HL+]	[HL],A ← [HL] – 1, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	0	1	0	1	0	0	1	√	√	√
DEC [XY+]	[XY],A ← [XY] – 1, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	0	1	1	1	0	0	1	√	√	√
DEC E:[HL+]	E:[HL],A ← E:[HL] – 1, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	1	0	0	1	√	√	√
DEC E:[XY+]	E:[XY],A ← E:[XY] – 1, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	0	0	1	1	0	0	1	√	√	√

Arithmetic Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
ADD sfr,A	sfr,A ← sfr + A	1	1	0	0	1	0	0	1	0	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ADD \cur,A	cur,A ← cur + A	1	1	0	0	1	1	0	1	0	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ADD [HL],A	[HL],A ← [HL] + A	1	1	0	0	0	0	0	1	0	1	0	0	1	0	0	0	1	0	√	√	—
ADD [XY],A	[XY],A ← [XY] + A	1	1	0	0	0	0	0	1	0	1	0	0	1	1	0	0	1	0	√	√	—
ADD E:[HL],A	E:[HL],A ← E:[HL] + A	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	0	√	√	—
ADD E:[XY],A	E:[XY],A ← E:[XY] + A	1	1	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	0	√	√	—
ADD [HL+],A	[HL],A ← [HL] + A, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	0	1	0	1	0	1	0	√	√	√
ADD [XY+],A	[XY],A ← [XY] + A, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	0	1	1	1	0	1	0	√	√	√
ADD E:[HL+],A	E:[HL],A ← E:[HL] + A, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	1	0	1	0	√	√	√
ADD E:[XY+],A	E:[XY],A ← E:[XY] + A, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	0	0	1	1	0	1	0	√	√	√
ADD \cur,#i4	cur,A ← cur + i4	1	1	1	0	0	0	i_3	i_2	i_1	i_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ADD [HL],#i4	[HL],A ← [HL] + i4	1	1	0	0	0	0	0	0	0	0	1	0	1	0	i_3	i_2	i_1	i_0	√	√	—
ADD [XY],#i4	[XY],A ← [XY] + i4	1	1	0	0	0	0	0	0	0	0	1	0	1	1	i_3	i_2	i_1	i_0	√	√	—
ADD E:[HL],#i4	E:[HL],A ← E:[HL] + i4	1	1	0	0	0	0	0	0	0	0	1	0	0	0	i_3	i_2	i_1	i_0	√	√	—
ADD E:[XY],#i4	E:[XY],A ← E:[XY] + i4	1	1	0	0	0	0	0	0	0	0	1	0	0	1	i_3	i_2	i_1	i_0	√	√	—
ADD [HL+],#i4	[HL],A ← [HL] + i4, HL ← HL + 1	1	1	0	0	0	0	0	0	0	1	1	0	1	0	i_3	i_2	i_1	i_0	√	√	√
ADD [XY+],#i4	[XY],A ← [XY] + i4, XY ← XY + 1	1	1	0	0	0	0	0	0	0	1	1	0	1	1	i_3	i_2	i_1	i_0	√	√	√
ADD E:[HL+],#i4	E:[HL],A ← E:[HL] + i4, HL ← HL + 1	1	1	0	0	0	0	0	0	0	1	1	0	0	0	i_3	i_2	i_1	i_0	√	√	√
ADD E:[XY+],#i4	E:[XY],A ← E:[XY] + i4, XY ← XY + 1	1	1	0	0	0	0	0	0	0	1	1	0	0	1	i_3	i_2	i_1	i_0	√	√	√
ADC sfr,A	sfr,A ← sfr + A + C	1	1	0	0	1	0	0	1	0	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ADC \cur,A	cur,A ← cur + A + C	1	1	0	0	1	1	0	1	0	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ADC [HL],A	[HL],A ← [HL] + A + C	1	1	0	0	0	0	0	1	0	1	0	0	1	0	0	0	1	1	√	√	—
ADC [XY],A	[XY],A ← [XY] + A + C	1	1	0	0	0	0	0	1	0	1	0	0	1	1	0	0	1	1	√	√	—
ADC E:[HL],A	E:[HL],A ← E:[HL] + A + C	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	1	√	√	—
ADC E:[XY],A	E:[XY],A ← E:[XY] + A + C	1	1	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	1	√	√	—
ADC [HL+],A	[HL],A ← [HL] + A + C, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	0	1	0	1	0	1	1	√	√	√
ADC [XY+],A	[XY],A ← [XY] + A + C, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	0	1	1	1	0	1	1	√	√	√
ADC E:[HL+],A	E:[HL],A ← E:[HL] + A + C, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	1	0	1	1	√	√	√
ADC E:[XY+],A	E:[XY],A ← E:[XY] + A + C, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	0	0	1	1	0	1	1	√	√	√

Arithmetic Instructions (continued)

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
ADCD sfr,A	sfr,A ← decimal adjustment {sfr + A + C}	1	1	0	0	1	0	0	1	1	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ADCD \cur,A	cur,A ← decimal adjustment {cur + A + C}	1	1	0	0	1	1	0	1	1	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ADCD [HL],A	[HL],A ← decimal adjustment {[HL] + A + C}	1	1	0	0	0	0	0	1	0	1	0	0	1	0	0	1	0	0	√	√	—
ADCD [XY],A	[XY],A ← decimal adjustment {[XY] + A + C}	1	1	0	0	0	0	0	1	0	1	0	0	1	1	0	1	0	0	√	√	—
ADCD E:[HL],A	E:[HL],A ← decimal adjustment {E:[HL] + A + C}	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	0	√	√	—
ADCD E:[XY],A	E:[XY],A ← decimal adjustment {E:[XY] + A + C}	1	1	0	0	0	0	0	1	0	1	0	0	0	1	0	1	0	0	√	√	—
ADCD [HL+],A	[HL],A ← decimal adjustment {[HL] + A + C}, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	0	1	0	1	1	0	0	√	√	√
ADCD [XY+],A	[XY],A ← decimal adjustment {[XY] + A + C}, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	0	1	1	1	1	0	0	√	√	√
ADCD E:[HL+],A	E:[HL],A ← decimal adjustment {E:[HL] + A + C}, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	1	1	0	0	√	√	√
ADCD E:[XY+],A	E:[XY],A ← decimal adjustment {E:[XY] + A + C}, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	0	0	1	1	1	0	0	√	√	√
ADCJ \cur,n	cur,A ← n-ary adjustment {cur + C}	1	1	0	0	0	1	0	n_2	n_1	n_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
ADCJ [HL],n	[HL],A ← n-ary adjustment {[HL] + C}	1	1	0	0	0	0	0	1	1	0	0	0	1	0	0	n_2	n_1	n_0	√	√	—
ADCJ [XY],n	[XY],A ← n-ary adjustment {[XY] + C}	1	1	0	0	0	0	0	1	1	0	0	0	1	1	0	n_2	n_1	n_0	√	√	—
ADCJ E:[HL],n	E:[HL],A ← n-ary adjustment {E:[HL] + C}	1	1	0	0	0	0	0	1	1	0	0	0	0	0	0	n_2	n_1	n_0	√	√	—
ADCJ E:[XY],n	E:[XY],A ← n-ary adjustment {E:[XY] + C}	1	1	0	0	0	0	0	1	1	0	0	0	0	1	0	n_2	n_1	n_0	√	√	—
ADCJ [HL+],n	[HL],A ← n-ary adjustment {[HL] + C}, HL ← HL + 1	1	1	0	0	0	0	0	1	1	1	0	0	1	0	0	n_2	n_1	n_0	√	√	√
ADCJ [XY+],n	[XY],A ← n-ary adjustment {[XY] + C}, XY ← XY + 1	1	1	0	0	0	0	0	1	1	1	0	0	1	1	0	n_2	n_1	n_0	√	√	√
ADCJ E:[HL+],n	E:[HL],A ← n-ary adjustment {E:[HL] + C}, HL ← HL + 1	1	1	0	0	0	0	0	1	1	1	0	0	0	0	0	n_2	n_1	n_0	√	√	√
ADCJ E:[XY+],n	E:[XY],A ← n-ary adjustment {E:[XY] + C}, XY ← XY + 1	1	1	0	0	0	0	0	1	1	1	0	0	0	1	0	n_2	n_1	n_0	√	√	√

Arithmetic Instructions (continued)

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
SUB sfr,A	sfr,A ← sfr – A	1	1	0	0	1	0	0	1	1	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
SUB \cur,A	cur,A ← cur – A	1	1	0	0	1	1	0	1	1	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
SUB [HL],A	[HL],A ← [HL] – A	1	1	0	0	0	0	0	1	0	1	0	0	1	0	0	1	0	1	√	√	—
SUB [XY],A	[XY],A ← [XY] – A	1	1	0	0	0	0	0	1	0	1	0	0	1	1	0	1	0	1	√	√	—
SUB E:[HL],A	E:[HL],A ← E:[HL] – A	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	1	√	√	—
SUB E:[XY],A	E:[XY],A ← E:[XY] – A	1	1	0	0	0	0	0	1	0	1	0	0	0	1	0	1	0	1	√	√	—
SUB [HL+],A	[HL],A ← [HL] – A, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	0	1	0	1	1	0	1	√	√	√
SUB [XY+],A	[XY],A ← [XY] – A, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	0	1	1	1	1	0	1	√	√	√
SUB E:[HL+],A	E:[HL],A ← E:[HL] – A, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	1	1	0	1	√	√	√
SUB E:[XY+],A	E:[XY],A ← E:[XY] – A, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	0	0	1	1	1	0	1	√	√	√
SUB \cur,#i4	cur,A ← cur – i4	1	1	1	0	0	1	i_3	i_2	i_1	i_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
SUB [HL],#i4	[HL],A ← [HL] – i4	1	1	0	0	0	0	0	0	1	0	1	0	1	0	i_3	i_2	i_1	i_0	√	√	—
SUB [XY],#i4	[XY],A ← [XY] – i4	1	1	0	0	0	0	0	0	1	0	1	0	1	1	i_3	i_2	i_1	i_0	√	√	—
SUB E:[HL],#i4	E:[HL],A ← E:[HL] – i4	1	1	0	0	0	0	0	0	1	0	1	0	0	0	i_3	i_2	i_1	i_0	√	√	—
SUB E:[XY],#i4	E:[XY],A ← E:[XY] – i4	1	1	0	0	0	0	0	0	1	0	1	0	0	1	i_3	i_2	i_1	i_0	√	√	—
SUB [HL+],#i4	[HL],A ← [HL] – i4, HL ← HL + 1	1	1	0	0	0	0	0	0	1	1	1	0	1	0	i_3	i_2	i_1	i_0	√	√	√
SUB [XY+],#i4	[XY],A ← [XY] – i4, XY ← XY + 1	1	1	0	0	0	0	0	0	1	1	1	0	1	1	i_3	i_2	i_1	i_0	√	√	√
SUB E:[HL+],#i4	E:[HL],A ← E:[HL] – i4, HL ← HL + 1	1	1	0	0	0	0	0	0	1	1	1	0	0	0	i_3	i_2	i_1	i_0	√	√	√
SUB E:[XY+],#i4	E:[XY],A ← E:[XY] – i4, XY ← XY + 1	1	1	0	0	0	0	0	0	1	1	1	0	0	1	i_3	i_2	i_1	i_0	√	√	√
SBC sfr,A	sfr,A ← sfr – A – C	1	1	0	0	1	0	1	0	0	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
SBC \cur,A	cur,A ← cur – A – C	1	1	0	0	1	1	1	0	0	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
SBC [HL],A	[HL],A ← [HL] – A – C	1	1	0	0	0	0	0	1	0	1	0	0	1	0	0	1	1	0	√	√	—
SBC [XY],A	[XY],A ← [XY] – A – C	1	1	0	0	0	0	0	1	0	1	0	0	1	1	0	1	1	0	√	√	—
SBC E:[HL],A	E:[HL],A ← E:[HL] – A – C	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	1	0	√	√	—
SBC E:[XY],A	E:[XY],A ← E:[XY] – A – C	1	1	0	0	0	0	0	1	0	1	0	0	0	1	0	1	1	0	√	√	—
SBC [HL+],A	[HL],A ← [HL] – A – C, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	0	1	0	1	1	1	0	√	√	√
SBC [XY+],A	[XY],A ← [XY] – A – C, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	0	1	1	1	1	1	0	√	√	√
SBC E:[HL+],A	E:[HL],A ← E:[HL] – A – C, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	1	1	1	0	√	√	√
SBC E:[XY+],A	E:[XY],A ← E:[XY] – A – C, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	0	0	1	1	1	1	0	√	√	√

Arithmetic Instructions (continued)

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
SBCD sfr,A	sfr,A ← decimal adjustment {sfr – A – C}	1	1	0	0	1	0	1	0	0	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
SBCD \cur,A	cur,A ← decimal adjustment {cur – A – C}	1	1	0	0	1	1	1	0	0	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
SBCD [HL],A	[HL],A ← decimal adjustment {[HL] – A – C}	1	1	0	0	0	0	0	1	0	1	0	0	1	0	0	1	1	1	√	√	—
SBCD [XY],A	[XY],A ← decimal adjustment {[XY] – A – C}	1	1	0	0	0	0	0	1	0	1	0	0	1	1	0	1	1	1	√	√	—
SBCD E:[HL],A	E:[HL],A ← decimal adjustment {E:[HL] – A – C}	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1	1	1	√	√	—
SBCD E:[XY],A	E:[XY],A ← decimal adjustment {E:[XY] – A – C}	1	1	0	0	0	0	0	1	0	1	0	0	0	1	0	1	1	1	√	√	—
SBCD [HL+],A	[HL],A ← decimal adjustment {[HL] – A – C}, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	0	1	0	1	1	1	1	√	√	√
SBCD [XY+],A	[XY],A ← decimal adjustment {[XY] – A – C}, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	0	1	1	1	1	1	1	√	√	√
SBCD E:[HL+],A	E:[HL],A ← decimal adjustment {E:[HL] – A – C}, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	1	1	1	1	√	√	√
SBCD E:[XY+],A	E:[XY],A ← decimal adjustment {E:[XY] – A – C}, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	0	0	1	1	1	1	1	√	√	√
SBCJ \cur,n	cur,A ← n-ary adjustment {cur – C}	1	1	0	0	0	1	1	n_2	n_1	n_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
SBCJ [HL],n	[HL],A ← n-ary adjustment {[HL] – C}	1	1	0	0	0	0	0	1	1	0	0	0	1	0	1	n_2	n_1	n_0	√	√	—
SBCJ [XY],n	[XY],A ← n-ary adjustment {[XY] – C}	1	1	0	0	0	0	0	1	1	0	0	0	1	1	1	n_2	n_1	n_0	√	√	—
SBCJ E:[HL],n	E:[HL],A ← n-ary adjustment {E:[HL] – C}	1	1	0	0	0	0	0	1	1	0	0	0	0	0	1	n_2	n_1	n_0	√	√	—
SBCJ E:[XY],n	E:[XY],A ← n-ary adjustment {E:[XY] – C}	1	1	0	0	0	0	0	1	1	0	0	0	0	1	1	n_2	n_1	n_0	√	√	—
SBCJ [HL+],n	[HL],A ← n-ary adjustment {[HL] – C}, HL ← HL + 1	1	1	0	0	0	0	0	1	1	1	0	0	1	0	1	n_2	n_1	n_0	√	√	√
SBCJ [XY+],n	[XY],A ← n-ary adjustment {[XY] – C}, XY ← XY + 1	1	1	0	0	0	0	0	1	1	1	0	0	1	1	1	n_2	n_1	n_0	√	√	√
SBCJ E:[HL+],n	E:[HL],A ← n-ary adjustment {E:[HL] – C}, HL ← HL + 1	1	1	0	0	0	0	0	1	1	1	0	0	0	0	1	n_2	n_1	n_0	√	√	√
SBCJ E:[XY+],n	E:[XY],A ← n-ary adjustment {E:[XY] – C}, XY ← XY + 1	1	1	0	0	0	0	0	1	1	1	0	0	0	1	1	n_2	n_1	n_0	√	√	√

Compare Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
CMP sfr,A	sfr – A	1	1	0	0	1	0	1	0	1	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
CMP \cur,A	cur – A	1	1	0	0	1	1	1	0	1	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
CMP [HL],A	[HL] – A	1	1	0	0	0	0	0	1	0	0	0	0	1	0	0	1	0	0	√	√	—
CMP [XY],A	[XY] – A	1	1	0	0	0	0	0	1	0	0	0	0	1	1	0	1	0	0	√	√	—
CMP E:[HL],A	E:[HL] – A	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	√	√	—
CMP E:[XY],A	E:[XY] – A	1	1	0	0	0	0	0	1	0	0	0	0	0	1	0	1	0	0	√	√	—
CMP [HL+],A	[XY] – A, HL ← HL + 1	1	1	0	0	0	0	0	1	0	0	0	0	1	0	1	1	0	0	√	√	√
CMP [XY+],A	[XY] – A, XY ← XY + 1	1	1	0	0	0	0	0	1	0	0	0	0	1	1	1	1	0	0	√	√	√
CMP E:[HL+],A	E:[HL] – A, HL ← HL + 1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	0	√	√	√
CMP E:[XY+],A	E:[XY] – A, XY ← XY + 1	1	1	0	0	0	0	0	1	0	0	0	0	0	1	1	1	0	0	√	√	√
CMP \cur,#i4	cur – i4	1	1	1	0	1	0	i_3	i_2	i_1	i_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	√	—
CMP [HL],#i4	[HL] – i4	1	1	0	0	0	0	0	1	1	0	1	0	1	0	i_3	i_2	i_1	i_0	√	√	—
CMP [XY],#i4	[XY] – i4	1	1	0	0	0	0	0	1	1	0	1	0	1	1	i_3	i_2	i_1	i_0	√	√	—
CMP E:[HL],#i4	E:[HL] – i4	1	1	0	0	0	0	0	1	1	0	1	0	0	0	i_3	i_2	i_1	i_0	√	√	—
CMP E:[XY],#i4	E:[XY] – i4	1	1	0	0	0	0	0	1	1	0	1	0	0	1	i_3	i_2	i_1	i_0	√	√	—
CMP [HL+],#i4	[HL] – i4, HL ← HL + 1	1	1	0	0	0	0	0	1	1	1	1	0	1	0	i_3	i_2	i_1	i_0	√	√	√
CMP [XY+],#i4	[XY] – i4, XY ← XY + 1	1	1	0	0	0	0	0	1	1	1	1	0	1	1	i_3	i_2	i_1	i_0	√	√	√
CMP E:[HL+],#i4	E:[HL] – i4, HL ← HL + 1	1	1	0	0	0	0	0	1	1	1	1	0	0	0	i_3	i_2	i_1	i_0	√	√	√
CMP E:[XY+],#i4	E:[XY] – i4, XY ← XY + 1	1	1	0	0	0	0	0	1	1	1	1	0	0	1	i_3	i_2	i_1	i_0	√	√	√

Logic Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
AND sfr,A	sfr,A ← sfr ∧ A	1	1	0	0	1	0	1	0	1	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
AND \cur,A	cur,A ← cur ∧ A	1	1	0	0	1	1	1	0	1	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
AND [HL],A	[HL],A ← [HL] ∧ A	1	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	1	√	—	—
AND [XY],A	[XY],A ← [XY] ∧ A	1	1	0	0	0	0	0	1	0	0	0	0	1	1	0	0	0	1	√	—	—
AND E:[HL],A	E:[HL],A ← E:[HL] ∧ A	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	√	—	—
AND E:[XY],A	E:[XY],A ← E:[XY] ∧ A	1	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	√	—	—
AND [HL+],A	[HL],A ← [HL] ∧ A, HL ← HL + 1	1	1	0	0	0	0	0	1	0	0	0	0	1	0	1	0	0	1	√	—	√
AND [XY+],A	[XY],A ← [XY] ∧ A, XY ← XY + 1	1	1	0	0	0	0	0	1	0	0	0	0	1	1	1	0	0	1	√	—	√
AND E:[HL+],A	E:[HL],A ← E:[HL] ∧ A, HL ← HL + 1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	1	√	—	√
AND E:[XY+],A	E:[XY],A ← E:[XY] ∧ A, XY ← XY + 1	1	1	0	0	0	0	0	1	0	0	0	0	0	1	1	0	0	1	√	—	√
AND \cur,#i4	cur,A ← cur ∧ i4	1	1	0	1	0	1	i_3	i_2	i_1	i_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
AND [HL],#i4	[HL],A ← [HL] ∧ i4	1	1	0	0	0	0	0	1	0	0	0	1	1	0	i_3	i_2	i_1	i_0	√	—	—
AND [XY],#i4	[XY],A ← [XY] ∧ i4	1	1	0	0	0	0	0	1	0	0	0	1	1	1	i_3	i_2	i_1	i_0	√	—	—
AND E:[HL],#i4	E:[HL],A ← E:[HL] ∧ i4	1	1	0	0	0	0	0	1	0	0	0	1	0	0	i_3	i_2	i_1	i_0	√	—	—
AND E:[XY],#i4	E:[XY],A ← E:[XY] ∧ i4	1	1	0	0	0	0	0	1	0	0	0	1	0	1	i_3	i_2	i_1	i_0	√	—	—
AND [HL+],#i4	[HL],A ← [HL] ∧ i4, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	1	1	0	i_3	i_2	i_1	i_0	√	—	√
AND [XY+],#i4	[XY],A ← [XY] ∧ i4, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	1	1	1	i_3	i_2	i_1	i_0	√	—	√
AND E:[HL+],#i4	E:[HL],A ← E:[HL] ∧ i4, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	1	0	0	i_3	i_2	i_1	i_0	√	—	√
AND E:[XY+],#i4	E:[XY],A ← E:[XY] ∧ i4, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	1	0	1	i_3	i_2	i_1	i_0	√	—	√
OR sfr,A	sfr,A ← sfr ∨ A	1	1	0	0	1	0	1	1	0	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
OR \cur,A	cur,A ← cur ∨ A	1	1	0	0	1	1	1	1	0	0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
OR [HL],A	[HL],A ← [HL] ∨ A	1	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	1	0	√	—	—
OR [XY],A	[XY],A ← [XY] ∨ A	1	1	0	0	0	0	0	1	0	0	0	0	1	1	0	0	1	0	√	—	—
OR E:[HL],A	E:[HL],A ← E:[HL] ∨ A	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	√	—	—
OR E:[XY],A	E:[XY],A ← E:[XY] ∨ A	1	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1	0	√	—	—
OR [HL+],A	[HL],A ← [HL] ∨ A, HL ← HL + 1	1	1	0	0	0	0	0	1	0	0	0	0	1	0	1	0	1	0	√	—	√
OR [XY+],A	[XY],A ← [XY] ∨ A, XY ← XY + 1	1	1	0	0	0	0	0	1	0	0	0	0	1	1	1	0	1	0	√	—	√
OR E:[HL+],A	E:[HL],A ← E:[HL] ∨ A, HL ← HL + 1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1	0	1	0	√	—	√
OR E:[XY+],A	E:[XY],A ← E:[XY] ∨ A, XY ← XY + 1	1	1	0	0	0	0	0	1	0	0	0	0	0	1	1	0	1	0	√	—	√

Logic Instructions (continued)

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
OR \cur,#i4	cur,A ← cur ∨ i4	1	1	0	1	1	0	i_3	i_2	i_1	i_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
OR [HL],#i4	[HL],A ← [HL] ∨ i4	1	1	0	0	0	0	0	0	1	0	0	1	1	0	i_3	i_2	i_1	i_0	√	—	—
OR [XY],#i4	[XY],A ← [XY] ∨ i4	1	1	0	0	0	0	0	0	1	0	0	1	1	1	i_3	i_2	i_1	i_0	√	—	—
OR E:[HL],#i4	E:[HL],A ← E:[HL] ∨ i4	1	1	0	0	0	0	0	0	1	0	0	1	0	0	i_3	i_2	i_1	i_0	√	—	—
OR E:[XY],#i4	E:[XY],A ← E:[XY] ∨ i4	1	1	0	0	0	0	0	0	1	0	0	1	0	1	i_3	i_2	i_1	i_0	√	—	—
OR [HL+],#i4	[HL],A ← [HL] ∨ i4, HL ← HL + 1	1	1	0	0	0	0	0	0	1	1	0	1	1	0	i_3	i_2	i_1	i_0	√	—	√
OR [XY+],#i4	[XY],A ← [XY] ∨ i4, XY ← XY + 1	1	1	0	0	0	0	0	0	1	1	0	1	1	1	i_3	i_2	i_1	i_0	√	—	√
OR E:[HL+],#i4	E:[HL],A ← E:[HL] ∨ i4, HL ← HL + 1	1	1	0	0	0	0	0	0	1	1	0	1	0	0	i_3	i_2	i_1	i_0	√	—	√
OR E:[XY+],#i4	E:[XY],A ← E:[XY] ∨ i4, XY ← XY + 1	1	1	0	0	0	0	0	0	1	1	0	1	0	1	i_3	i_2	i_1	i_0	√	—	√
XOR sfr,A	sfr,A ← sfr ∀ A	1	1	0	0	1	0	1	1	0	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
XOR \cur,A	cur,A ← cur ∀ A	1	1	0	0	1	1	1	1	0	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
XOR [HL],A	[HL],A ← [HL] ∀ A	1	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	1	1	√	—	—
XOR [XY],A	[XY],A ← [XY] ∀ A	1	1	0	0	0	0	0	1	0	0	0	0	1	1	0	0	1	1	√	—	—
XOR E:[HL],A	E:[HL],A ← E:[HL] ∀ A	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	√	—	—
XOR E:[XY],A	E:[XY],A ← E:[XY] ∀ A	1	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1	1	√	—	—
XOR [HL+],A	[HL],A ← [HL] ∀ A, HL ← HL + 1	1	1	0	0	0	0	0	1	0	0	0	0	1	0	1	0	1	1	√	—	√
XOR [XY+],A	[XY],A ← [XY] ∀ A, XY ← XY + 1	1	1	0	0	0	0	0	1	0	0	0	0	1	1	1	0	1	1	√	—	√
XOR E:[HL+],A	E:[HL],A ← E:[HL] ∀ A, HL ← HL + 1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1	0	1	1	√	—	√
XOR E:[XY+],A	E:[XY],A ← E:[XY] ∀ A, XY ← XY + 1	1	1	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1	√	—	√
XOR \cur,#i4	cur,A ← cur ∀ i4	1	1	0	1	1	1	i_3	i_2	i_1	i_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
XOR [HL],#i4	[HL],A ← [HL] ∀ i4	1	1	0	0	0	0	0	0	0	0	0	1	1	0	i_3	i_2	i_1	i_0	√	—	—
XOR [XY],#i4	[XY],A ← [XY] ∀ i4	1	1	0	0	0	0	0	0	0	0	0	1	1	1	i_3	i_2	i_1	i_0	√	—	—
XOR E:[HL],#i4	E:[HL],A ← E:[HL] ∀ i4	1	1	0	0	0	0	0	0	0	0	0	1	0	0	i_3	i_2	i_1	i_0	√	—	—
XOR E:[XY],#i4	E:[XY],A ← E:[XY] ∀ i4	1	1	0	0	0	0	0	0	0	0	0	1	0	1	i_3	i_2	i_1	i_0	√	—	—
XOR [HL+],#i4	[HL],A ← [HL] ∀ i4, HL ← HL + 1	1	1	0	0	0	0	0	0	0	1	0	1	1	0	i_3	i_2	i_1	i_0	√	—	√
XOR [XY+],#i4	[XY],A ← [XY] ∀ i4, XY ← XY + 1	1	1	0	0	0	0	0	0	0	1	0	1	1	1	i_3	i_2	i_1	i_0	√	—	√
XOR E:[HL+],#i4	E:[HL],A ← E:[HL] ∀ i4, HL ← HL + 1	1	1	0	0	0	0	0	0	0	1	0	1	0	0	i_3	i_2	i_1	i_0	√	—	√
XOR E:[XY+],#i4	E:[XY],A ← E:[XY] ∀ i4, XY ← XY + 1	1	1	0	0	0	0	0	0	0	1	0	1	0	1	i_3	i_2	i_1	i_0	√	—	√

Mask Operation Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
MTST sfr,A	Testing of all bits in sfr not masked by A	1	1	0	0	1	0	1	1	1	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
MTST \cur,A	Testing of all bits in cur not masked by A	1	1	0	0	1	1	1	1	1	1	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
MTST [HL],A	Testing of all bits in [HL] not masked by A	1	1	0	0	0	0	0	1	0	0	0	0	1	0	0	1	0	1	√	—	—
MTST [XY],A	Testing of all bits in [XY] not masked by A	1	1	0	0	0	0	0	1	0	0	0	0	1	1	0	1	0	1	√	—	—
MTST E:[HL],A	Testing of all bits in E:[HL] not masked by A	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1	√	—	—
MTST E:[XY],A	Testing of all bits in E:[XY] not masked by A	1	1	0	0	0	0	0	1	0	0	0	0	0	1	0	1	0	1	√	—	—
MTST [HL+],A	Testing of all bits in [HL] not masked by A, HL ← HL + 1	1	1	0	0	0	0	0	1	0	0	0	0	1	0	1	1	0	1	√	—	√
MTST [XY+],A	Testing of all bits in [XY] not masked by A, XY ← XY + 1	1	1	0	0	0	0	0	1	0	0	0	0	1	1	1	1	0	1	√	—	√
MTST E:[HL+],A	Testing of all bits in E:[HL] not masked by A, HL ← HL + 1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	1	√	—	√
MTST E:[XY+],A	Testing of all bits in E:[XY] not masked by A, XY← XY + 1	1	1	0	0	0	0	0	1	0	0	0	0	0	1	1	1	0	1	√	—	√
MTST \cur,#m	Testing of all bits in cur not masked by #m	1	1	1	0	1	1	m_3	m_2	m_1	m_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
MTST [HL],#m	Testing of all bits in [HL] not masked by #m	1	1	0	0	0	0	0	1	0	0	1	0	1	0	m_3	m_2	m_1	m_0	√	—	—
MTST [XY],#m	Testing of all bits in [XY] not masked by #m	1	1	0	0	0	0	0	1	0	0	1	0	1	1	m_3	m_2	m_1	m_0	√	—	—
MTST E:[HL],#m	Testing of all bits in E:[HL] not masked by #m	1	1	0	0	0	0	0	1	0	0	1	0	0	0	m_3	m_2	m_1	m_0	√	—	—
MTST E:[XY],#m	Testing of all bits in E:[XY] not masked by #m	1	1	0	0	0	0	0	1	0	0	1	0	0	1	m_3	m_2	m_1	m_0	√	—	—
MTST [HL+],#m	Testing of all bits in [HL] not masked by #m, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	1	0	1	0	m_3	m_2	m_1	m_0	√	—	√
MTST [XY+],#m	Testing of all bits in [XY] not masked by #m, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	1	0	1	1	m_3	m_2	m_1	m_0	√	—	√
MTST E:[HL+],#m	Testing of all bits in E:[HL] not masked by #m, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	1	0	0	0	m_3	m_2	m_1	m_0	√	—	√
MTST E:[XY+],#m	Testing of all bits in E:[XY] not masked by #m, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	1	0	0	1	m_3	m_2	m_1	m_0	√	—	√

Mask Operation Instructions (continued)

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
MCLR \cur,#m	Clearing of all bits in cur not masked by #m, A ← cur	1	1	0	1	0	1	m_3	m_2	m_1	m_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
MCLR [HL],#m	Clearing of all bits in [HL] not masked by #m, A ← [HL]	1	1	0	0	0	0	0	1	0	0	0	1	1	0	m_3	m_2	m_1	m_0	√	—	—
MCLR [XY],#m	Clearing of all bits in [XY] not masked by #m, A ← [XY]	1	1	0	0	0	0	0	1	0	0	0	1	1	1	m_3	m_2	m_1	m_0	√	—	—
MCLR E:[HL],#m	Clearing of all bits in E:[HL] not masked by #m, A ← E:[HL]	1	1	0	0	0	0	0	1	0	0	0	1	0	0	m_3	m_2	m_1	m_0	√	—	—
MCLR E:[XY],#m	Clearing of all bits in E:[XY] not masked by #m, A ← E:[XY]	1	1	0	0	0	0	0	1	0	0	0	1	0	1	m_3	m_2	m_1	m_0	√	—	—
MCLR [HL+],#m	Clearing of all bits in [HL] not masked by #m, A ← [HL], HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	1	1	0	m_3	m_2	m_1	m_0	√	—	√
MCLR [XY+],#m	Clearing of all bits in [XY] not masked by #m, A ← [XY], XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	1	1	1	m_3	m_2	m_1	m_0	√	—	√
MCLR E:[HL+],#m	Clearing of all bits in E:[HL] not masked by #m, A ← E:[HL], HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	1	0	0	m_3	m_2	m_1	m_0	√	—	√
MCLR E:[XY+],#m	Clearing of all bits in E:[XY] not masked by #m, A ← E:[XY], XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	1	0	1	m_3	m_2	m_1	m_0	√	—	√

Mask Operation Instructions (continued)

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
MSET \cur,#m	Setting of all bits in cur not masked by #m, A ← cur	1	1	0	1	1	0	m_3	m_2	m_1	m_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
MSET [HL],#m	Setting of all bits in [HL] not masked by #m, A ← [HL]	1	1	0	0	0	0	0	0	1	0	0	1	1	0	m_3	m_2	m_1	m_0	√	—	—
MSET [XY],#m	Setting of all bits in [XY] not masked by #m, A ← [XY]	1	1	0	0	0	0	0	0	1	0	0	1	1	1	m_3	m_2	m_1	m_0	√	—	—
MSET E:[HL],#m	Setting of all bits in E:[HL] not masked by #m, A ← E:[HL]	1	1	0	0	0	0	0	0	1	0	0	1	0	0	m_3	m_2	m_1	m_0	√	—	—
MSET E:[XY],#m	Setting of all bits in E:[XY] not masked by #m, A ← E:[XY]	1	1	0	0	0	0	0	0	1	0	0	1	0	1	m_3	m_2	m_1	m_0	√	—	—
MSET [HL+],#m	Setting of all bits in [HL] not masked by #m, A ← [HL], HL ← HL + 1	1	1	0	0	0	0	0	0	1	1	0	1	1	0	m_3	m_2	m_1	m_0	√	—	√
MSET [XY+],#m	Setting of all bits in [XY] not masked by #m, A ← [XY], XY ← XY + 1	1	1	0	0	0	0	0	0	1	1	0	1	1	1	m_3	m_2	m_1	m_0	√	—	√
MSET E:[HL+],#m	Setting of all bits in E:[HL] not masked by #m, A ← E:[HL], HL ← HL + 1	1	1	0	0	0	0	0	0	1	1	0	1	0	0	m_3	m_2	m_1	m_0	√	—	√
MSET E:[XY+],#m	Setting of all bits in E:[XY] not masked by #m, A ← E:[XY], XY ← XY + 1	1	1	0	0	0	0	0	0	1	1	0	1	0	1	m_3	m_2	m_1	m_0	√	—	√

Mask Operation Instructions (continued)

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
MNOT \cur,#m	Inverting of all bits in cur not masked by #m, A ← cur	1	1	0	1	1	1	m_3	m_2	m_1	m_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
MNOT [HL],#m	Inverting of all bits in [HL] not masked by #m, A ← [HL]	1	1	0	0	0	0	0	0	0	0	0	1	1	0	m_3	m_2	m_1	m_0	√	—	—
MNOT [XY],#m	Inverting of all bits in [XY] not masked by #m, A ← [XY]	1	1	0	0	0	0	0	0	0	0	0	1	1	1	m_3	m_2	m_1	m_0	√	—	—
MNOT E:[HL],#m	Inverting of all bits in E:[HL] not masked by #m, A ← E:[HL]	1	1	0	0	0	0	0	0	0	0	0	1	0	0	m_3	m_2	m_1	m_0	√	—	—
MNOT E:[XY],#m	Inverting of all bits in E:[XY] not masked by #m, A ← E:[XY]	1	1	0	0	0	0	0	0	0	0	0	1	0	1	m_3	m_2	m_1	m_0	√	—	—
MNOT [HL+],#m	Inverting of all bits in [HL] not masked by #m, A ← [HL], HL ← HL + 1	1	1	0	0	0	0	0	0	0	1	0	1	1	0	m_3	m_2	m_1	m_0	√	—	√
MNOT [XY+],#m	Inverting of all bits in [XY] not masked by #m, A ← [XY], XY ← XY + 1	1	1	0	0	0	0	0	0	0	1	0	1	1	1	m_3	m_2	m_1	m_0	√	—	√
MNOT E:[HL+],#m	Inverting of all bits in E:[HL] not masked by #m, A ← E:[HL], HL ← HL + 1	1	1	0	0	0	0	0	0	0	1	0	1	0	0	m_3	m_2	m_1	m_0	√	—	√
MNOT E:[XY+],#m	Inverting of all bits in E:[XY] not masked by #m, A ← E:[XY], XY ← XY + 1	1	1	0	0	0	0	0	0	0	1	0	1	0	1	m_3	m_2	m_1	m_0	√	—	√

Bit Operation Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
BTST \cur.n	Bit testing of cur.n	1	1	1	0	1	1	n_3	n_2	n_1	n_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
BTST [HL].n	Bit testing of [HL].n	1	1	0	0	0	0	0	1	0	0	1	0	1	0	n_3	n_2	n_1	n_0	√	—	—
BTST [XY].n	Bit testing of [XY].n	1	1	0	0	0	0	0	1	0	0	1	0	1	1	n_3	n_2	n_1	n_0	√	—	—
BTST E:[HL].n	Bit testing of E:[HL].n	1	1	0	0	0	0	0	1	0	0	1	0	0	0	n_3	n_2	n_1	n_0	√	—	—
BTST E:[XY].n	Bit testing of E:[XY].n	1	1	0	0	0	0	0	1	0	0	1	0	0	1	n_3	n_2	n_1	n_0	√	—	—
BTST [HL+].n	Bit testing of [HL].n, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	1	0	1	0	n_3	n_2	n_1	n_0	√	—	√
BTST [XY+].n	Bit testing of [XY].n, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	1	0	1	1	n_3	n_2	n_1	n_0	√	—	√
BTST E:[HL+].n	Bit testing of E:[HL].n, HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	1	0	0	0	n_3	n_2	n_1	n_0	√	—	√
BTST E:[XY+].n	Bit testing of E:[XY].n, XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	1	0	0	1	n_3	n_2	n_1	n_0	√	—	√
BCLR \cur.n	cur.n ← 0, A ← cur	1	1	0	1	0	1	n_3	n_2	n_1	n_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
BCLR [HL].n	[HL].n ← 0, A ← [HL]	1	1	0	0	0	0	0	1	0	0	0	1	1	0	n_3	n_2	n_1	n_0	√	—	—
BCLR [XY].n	[XY].n ← 0, A ← [XY]	1	1	0	0	0	0	0	1	0	0	0	1	1	1	n_3	n_2	n_1	n_0	√	—	—
BCLR E:[HL].n	E:[HL].n ← 0, A ← E:[HL]	1	1	0	0	0	0	0	1	0	0	0	1	0	0	n_3	n_2	n_1	n_0	√	—	—
BCLR E:[XY].n	E:[XY].n ← 0, A ← E:[XY]	1	1	0	0	0	0	0	1	0	0	0	1	0	1	n_3	n_2	n_1	n_0	√	—	—
BCLR [HL+].n	[HL].n ← 0, A ← [HL], HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	1	1	0	n_3	n_2	n_1	n_0	√	—	√
BCLR [XY+].n	[XY].n ← 0, A ← [XY], XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	1	1	1	n_3	n_2	n_1	n_0	√	—	√
BCLR E:[HL+].n	E:[HL].n ← 0, A ← E:[HL], HL ← HL + 1	1	1	0	0	0	0	0	1	0	1	0	1	0	0	n_3	n_2	n_1	n_0	√	—	√
BCLR E:[XY+].n	E:[XY].n ← 0, A ← E:[XY], XY ← XY + 1	1	1	0	0	0	0	0	1	0	1	0	1	0	1	n_3	n_2	n_1	n_0	√	—	√
BSET \cur.n	cur.n ← 1, A ← cur	1	1	0	1	1	0	n_3	n_2	n_1	n_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
BSET [HL].n	[HL].n ← 1, A ← [HL]	1	1	0	0	0	0	0	0	1	0	0	1	1	0	n_3	n_2	n_1	n_0	√	—	—
BSET [XY].n	[XY].n ← 1, A ← [XY]	1	1	0	0	0	0	0	0	1	0	0	1	1	1	n_3	n_2	n_1	n_0	√	—	—
BSET E:[HL].n	E:[HL].n ← 1, A ← E:[HL]	1	1	0	0	0	0	0	0	1	0	0	1	0	0	n_3	n_2	n_1	n_0	√	—	—
BSET E:[XY].n	E:[XY].n ← 1, A ← E:[XY]	1	1	0	0	0	0	0	0	1	0	0	1	0	1	n_3	n_2	n_1	n_0	√	—	—
BSET [HL+].n	[HL].n ← 1, A ← [HL], HL ← HL + 1	1	1	0	0	0	0	0	0	1	1	0	1	1	0	n_3	n_2	n_1	n_0	√	—	√
BSET [XY+].n	[XY].n ← 1, A ← [XY], XY ← XY + 1	1	1	0	0	0	0	0	0	1	1	0	1	1	1	n_3	n_2	n_1	n_0	√	—	√
BSET E:[HL+].n	E:[HL].n ← 1, A ← E:[HL], HL ← HL + 1	1	1	0	0	0	0	0	0	1	1	0	1	0	0	n_3	n_2	n_1	n_0	√	—	√
BSET E:[XY+].n	E:[XY].n ← 1, A ← E:[XY], XY ← XY + 1	1	1	0	0	0	0	0	0	1	1	0	1	0	1	n_3	n_2	n_1	n_0	√	—	√

Bit Operation Instructions (continued)

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
BNOT \cur.n	cur.n ← $\overline{\text{cur.n}}$, A ← cur	1	1	0	1	1	1	n_3	n_2	n_1	n_0	r_7	r_6	r_5	r_4	r_3	r_2	r_1	r_0	√	—	—
BNOT [HL].n	[HL].n ← $\overline{\text{[HL].n}}$, A ← [HL]	1	1	0	0	0	0	0	0	0	0	0	1	1	0	n_3	n_2	n_1	n_0	√	—	—
BNOT [XY].n	[XY].n ← $\overline{\text{[XY].n}}$, A ← [XY]	1	1	0	0	0	0	0	0	0	0	0	1	1	1	n_3	n_2	n_1	n_0	√	—	—
BNOT E:[HL].n	E:[HL].n ← $\overline{\text{E:[HL].n}}$, A ← E:[HL]	1	1	0	0	0	0	0	0	0	0	0	1	0	0	n_3	n_2	n_1	n_0	√	—	—
BNOT E:[XY].n	E:[XY].n ← $\overline{\text{E:[XY].n}}$, A ← E:[XY]	1	1	0	0	0	0	0	0	0	0	0	1	0	1	n_3	n_2	n_1	n_0	√	—	—
BNOT [HL+].n	[HL].n ← $\overline{\text{[HL].n}}$, A ← [HL], HL ← HL + 1	1	1	0	0	0	0	0	0	0	1	0	1	1	0	n_3	n_2	n_1	n_0	√	—	√
BNOT [XY+].n	[XY].n ← $\overline{\text{[XY].n}}$, A ← [XY], XY ← XY + 1	1	1	0	0	0	0	0	0	0	1	0	1	1	1	n_3	n_2	n_1	n_0	√	—	√
BNOT E:[HL+].n	E:[HL].n ← $\overline{\text{E:[HL].n}}$, A ←E:[HL], HL ← HL + 1	1	1	0	0	0	0	0	0	0	1	0	1	0	0	n_3	n_2	n_1	n_0	√	—	√
BNOT E:[XY+].n	E:[XY].n ← $\overline{\text{E:[XY].n}}$, A ← E:[XY], XY ← XY + 1	1	1	0	0	0	0	0	0	0	1	0	1	0	1	n_3	n_2	n_1	n_0	√	—	√

ROM Table Reference Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
MOVHB [HL],[RA]	$[HL],[HL+1] \leftarrow (RA)_{15-8}$	1	2	0	0	0	0	0	0	1	1	0	0	1	0	0	0	1	0	—	—	—
MOVHB [XY],[RA]	$[XY],[XY+1] \leftarrow (RA)_{15-8}$	1	2	0	0	0	0	0	0	1	1	0	0	1	1	0	0	1	0	—	—	—
MOVHB E:[HL],[RA]	$E:[HL],E:[HL+1] \leftarrow (RA)_{15-8}$	1	2	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	0	—	—	—
MOVHB E:[XY],[RA]	$E:[XY],E:[XY+1] \leftarrow (RA)_{15-8}$	1	2	0	0	0	0	0	0	1	1	0	0	0	1	0	0	1	0	—	—	—
MOVHB [HL+],[RA]	$[HL],[HL+1] \leftarrow (RA)_{15-8}$, $HL \leftarrow HL+2$	1	2	0	0	0	0	0	0	1	1	0	0	1	0	1	0	1	0	—	—	√
MOVHB [XY+],[RA]	$[XY],[XY+1] \leftarrow (RA)_{15-8}$, $XY \leftarrow XY+2$	1	2	0	0	0	0	0	0	1	1	0	0	1	1	1	0	1	0	—	—	√
MOVHB E:[HL+],[RA]	$E:[HL],E:[HL+1] \leftarrow (RA)_{15-8}$, $HL \leftarrow HL+2$	1	2	0	0	0	0	0	0	1	1	0	0	0	0	1	0	1	0	—	—	√
MOVHB E:[XY+],[RA]	$E:[XY],E:[XY+1] \leftarrow (RA)_{15-8}$, $XY \leftarrow XY+2$	1	2	0	0	0	0	0	0	1	1	0	0	0	1	1	0	1	0	—	—	√
MOVHB [HL],cadr16	$[HL],[HL+1] \leftarrow (cadr16)_{15-8}$	2	3	0	0	0	0	0	0	1	1	0	0	1	0	0	1	0	0	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVHB [XY],cadr16	$[XY],[XY+1] \leftarrow (cadr16)_{15-8}$	2	3	0	0	0	0	0	0	1	1	0	0	1	1	0	1	0	0	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVHB E:[HL],cadr16	$E:[HL],E:[HL+1] \leftarrow (cadr16)_{15-8}$	2	3	0	0	0	0	0	0	1	1	0	0	0	0	0	1	0	0	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVHB E:[XY],cadr16	$E:[XY],E:[XY+1] \leftarrow (cadr16)_{15-8}$	2	3	0	0	0	0	0	0	1	1	0	0	0	1	0	1	0	0	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVHB [HL+],cadr16	$[HL],[HL+1] \leftarrow (cadr16)_{15-8}$, $HL \leftarrow HL+2$	2	3	0	0	0	0	0	0	1	1	0	0	1	0	1	1	0	0	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVHB [XY+],cadr16	$[XY],[XY+1] \leftarrow (cadr16)_{15-8}$, $XY \leftarrow XY+2$	2	3	0	0	0	0	0	0	1	1	0	0	1	1	1	1	0	0	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVHB E:[HL+],cadr16	$E:[HL],E:[HL+1] \leftarrow (cadr16)_{15-8}$, $HL \leftarrow HL+2$	2	3	0	0	0	0	0	0	1	1	0	0	0	0	1	1	0	0	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVHB E:[XY+],cadr16	$E:[XY],E:[XY+1] \leftarrow (cadr16)_{15-8}$, $XY \leftarrow XY+2$	2	3	0	0	0	0	0	0	1	1	0	0	0	1	1	1	0	0	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			

ROM Table Reference Instructions (continued)

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
MOVLB [HL],[RA]	[HL],[HL + 1] ← $(RA)_{7-0}$	1	2	0	0	0	0	0	0	1	1	0	0	1	0	0	0	1	1	—	—	—
MOVLB [XY],[RA]	[XY],[XY + 1] ← $(RA)_{7-0}$	1	2	0	0	0	0	0	0	1	1	0	0	1	1	0	0	1	1	—	—	—
MOVLB E:[HL],[RA]	E:[HL],E:[HL + 1] ← $(RA)_{7-0}$	1	2	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	—	—	—
MOVLB E:[XY],[RA]	E:[XY],E:[XY + 1] ← $(RA)_{7-0}$	1	2	0	0	0	0	0	0	1	1	0	0	0	1	0	0	1	1	—	—	—
MOVLB [HL+],[RA]	[HL],[HL + 1] ← $(RA)_{7-0}$, HL ← HL + 2	1	2	0	0	0	0	0	0	1	1	0	0	1	0	1	0	1	1	—	—	√
MOVLB [XY+],[RA]	[XY],[XY + 1] ← $(RA)_{7-0}$, XY ← XY + 2	1	2	0	0	0	0	0	0	1	1	0	0	1	1	1	0	1	1	—	—	√
MOVLB E:[HL+],[RA]	E:[HL],E:[HL + 1] ← $(RA)_{7-0}$, HL ← HL + 2	1	2	0	0	0	0	0	0	1	1	0	0	0	0	1	0	1	1	—	—	√
MOVLB E:[XY+],[RA]	E:[XY],E:[XY + 1] ← $(RA)_{7-0}$, XY ← XY + 2	1	2	0	0	0	0	0	0	1	1	0	0	0	1	1	0	1	1	—	—	√
MOVLB [HL],cadr16	[HL],[HL + 1] ← $(cadr16)_{7-0}$	2	3	0	0	0	0	0	0	1	1	0	0	1	0	0	1	0	1	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVLB [XY],cadr16	[XY],[XY + 1] ← $(cadr16)_{7-0}$	2	3	0	0	0	0	0	0	1	1	0	0	1	1	0	1	0	1	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVLB E:[HL],cadr16	E:[HL],E:[HL + 1] ← $(cadr16)_{7-0}$	2	3	0	0	0	0	0	0	1	1	0	0	0	0	0	1	0	1	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVLB E:[XY],cadr16	E:[XY],E:[XY + 1] ← $(cadr16)_{7-0}$	2	3	0	0	0	0	0	0	1	1	0	0	0	1	0	1	0	1	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVLB [HL+],cadr16	[HL],[HL + 1] ← $(cadr16)_{7-0}$, HL ← HL + 2	2	3	0	0	0	0	0	0	1	1	0	0	1	0	1	1	0	1	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVLB [XY+],cadr16	[XY],[XY + 1] ← $(cadr16)_{7-0}$, XY ← XY + 2	2	3	0	0	0	0	0	0	1	1	0	0	1	1	1	1	0	1	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVLB E:[HL+],cadr16	E:[HL],E:[HL + 1] ← $(cadr16)_{7-0}$, HL ← HL + 2	2	3	0	0	0	0	0	0	1	1	0	0	0	0	1	1	0	1	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVLB E:[XY+],cadr16	E:[XY],E:[XY + 1] ← $(cadr16)_{7-0}$, XY ← XY + 2	2	3	0	0	0	0	0	0	1	1	0	0	0	1	1	1	0	1	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			

External Memory Transfer Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
MOVXB [HL],[RA]	[HL],[HL + 1] ← (RA)	1	2	0	0	0	0	0	0	1	1	0	0	1	0	0	1	1	0	—	—	—
MOVXB [XY],[RA]	[XY],[XY + 1] ← (RA)	1	2	0	0	0	0	0	0	1	1	0	0	1	1	0	1	1	0	—	—	—
MOVXB E:[HL],[RA]	E:[HL],E:[HL + 1] ← (RA)	1	2	0	0	0	0	0	0	1	1	0	0	0	0	0	1	1	0	—	—	—
MOVXB E:[XY],[RA]	E:[XY],E:[XY + 1] ← (RA)	1	2	0	0	0	0	0	0	1	1	0	0	0	1	0	1	1	0	—	—	—
MOVXB [HL+],[RA]	[HL],[HL + 1] ← (RA), HL ← HL + 2	1	2	0	0	0	0	0	0	1	1	0	0	1	0	1	1	1	0	—	—	√
MOVXB [XY+],[RA]	[XY],[XY + 1] ← (RA), XY ← XY + 2	1	2	0	0	0	0	0	0	1	1	0	0	1	1	1	1	1	0	—	—	√
MOVXB E:[HL+],[RA]	E:[HL],E:[HL + 1] ← (RA), HL ← HL + 2	1	2	0	0	0	0	0	0	1	1	0	0	0	0	1	1	1	0	—	—	√
MOVXB E:[XY+],[RA]	E:[XY],E:[XY + 1] ← (RA), XY ← XY + 2	1	2	0	0	0	0	0	0	1	1	0	0	0	1	1	1	1	0	—	—	√
MOVXB [RA],[HL]	(RA) ← [HL],[HL + 1]	1	3	0	0	0	0	0	0	1	1	0	0	1	0	0	1	1	1	—	—	—
MOVXB [RA],[XY]	(RA) ← [XY],[XY + 1]	1	3	0	0	0	0	0	0	1	1	0	0	1	1	0	1	1	1	—	—	—
MOVXB [RA],E:[HL]	(RA) ← E:[HL],E:[HL + 1]	1	3	0	0	0	0	0	0	1	1	0	0	0	0	0	1	1	1	—	—	—
MOVXB [RA],E:[XY]	(RA) ← E:[XY],E:[XY + 1]	1	3	0	0	0	0	0	0	1	1	0	0	0	1	0	1	1	1	—	—	—
MOVXB [RA],[HL+]	(RA) ← [HL],[HL + 1], HL ← HL + 2	1	3	0	0	0	0	0	0	1	1	0	0	1	0	1	1	1	1	—	—	√
MOVXB [RA],[XY+]	(RA) ← [XY],[XY + 1], XY ← XY + 2	1	3	0	0	0	0	0	0	1	1	0	0	1	1	1	1	1	1	—	—	√
MOVXB [RA],E:[HL+]	(RA) ← E:[HL],E:[HL + 1], HL ← HL + 2	1	3	0	0	0	0	0	0	1	1	0	0	0	0	1	1	1	1	—	—	√
MOVXB [RA],E:[XY+]	(RA) ← E:[XY],E:[XY + 1], XY ← XY + 2	1	3	0	0	0	0	0	0	1	1	0	0	0	1	1	1	1	1	—	—	√

External Memory Transfer Instructions (continued)

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
MOVXB [HL],xadr16	[HL],[HL + 1] ← (xadr16)	2	3	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB [XY],xadr16	[XY],[XY + 1] ← (xadr16)	2	3	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB E:[HL],xadr16	E:[HL],E:[HL + 1] ← (xadr16)	2	3	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB E:[XY],xadr16	E:[XY],E:[XY + 1] ← (xadr16)	2	3	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB [HL+],xadr16	[HL],[HL + 1] ← (xadr16), HL ← HL + 2	2	3	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB [XY+],xadr16	[XY],[XY + 1] ← (xadr16), XY ← XY + 2	2	3	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB E:[HL+],xadr16	E:[HL],E:[HL + 1] ← (xadr16), HL ← HL + 2	2	3	0	0	0	0	0	0	1	1	1	1	0	0	1	0	0	0	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB E:[XY+],xadr16	E:[XY],E:[XY + 1] ← (xadr16), XY ← XY + 2	2	3	0	0	0	0	0	0	1	1	1	1	0	1	1	0	0	0	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB xadr16,[HL]	(xadr16) ← [HL],[HL + 1]	2	3	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	1	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB xadr16,[XY]	(xadr16) ← [XY],[XY + 1]	2	3	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	1	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB xadr16,E:[HL]	(xadr16) ← E:[HL],E:[HL + 1]	2	3	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	1	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB xadr16,E:[XY]	(xadr16) ← E:[XY],E:[XY + 1]	2	3	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	1	—	—	—
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB xadr16,[HL+]	(xadr16) ← [HL],[HL + 1], HL ← HL + 2	2	3	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	1	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB xadr16,[XY+]	(xadr16) ← [XY],[XY + 1], XY ← XY + 2	2	3	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	1	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB xadr16,E:[HL+]	(xadr16) ← E:[HL],E: [HL + 1], HL ← HL + 2	2	3	0	0	0	0	0	0	1	1	1	1	0	0	1	0	0	1	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
MOVXB xadr16,E:[XY+]	(xadr16) ← E:[XY],E: [XY + 1], XY ← XY + 2	2	3	0	0	0	0	0	0	1	1	1	1	0	1	1	0	0	1	—	—	√
				a_{15}	a_{14}	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			

Stack Operation Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
PUSH HL	(RSP) ← {FLAG, A, HL}, RSP ← RSP + 1	1	2	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	—	—	—
PUSH XY	(RSP) ← {CBR, EBR, XY}, RSP ← RSP + 1	1	2	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	—	—	—
POP HL	RSP ← RSP – 1, {FLAG, A, HL} ← (RSP)	1	2	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	√	√	√
POP XY	RSP ← RSP – 1, {CBR, EBR, XY} ← (RSP)	1	2	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	—	—	—

Flag Operation Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
FCLR G	G ← 0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	—	—	√
FCLR C	C ← 0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	—	√	—
FCLR Z	Z ← 0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	√	—	—
FSET G	G ← 1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	—	—	√
FSET C	C ← 1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	—	√	—
FSET Z	Z ← 1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	√	—	—

Jump Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
LJMP cadr14	PC ← cadr14	2	2	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	—	—	—
				0	0	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
JMP cadr12	PC_{11-0} ← cadr12	1	1	1	1	1	0	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0	—	—	—
SJMP radr8	PC ← Next PC + radr8	1	1	0	0	0	0	1	0	0	a_7	1	a_6	a_5	a_4	a_3	a_2	a_1	a_0	—	—	—
JMP PC + A	PC ← PC + A + 1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	—	—	—

Conditional Branch Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
BC radr8 BLT radr8	if C = 1 then PC ← Next PC + radr8 (<)	1	1	0	0	0	0	1	0	1	a_7	0	a_6	a_5	a_4	a_3	a_2	a_1	a_0	—	—	—
BNC radr8 BGE radr8	if C = 0 then PC ← Next PC + radr8 (≥)	1	1	0	0	0	0	1	0	1	a_7	1	a_6	a_5	a_4	a_3	a_2	a_1	a_0	—	—	—
BZ radr8 BEQ radr8	If Z = 1 then PC ← Next PC + radr8 (=)	1	1	0	0	0	0	1	1	0	a_7	0	a_6	a_5	a_4	a_3	a_2	a_1	a_0	—	—	—
BNZ radr8 BNE radr8	If Z = 0 then PC ← Next PC + radr8 (≠)	1	1	0	0	0	0	1	1	0	a_7	1	a_6	a_5	a_4	a_3	a_2	a_1	a_0	—	—	—
BLE radr8	If (C = 1) ∨ (Z = 1) then PC ← Next PC + radr8 (≤)	1	1	0	0	0	0	1	1	1	a_7	0	a_6	a_5	a_4	a_3	a_2	a_1	a_0	—	—	—
BGT radr8	If (C = 0) ∧ (Z =0) then PC ← Next PC + radr8 (>)	1	1	0	0	0	0	1	1	1	a_7	1	a_6	a_5	a_4	a_3	a_2	a_1	a_0	—	—	—
BNG radr8	if G = 0 then PC ← Next PC + radr8	1	1	0	0	0	0	1	0	0	a_7	0	a_6	a_5	a_4	a_3	a_2	a_1	a_0	—	—	—

Call/Return Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
LCAL cadr14	(SP) ← PC, PC ← cadr14, SP ← SP + 1	2	2	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	—	—	—
				0	0	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
CAL cadr12	(SP) ← PC, PC_{11-0} ← cadr12, SP ← SP + 1	1	1	1	1	1	1	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0	—	—	—
RT	PC ← (SP) + 1, SP ← SP – 1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	—	—	—
RTI	PC ← (SP) + 1, SP ← SP – 1, MIE ← 1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	—	—	—
RTNMI	PC ← (SP) + 1, SP ← SP – 1 MIE ← status of MIE before an interrupt occurs	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	—	—	—

Control Instructions

MNEMONIC	OPERATION	W	C	INSTRUCTION CODE																FLAG		
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Z	C	G
NOP	NO OPERATION	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	—	—	—
HALT	HALT CPU	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	—	—	—
EI	MIE ← 1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	—	—	—
DI	MIE ← 0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	—	—	—
INCB HL	HL ← HL + 1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	—	—	√
INCB XY	XY ← XY + 1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	—	—	√
INCW RA	RA ← RA + 1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	—	—	√
MOV CBR,#i4	CBR ← i4	1	1	0	0	0	0	0	0	0	0	0	0	1	1	i_3	i_2	i_1	i_0	—	—	—
MOV EBR,#i4	EBR ← i4	1	1	0	0	0	0	0	0	0	0	0	0	1	0	i_3	i_2	i_1	i_0	—	—	—
MOV RA0,#i4	RA0 ← i4	1	1	0	0	0	0	0	0	1	0	0	0	0	0	i_3	i_2	i_1	i_0	—	—	—
MOV RA1,#i4	RA1 ← i4	1	1	0	0	0	0	0	0	1	0	0	0	0	1	i_3	i_2	i_1	i_0	—	—	—
MOV RA2,#i4	RA2 ← i4	1	1	0	0	0	0	0	0	1	0	0	0	1	0	i_3	i_2	i_1	i_0	—	—	—
MOV RA3,#i4	RA3 ← i4	1	1	0	0	0	0	0	0	1	0	0	0	1	1	i_3	i_2	i_1	i_0	—	—	—
MOV H,#i4	H ← i4	1	1	0	0	0	0	0	0	0	1	0	0	1	1	i_3	i_2	i_1	i_0	—	—	—
MOV L,#i4	L ← i4	1	1	0	0	0	0	0	0	0	1	0	0	1	0	i_3	i_2	i_1	i_0	—	—	—
MOV X,#i4	X ← i4	1	1	0	0	0	0	0	0	0	1	0	0	0	1	i_3	i_2	i_1	i_0	—	—	—
MOV Y,#i4	Y ← i4	1	1	0	0	0	0	0	0	0	1	0	0	0	0	i_3	i_2	i_1	i_0	—	—	—
MSA cadr14	Melody output starts	2	3	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	—	—	—
				0	0	a_{13}	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			

Note:

The MSA cardr14 (melody output start) instruction is used only for MSM63188A.

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