OKI

MSM64167E

User's Manual

CMOS 4-bit microcontroller

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Introduction

The MSM64167E is a high-performance microcontroller that uses a 4-bit CPU core of nX-4/20 under Oki's original architecture to integrate peripheral functions.

This manual explains hardware of the MSM64167E.

For details of the nX-4/20 core instruction set, refer to the nX-4/20 Core Instruction Manual or nX-4/30 Core Instruction Manual.

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Chapter 1

Overview

Chapter 1 Overview

1.1 Overview

The MSM64167E is a CMOS 4-bit one-chip microcontroller that has built-in 256-nibble RAM, 12 I/O ports, buzzer output, a serial port, a dual slope type A/D converter, a 16-bit timer, and 31 LCD segment drivers.

The CPU uses a high-performance 4-bit CPU core of nX-4/20 with byte processing instructions and is best suited for applications such as thermometers, hygrometers and manometers because of the compact chip layout and ample peripheral functions.

1.2 Features

(1) Ample instruction set including byte arithmetic instructions
- 148 instructions
- Byte addition/subtraction, byte transfer and byte comparison instructions
- Bit operation instructions
- Data exchange instructions

(2) Ample addressing modes
- Two kinds of indirect addressing modes using HL registers and XY registers
- Bit operations on entire data memory area
- Byte operations on entire data memory area

(3) Operating frequencies
- Low speed clock: 32.768 kHz crystal oscillation
- High speed clock: 700 kHz, RC oscillation
- Minimum instruction execution time: 91 µs @ 32.768 kHz system clock
  4.3 µs @ 700 kHz system clock

(4) Internal program memory: 4064 bytes

(5) Internal data memory: 256 nibbles

(6) I/O ports: 12
- 4-bit input/output port (NMOS open drain output/CMOS output selectable, input with pull-down/pull-up resistance or high-impedance input selectable) × 3

(7) Buzzer output: 1
- 4 output modes selectable

(8) Serial port: 1
- Synchronous mode / asynchronous mode support
- Synchronous mode: 32.768 kHz/external clock
- Asynchronous mode: 9600 bps / 4800 bps / 2400 bps / 1200 bps

(9) LCD driver: 31
- At 1/4 duty and 1/3 bias: 108 segments (27 × 4)
- At 1/3 duty and 1/3 bias: 84 segments (28 × 3)
- At 1/2 duty and 1/2 bias: 58 segments (29 × 2)
- Output port selectable by mask option for 8 drivers

(10) Dual slope type A/D converter: 1
- Analog input: 4 channels
- Reference voltage internal generation
- Voice amplification circuit

(11) Timer: 16-bit × 1
- Auto reload mode
- Capture mode
- Clock frequency measurement mode

(12) Watchdog timer

(13) Interrupt factors: 10
- 2 external factors, 3 time base factors, 1 timer factor, 2 serial port factors, 1 A/D converter factor and 1 watchdog timer factor

(14) Power supply voltage
- 2.6 V to 3.6 V
- Low current consumption

(15) Exterior
- Chip
- 80-pin flat package GA: QFP (QFP80-P-1420-0.80-BK)
  TB: TQFP (TQFP80-P-1212-0.50-K)

1.3 Block Diagram

Figure 1-1 shows the block diagram of the MSM64167E.

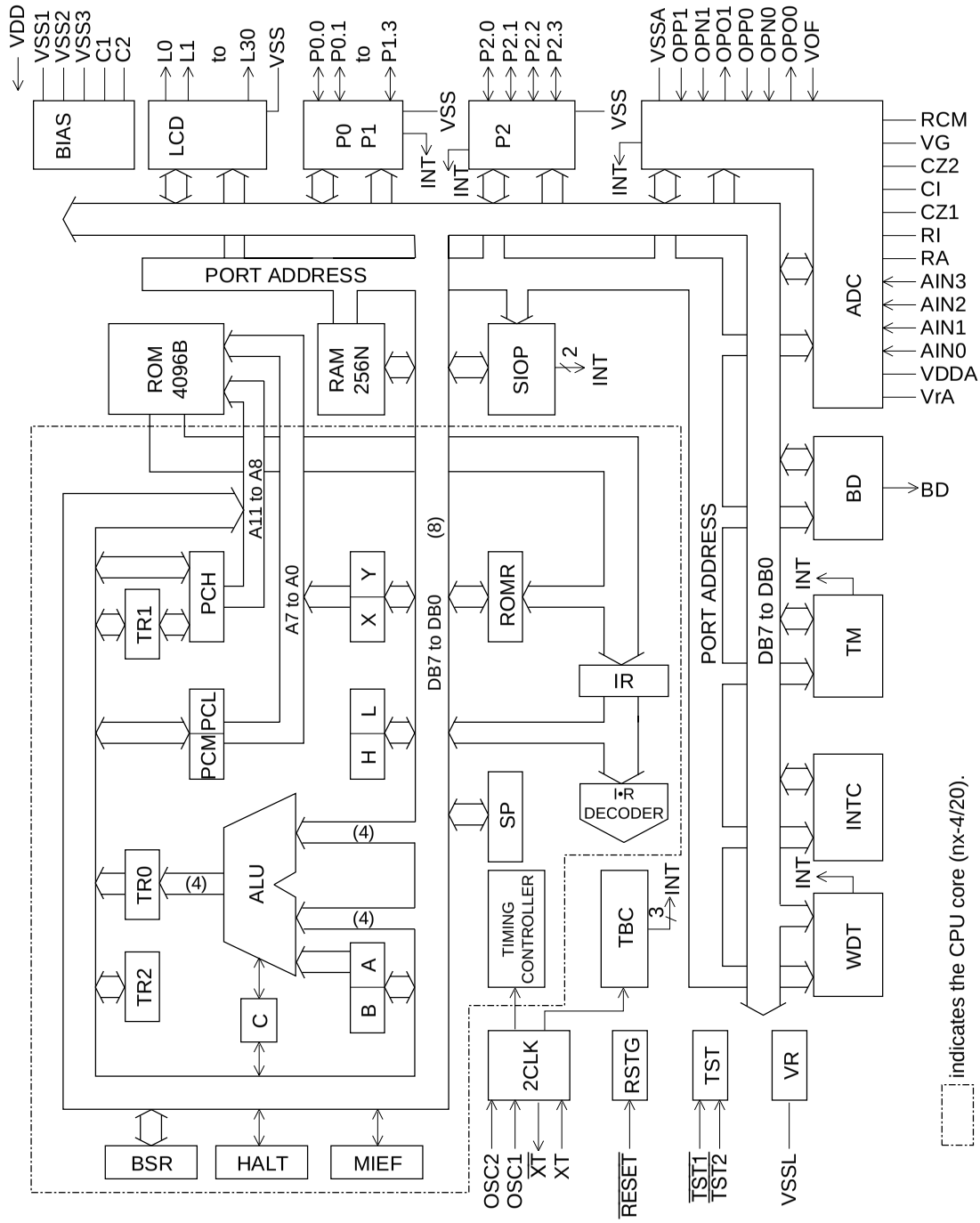


Figure 1-1 MSM64167E Block Diagram

1.4 Pin Configuration

Figures 1-2 and 1-3 show the MSM64167E package pin configurations and Figure 1-4 is the top view of the chip.

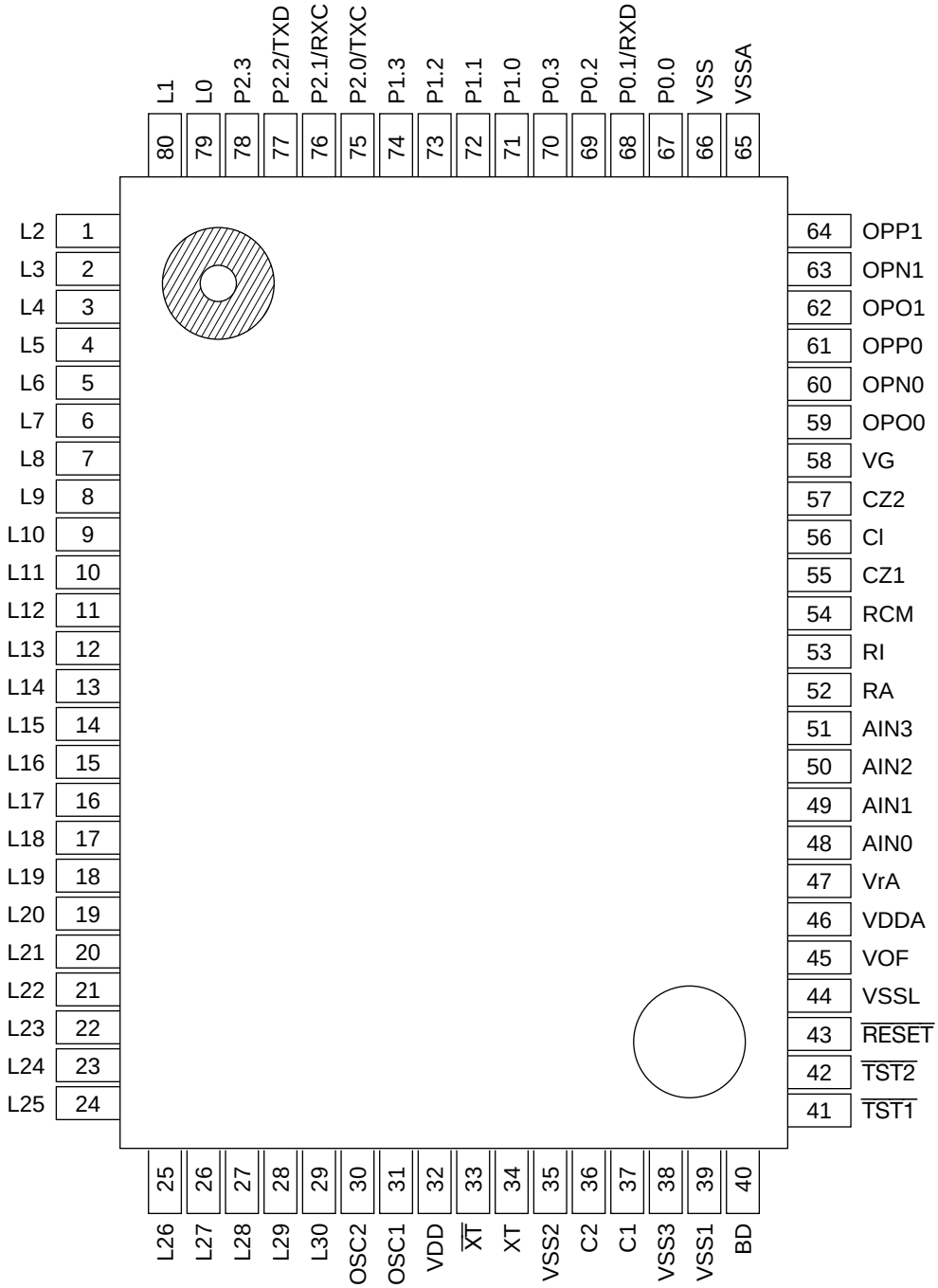


Figure 1-2 MSM64167E-GA (QFP) Pin Configuration

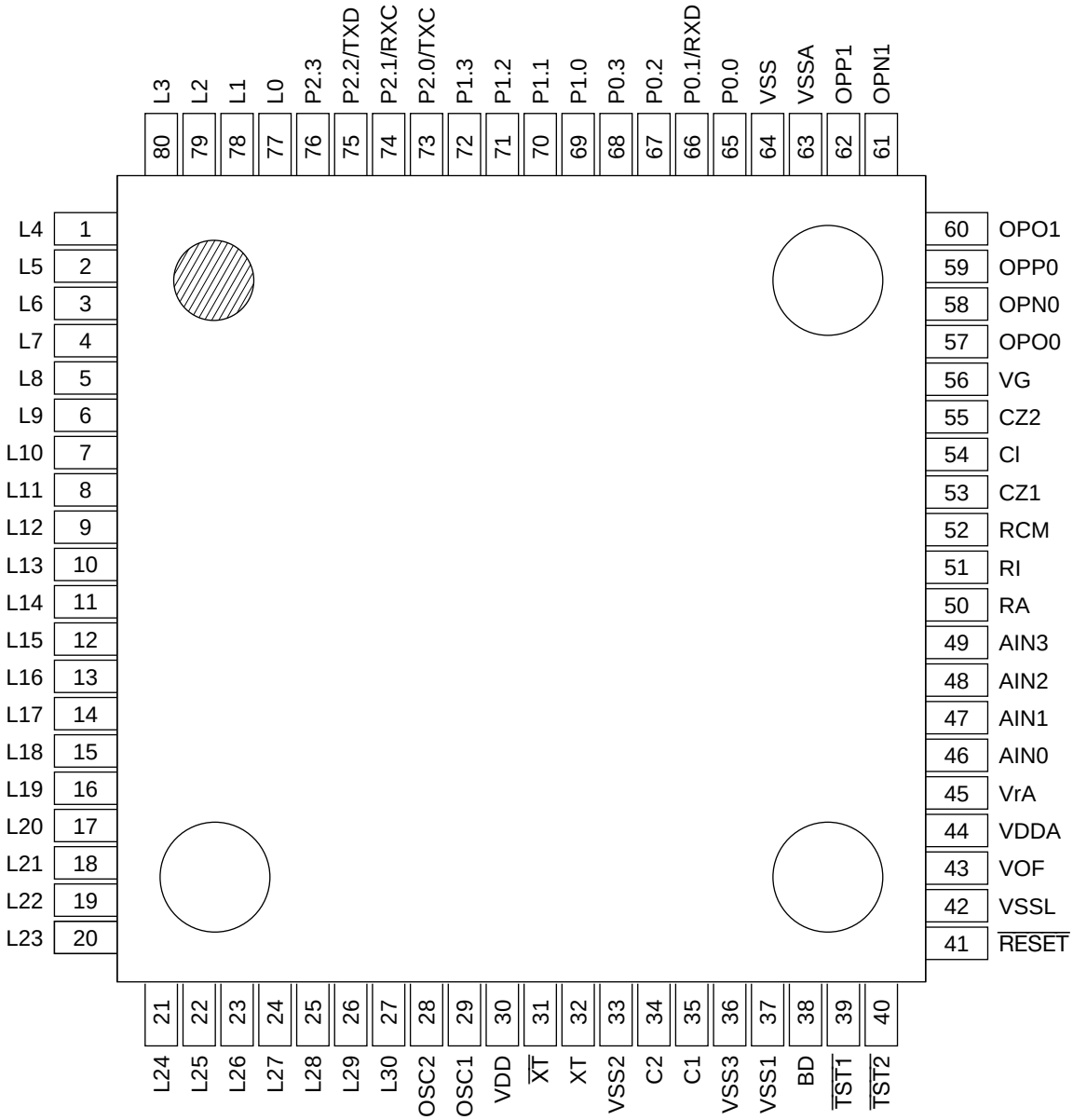
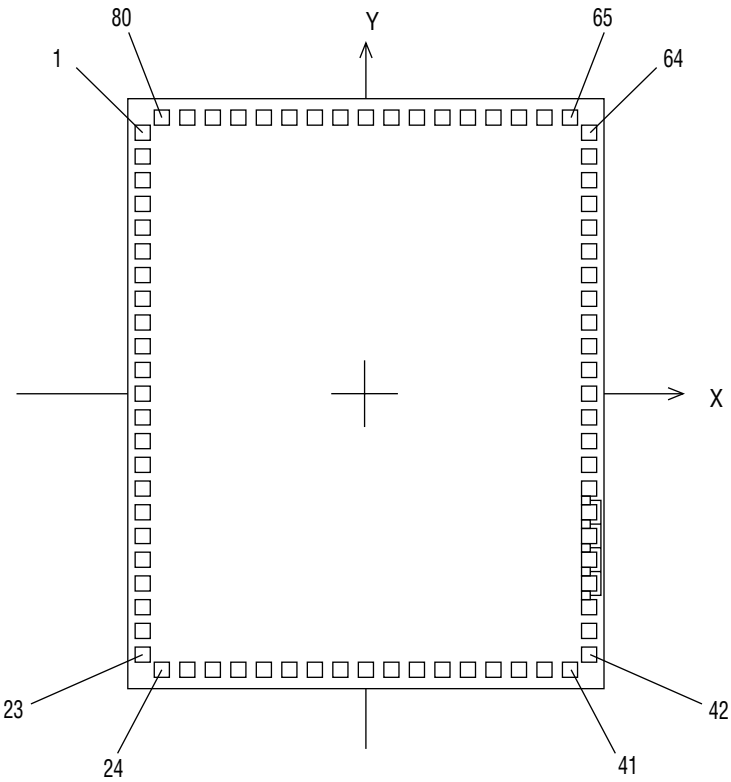


Figure 1-3 MSM64167E-TB (TQFP) Pin Configuration

Chip Size : 5.95 mm × 4.62 mm
Chip Thickness : 350 μm (Typ.)



Note: The chip substrate voltage is V_{DD}.

Figure 1-4 MSM64167E Chip External View

1.5 Description of Pins

1.5.1 Description of Each Pin

Table 1-1 lists the MSM64167E pin basic functions and Table 1-2 the pin secondary functions.

Table 1-1 (a) Pin Descriptions (Basic Functions)

Classification	Pin Name	Pin No.		Pad No.	I/O	Function
		GA	TB			
Power Supply	VDD	32	30	32	—	0 V power supply.
	VSS1	39	37	39	—	Bias output for driving LCD (–1.5 V).
	VSS2	35	33	35	—	Negative side power supply. Bias output for driving LCD (–3.0 V).
	VSS3	38	36	38	—	Bias output for driving LCD (–4.5 V).
	VSS	66	64	66	—	Negative side power supply for input/output port interface.
	C1	37	35	37	—	Capacitor connection for LCD driving bias generation.
	C2	36	34	36	—	
	VSSL	44	42	44	—	Negative side power supply pin for internal logic (internally generated constant voltage).
	VSSA	65	63	65	—	Externally connects to VSS2 negative side power supply for A/D converter.
	VDDA	46	44	46	—	Externally connects to VDD. 0 V power supply for A/D converter.
Oscillation	XT	34	32	34	I	Low speed side clock oscillation input pin: Connects to the crystal (32.768 kHz).
	$\overline{XT}$	33	31	33	O	
	OSC1	31	29	31	I	High speed side clock pin: Connects to the resistance for oscillation.
	OSC2	30	28	30	O	
Test	$\overline{TST1}$	41	39	41	I	Input pin for test: Pulled-up to VDD internally.
	$\overline{TST2}$	42	40	42	I	
Reset	$\overline{RESET}$	43	41	43	I	System reset input: When this pin becomes "H" level from "L" level, the internal state is initialized and execution of an instruction starts from address 000H. Pulled-up to VDD internally.

Table 1-1 (b) Pin Descriptions (Basic Functions)

Classification	Pin Name	Pin No.		Pad No.	I/O	Function
		GA	TB			
Port	P0.0	67	65	67	I/O	4-bit I/O Port (P0): 4-bit I/O port that can select I/O, pull-up/pull-down resistance input/high impedance input, and NMOS open drain output/CMOS output for each bit by port 0 control registers 0–3 (P00CON–P03CON). External interrupt function is assigned to each pin.
	P0.1	68	66	68	I/O	
	P0.2	69	67	69	I/O	
	P0.3	70	68	70	I/O	
	P1.0	71	69	71	I/O	4-bit I/O Port (P1): 4-bit I/O port that can select I/O, pull-up/pull-down resistance input/high impedance input, and NMOS open drain output/CMOS output for each bit by port 1 control registers 0–3 (P10CON–P13CON). External interrupt function is assigned to each pin.
	P1.1	72	70	72	I/O	
	P1.2	73	71	73	I/O	
	P1.3	74	72	74	I/O	
	P2.0	75	73	75	I/O	4-bit I/O Port (P2): 4-bit I/O port that can select I/O, pull-up/pull-down resistance input/high impedance input, and NMOS open drain output/ CMOS output for each bit by port 2 control registers 0–3 (P20CON–P23CON). External interrupt function is assigned to each pin.
	P2.1	76	74	76	I/O	
	P2.2	77	75	77	I/O	
	P2.3	78	76	78	I/O	
Buzzer	BD	40	38	40	O	Output pin of buzzer driver.
A/D Converter	AIN0	48	46	48	I	Analog voltage input pin. Can be selected to constant current for each pin by AD control register 0 (ADCON0).
	AIN1	49	47	49	I	
	AIN2	50	48	50	I	
	AIN3	51	49	51	I	
	RA	52	50	52	—	Resistance connection pin for current adjustment.
	RI	53	51	53	—	Resistance connection pin for integral.
	RCM	54	52	54	—	Common connection pin of resistance for integral, capacitor 1 for offset compensation, and capacitor integral.
	CZ1	55	53	55	—	Connection pin of capacitor 1 for offset compensation.
	CI	56	54	56	—	Connection pin of capacitor for integral.
	CZ2	57	55	57	—	Connection pin of capacitor 2 for offset compensation.
	VG	58	56	58	—	
	VOF	45	43	45	I	Connection pin of resistance for voltage amplification circuit offset adjustment.
	OPP0	61	59	61	I	Analog micro-voltage input pin.
	OPP1	64	62	64	I	
	OPN0	60	58	60	I	Connection pin of resistance for voltage amplification rate adjustment.
	OPN1	63	61	63	I	
	OPO0	59	57	59	O	
	OPO1	62	60	62	O	
	VrA	47	45	47	—	Standard voltage for A/D converter (internally generated constant voltage).

Table 1-1 (c) Description of Pins (Basic Functions)

Classification	Pin Name	Pin No.		Pad No.	I/O	Function
		GA	TB			
LCD Driver	L0	79	77	79	O	LCD segment and common signal output pins.
	L1	80	78	80	O	Becomes output port by mask option.
	L2	1	79	1	O	
	L3	2	80	2	O	
	L4	3	1	3	O	
	L5	4	2	4	O	
	L6	5	3	5	O	
	L7	6	4	6	O	
	L8	7	5	7	O	LCD segment and common signal output pins.
	L9	8	6	8	O	
	L10	9	7	9	O	
	L11	10	8	10	O	
	L12	11	9	11	O	
	L13	12	10	12	O	
	L14	13	11	13	O	
	L15	14	12	14	O	
	L16	15	13	15	O	
	L17	16	14	16	O	
	L18	17	15	17	O	
	L19	18	16	18	O	
	L20	19	17	19	O	
	L21	20	18	20	O	
	L22	21	19	21	O	
	L23	22	20	22	O	
	L24	23	21	23	O	
	L25	24	22	24	O	
	L26	25	23	25	O	
	L27	26	24	26	O	
	L28	27	25	27	O	
	L29	28	26	28	O	
	L30	29	27	29	O	

Table 1-2 Description of Pins (Secondary Functions)

Classification	Pin Name	Pin No.		Pad No.	I/O	Function
		GA	TB			
External Interrupt	P0.0	67	65	67	I	External interrupt input pins. Interrupt is enabled by level change.
	P0.1	68	66	68		
	P0.2	69	67	69		
	P0.3	70	68	70		
	P1.0	71	69	71		
	P1.1	72	70	72		
	P1.2	73	71	73		
	P1.3	74	72	74		
	P2.0	75	73	75		
	P2.1	76	74	76		
	P2.2	77	75	77		
	P2.3	78	76	78		
Serial Port	P0.1	68	66	68	I	Becomes receive data input pin (RXD) of serial port.
	P2.0	75	73	75	I/O	Becomes transmit clock I/O pin (TXC) of serial port.
	P2.1	76	74	76	I/O	Becomes receive clock output pin (RXC) of serial port.
	P2.2	77	75	77	O	Becomes transmit data output pin (TXD) of serial port.
Timer	P0.0	67	65	67	I	Becomes capture trigger input pin of timer.
	P0.2	69	67	69	I	Becomes external clock input pin (TMC) of timer.
	P2.3	78	76	78	O	Becomes timer overflow flag output pin (TMO) of timer.

1.5.2 Connections of Unused Pins

Table 1-3 shows unused pin connections.

Table 1-3 Connections of Unused Pins

Pin	Recommended Pin Connection	
OSC1	Open	
OSC2	Open	
$\overline{\text{TST1}}$, $\overline{\text{TST2}}$	Open	
$\overline{\text{RESET}}$	Open	
P0.0 to P0.3	When set to input:	"L" level, "H" level or open (depends on input mode selection)
	When set to output:	Open.
P1.0 to P1.3	When set to input:	"L" level, "H" level or open (depends on input mode selection)
	When set to output:	Open.
P2.0 to P2.3	When set to input:	"L" level, "H" level or open (depends on input mode selection)
	When set to output:	Open.
AIN0 to AIN3	Open	
VrA	Open	
VOF	Open	
RA	Open	
RI	Open	
RCM	Open	
CZ1, CZ2	Open	
VG	Open	
OPP0, OPP1	Open	
OPN0, OPN1	Open	
OPO0, OPO1	Open	
L0 to L30	Open	
BD	Open	

1.6 Basic Timing

The MSM64167E generates a system clock (CLK) without dividing the 32.768 kHz oscillation clocks by XT and ($\overline{XT}$) pins or 700 kHz RC oscillation clocks by OSC1 and OSC2 pins. A CLK signal phase matches the ($\overline{XT}$) pin of OSC1 pin phase.

Each instruction is processed with a machine cycle unit, and executed between one machine cycle (minimum) and five machine cycles (maximum).

One machine cycle includes three intervals of S1–S3 states. "State" is defined as an interval from the fall edge of the system clock (CLK) to the next fall. The S1 state of the first machine cycle (M1) of an instruction is M1 • S1.

Figure 1-5 shows an example of the relationship among the system clock, states, and machine cycles.

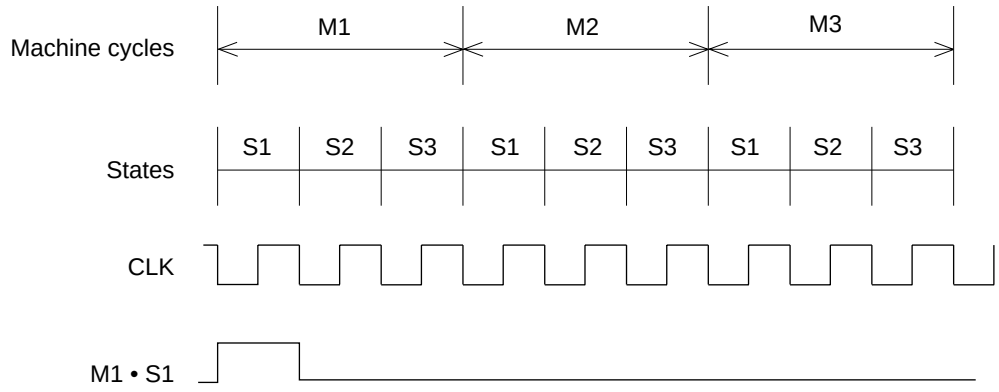


Figure 1-5 Definition of Machine Cycle

Chapter 2

CPU

Chapter 2 CPU

2.1 Overview

The instruction set of the MSM64167E is composed of 148 types of instructions that contain byte operations. The address space of the MSM64167E is divided into an 8-bit wide program memory area and a 4-bit wide data memory area.

A program data area and a 32-byte test data area are assigned to the program memory area. The data memory area has a 256-nibble RAM assigned to Bank 7, and the special function registers (SFRs) are assigned to Bank 0.

Stacks for subroutines and interrupts are assigned to 128 nibbles from address 7FFH to address 780H in Bank 7 by the stack pointer. Figure 2-1 shows each register and memory space.

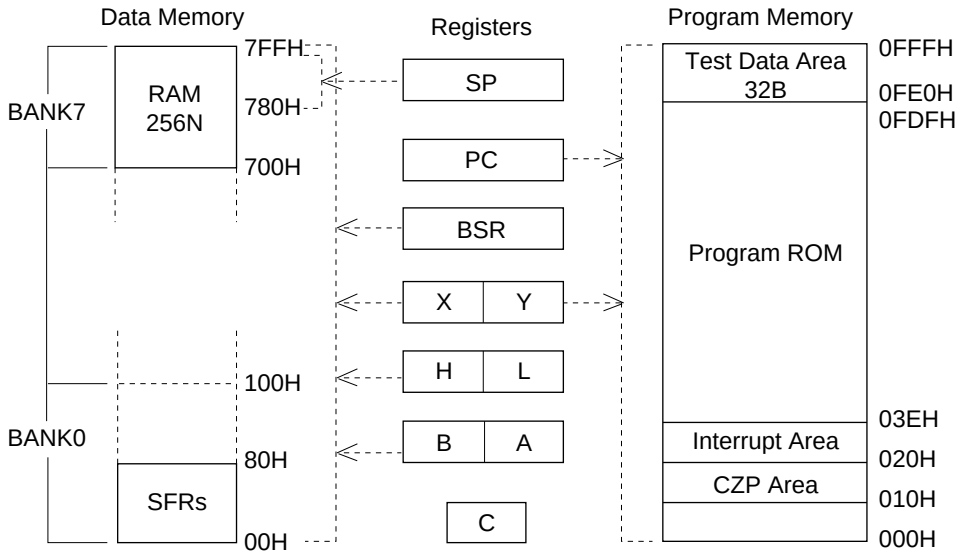


Figure 2-1 Registers and Memory Space

Notes:

(1) Banks in data memory are specified by the bank select register (BSR). In other words, they are specified by the contents of the bank select registers (BSR0 and BSR1) and the state of the bank control flags (BCF and BEF).

(2) The 32 bytes of 0FE0H–0FFFH of program memory are for the test data area and cannot be used as a program data area.

2.2 Configuration of Registers

Figure 2-2 shows the configuration of registers of MSM64167E.

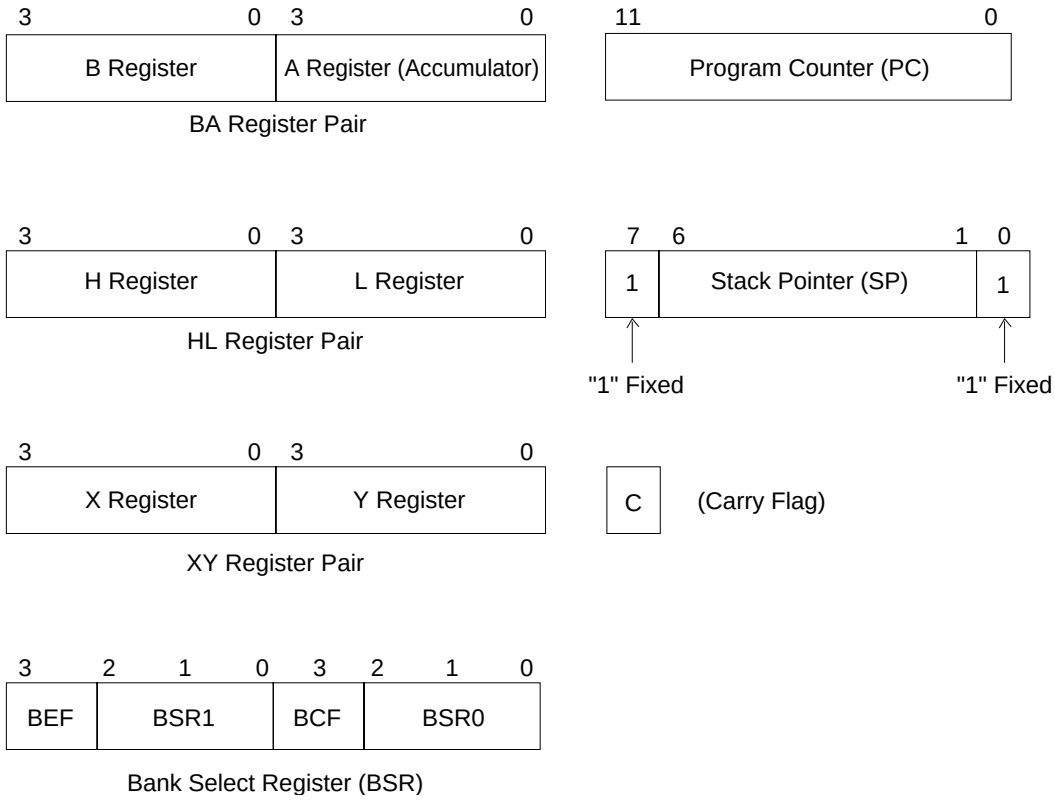
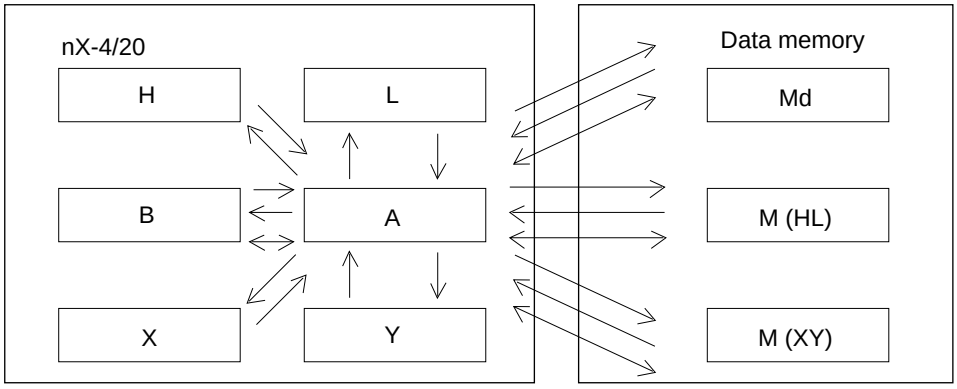


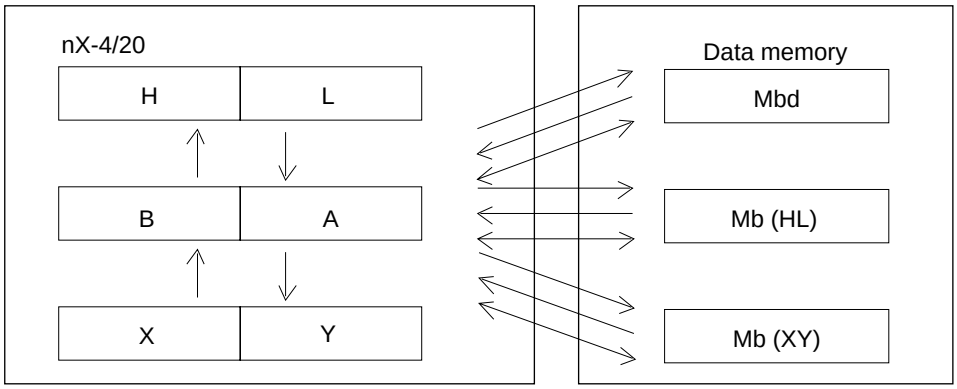
Figure 2-2 Configuration of MSM64167E Registers

2.2.1 Registers A, B, H, L, X and Y

The A register (accumulator) is a central register of each operation processing. B, H, L, X and Y are working registers. B and A register pairs play a central role in processing byte data. H and L register pairs and X and Y register pairs are used for the indirect addressing of data memory and for the working registers of byte processing. Figure 2-3 shows the possible combination of data transfers between each register and data memory.



(a) 4-bit Transfer



(b) 8-bit Transfer

Note:, →, ← : data transfer instruction
↔ : data exchange instruction

Figure 2-3 Combination of Data Transfers between Registers

In Figure 2-3, "M" indicates data memory, "d" indicates direct addressing mode specification, "(HL)" and "(XY)" indicate indirect addressing mode specification, and "b" indicates byte data. Arrows indicate the direction of data transfer.

When an interrupt occurs, BA and HL register pairs are automatically saved to a stack.

2.2.2 Program Counter (PC)

The program counter has 12 valid bits and can select a program memory area of 4K bytes.

2.2.3 Stack Pointer (SP)

The stack pointer (SP) is a register used to indicate the first address of a stack, and is assigned from 7EH–7FH of data memory bank 0.

The least significant bit and most significant bit of SP is fixed to "1". The remaining 6 bits function as an up/down counter for byte processing, which is decremented when data is saved to the stack and incremented when returned from the stack.

At system reset, SP becomes "0FFH" and the stack addresses become 0FFH and 0FEH in Bank 7.

Use a byte processing instruction when modifying or reading out the contents of SP. The content of SP cannot be read/written by a 4-bit processing instruction.

Bits 0 and 7 of SP are ignored if data write instructions are used, and is always "1" if a data read instruction is used.

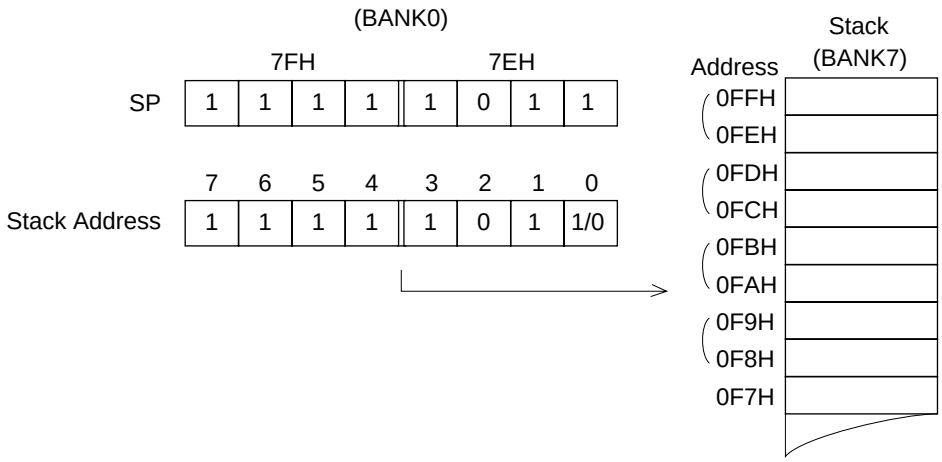


Figure 2-4 Relationship between Stack Pointer (SP) and Stack Address

2.2.4 Carry Flag (C)

A carry flag is a one-bit flag. A carry is loaded for an addition instruction, and a borrow is loaded for a subtraction instruction. When an interrupt occurs, a carry flag is automatically saved to a stack.

2.3 Memory Space

2.3.1 Program Memory

Program memory is a memory area for program data, interrupt area, the CZP area, the start address area and the test data area.

Data length is 8 bits with addresses 0–4095 assigned.

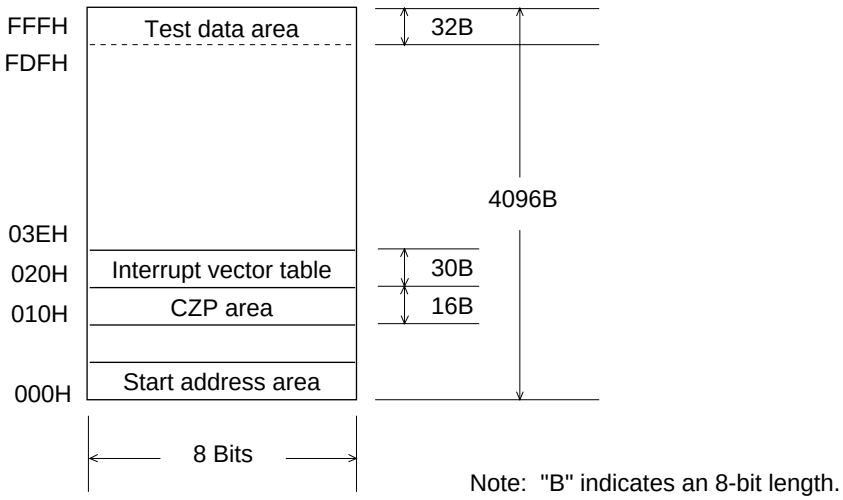


Figure 2-5 Program Memory Address Space

The address space of program memory is shown in Figure 2-5.

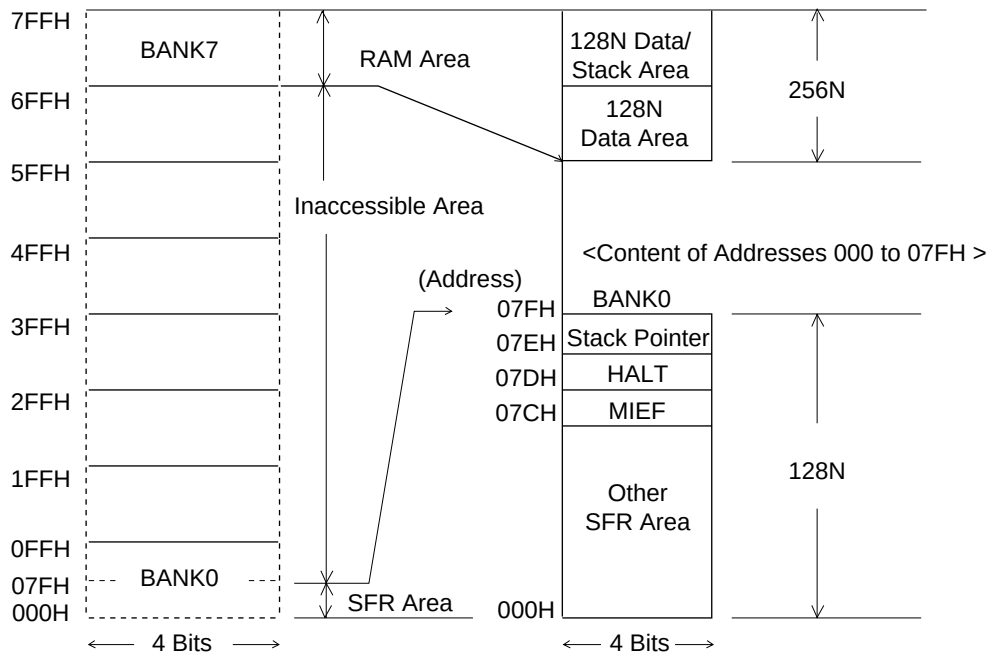
Address 0H is the instruction execution start address at system reset. CZP area from addresses 10H–1FH is the subroutine start address area for a 1-byte call instruction CZP. A maximum of 8 instructions can be assigned. The interrupt area is assigned from addresses 020H–03DH. Test data area is 32 bytes from addresses 0FE0H–0FFFH, and cannot be used as a program memory area.

For details on interrupts, refer to Chapter 4 "Interrupt" and related chapters for peripheral functions.

2.3.2 Data Memory

2.3.2.1 Data Memory Area

RAM and special function registers (SFRs) are assigned to data memory. Data memory is assigned to a different address than program memory. The data length is 4 bits (1 nibble). 256 nibbles is 1 bank unit. Data memory consists of two banks: one for the SFR area that uses part of Bank 0; and a RAM area that includes stacks of Bank 7.



Note: "N" indicates a 4-bit length.

Figure 2-6 Data Memory Address Space

Figure 2-6 shows the address space of data memory. The "stack area" is a data save area used for subroutines and interrupts, and is effective from the highest address of data memory address 7FFH, to a maximum 128N in the lower address direction.

Special function registers (SFRs) are assigned in the low order address direction from address 07FH of BANK 0. For addressing mode of the data memory space, the upper 3 bits of the 11 bits of the data memory address are determined by bank specification. The lower 8 bits are determined by either HL indirect addressing mode, XY indirect addressing mode or direct addressing mode.

However, addresses 0H–7FH of BANK 0 is a special area. If this area is specified by direct addressing mode when the bank common flag (BCF) is 1, Bank 0 is always selected. Bank specification is ignored only in this case.

2.3.2.2 Bank Specification of Data Memory

Banks of data memory are specified by dedicated bank select registers (BSR0 and BSR1), the bank common flag (BCF) and by the bank enable flag (BEF). These registers and flags can be saved and resorted to the stack at the same time by the "PUSH BSR" and "POP BSR" instructions.

There are four modes to address internal banks of data memory: HL indirect addressing mode, XY indirect addressing mode, direct addressing mode and the stack indirect addressing mode. The bank specification method differs depending on the mode.

Table 2-1 shows the BCF and BEF function table. As shown in this table, the bank specification method is determined by BCF, BEF and addressing mode. "BSR0" and "BSR1" in the table indicate that a bank is specified by BSR0 and BSR1. In direct addressing mode, Bank 0 is always specified only when BCF = 1 and the addresses are specified as 0–7FH.

Table 2-2 shows the correspondence between the contents of BSR0 and BSR1 and the bank number.

Table 2-1 Relationship between BCF, BEF and Bank Specification by Addressing Mode

BCF	BEF	HL indirect addressing	XY indirect addressing	Direct addressing	SP indirect addressing
0	0	BSR0	BSR0	BSR0	<BANK7>
0	1	BSR0	BSR1	BSR1	
1	0	BSR0	BSR0	• When internal bank addresses are 0 to 7FH:<BANK0> • When internal bank addresses are 80 to FFH:BSR0	
1	1	BSR0	BSR1	• When internal bank addresses are 0 to 7FH:<BANK0> • When internal bank addresses are 80 to FFH:BSR1	

Table 2-2 Correspondance between Contents of BSR0, BSR1 and Bank Number

BSR0, BSR1	Bank number	BSR0, BSR1	Bank number
0	BANK0	4	BANK0
1	BANK7	5	BANK7
2	BANK0	6	BANK0
3	BANK7	7	BANK7

2.3.2.3 Addressing Modes of Data Memory

(1) HL indirect addressing mode

Internal bank addresses can be specified by an HL register pair.

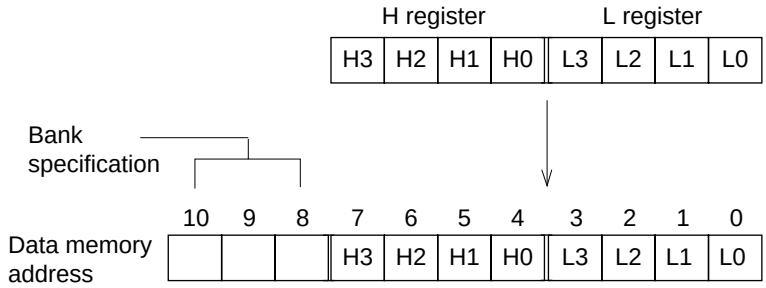


Figure 2-6 Data Memory Address by HL Indirect Addressing

(2) XY indirect addressing mode

Internal bank addresses can be specified by an XY register pair.

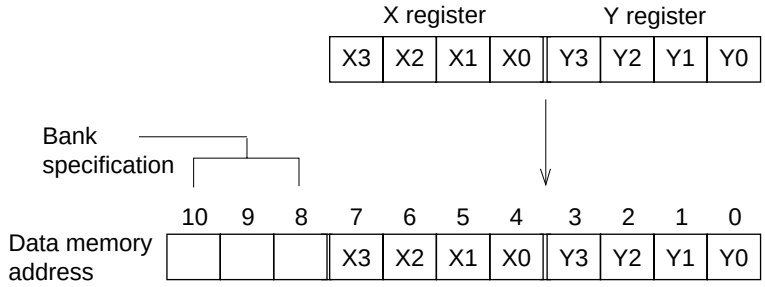


Figure 2-7 Data Memory Address by XY Indirect Addressing

(3) Direct addressing mode

Internal bank addresses can be directly specified by 8-bit immediate data included in the instruction code.

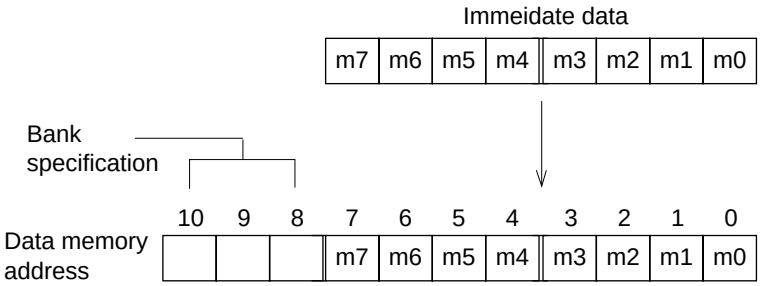


Figure 2-8 Data Memory Address by Direct Addressing

(4) Stack pointer indirect addressing mode

Addresses in Bank 7 can be specified by stack pointer (SP). This mode is used for stack operation in "PUSH" and "POP" instructions, subroutine jumps, return instructions and interrupts.

Since data is always handled as 8 bits in this mode, bit 0 of this address is invalid. Although SP is 8 bits, the most significant bit and the least significant bit are fixed to "1". The remaining 6 bits function as an up/down counter.

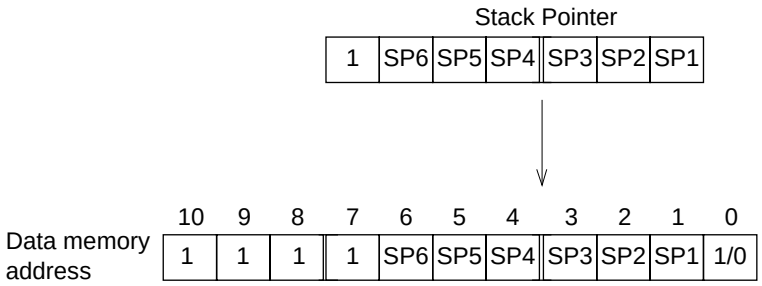


Figure 2-9 Data Memory Address by Stack Pointer Indirect Addressing

Chapter 3

CPU Control Functions

Chapter 3 CPU Control Functions

3.1 Overview

The MSM64167E has halt mode in addition to normal operation mode. Operation status can be classified as follows:

- Normal operation mode
- System reset mode
- Halt mode

Figure 3-1 shows the transition of each state.

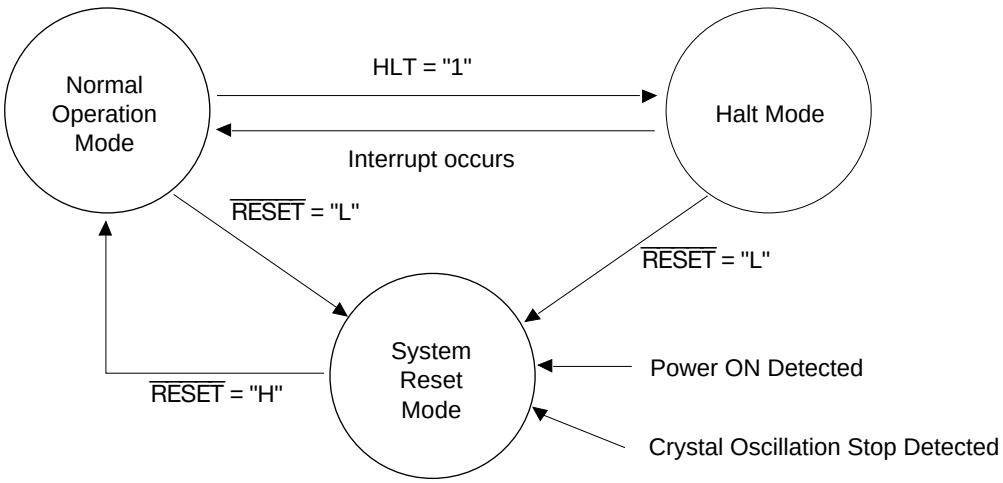


Figure 3-1 Operation Status Transition Diagram

In normal operation mode, the CPU executes instructions successively. In system reset mode, the CPU enters system reset processing by reset input, and each register and pin are initialized to start execution of the instruction. After system reset processing, instruction execution starts from address 000H.

In halt mode, the CPU stops and instruction execution is interrupted. PC is not incremented. Although instruction execution stops, internal peripheral functions continue operation. To enter halt mode, set the HLT flag to "1".

Port and peripheral functions do not change even in halt mode.

3.2 System Reset Function

3.2.1 System Reset Mode

MSM64167E enters system reset mode if one of the following is met: a) power-on is detected, b) crystal oscillation STOP is detected, c) the $\overline{\text{RESET}}$ pin is set to "L" level. In system clock mode, the following operation is performed:

(1) CPU is initialized.

(2) In power ON state, if the $\overline{\text{RESET}}$ pin is in "L" level, constant voltage generation circuit (VR) reaches excitation status.

(3) Output of all LCD drivers are turned off at the VDD level. At about 63 ms after oscillation start, display wave forms are output to the LCD driver. (If not in LCD OFF mode)

(4) All the special function registers (SFRs), other than TMD0–3, TMC0–3, are initialized.

After system reset, instruction execution starts from address 000H.

Figures 3-2 and 3-3 show the system reset generation circuit and each signal at system reset.

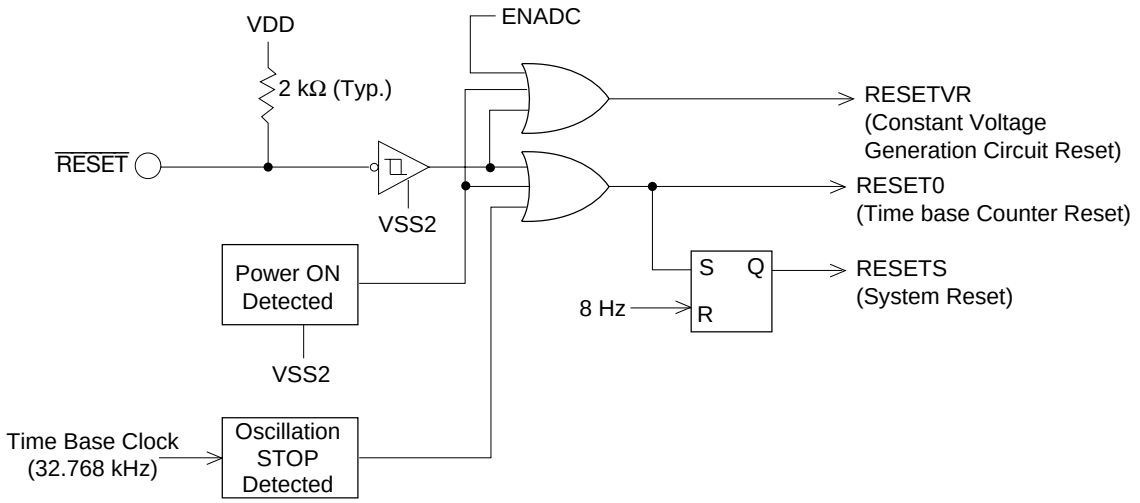


Figure 3-2 System Reset Generation Circuit

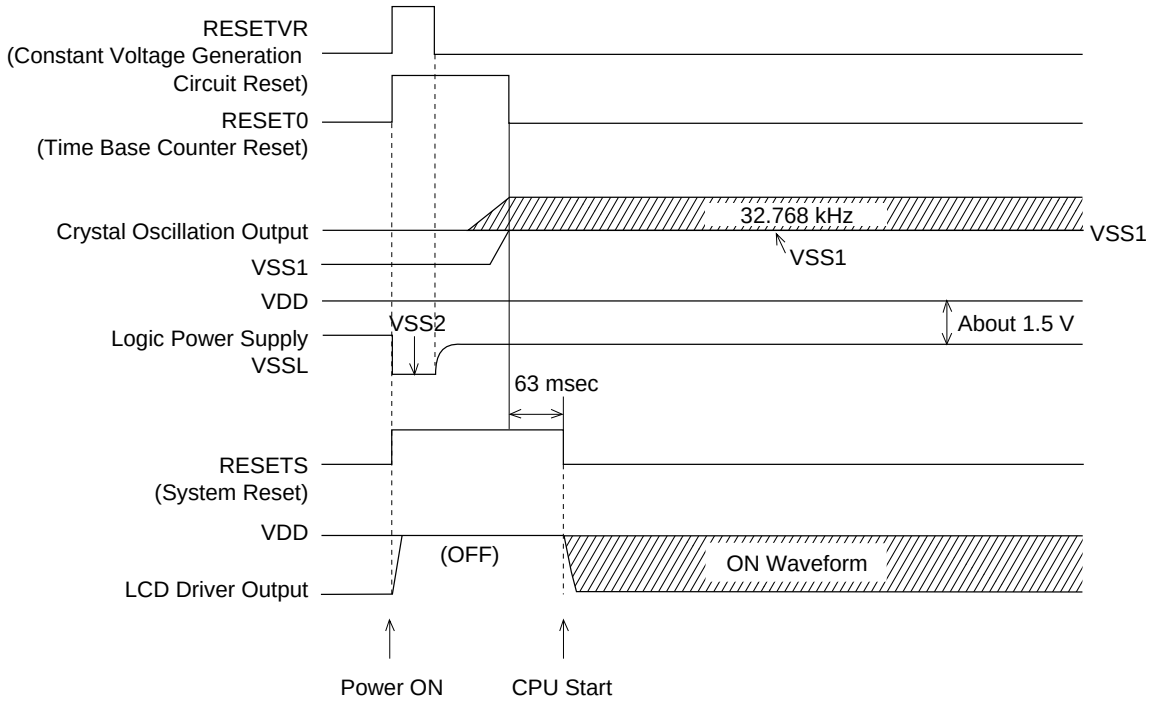


Figure 3-3 Each Signal at System Reset Generation

3.2.2 Status at System Reset

Table 3-1 shows the status of the registers after system reset.

Table 3-1 (a) Initial Values at System Reset

Register/Flag	Value at system reset	Note
Program counter (PC)	000H	
A register (A)	0H	
B register (B)	0H	
Carry flag (C)	0	
HL register pair (HL)	00H	
XY register pair (XY)	00H	
Stack pointer (SP)	0FFH	
Bank select register 0 (BSR0)	0H	
Bank select register 1 (BSR1)	0H	
Bank common flag (BCF)	0	
Bank enable flag (BEF)	0	
Port 0 register (P0)	0H	
Port 1 register (P1)	0H	
Port 2 register (P2)	0H	
Port 00 control register (P00CON)	0H	Input mode, input with pull-up/pull-down resistance, 64 Hz sampling, interrupt disabled
Port 01 control register (P01CON)	0H	Input mode, input with pull-up/pull-down resistance, 64 Hz sampling, interrupt disabled
Port 02 control register (P02CON)	0H	Input mode, input with pull-up/pull-down resistance, 64 Hz sampling, interrupt disabled
Port 03 control register (P03CON)	0H	Input mode, input with pull-up/pull-down resistance, 64 Hz sampling, interrupt disabled

Table 3-1 (b) Initial Values at System Reset

Register/Flag	Value at system reset	Note
Port 10 control register (P10CON)	0H	Input mode, input with pull-up/pull-down resistance, 64 Hz sampling, interrupt disabled
Port 11 control register (P11CON)	0H	Input mode, input with pull-up/pull-down resistance, 64 Hz sampling, interrupt disabled
Port 12 control register (P12CON)	0H	Input mode, input with pull-up/pull-down resistance, 64 Hz sampling, interrupt disabled
Port 13 control register (P13CON)	0H	Input mode, input with pull-up/pull-down resistance, 64 Hz sampling, interrupt disabled
Port 20 control register (P20CON)	0H	Input mode, input with pull-up/pull-down resistance, 64 Hz sampling, interrupt disabled
Port 21 control register (P21CON)	0H	Input mode, input with pull-up/pull-down resistance, 64 Hz sampling, interrupt disabled
Port 22 control register (P22CON)	0H	Input mode, input with pull-up/pull-down resistance, 64 Hz sampling, interrupt disabled
Port 23 control register (P23CON)	0H	Input mode, input with pull-up/pull-down resistance, 64 Hz sampling, interrupt disabled
Port control register (PCON)	0EH	P0, P1, P2 input with pullup resistance
Frequency control register (FCON)	0EH	Crystal oscillation clock
Buzzer driver control register (BDCON)	0H	Positive logic output, Buzzer disabled, intermittent sound 1 output
Buzzer frequency control register (BFCON)	0EH	Buzzer frequency 4 kHz
Display control register (DSPCON)	8H	1/4 duty
Display control registers 0 to 30 (DSPR0 to 30)	0H	

Table 3-1 (c) Initial Values at System Reset

Register/Flag	Value at system reset	Note
Timer data register 0 (TMD0)	Undefined	
Timer data register 1 (TMD1)	Undefined	
Timer data register 2 (TMD2)	Undefined	
Timer data register 3 (TMD3)	Undefined	
Timer counter register 0 (TMC0)	Undefined	
Timer counter register 1 (TMC1)	Undefined	
Timer counter register 2 (TMC2)	Undefined	
Timer counter register 3 (TMC3)	Undefined	
Timer control register 0 (TMCON0)	0H	Auto reload mode, counter stop
Timer control register 1 (TMCON1)	0H	TMCLK = 32.768 kHz
Timer status register (TMSTAT)	0H	
AD control register 0 (ADCON0)	0H	
AD control register 1 (ADCON1)	1H	
AD control register 2 (ADCON2)	8H	
Transmit control register (L) (STCONL)	0H	
Transmit control register (H) (STCONH)	0H	
Transmit buffer register (L) (STBUFL)	0H	
Transmit buffer register (H) (STBUFH)	0H	
Receive control register (L) (SRCONL)	0H	
Receive control register (H) (SRCONH)	0H	
Receive baud rate setting register (SRBRT)	0CH	
Status Register (SSTAT)	0H	

Table 3-1 (d) Initial Values at System Reset

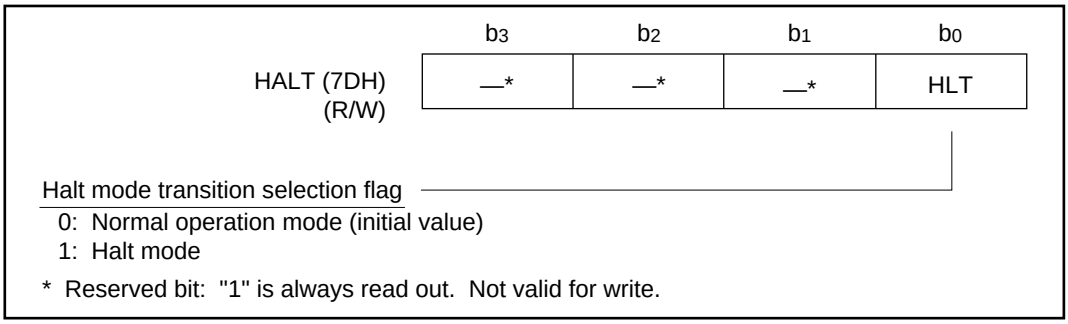
Register/Flag	Value at system reset	Note
Watchdog timer control register (WDTCON)	—	Stop
VSSL control register (VSSLCON)	0EH	VDD – 1.5 V level
Interrupt request register 0 (IRQ0)	0H	
Interrupt request register 1 (IRQ1)	0H	
Interrupt request register 2 (IRQ2)	0CH	
Interrupt enable register 0 (IE0)	0H	Interrupt disalbed
Interrupt enable register 1 (IE1)	0H	Interrupt disabled
Interrupt enable register 2 (IE2)	0EH	Interrupt disabled
Halt mode register (HALT)	0EH	Normal operation mode
Master interrupt enable register (MIEF)	0EH	Interrupt disabled

Note: System reset has priority over all processings, stopping previous processing. Therefore, the content of RAM, TMD0–TMD3, and TMC0–TMC3, not initialized at system reset, is not guaranteed.

3.3 Halt Mode

3.3.1 Halt Mode Register (HALT)

This is a special function register (SFR) that controls conversion to halt mode.



Bit 0: HLT

Flag to enter halt mode. If the HLT flag is set to "1", CPU enters halt mode at the first machine cycle of the next instruction.

3.3.2 Operation in Halt Mode

If an instruction to set an HLT flag to "1" is executed, the CPU enters halt mode at the first machine cycle of the next instruction. However, if in interrupt request status, the CPU does not enter halt mode.

In halt mode, oscillation and time base counter operations continue, and the CPU repeats fetching next instruction at S1 state.

Either system reset or an interrupt can release halt mode (reset HLT flag). If halt mode is released by an interrupt, set the interrupt enable flag used for release to "1" before entering halt mode.

Figure 3-4 shows the timing to enter halt mode and the release timing of halt mode by an interrupt.

Instruction execution after the release differs depending on the status of the master interrupt enable flag (MI). If the MI flag is "1", instruction execution restarts from the interrupt processing routine after one dummy cycle, as shown in Figure 3-4. If the MI flag is "0", instruction execution restarts from the next address of the halt instruction without a dummy cycle.

Note: To release halt mode, the individual interrupt enable flag must be set to "1", regardless of the MI flag state. If the individual interrupt enable flag is set to "0", the HLT flag cannot be reset, because of the interrupt request signal that corresponds to the enable flag.

If an individual interrupt enable flag was set, the interrupt request flag is set to "1", even if the MI flag is "0" when halt mode was released by an interrupt.

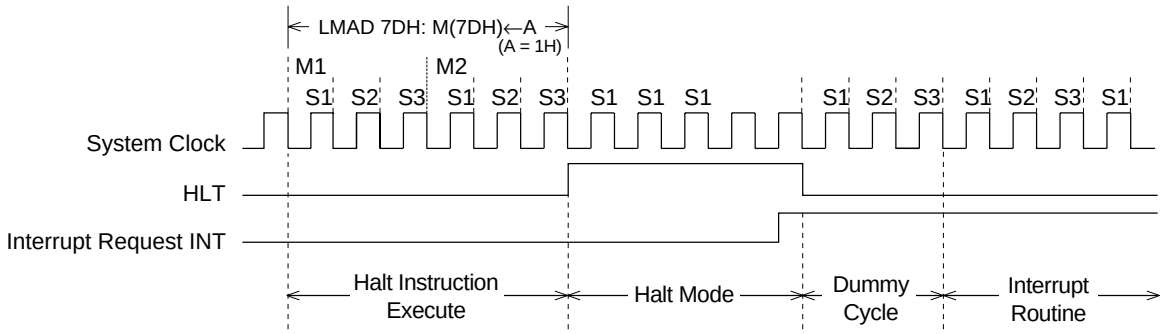


Figure 3-4 Timing of Halt Mode Set and Halt Mode Reset by Interrupt (when the MI flag = 1)

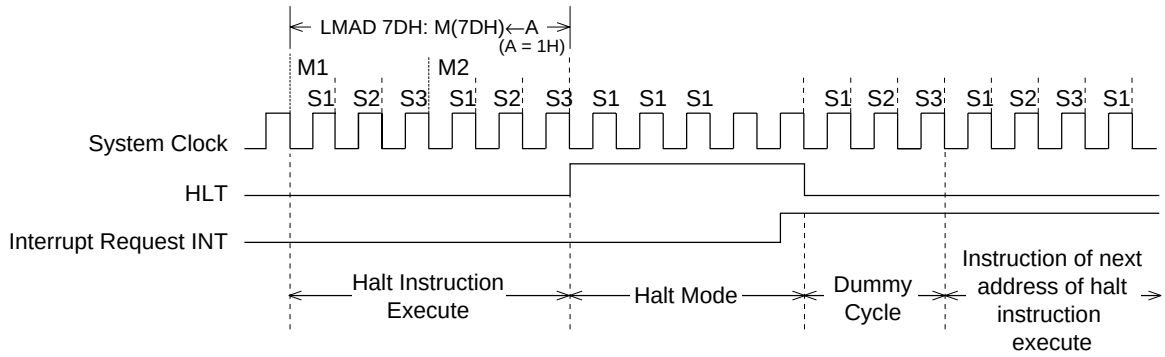


Figure 3-5 Timing of Halt Mode Set and Halt Mode Reset by Interrupt (when the MI flag = 0)

Chapter 4

Interrupt (INTC)

Chapter 4 Interrupt (INTC)

4.1 Overview

The MSM64167E has two external interrupt factors from ports and eight internal interrupt factors, totaling 10 interrupt factors (10 vector addresses). Of these 10 interrupt factors, only the watchdog timer interrupt cannot be disabled (non-maskable interrupt). Enable/disable of the other nine interrupts are controlled by the master interrupt enable flag (MI) and each interrupt enable register (IE0, IE1, IE2). If interrupt conditions are met, the program branches to vector addresses determined for each interrupt factor, and enters an interrupt routine.

Table 4-1 lists interrupt factors. Figure 4-1 shows an interrupt control equivalent circuit.

Table 4-1 Interrupt Factors

No.	Interrupt Factor	Abbreviated Name	Vector Address
1	Watchdog timer interrupt	WDTINT	03BH
2	External 0 interrupt (P0, P1)	XI0INT	038H
3	Serial port receive interrupt	SRINT	035H
4	Serial port transmit interrupt	STINT	032H
5	External 1 interrupt (P2)	XI1INT	02FH
6	Timer interrupt	TMINT	02CH
7	A/D converter interrupt	ADINT	029H
8	32 Hz interrupt	32HzINT	026H
9	16 Hz interrupt	16HzINT	023H
10	1 Hz interrupt	1HzINT	020H

If interrupt factors are generated at the same time, the interrupt with the bigger vector address has execution priority (WDTINT has the highest priority). For details on each interrupt operation, see Chapter 6 "Time Base Counter", Chapter 7 "Ports", Chapter 8 "Timer", Chapter 9 "Serial Port", Chapter 11 "Watchdog Timer" and Chapter 12 "A/D Converter".

Note: Interrupt requests generated under the following conditions are temporarily held.

1) When skip conditions are established after executing a skip instruction. (A skip operation requires the same time as a machine cycle to execute the instruction to be skipped. Therefore such an interrupt request is held for the same length of time as a machine cycle to execute the instruction to be skipped.)
2) When LAI and LLI instructions (vertical stack instructions) are executed.
3) When ADCS and SUBCS instructions are executed.

If the next instruction does not satisfy the above conditions, interrupt requests that are held under the above conditions are accepted after the instruction is executed.

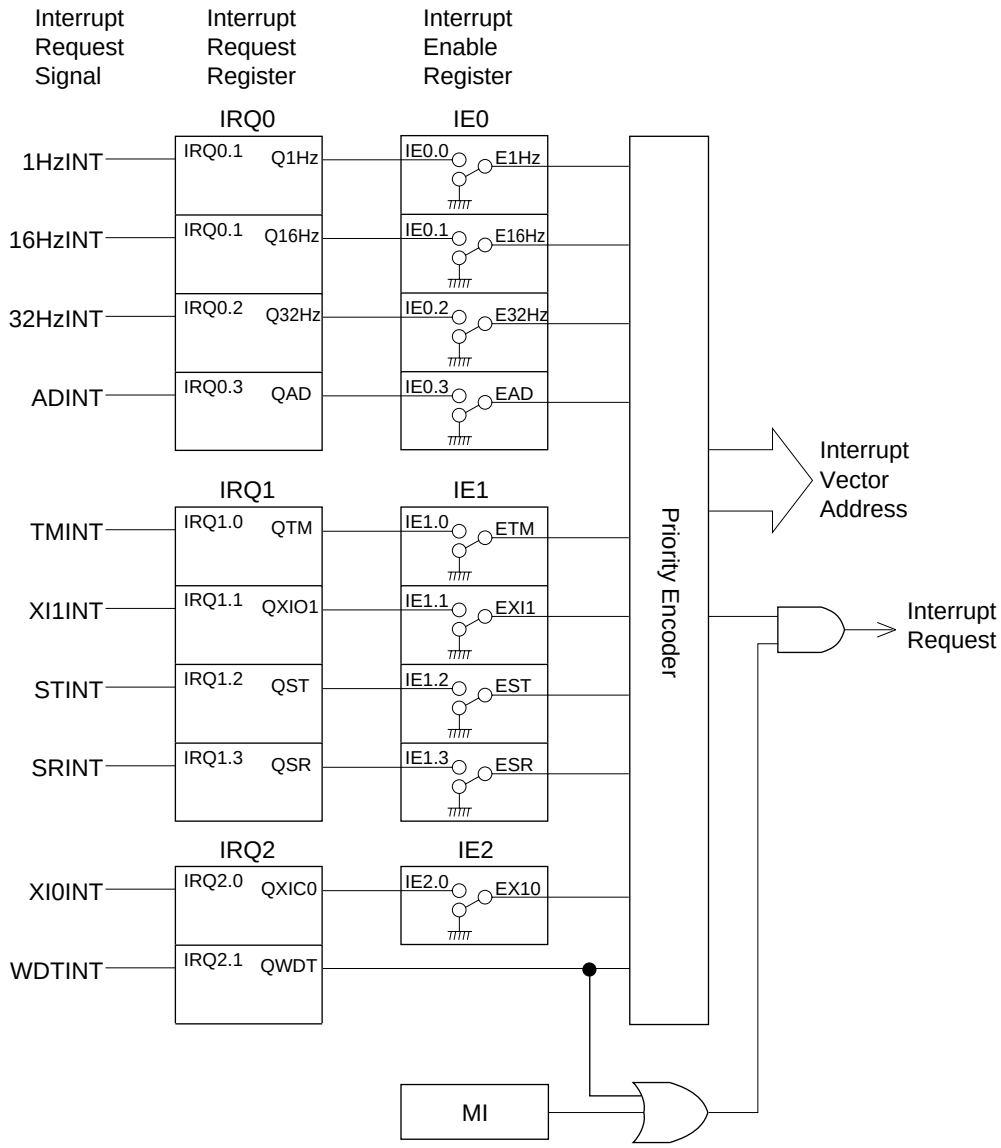


Figure 4-1 Interrupt Control Equivalent Circuit

4.2 Interrupt Sequence

If interrupt conditions are met and the interrupt is accepted, the next interrupt process starts immediately after the executing instruction at that time ends, or immediately after one machine cycle (dummy cycle) if in halt mode.

Conversion to an interrupt routine is performed in five machine cycles after executing the following processes.

(1) MI flag is reset to "0".

(2) Content of PC, A, B, H and L registers and carry flag (C) are saved to a stack.

(3) The stack pointer (SP) is decremented by 4. (SP ← SP – 4)

(4) Vector address is loaded to program counter (PC). At the same time, the interrupt request flag corresponding to the interrupt is reset.

Figure 4-2 shows the content of a stack after an interrupt is generated.

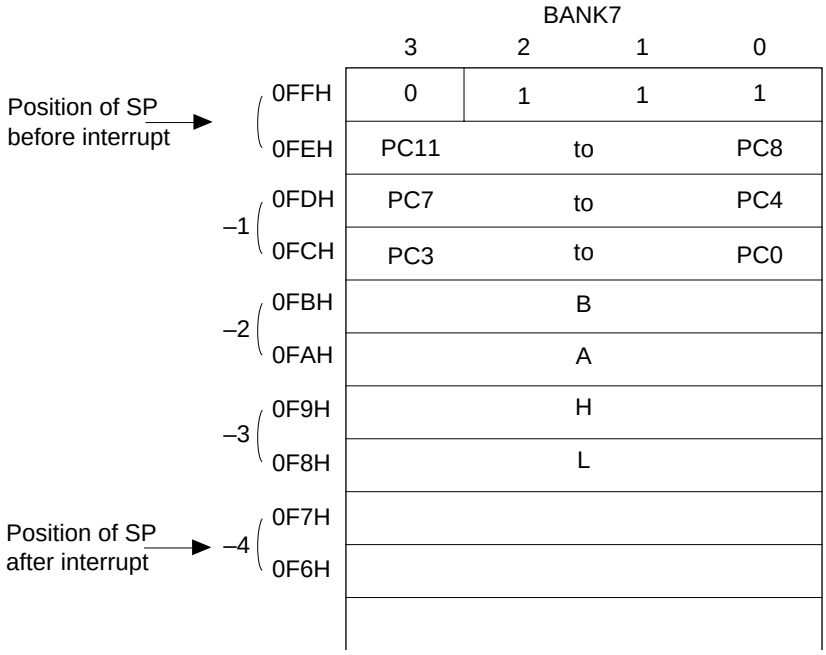


Figure 4-2 Content of Stack after Interrupt is Generated

Use an RTI instruction to return from interrupt routine.

The return cycle is performed in five machine cycles. The following processes are executed.

(1) Content of PC, A, B, H and L registers and carry flag (C) are returned from a stack.
(2) The stack pointer (SP) is incremented by 4. (SP ← SP + 4)
(3) MI flag is set to "1".

4.3 Interrupt Control Registers

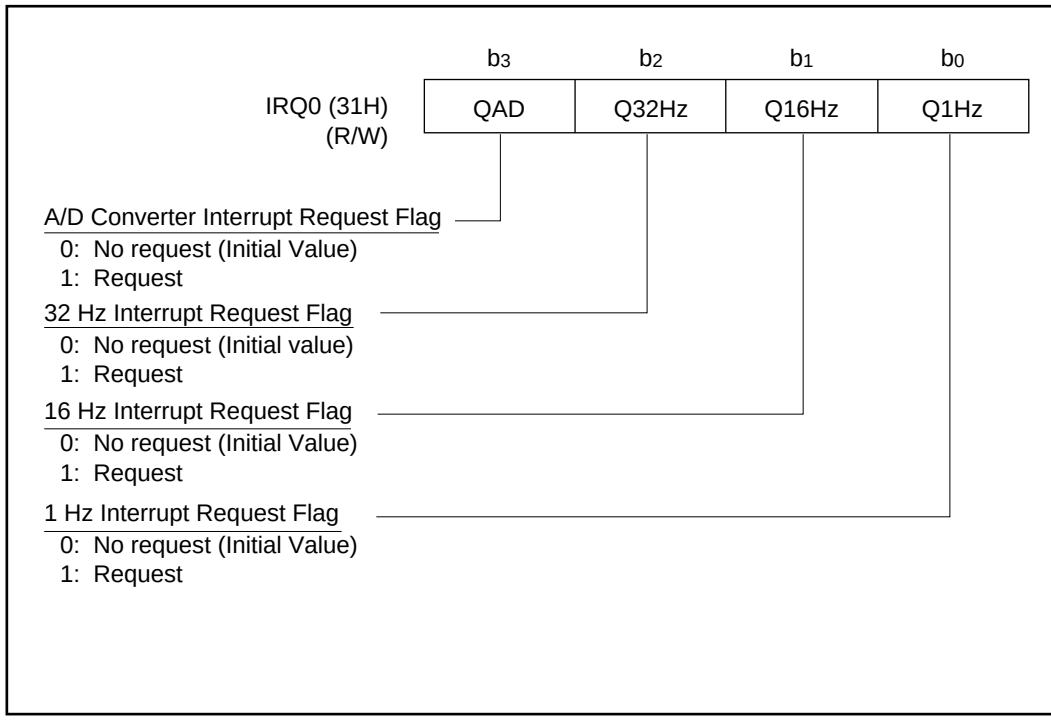
4.3.1 Interrupt Request Registers (IRQ0, IRQ1 and IRQ2)

Interrupt request registers (IRQ0, IRQ1 and IRQ2) are 4-bit registers. If an interrupt request is generated, the corresponding bit is set to "1" at the first S1 state. If an interrupt was enabled by an interrupt enable register (IE0 to 2) at this time, an interrupt is requested to the CPU. The watchdog timer, however, has no interrupt mask function by an interrupt enable register.

A software interrupt occurs by writing "1" to an interrupt request register.

If an interrupt is accepted, corresponding bits to IRQ0, IRQ1, and IRQ2 are reset to "0" by hardware during an interrupt conversion cycle.

IRQ0, IRQ1, and IRQ2 are initialized to 0H at system reset.



Bit 3: QAD

Set to "1" by counter over flow signal of A/D converter.

Bit 2: Q32Hz

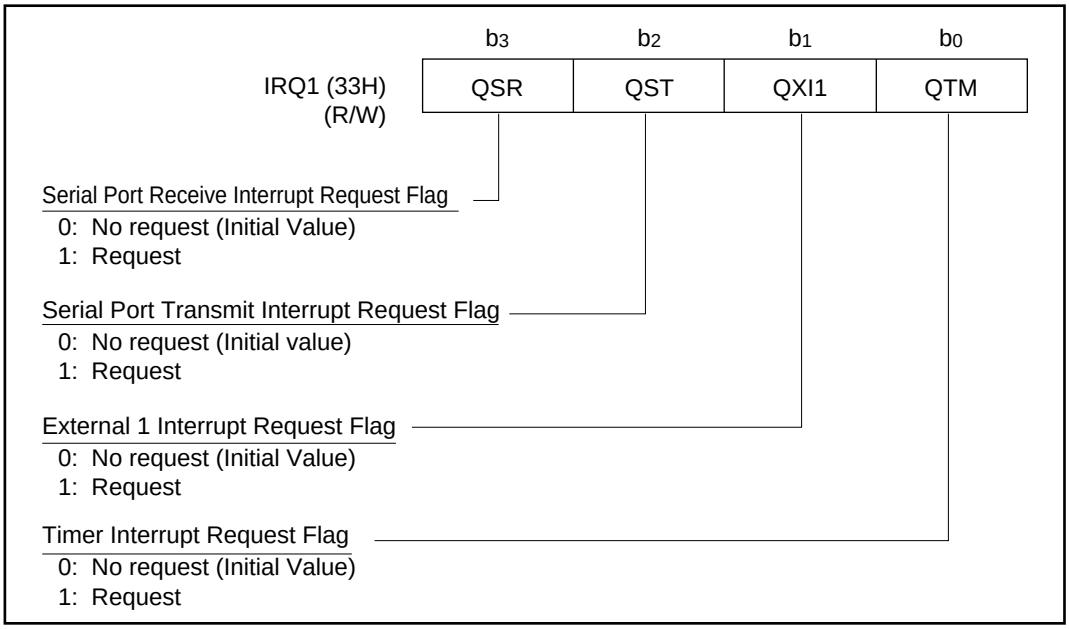
Set to "1" at fall of 32 Hz of time base counter.

Bit 1: Q16Hz

Set to "1" at fall of 16 Hz of time base counter.

Bit 0: Q1Hz

Set to "1" at fall of 1 Hz of time base counter.



Bit 3: QSR

Set to "1" if receive data of serial port is set to receive register.

Bit 2: QST

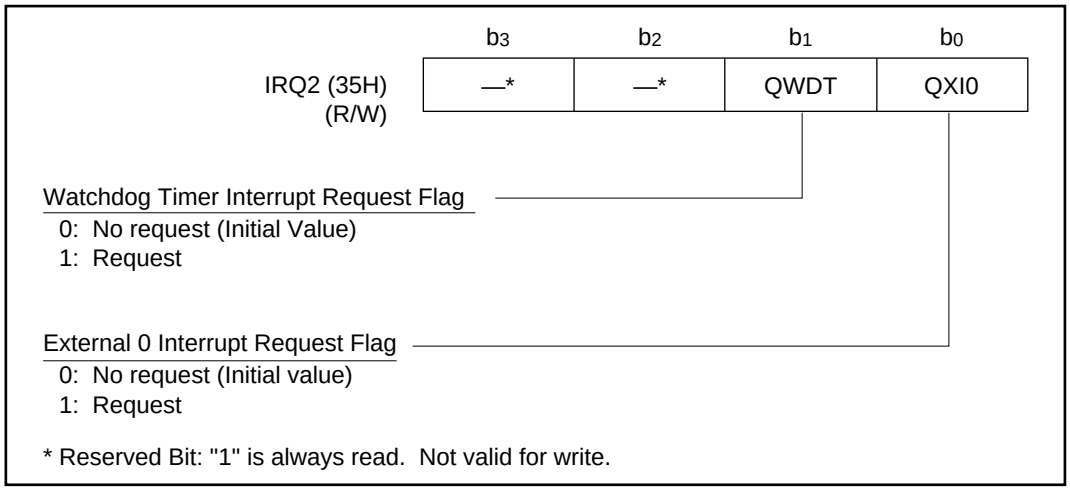
Set to "1" if transmit data of serial port is set to transmit register.

Bit 1: QXI1

Set to "1" by change of input level of P2.0–P2.3.

Bit 0: QTM

Set to "1" by overflow of timer.



Bit 1: QWDT

Set to "1" by overflow of watchdog timer. Interrupt cannot be disabled by interrupt enable register.

Bit 0: QXI0

Set to "1" by change of input level of P0.0–P0.3 and P1.0–P1.3.

4.3.2 Interrupt Enable Registers (IE0, IE1 and IE2)

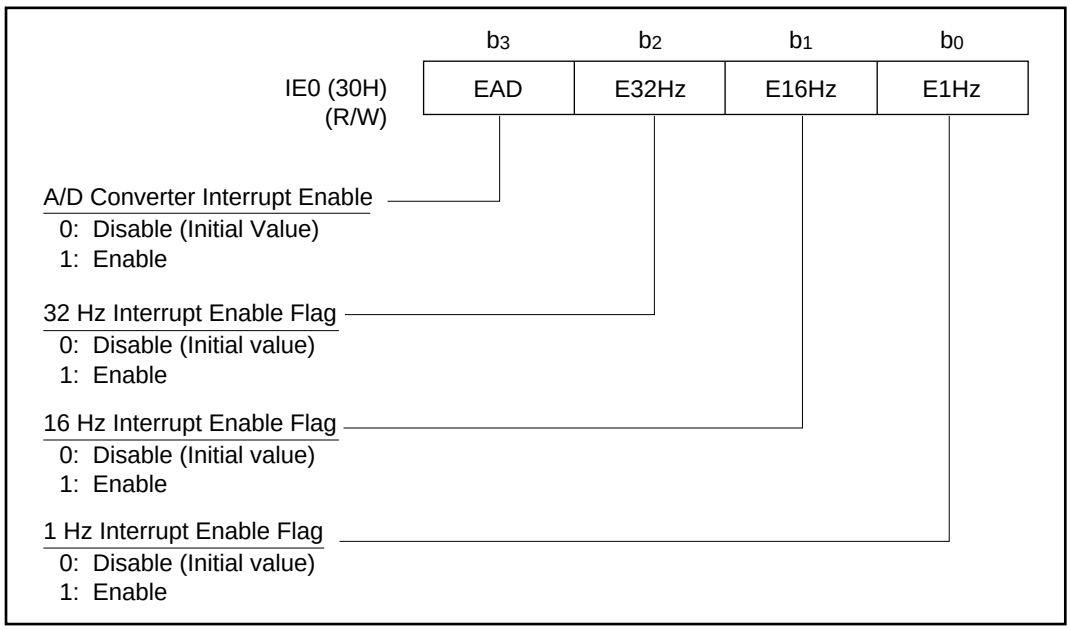
Interrupt enable registers (IE0, IE1 and IE2) are 4-bit registers that determine whether each interrupt is requested to the CPU, depending on the logical product with the corresponding bits of interrupt request registers (IRQ0, IRQ1 and IRQ2).

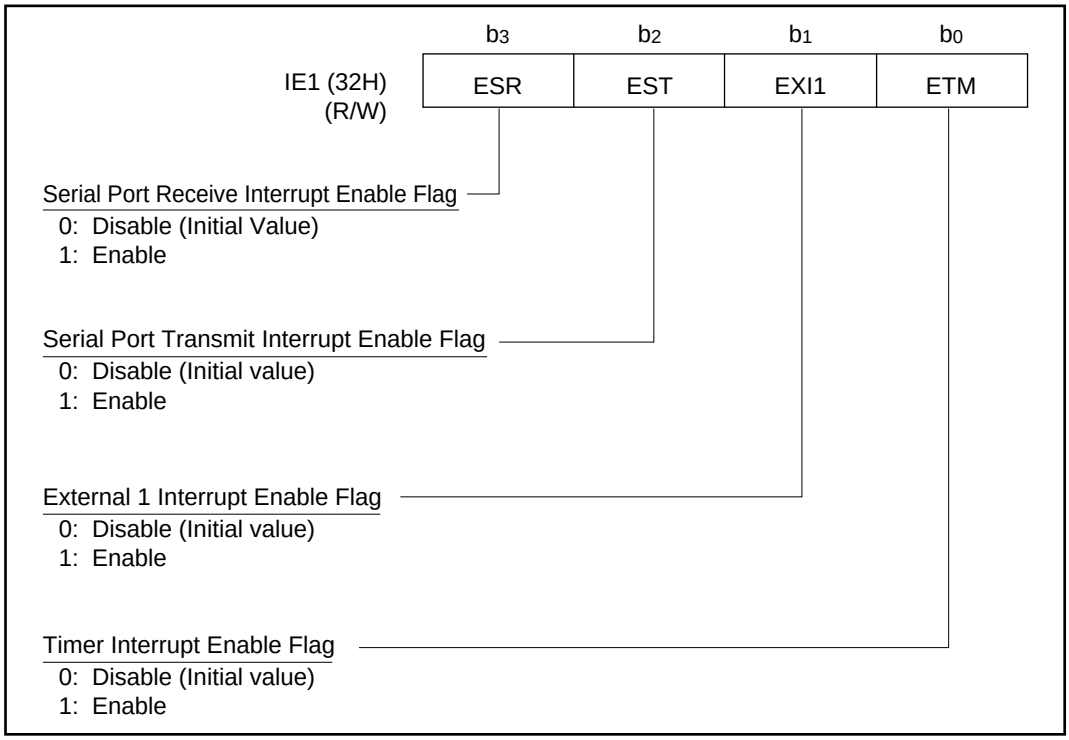
If multiple interrupts are requested to the CPU at the same time, the interrupt with the highest priority (bigger vector address) shown in Table 4-1, and other interrupt requests are held.

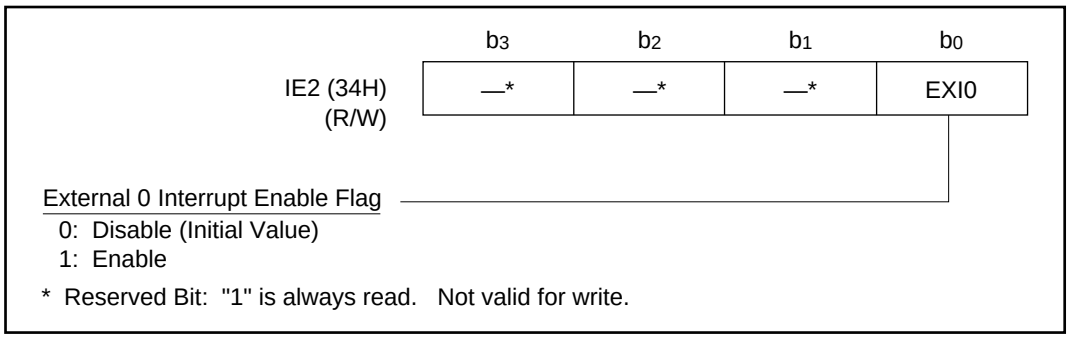
During an interrupt conversion cycle, the mask interrupt enable flag (MI) is cleared to "0", but each IE0 to 2 bit is not.

Held interrupt requests are held until the MI flag is set to "1" when processing an accepted interrupt request. If interrupt processing is ended by an RTI instruction, the MI flag is automatically set, and held interrupt requests are accepted.

Interrupt enable registers (IE0 to 2) can be rewritten only when the master enable flag (MI) is reset to "0".







* Reserved Bit: "1" is always read. Not valid for write.

4.3.3 Master Interrupt Enable Register (MIEF)

The MI flag in the master interrupt enable register (MIEF) controls disable/enable of all interrupts except the watchdog timer interrupt. If the MI flag is set to "1", an interrupt is enabled, and if reset to "0", interrupt is disabled. The MI flag is reset to "0" during an interrupt conversion cycle when an interrupt is accepted, and is set to "1" by executing an RTI instruction, a return instruction from an interrupt processing routine.

By setting the MI flag to "1" during an interrupt processing routine, multiple interrupt processing is possible.

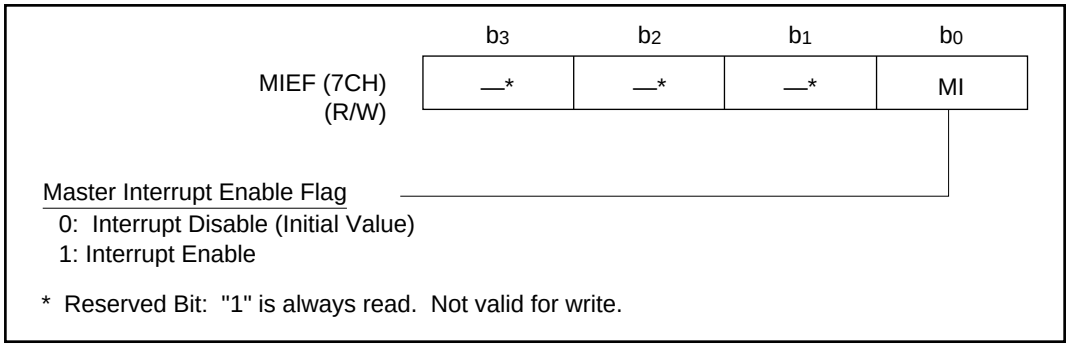


Table 4-2 shows interrupt related registers.

Table 4-2 Interrupt Related Registers

Register Name	Symbol	Address	Read/Write	Value at System Reset
Interrupt Enable Register 0	IE0	30H	R/W	0H
Interrupt Request Register 0	IRQ0	31H	R/W	0H
Interrupt Enable Register 1	IE1	32H	R/W	0H
Interrupt Request Register 1	IRQ1	33H	R/W	0H
Interrupt Enable Register 2	IE2	34H	R/W	0EH
Interrupt Request Register 2	IRQ2	35H	R/W	0CH
Master Interrupt Enable Register	MIEF	7CH	R/W	0EH

Chapter 5

Clock Generation Circuit (2CLK)

Chapter 5 Clock Generation Circuit (2CLK)

5.1 Overview

The clock generation circuit (2CLK) is comprised of a 32.768 kHz crystal oscillation circuit, a 700 kHz RC oscillation circuit and a clock control component, generating a system clock (CLK), crystal oscillation clock (32.768 kHz) and a RC oscillation clock (700 kHz).

The system clock is the basic operation clock for the CPU. The crystal oscillation clock is the basic operation clock for the time base counter and for the buzzer driver. The crystal oscillation clock and the RC oscillation clock can be the timer clock source supplying the timer.

The frequency of the system clock can be switched to either 32.768 kHz, the crystal oscillation circuit output, or to 700 kHz, the output of the RC oscillation circuit.

Note: The oscillation frequency of the RC oscillation circuit fluctuates depending on the value of external resistance (ROS), operating power voltage (VSS2), ambient temperature (Ta), etc. For explanatory purposes, this manual regards the output of the RC oscillation circuit as 700 kHz.

5.2 Configuration of Clock Generation Circuit

Figure 5-1 shows the configuration of the clock generation circuit.

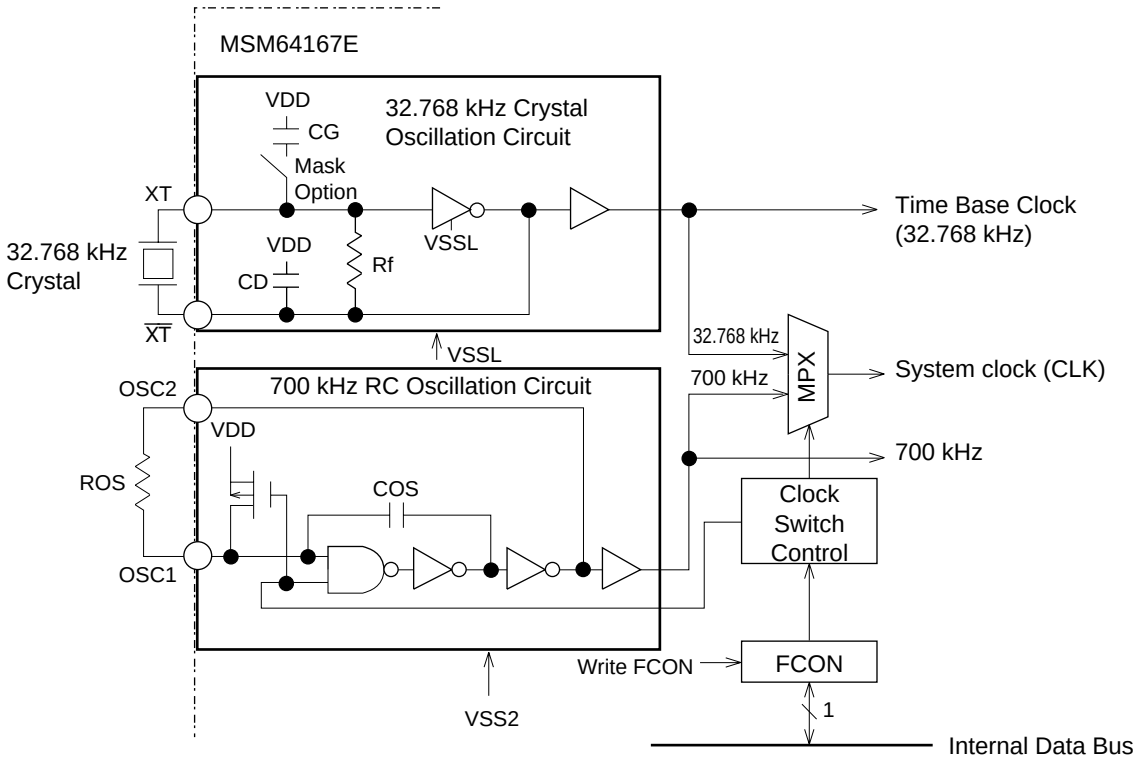


Figure 5-1 Configuration of Clock Generation Circuit

5.3 Operation of Clock Generation Circuit

The 32.768 kHz crystal oscillation circuit oscillates by an external 32.768 kHz crystal. When this frequency is finely adjusted by an external capacitor, the internal capacity (CG) can be cut off by a mask option.

The 700 kHz RC oscillation circuit oscillates by external resistance (ROS). The RC oscillation circuit operates only when the system clock is selected to the 700 kHz RC oscillation clock, or when it is set to the RC oscillation test mode. Otherwise oscillation stops.

For details on test functions, see Chapter 15, Test Circuit.

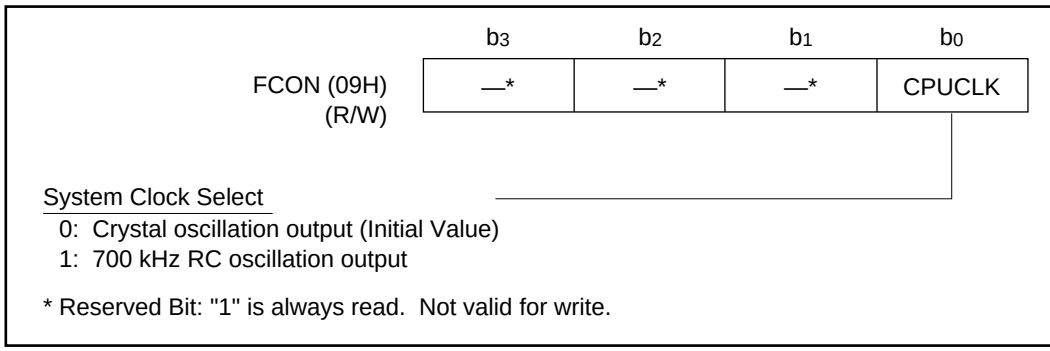
The system clock is selected by the frequency control register (FCON). If bit 0 (CPUCLK) of FCON is reset to "0", the output of crystal oscillation circuit (32.768 kHz) becomes the system clock. If CPUCLK is set to "1", the output of the RC oscillation circuit (700 kHz) becomes the system clock. Even if the RC oscillation circuit is selected, the crystal oscillation circuit does not stop oscillation.

If the crystal oscillation circuit is selected as the system clock, the oscillation of the RC oscillation circuit stops, and the power consumption of the RC oscillation circuit becomes "0". Therefore by creating software in which the output of the crystal oscillation circuit is normally selected (CPUCLK = 0), and the output of the RC oscillation circuit is selected (CPUCLK = 1) only when high speed operation is necessary, power consumption can be minimized.

The OSC1 pin is pulled up to VDD when the 700 kHz RC oscillation circuit is not selected, therefore set the OSC1/OSC2 pins to open if the output of the RC oscillation circuit (700 kHz) is not to be used at all.

5.4 Frequency Control Register (FCON)

The frequency control register (FCON) is a 4-bit special function register (SFR) that selects the system clock.



Bit 0: CPUCLK

Bit to select the system clock. CPUCLK is reset to "0" and crystal oscillation output is selected at system reset.

5.5 System Clock Switching Timing

When the CPUCLK bit of the frequency control register (FCON) is set to "1", the system clock is switched from the crystal oscillation output (32.768 kHz) to the RC oscillation output (700 kHz), which means that the system clock is switched from the low-speed clock to the high-speed clock. At the same time, the internal logic power supply is also switched from the VSSL level to the applied supply voltage level VSS2, because for the high-speed operation of the CPU, to heighten the internal-voltage to the proper level is needed.

In fact, the CPU starts high-speed operation before the internal logic power supply reaches to the applied supply voltage level because the internal logic power supply takes a time to reach the same level as the applied power supply voltage.

By these reasons indicated above, we would like you to program as shown below to guarantee right operation of the system clock in high-speed clock.

(1) Set bit 0 (VSSLH) of the VSSL control register (VSSLCON) to "1" and switch the internal logic voltage to the level of power supply, VSS2, before switching the system clock to the high-speed clock. (①)

(2) After (1) done, set the CPUCLK bit of the frequency control register (FCON) to "1" and switch the system clock from the crystal oscillation output (32.768 kHz) to the RC oscillation output (700 kHz). (②)

★AN EXAMPLE OF PROGRAM

```
SMBD  08H, 0      ; Set VSSLH to "1".
SMBD  09H, 0      ; Set CPUCLK to "1".
```

(For SMBD 09H, 0, it takes 180 µs to execute this instruction because it is a 2-machine-cycle instruction.)

(3) After switching the system clock to high-speed clock, VSSLH can be reset to "0" anytime, but pay attention to VSSLH. The system clock is switched back to the low-speed clock. Unless VSSLH is reset, the CPU is not operated on low-consumption current. (③)

Figure 5-2 shows the system clock switch timing and the internal logic power supply.

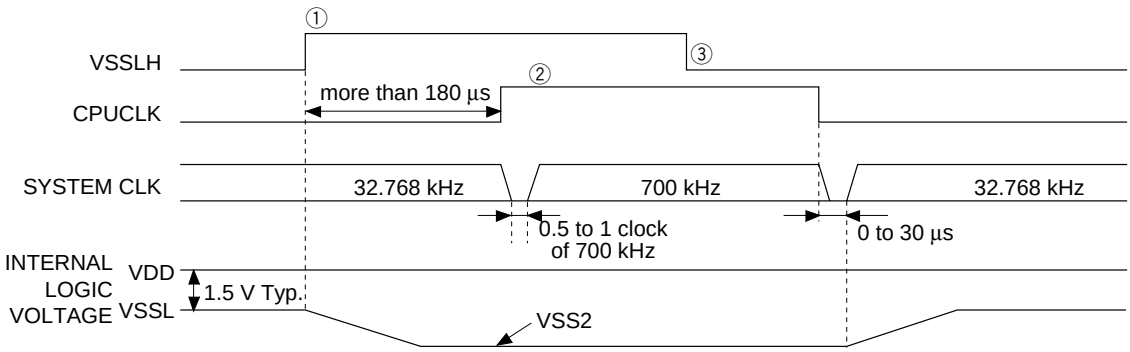


Table 5-1 Clock Generation Circuit-Related Pins

Pin name	Pin No.		Pad No.	I/O	Note
	GA	TB			
XT	34	32	34	I	Low speed clock oscillation pin:
$\overline{XT}$	33	31	33	O	Connects crystal (32.768 kHz)
OSC1	31	29	31	I	High speed clock oscillation pin:
OSC2	30	28	30	O	Connects external resistance (ROS) for oscillation

Table 5-2 Typical Values of Oscillation Frequency of RC Oscillation Circuit (Ta = 25°C)

VDD (V)	ROS (kΩ)	fOSC (kHz)
3.0	100	700

Chapter 6

Time Base Counter (TBC)

Chapter 6 Time Base Counter (TBC)

6.1 Overview

The MSM64167E has a built-in time base counter (TBC) to generate clocks to supply internal peripheral circuits.

The time base counter is a 15-step binary counter. The oscillation clock of the crystal oscillation circuit (32.768 kHz) is supplied to the time base count clock.

Output of the time base counter is used for the buzzer driver, system reset circuit, timer, watchdog timer, time base interrupt, the sampling clock of each port and LCD drivers.

6.2 Configuration of Time Base Counter

Figure 6-1 shows the configuration of the time base counter (TBC).

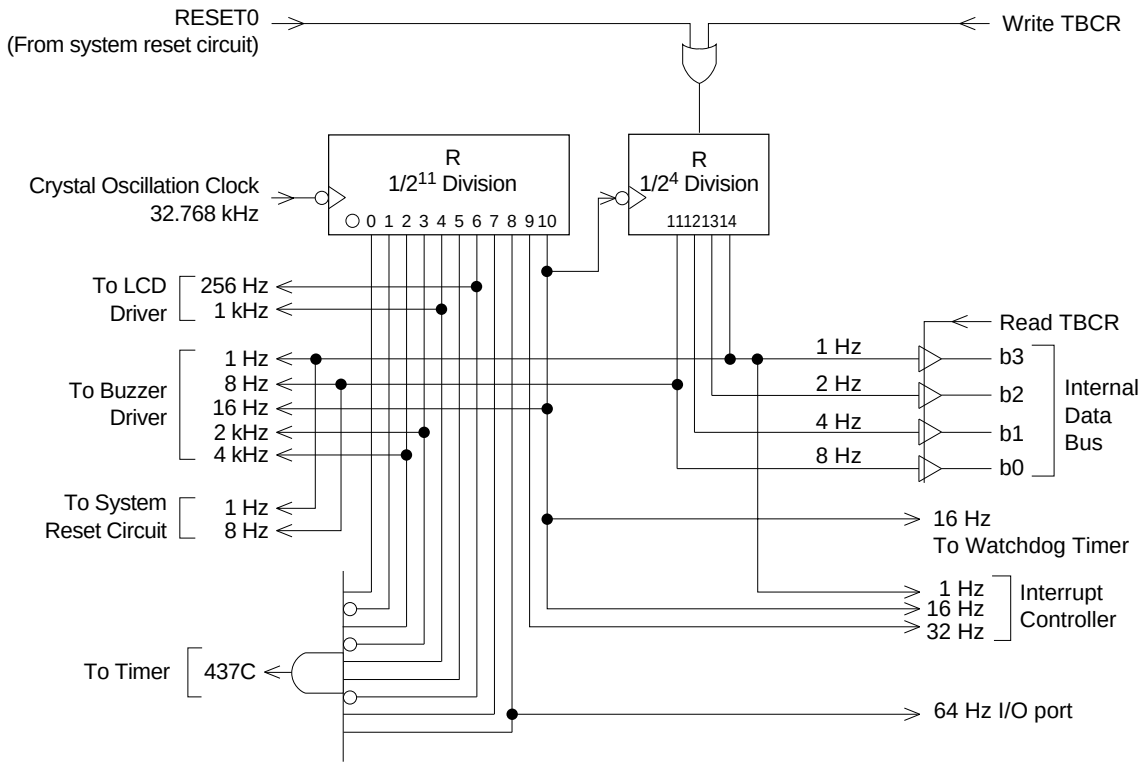


Figure 6-1 Configuration of Time Base Counter

6.3 Operation of Time Base Counter

Time base counter (TBC) starts counting from 0000H after system reset. The count is incremented at the fall of the time base clock (32.768 kHz).

32 Hz/16 Hz/1 Hz output of the time base counter are used as time base interrupts, and to generate time base interrupt requests at the fall of a respective output.

16 Hz output of the time base counter is output to the watchdog timer. 4 kHz/2 kHz/16 Hz/8 Hz/1 Hz output are input to the buzzer driver to output various buzzer sounds. 64 Hz output is used as the sampling clock of input ports. 8 Hz/1 Hz output are input to the system reset circuit, and are used to generate reset timing at system reset. 8 Hz/4 Hz/2 Hz/1 Hz output of the time base counter can be read at the time base counter register (TBCR). If TBCR is written, the 8 Hz/4 Hz/2 Hz/1 Hz counter is reset to "0".

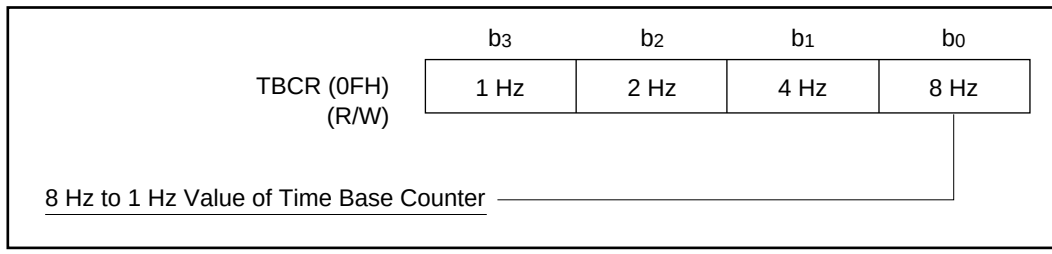
437C output is a pulse signal that rises at 437/32768 seconds after the fall of 64 Hz. 437C output is input to the timer and is used to set the baud rates of serial ports.

Figure 6-2 shows the interrupt timing of the time base counter, and reset timing by writing to TBCR.

Note: 8 Hz to 1 Hz output of the time base counter can be read at the time base counter register (TBCR). If TBCR is written, 8 Hz to 1 Hz output is reset to "0". In this writing, written data has no meaning. For example, if data is written by an LMAD TBCR instruction, data does not depend on the content of register A. When TBCR is written and an 8 Hz to 1 Hz time base counter is reset, a time base interrupt is generated if output is "1". For example, if a 1 Hz output is "1", a 1 Hz interrupt request is generated. To make an interrupt invalid, reset the master interrupt enable flag (MI), or the interrupt enable flag (E1Hz) to "0" first, then write to TBCR (reset each output), and reset the interrupt request flag (Q1Hz) to "0".

6.4 Time Base Counter Register (TBCR)

TBCR is a 4-bit special function register (SFR) to read 8 Hz to 1 Hz output. If TBCR is written, the 8 Hz to 1 Hz output of the time base counter is reset.



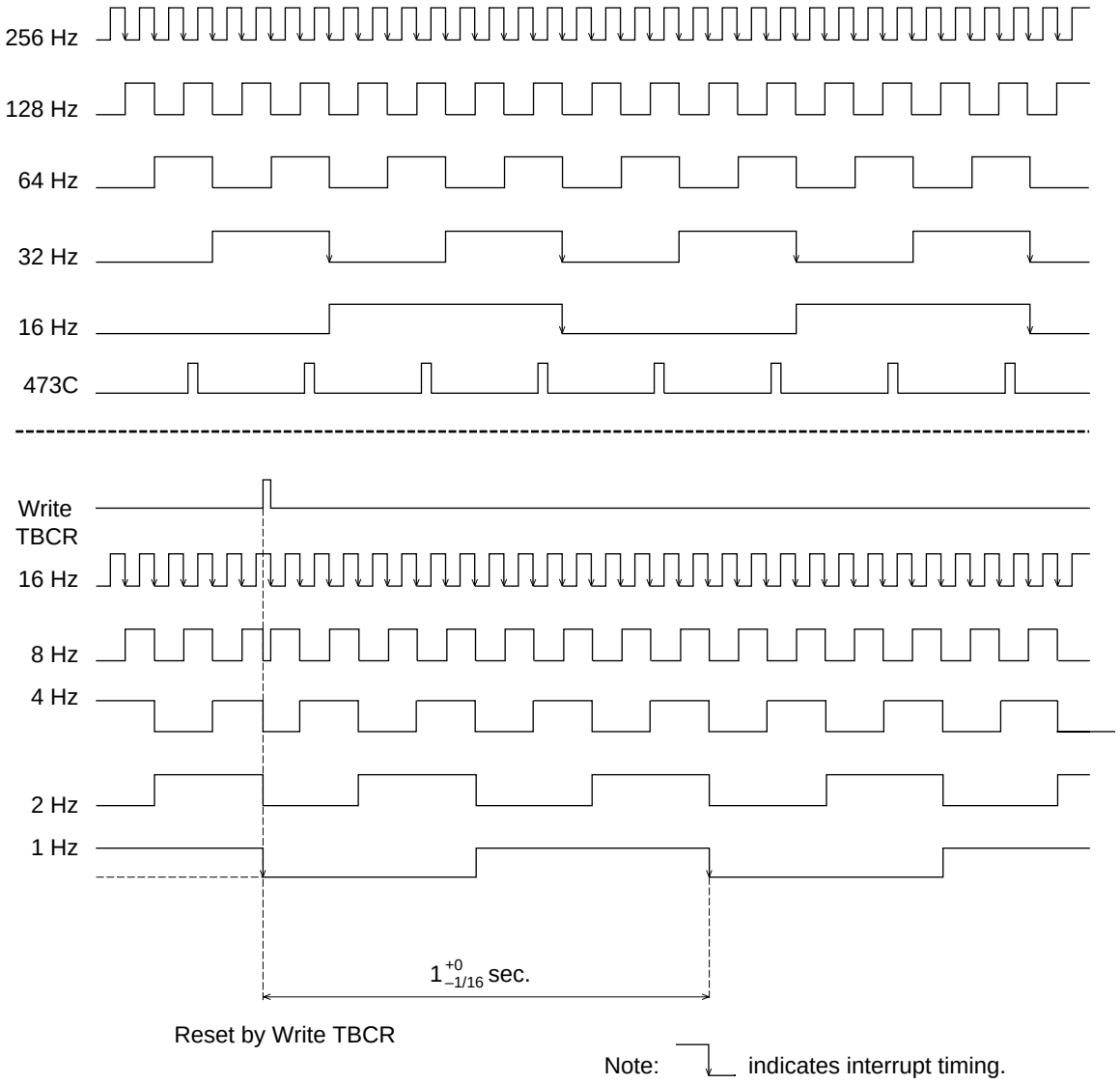


Figure 6-2 Time Base Counter Interrupt Timing and Reset Timing by Writing to TBCR

Chapter 7

Ports (P0, P1 and P2)

Chapter 7 Ports (P0, P1 and P2)

7.1 Overview

The MSM64167E has 4-bit × 3 internal I/O ports (P0, P1 and P2). Table 7-1 lists the functions of each port. For the secondary functions of the timer and of the serial ports, see Chapter 8 "Timer", and Chapter 9 "Serial Port" respectively.

Table 7-1 Function of Each Port

Pin name	Pin No.		Pad No.	I/O	Function
	GA	TB			
P0.0/CAP	67	65	67	I/O	4-bit I/O port (P0): 4-bit I/O port that can select I/O, pull-up/pull-down resistance, input/high impedance input, and NMOS open drain output/CMOS output for each bit by PORT 0 control registers 0 to 3 (P00CON to P03CON). As a secondary function, an external interrupt function is assigned to P0.0 to P0.3, capture trigger input (CAP) function of timer is assigned to P0.0. Receive data input (RXD) function of serial port is assigned to P0.1, and external clock input (TMC) function of timer is assigned to P0.2.
P0.1/RXD	68	66	68	I/O	
P0.2/TMC	69	67	69	I/O	
P0.3	70	68	70	I/O	
P1.0	71	69	71	I/O	4-bit I/O port (P1): 4-bit I/O port that can select I/O, pull-up/pull-down resistance, input/high impedance input, and NMOS open drain output/CMOS output for each bit by PORT 1 control registers 0 to 3 (P10CON to P13CON). As a secondary function, external interrupt function is assigned to P1.0 to P1.3.
P1.1	72	70	72	I/O	
P1.2	73	71	73	I/O	
P1.3	74	72	74	I/O	
P2.0/TXC	75	73	75	I/O	4-bit I/O port (P2): 4-bit I/O port that can select I/O, pull-up/pull-down resistance input/high impedance input, NMOS open drain output/CMOS output for each bit by PORT 2 control registers 0 to 3 (P20CON to P23CON). As a secondary function, external interrupt function is assigned to P2.0 to P2.3, transmit clock I/O (TXC) function of serial port is assigned to P2.1, transmit data output (TXD) function of serial port is assigned to P2.2, and over flow flag output (TMO) function of timer is assigned to P2.3.
P2.1/RXC	76	74	76	I/O	
P2.2/TXD	77	75	77	I/O	
P2.3/TMO	78	76	78	I/O	

7.2 Port 0, Port 1 and Port 2 (P0.0–P0.3, P1.0–P1.3 and P2.0–P2.3)

7.2.1 Configuration of Port 0, Port 1 and Port 2

Ports 0–2 are 4-bit I/O ports. Each bit can be switched to pullup resistance or pulldown resistance input/high impedance input, CMOS output/NMOS open drain output by control registers (P00CON–P03CON, P10CON–P13CON, P20CON–P23CON) of Ports 0–2. In the case of pull-up or pull-down resistance inputs, either can be selected by the PUD bit of the port control register (PCON).

As a secondary function, an external interrupt function by level change is assigned. Also serial port I/O functions are assigned to P0.1 and P2.0–P2.2, and a timer I/O function is assigned to P0.0, P0.2 and P2.3. For functions of the timer and serial ports, see Chapter 8 "Timer", and Chapter 9 "Serial Port" respectively.

Figure 7-1 shows the configuration of Ports 0 and 1. Figure 7-2 shows the configuration of Port 2.

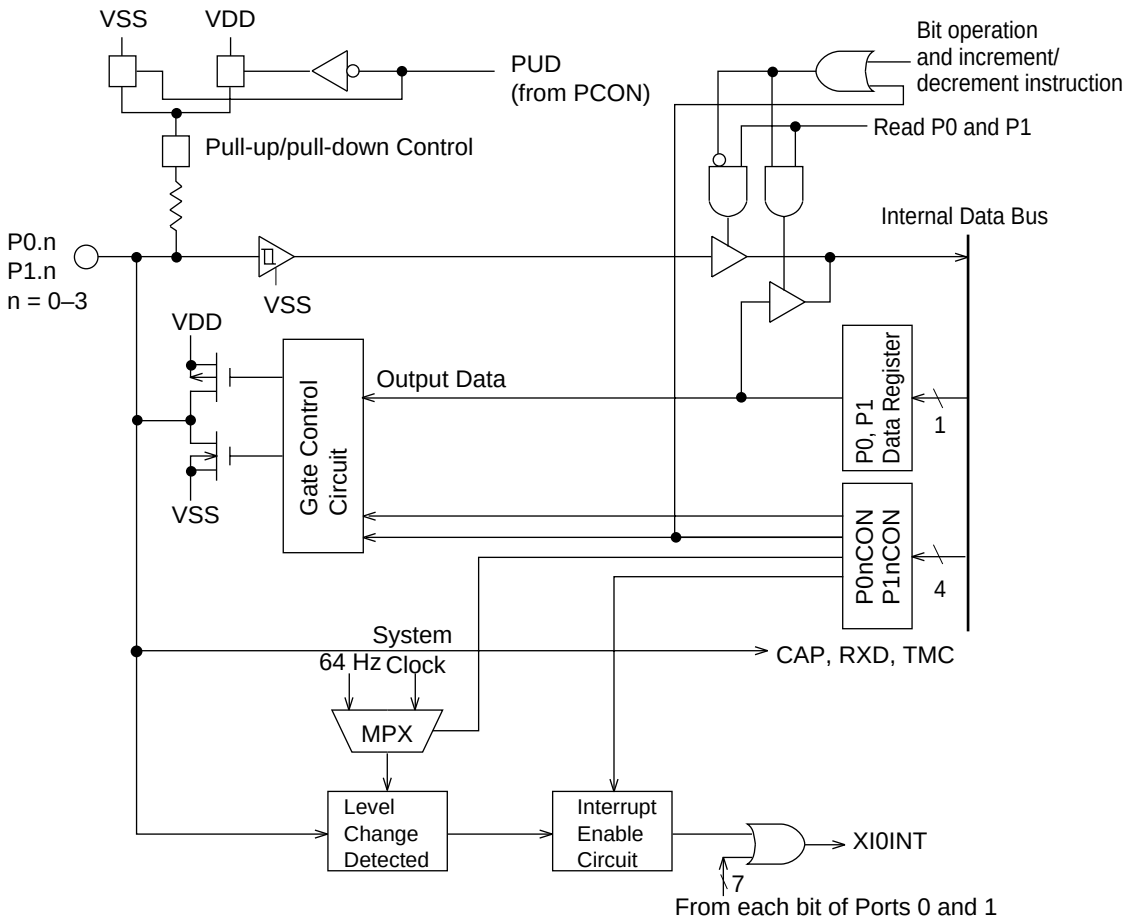


Figure 7-1 Configuration of Port 0 and Port 1

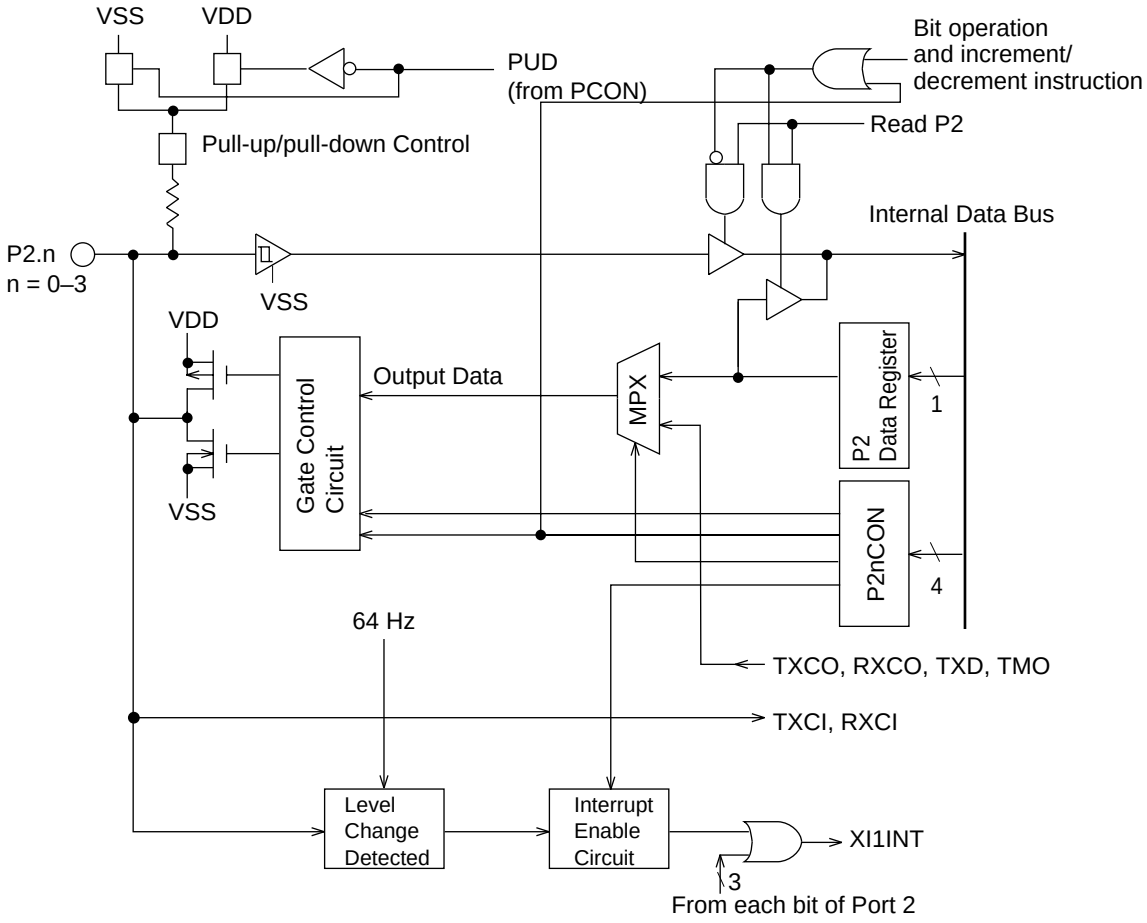


Figure 7-2 Configuration of Port 2

The power supply of I/O circuits of Ports 0, 1 and 2 are at the VDD–VSS level. If Ports 0–2 are connected to external equipment that is operating under a different power supply, the power supply of the external equipment to VDD–VSS pins is as shown in Figure 7-3.

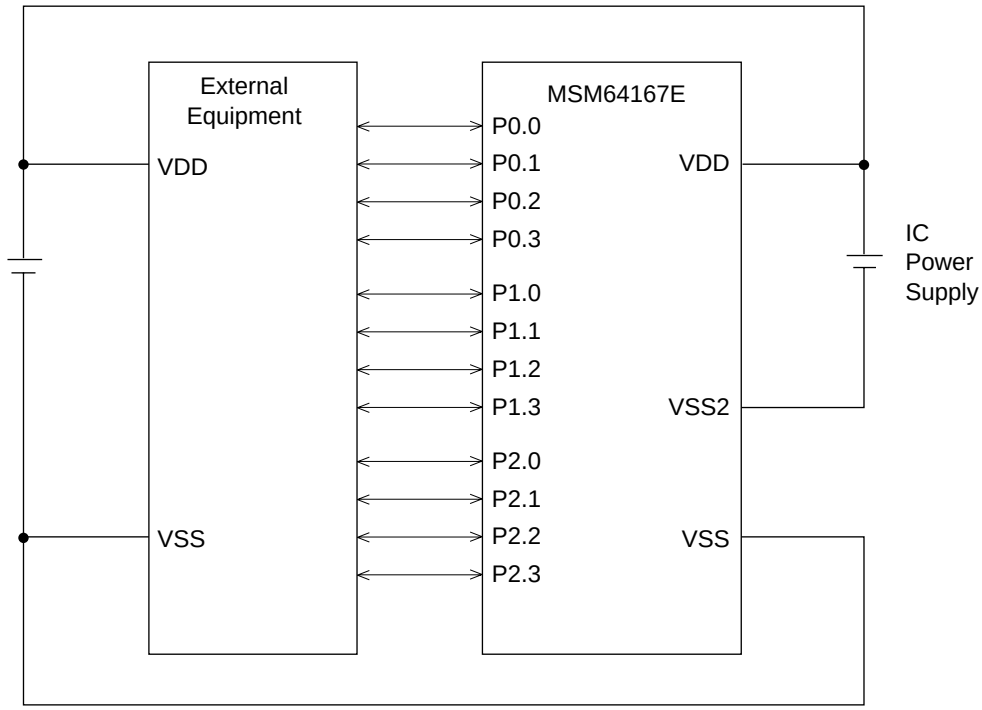


Figure 7-3 Connection of Port 0, Port 1 and Port 2 to External Equipment with Different Power Supply

If the signal level of all Ports 0–2 can be the same power voltage level of the IC, connect VSS pin to VSS2 pin.

7.2.2 Port 0, Port 1 and Port 2 Related Registers

(1) Port 0 Register (P0)

Port 0 register (P0) is a 4-bit special function register (SFR) that sets the output value of a port. If "1" is set at bit 1 (P00DIR to P03DIR) of Port 0 control register (P00CON to P03CON), and output mode is selected, the content of Port 0 register is output to that port.

If P0 is read when output mode is selected (P00DIR to P03DIR = 1), the content of Port 0 register is read, but if P0 is read when input mode is selected (P00DIR to P03DIR = 0), the pin level of that port is read.

P0 (00H) (R/W)

b_3	b_2	b_1	b_0
P03	P02	P01	P00

(2) Port 1 Register (P1)

Port 1 register (P1) is a 4-bit special function register (SFR) that sets the output value of a port. If "1" is set at bit 1 (P10DIR to P13DIR) of Port 1 control register (P10CON to P13CON), and output mode is selected, the content of Port 1 register is output to that port.

If P1 is read when output mode is selected (P10DIR to P13DIR = 1), the content of Port 1 register is read, but if P1 is read when input mode is selected (P10DIR to P13DIR = 0), the pin level of that port is read.

P1 (01H) (R/W)

b_3	b_2	b_1	b_0
P13	P12	P11	P10

(3) Port 2 Register (P2)

Port 2 register (P2) is a 4-bit special function register (SFR) that sets the output value of a port. If "1" is set at bit 1 (P20DIR to P23DIR) of Port 2 control register (P20CON to P23CON), and output mode is selected, the content of Port 2 register is output to that port.

If P2 is read when output mode is selected (P20DIR to P23DIR = 1), the content of Port 2 register is read, but if P2 is read when input mode is selected (P20DIR to P23DIR = 0), the pin level of that port is read.

P2 (02H) (R/W)

b_3	b_2	b_1	b_0
P23	P22	P21	P20

For Ports 0–2, I/O can be selected for each bit by each port control register, therefore when reading, a bit to read the content of each register and a bit to read each pin level may mix, depending on the specification of each DIR bit.

At system reset, each of the port data registers (P0, P1 and P2) is reset to "0H".

When data is written to each register, the timing when a pin actually changes is at the latter half of state 3 (S3) of the last machine cycle of a write instruction.

Figure 7-4 shows an example of timing.

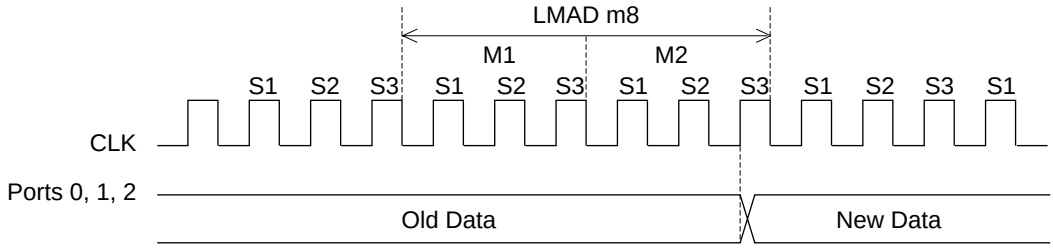


Figure 7-4 Example of Writing to Port Data Register by "LMAD m8" Instruction

When data is read from a port, the data is captured to an accumulator (Register A) or a BA register pair at the latter half of state 2 (S2) of the last machine cycle of a read instruction.

Figure 7-5 shows an example of timing.

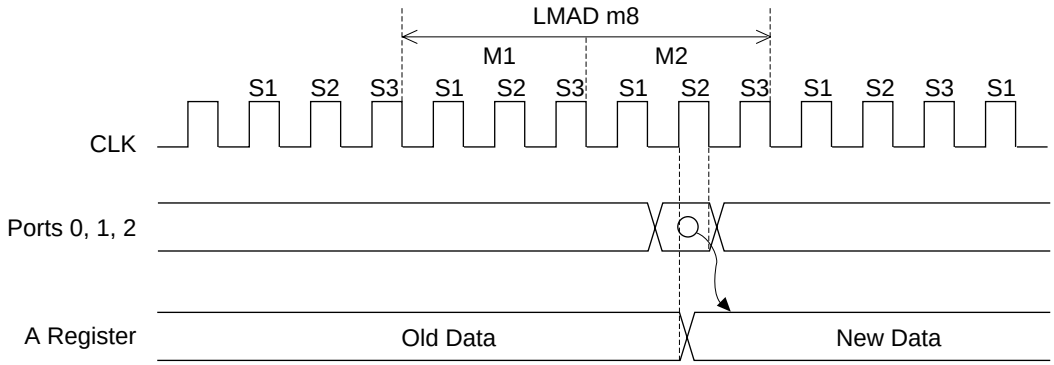
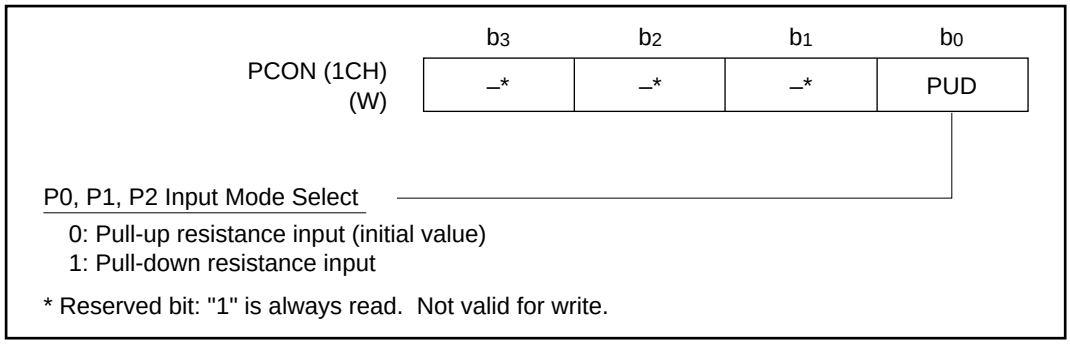


Figure 7-5 Example of Reading the Data from the Port by the "LAMD m8" Instruction

(4) Port Control Register (PCON)

Port control register (PCON) is a 4-bit special function register (SFR) that controls pull-up/pull-down resistance input when Ports 0–2 are set to input. Since PCON is a write only register, bit operation instructions, and increment and decrement instructions cannot be used.



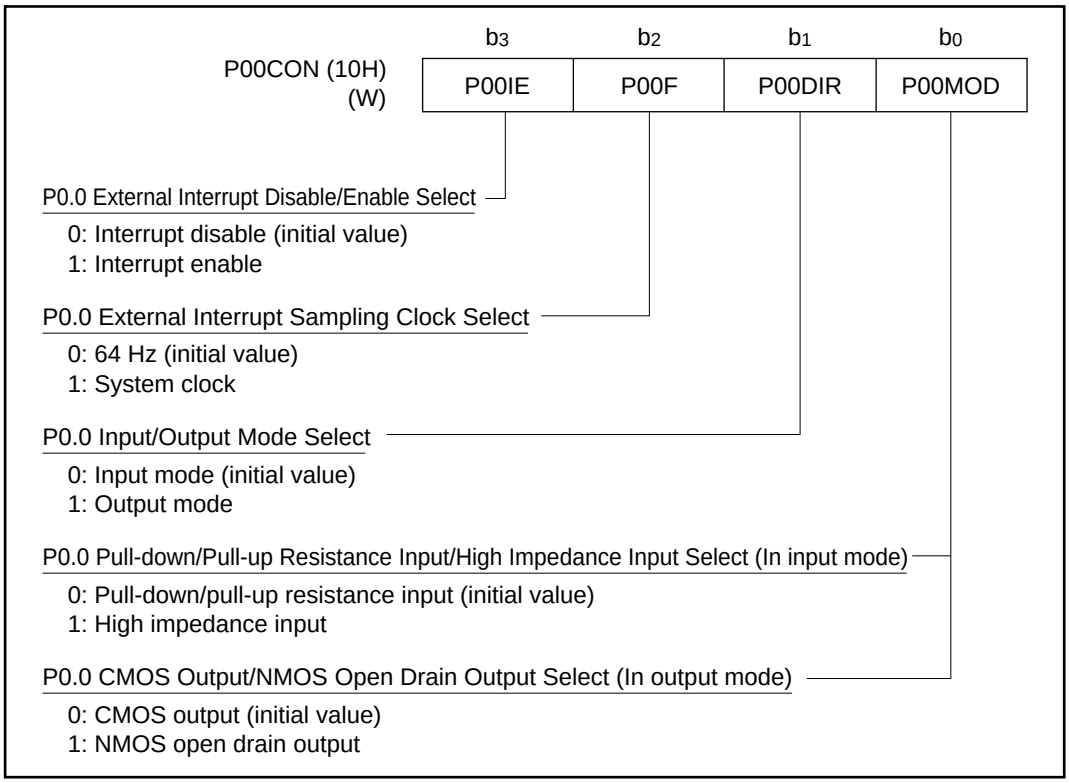
Bit 0: PUD

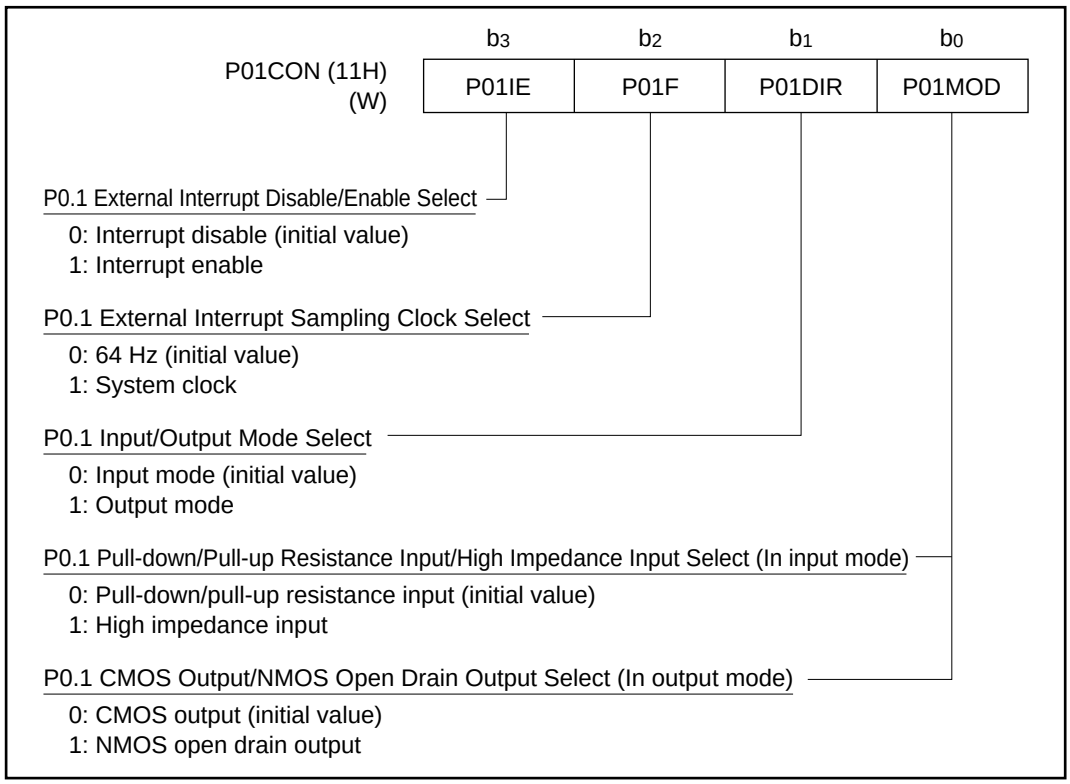
Pull-up or pull-down resistance input is selected by PUD when Ports 0–2 are set to input, and pull-up/pull-down resistance input is selected. PUD is reset to "0" at system reset.

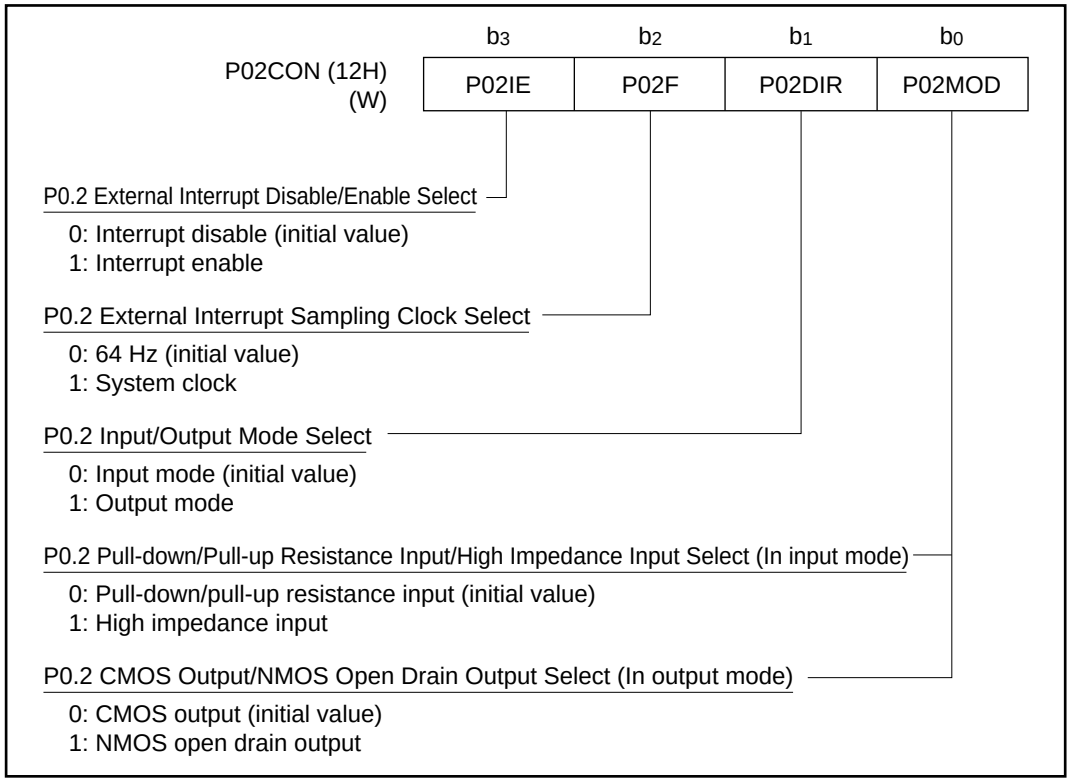
Note: Individual specification of pull-up or pull-down resistance input for Ports 0–2 is not possible.

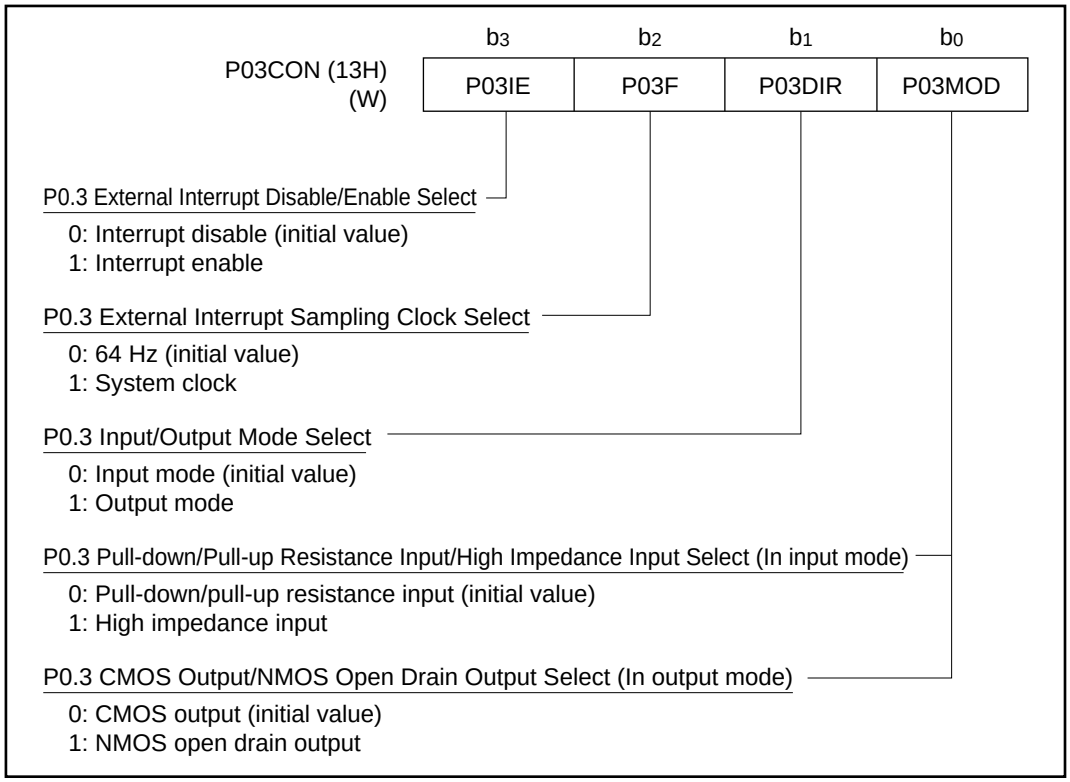
(5) Port 0 Control Registers (P00CON to P03CON)

Port 0 control registers (P00CON to P03CON) are 4-bit special function registers (SFRs) that select input/output mode, pull-down/pull-up resistance input/high impedance input in input mode, CMOS output/NMOS open drain output in output mode, external interrupt disable/enable, and the sampling clocks of external interrupts for Port 0. Since P00CON to P03CON are write only registers, bit operation instructions, and increment and decrement instructions cannot be used.



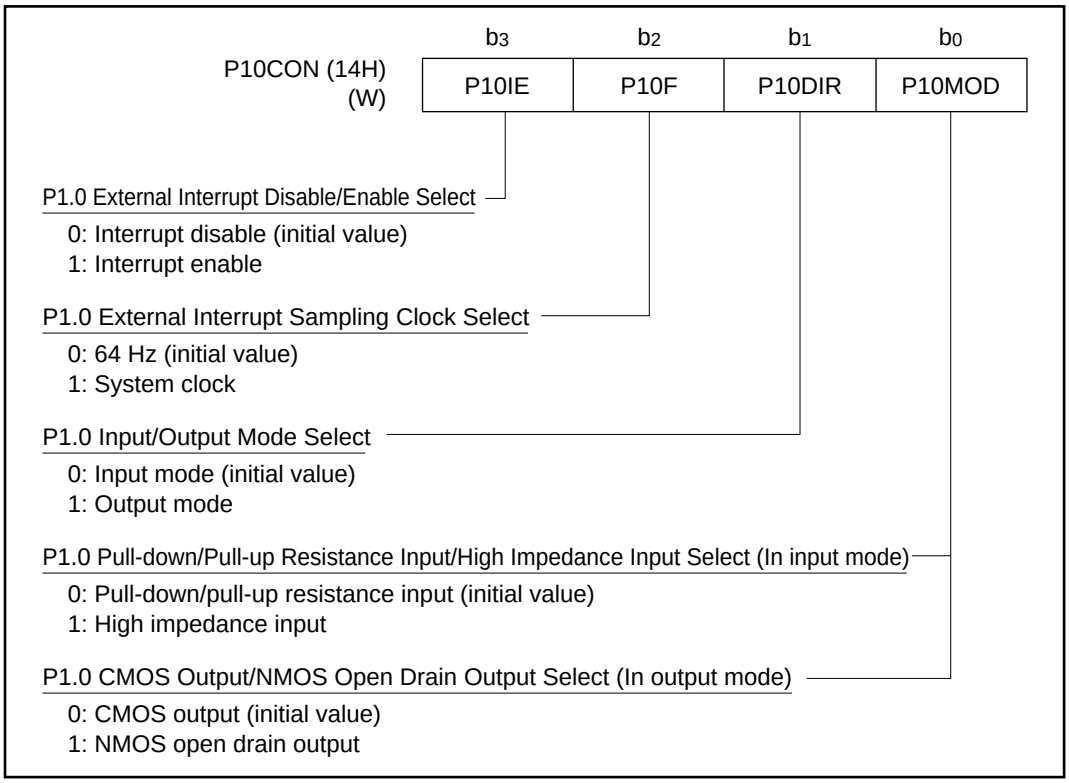

b3 b2 b1 b0
P01CON (11H)
(W)
P01IE P01F P01DIR P01MOD
P0.1 External Interrupt Disable/Enable Select
0: Interrupt disable (initial value)
1: Interrupt enable
P0.1 External Interrupt Sampling Clock Select
0: 64 Hz (initial value)
1: System clock
P0.1 Input/Output Mode Select
0: Input mode (initial value)
1: Output mode
P0.1 Pull-down/Pull-up Resistance Input/High Impedance Input Select (In input mode)
0: Pull-down/pull-up resistance input (initial value)
1: High impedance input
P0.1 CMOS Output/NMOS Open Drain Output Select (In output mode)
0: CMOS output (initial value)
1: NMOS open drain output

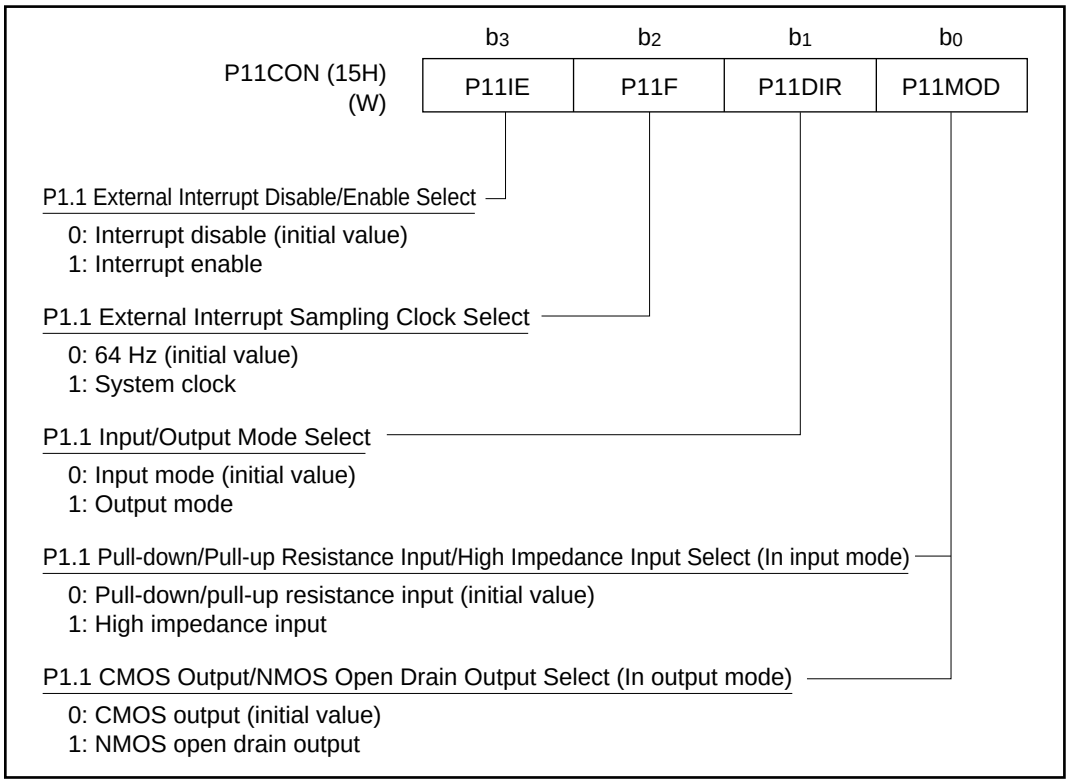

b3 b2 b1 b0
P02CON (12H)
(W)
P02IE P02F P02DIR P02MOD
P0.2 External Interrupt Disable/Enable Select
0: Interrupt disable (initial value)
1: Interrupt enable
P0.2 External Interrupt Sampling Clock Select
0: 64 Hz (initial value)
1: System clock
P0.2 Input/Output Mode Select
0: Input mode (initial value)
1: Output mode
P0.2 Pull-down/Pull-up Resistance Input/High Impedance Input Select (In input mode)
0: Pull-down/pull-up resistance input (initial value)
1: High impedance input
P0.2 CMOS Output/NMOS Open Drain Output Select (In output mode)
0: CMOS output (initial value)
1: NMOS open drain output

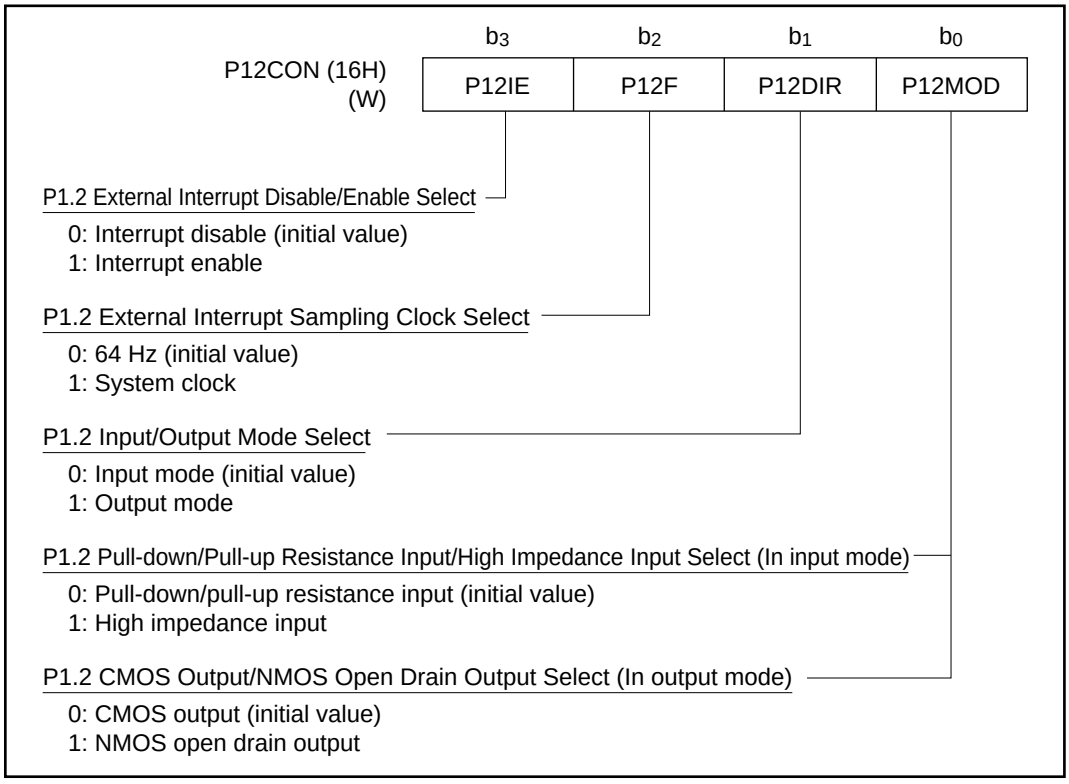

b3
b2
b1
b0
P03CON (13H)
(W)
P03IE
P03F
P03DIR
P03MOD
P0.3 External Interrupt Disable/Enable Select
0: Interrupt disable (initial value)
1: Interrupt enable
P0.3 External Interrupt Sampling Clock Select
0: 64 Hz (initial value)
1: System clock
P0.3 Input/Output Mode Select
0: Input mode (initial value)
1: Output mode
P0.3 Pull-down/Pull-up Resistance Input/High Impedance Input Select (In input mode)
0: Pull-down/pull-up resistance input (initial value)
1: High impedance input
P0.3 CMOS Output/NMOS Open Drain Output Select (In output mode)
0: CMOS output (initial value)
1: NMOS open drain output

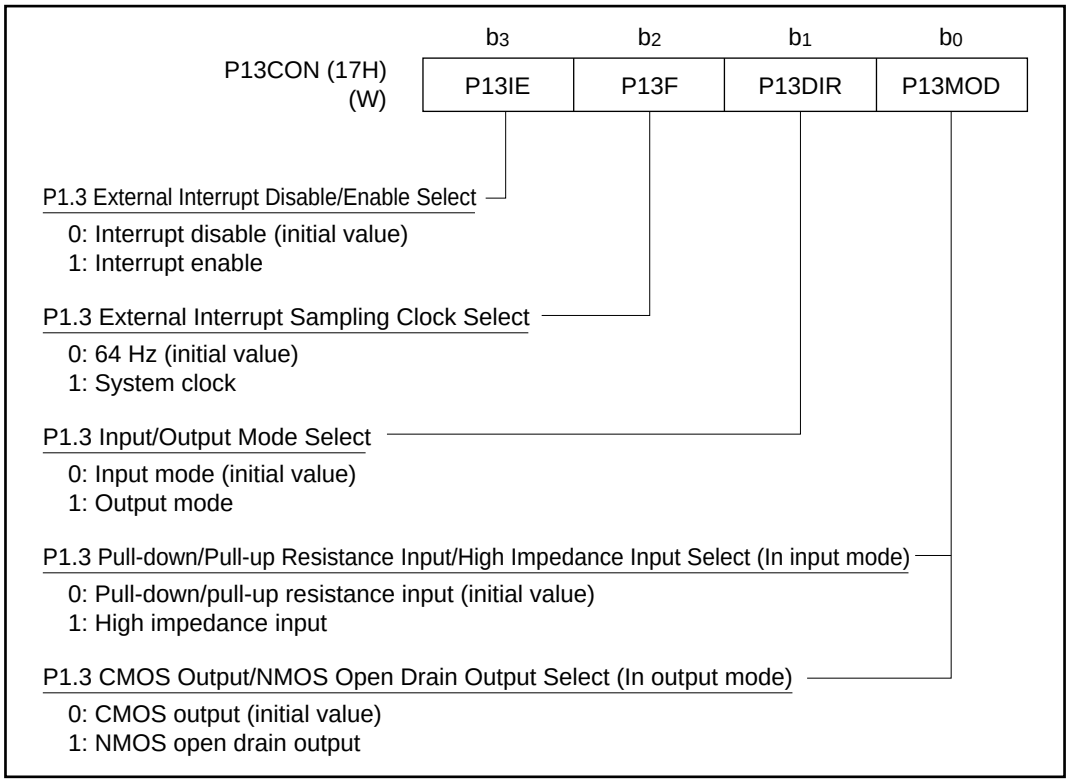
(6) Port 1 Control Registers (P10CON to P13CON)

Port 1 control registers (P10CON to P13CON) are 4-bit special function registers (SFRs) that select input/output mode, pull-down/pull-up resistance input/high impedance input in input mode, CMOS output/NMOS open drain output in output mode, external interrupt disable/enable, and the sampling clocks of external interrupts for Port 1. Since P10CON to P13CON are write only registers, bit operation instructions, and increment and decrement instructions cannot be used.



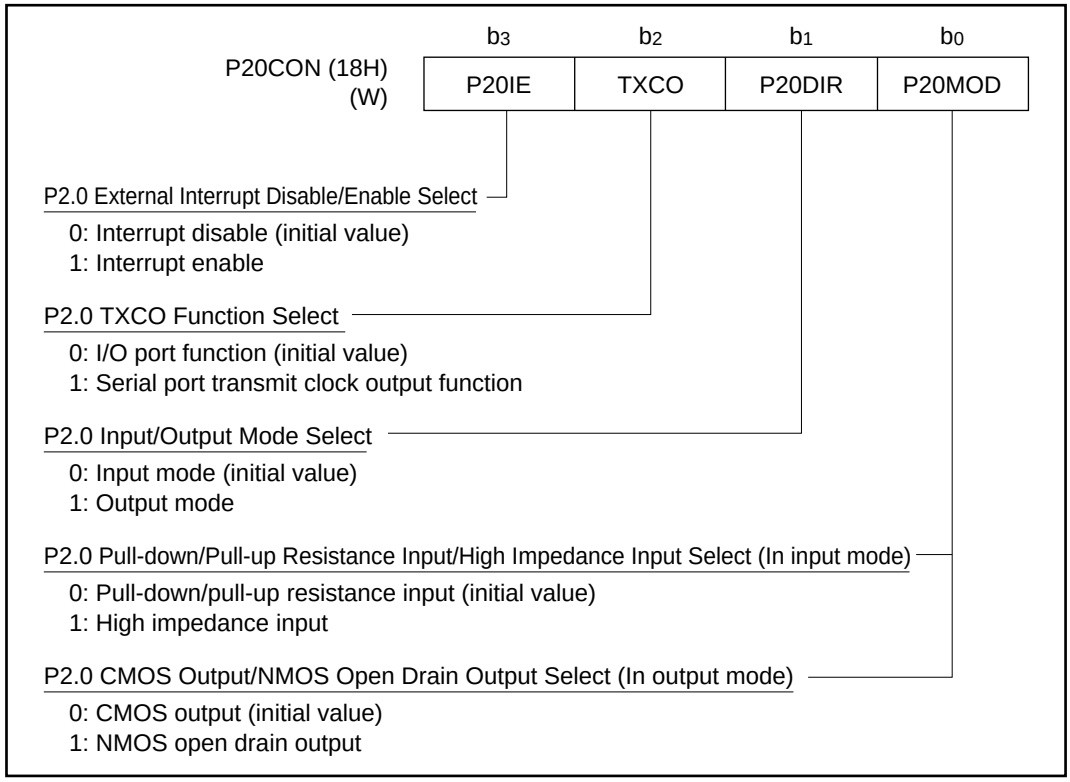

b3 b2 b1 b0
P11CON (15H)
(W)
P11IE P11F P11DIR P11MOD
P1.1 External Interrupt Disable/Enable Select
0: Interrupt disable (initial value)
1: Interrupt enable
P1.1 External Interrupt Sampling Clock Select
0: 64 Hz (initial value)
1: System clock
P1.1 Input/Output Mode Select
0: Input mode (initial value)
1: Output mode
P1.1 Pull-down/Pull-up Resistance Input/High Impedance Input Select (In input mode)
0: Pull-down/pull-up resistance input (initial value)
1: High impedance input
P1.1 CMOS Output/NMOS Open Drain Output Select (In output mode)
0: CMOS output (initial value)
1: NMOS open drain output


b3 b2 b1 b0
P12CON (16H)
(W)
P12IE P12F P12DIR P12MOD
P1.2 External Interrupt Disable/Enable Select
0: Interrupt disable (initial value)
1: Interrupt enable
P1.2 External Interrupt Sampling Clock Select
0: 64 Hz (initial value)
1: System clock
P1.2 Input/Output Mode Select
0: Input mode (initial value)
1: Output mode
P1.2 Pull-down/Pull-up Resistance Input/High Impedance Input Select (In input mode)
0: Pull-down/pull-up resistance input (initial value)
1: High impedance input
P1.2 CMOS Output/NMOS Open Drain Output Select (In output mode)
0: CMOS output (initial value)
1: NMOS open drain output


b3
b2
b1
b0
P13CON (17H)
(W)
P13IE
P13F
P13DIR
P13MOD
P1.3 External Interrupt Disable/Enable Select
0: Interrupt disable (initial value)
1: Interrupt enable
P1.3 External Interrupt Sampling Clock Select
0: 64 Hz (initial value)
1: System clock
P1.3 Input/Output Mode Select
0: Input mode (initial value)
1: Output mode
P1.3 Pull-down/Pull-up Resistance Input/High Impedance Input Select (In input mode)
0: Pull-down/pull-up resistance input (initial value)
1: High impedance input
P1.3 CMOS Output/NMOS Open Drain Output Select (In output mode)
0: CMOS output (initial value)
1: NMOS open drain output

(7) Port 2 Control Registers (P20CON to P23CON)

Port 2 control registers (P20CON to P23CON) are 4-bit special function registers (SFRs) that select input/output mode, pull-down/pull-up resistance input/high impedance input in input mode, CMOS output/NMOS open drain output in output mode, external interrupt disable/enable, as well as TXC, RXC and TXD functions of serial ports, and the TMO function of the timer (secondary function) of Port 2.
Since P20CON to P23CON are write only registers, bit operation instructions and increment/decrement instructions cannot be used.



P21CON (19H) (W)

b_3	b_2	b_1	b_0
P21IE	RXCO	P21DIR	P21MOD

P2.1 External Interrupt Disable/Enable Select
0: Interrupt disable (initial value)
1: Interrupt enable

P2.1 RXCO Function Select
0: I/O port function (initial value)
1: Serial port receive clock output function

P2.1 Input/Output Mode Select
0: Input mode (initial value)
1: Output mode

P2.1 Pull-down/Pull-up Resistance Input/High Impedance Input Select (In input mode)
0: Pull-down/pull-up resistance input (initial value)
1: High impedance input

P2.1 CMOS Output/NMOS Open Drain Output Select (In output mode)
0: CMOS output (initial value)
1: NMOS open drain output

P22CON (1AH) (W)

b_3	b_2	b_1	b_0
P22IE	TXD	P22DIR	P22MOD

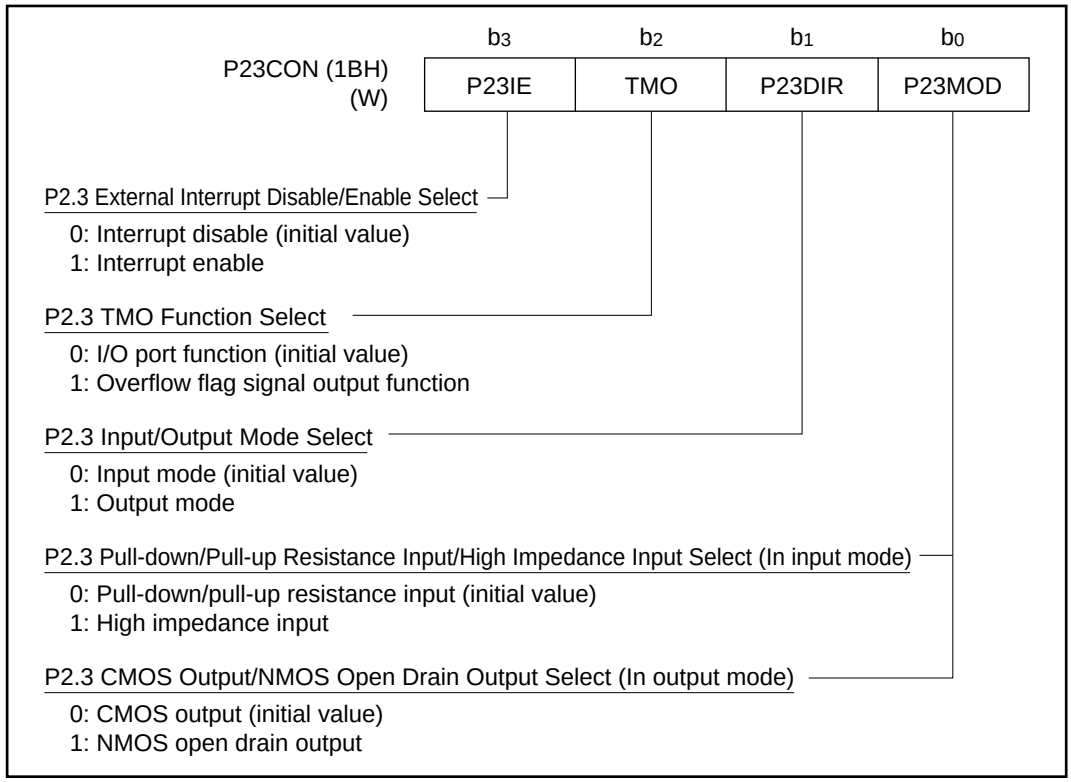
P2.2 External Interrupt Disable/Enable Select
0: Interrupt disable (initial value)
1: Interrupt enable

P2.2 SCLK Function Select
0: I/O port function (initial value)
1: Serial port transmit data output funciton

P2.2 Input/Output Mode Select
0: Input mode (initial value)
1: Output mode

P2.2 Pull-down/Pull-up Resistance Input/High Impedance Input Select (In input mode)
0: Pull-down/pull-up resistance input (initial value)
1: High impedance input

P2.2 CMOS Output/NMOS Open Drain Output Select (In output mode)
0: CMOS output (initial value)
1: NMOS open drain output



Bit 3: P00IE to P03IE, P10IE to P13IE and P20IE to P23IE

Bit to select external interrupt disable/enable. If each IE bit is reset to "0", the external interrupt is disabled, and if set to "1" and the port is an input port, the input level change of the pin is detected, and an external 0 interrupt request is generated. Each IE bit is reset to "0" at system reset.

Bit 2: P00F to P03F and P10F to P13F

Bit to select external interrupt sampling clock. If each F bit is reset to "0", the 64 Hz time base counter output is selected for the sampling clock, and if set to "1", the system clock (32.768 kHz or 700 kHz) is selected. Each F bit is reset to "0" at system reset. P2.0 to P2.3 have no external interrupt sampling clock select function, and are fixed to 64 Hz.

Bit 2: TXCO (P20CON)

Bit to set transmit clock output (TXCO) of serial ports, a secondary function of Port 2.0. If TXCO is reset to "0", the output of P2.0 becomes bit 0 of Port 2 register. If TXCO is set to "1", the output of P2.0 becomes the transmit clock of a serial port. TXCO is reset to "0" at system reset.

Bit 2: RXCO (P21CON)

Bit to set the receive clock output (RXCO) of a serial port, a secondary function of Port 2.1.

If RXCO is reset to "0", the output of P2.1 becomes bit 1 of Port 2 register. If RXCO is set to "1", the output of P2.1 becomes the receive clock of a serial port. RXCO is reset to "0" at system reset.

Bit 2: TXD (P22CON)

Bit to set transfer data output of serial ports, a secondary function of Port 2.2. If TXD is reset to "0", the output of P2.2 becomes bit 2 of Port 2. If TXD is set to "1", the output of P2.2 becomes the transfer data of a serial port. TXD is reset to "0" at system reset.

Bit 2: TMO (P23CON)

Bit to reset overflow flag output (TMO), a secondary function of Port 2.3. If TMO is reset to "0", the output of P2.3 becomes bit 3 of Port 2 register. If TMO is set to "1", the output of P2.3 becomes an overflow flag. TMO is reset to "0" at system reset.

Bit 1: P00DIR to P03DIR, P10DIR to P13DIR and P20DIR to P23DIR

Bit to select the input/output of each port. If each DIR bit is reset to "0", each port enters input mode, and if set to "1", each port enters output mode. Each DIR bit is reset to "0" at system reset.

Bit 0: P00MOD to P03MOD, P10MOD to P13MOD and P20MOD to P23MOD

If each DIR bit is reset to "0" setting input mode, these bits select pull-down/pull-up resistance input/high impedance input.

If each DIR bit is set to "1" setting output mode, these bits select CMOS output/NMOS open drain output.

If each MOD bit is reset to "0", pull-down/pull-up resistance input is selected in input mode, and CMOS output is selected in output mode. If each MOD bit is set to "1", high impedance input is selected in input mode, and NMOS open drain output mode is selected in output mode. Pull-down/pull-up resistance input is selected by bit 0 (PUD) of the port control register (PCON). If PUD is reset to "0", pull-up resistance input is selected, and if PUD is set to "1", pull-down resistance input is selected.

Each MOD bit is reset to "0" at system reset.

Table 7-2 shows the relationship among each DIR bit, each MOD bit and PUD bits.

Table 7-2 Relationship among Each DIR Bit, Each MOD Bit and PUD Bit

Each DIR	Each MOD	PUD	Status of I/O Port
0	0	0	Pull-up resistance input
0	0	1	Pull-down resistance input
0	1	–	High impedance input
1	0	–	CMOS output
1	1	–	NMOS open drain output

7.2.3 External Interrupt Generation Timing of Port 0, Port 1 and Port 2

External interrupts of Ports 0–2 are generated by the change of input level of the ports which enter interrupt enable when IE bits (P00IE to P031IE, P10IE to P13IE and P20IE to P23IE) are set to "1", and which enter input mode when DIR bits (P00DIR to P03DIR, P10DIR to P13DIR and P20DIR to P23DIR) are set to "0".

External 0 interrupt signal XI0INT is the logical sum of the input level change detection signals of P0.0 to P0.3 and P1.0 to P1.3. External interrupt signal XI1INT is the logical sum of the input level change detection signals of P2.0 to P2.3.

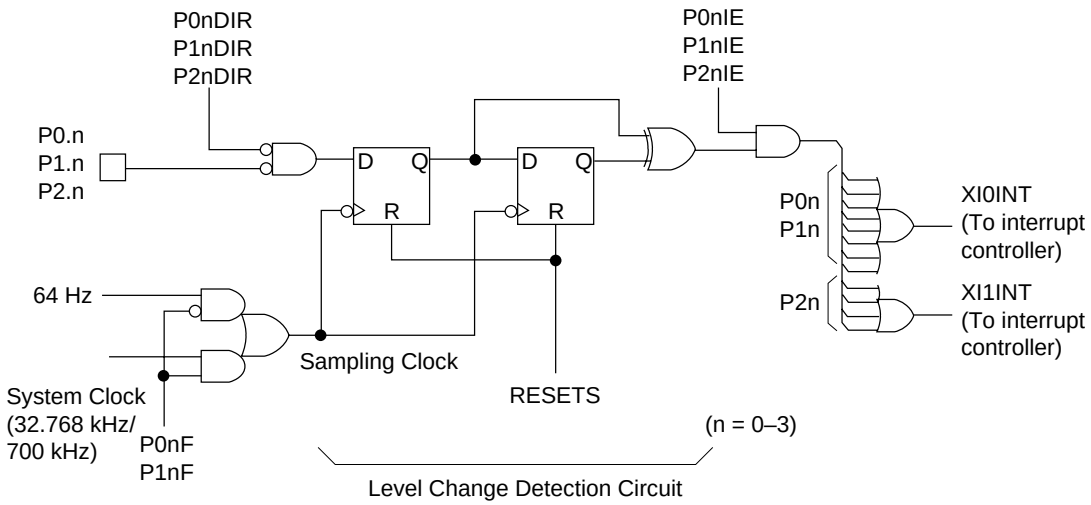
The change of input level is sampled at 64 Hz output of the time base counter which is the sampling clock or at falling of the system clock (32.768 kHz or 700 kHz).

The sampling clock is selected by bit 2 of each port control register (P00F to P03F, P10F to P13F). If the F bit is reset to "0", the sampling clock becomes 64 Hz, and if the F bit is reset to "1", the system clock is selected. P2.0 to P2.3 have no sampling clock select function, and are fixed to a 64 Hz output of the time base counter.

The delay time from the level where Ports 0–2 change, XI0INT and XI1INT signals are output until external 0 interrupt request flag (QXI0) and external 1 interrupt request flag (QXI1) are set to 1 cycle of the sample clock. External 0 and 1 interrupt request flags (QXI0, QXI1) are set by the input level change of one of Ports 0–2. Therefore if it is necessary to determine the port originating the interrupt request, read each port to check the signal level.

The vector address of external 0 interrupt XI0INT is 038H, and the vector address of external interrupt XI1INT is 02FH.

Figures 7-6 and 7-7 show external 0 and 1 interrupt circuits, and external 0 and 1 interrupt generation timing.



Note: Sampling clock of P2n is fixed at 64 Hz.

Figure 7-6 External 0 and 1 Interrupt Generation Circuit (For 1 bit)

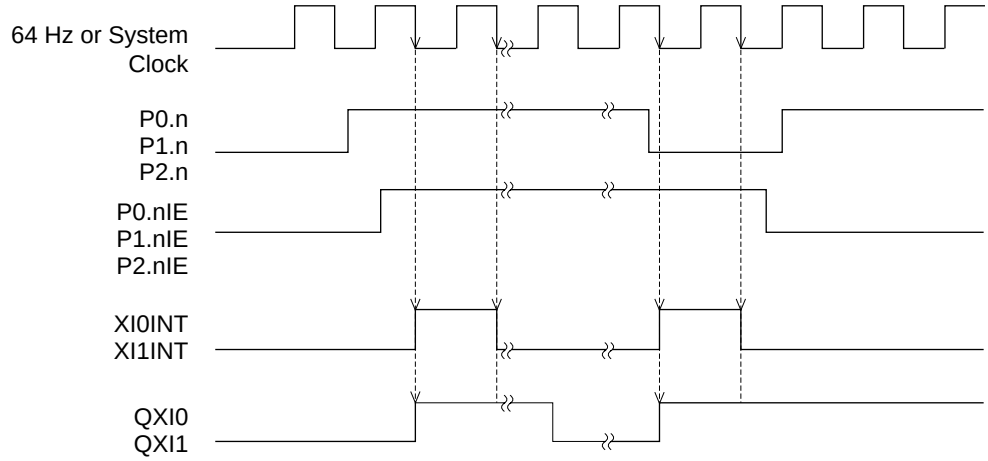


Figure 7-7 External Interrupt Generation Timing

Table 7-3 shows port-related registers.

Table 7-3 Port-Related Registers

Register Name	Symbol	Address	Read/Write	Value at System Reset
Port 0 Register	P0	00H	R/W	0H
Port 1 Register	P1	01H	R/W	0H
Port 2 Register	P2	02H	R/W	0H
Port 00 Control Register	P00CON	10H	W	0H
Port 01 Control Register	P01CON	11H	W	0H
Port 02 Control Register	P02CON	12H	W	0H
Port 03 Control Register	P03CON	13H	W	0H
Port 10 Control Register	P10CON	14H	W	0H
Port 11 Control Register	P11CON	15H	W	0H
Port 12 Control Register	P12CON	16H	W	0H
Port 13 Control Register	P13CON	17H	W	0H
Port 20 Control Register	P20CON	18H	W	0H
Port 21 Control Register	P21CON	19H	W	0H
Port 22 Control Register	P22CON	1AH	W	0H
Port 23 Control Register	P23CON	1BH	W	0H
Port Control Register	PCON	1CH	W	0EH
Interrupt Enable Register 1	IE1	32H	R/W	0H
Interrupt Request Register 1	IRQ1	33H	R/W	0H
Interrupt Enable Register 2	IE2	34H	R/W	0H
Interrupt Request Register 2	IRQ2	35H	R/W	0H

Chapter 8

Timer (TM)

Chapter 8 Timer (TM)

8.1 Overview

The MSM64167E has an internal 16-bit timer (TM). This timer has three operation modes: auto reload mode, capture mode, and clock frequency measurement mode, and it operates at 32.768 kHz, 700 kHz, or via an external clock. The timer is used for pulse generation, time measurement, etc., and is also used as an AD conversion counter during AD conversion, and as a baud rate generator during serial communication.

8.2 Configuration of Timer

Figure 8-1 shows the timer configuration.

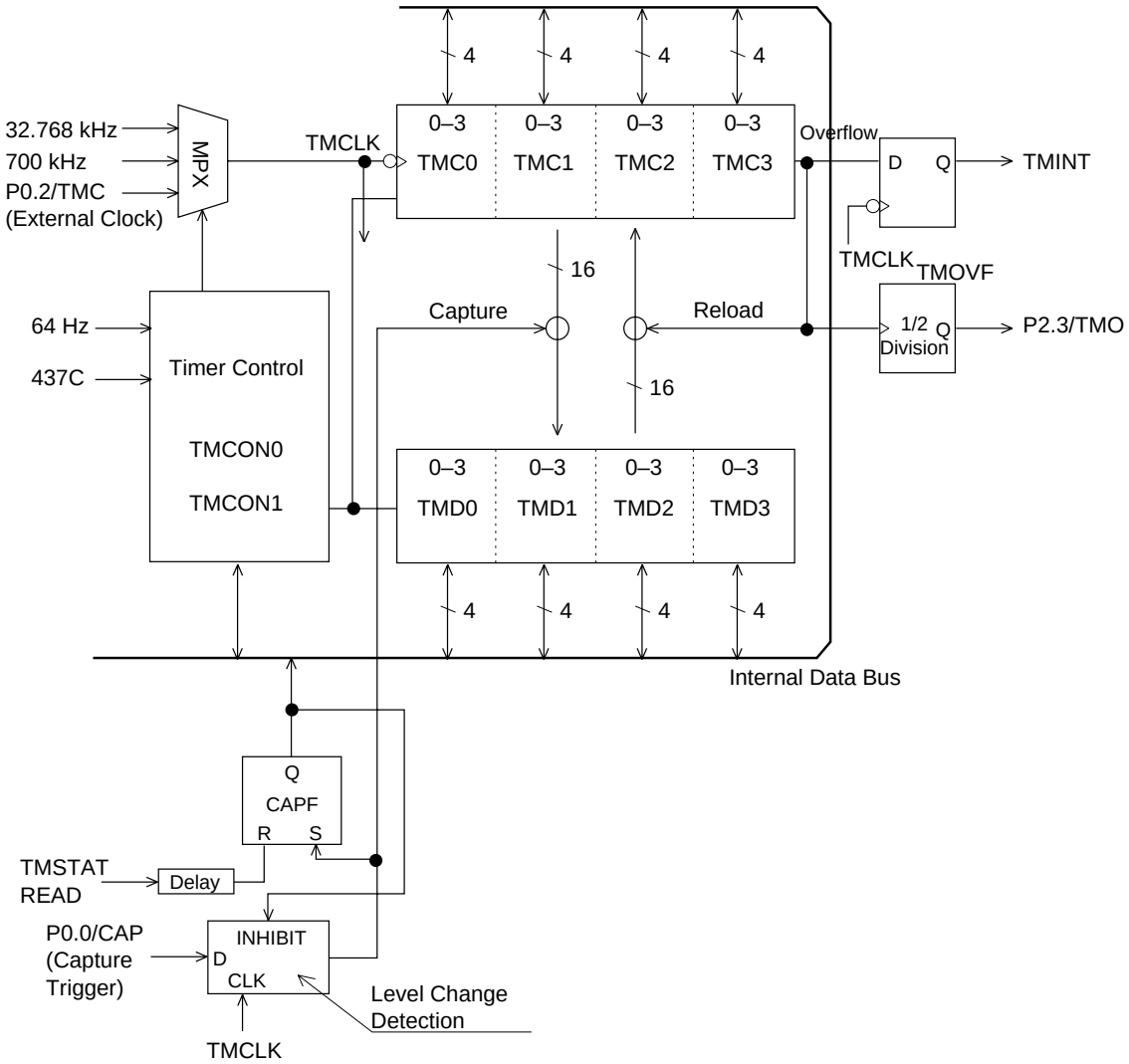


Figure 8-1 Timer Configuration

8.3 Operation of Timer

8.3.1 Timer Clock (TMCLK)

There are three types of timer clocks: 32.768 kHz, 700 kHz and an external clock, selected by timer control register 1 (TMCON1). 32.768 kHz and 700 kHz are internal signals generated by the clock generation circuit. The external clock is an external input signal from Port 0.2 (TMC).

8.3.2 Timer Counter Registers 0–3 (TMC0–3)

Timer counter registers 0–3 (TMC0–3) function as a 16-bit (4-bit × 4) binary counter that is incremented at the fall of the timer clock (TMCLK). LSB is bit 0 of TMC0, and MSB is bit 3 of TMC3. The value of TMC0–3 can be read/written by software, but caution is advised for access during a count operation. If a value is written to a timer counter register, that same value is also written to the corresponding timer data register.

8.3.3 Timer Data Registers 0–3 (TMD0–3)

Timer data registers 0–3 (TMD0–3) function as a 16-bit (4-bit × 4) register. In auto reload mode, a timer data register becomes a register that maintains the value to reload to the timer counter register when the timer counter register overflows. In capture mode, a timer data register becomes a register that holds the value of a timer counter register when a capture signal is received.

LSB is bit 0 of TMD0, and MSB is bit 3 of TMD3. The value of TMD0–3 can be read/written by software, but even if a value is written to a timer data register, the value of a timer counter register does not change.

8.3.4 Timer Interrupt Request (TMINT) and Timer Overflow Flag (TMOVF)

The timer generates a timer interrupt request (TMINT) every time a timer counter register overflows. A timer overflow flag signal (TMOVF) is output to invert "1" and "0" every time an overflow occurs to P2.3 (secondary function of P2.3).

Figure 8-2 shows the operation timing when a timer counter register overflows.

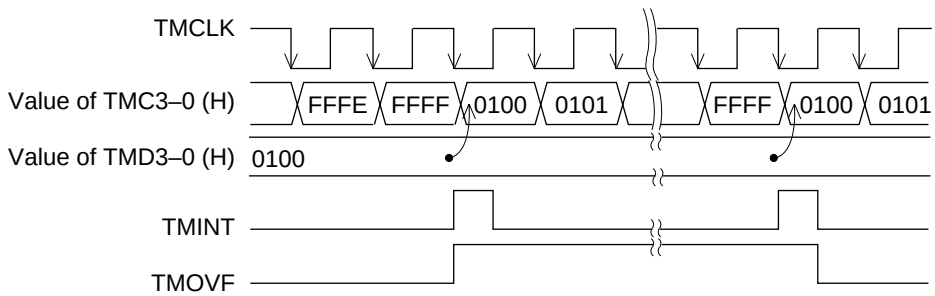


Figure 8-2 Operation Timing when Timer Counter Register Overflows

8.3.5 Operation in Auto Reload Mode

If both bit 1 (FMEAS) and bit 2 (ECAP) of timer control register 0 (TMCON0) are set to "0", the timer enters auto reload mode. In auto reload mode, the value of the timer data register (0 to 3) is reloaded to the timer counter register 0 to 3 every time the timer counter register overflows. The counting starts again from that value.

The count operation is enabled when bit 0 (TMRUN) of timer control register 0 (TMCON0) is "1", and is stopped when the bit is "0".

Figure 8-3 shows the operation timing in auto reload mode.

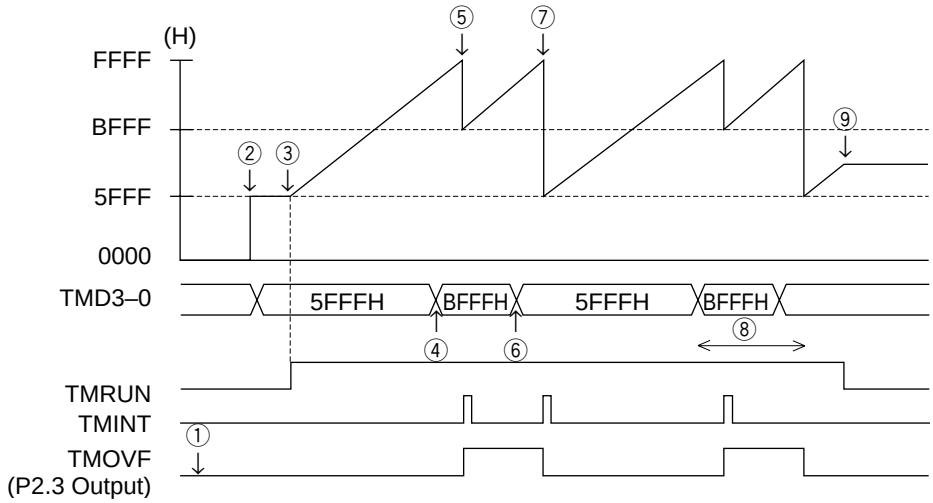


Figure 8-3 Operation Timing in Auto Reload Mode

Figure 8-3 is an example when auto reload mode is applied to pulse generation. The operation procedure follows.

① Set P2.3 to output mode (TMO) at the secondary function side.
② Write 5FFFH to TMC3–0 and TMD3–0.
③ Set TMCON0 to auto reload mode, and set TMRUN to "1", the timer counter register then starts to count from 5FFFH.
④ Write the next BFFFH reload value to the timer data register before the timer counter register overflows.
⑤ If the timer counter register overflows, BFFFH is set at the timer counter register, timer interrupt request TMINT is generated, and timer overflow flag TMOVF inverts. The timer counter register continues to count from BFFFH.
⑥ Write the next 5FFFH reload value to the timer data register before the timer counter overflows.
⑦ If the timer counter register overflows, 5FFFH is set at the timer counter register, and timer interrupt request TMINT is generated, and timer overflow flag TMO inverts. The timer counter register continues to count from 5FFFH.
⑧ Repeat from ④ to ⑦. In this way any pulse can be output to P2.3.
⑨ If TMRUN is set to "0", the count stops.
Figure 8-4 shows the count start/stop timing by TMRUN.

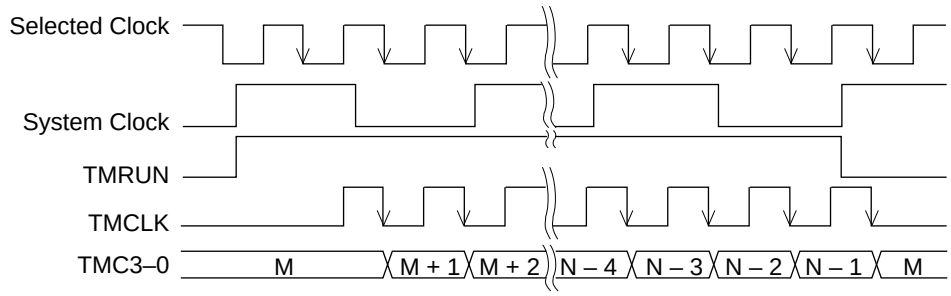


Figure 8-4 Count Start/Stop Timing by TMRUN

If TMRUN is set to "1", the timer counter register starts counting at the 2nd fall of the selected clock. If TMRUN is reset to "0", the timer counter register is incremented at the next fall of the selected clock, then the count stops.

If the timer is used for AD conversion, TMRUN is reset to "0" at the same time as an A/D converter interrupt requirement (ADINT) is generated.

Figure 8-5 shows the operation timing when ADINT is generated.

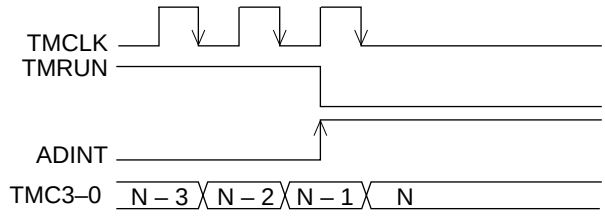


Figure 8-5 Operation Timing when ADINT is Generated

8.3.6 Operation in Capture Mode

If bit 1 (FMEAS) of timer control register is set to "0" and bit 2 (ECAP) is set to "1", timer enters capture mode. In capture mode, the reload operation from the timer data register to the timer counter register is disabled, and if the timer counter register overflows, counting is restarted from "0000H".

If a capture trigger occurs (level of P0.0 input changes) when the timer counter register is operating, the value of the timer counter register at that time is saved to the timer data register. This operation is called "capture". If a capture occurs, the capture flag (CAPF), bit "0" of the timer status register (TMSTAT), is set to "1". The next capture is disabled when CAPF is "1". CAPF is automatically reset to "0" if TMSTAT is read.

Figure 8-6 shows the operation timing of capture mode.

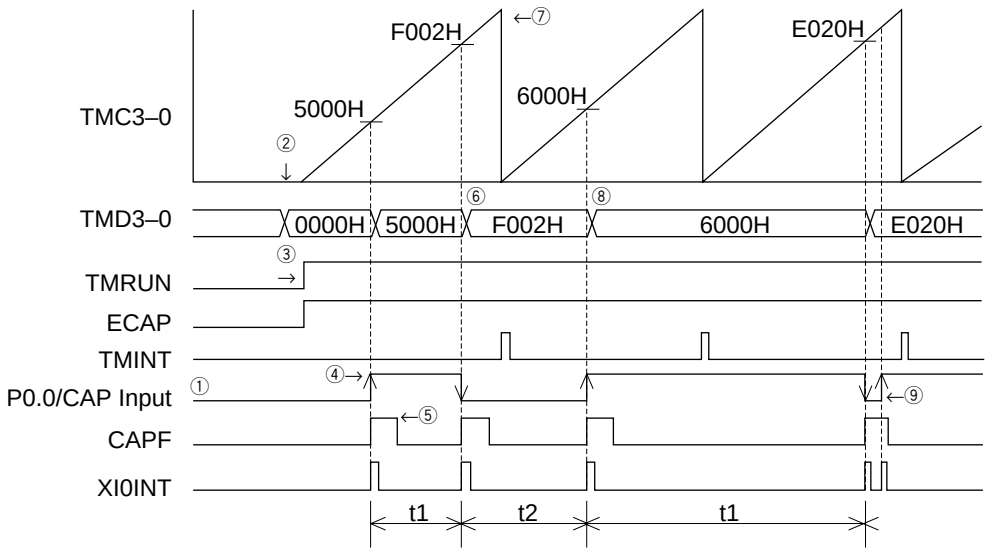


Figure 8-6 Operation Timing in Capture Mode

Figure 8-6 shows an example of when capture mode is applied to a measuring pulse width. The operation procedure follows.

① Set P0.0/CAP to input mode and enable XIOINT, TMINT.
② Clear all bits of the timer counter registers and the timer data registers to zero.
③ Set TMCON0 to capture mode and set TMRUN to "1" to start counting.
④ If P0.0 input changes, the value of TMC3–0 at that time is captured to TMD3–0 and CAPF is set to "1" (1st capture). The CPU detects this by XIOINT and reads the values of TMD3–0.
⑤ When the reading of TMD3–0 ends, reset CAPF to "0", and wait for the next capture.
⑥ If P0.0/CAP input changes, operations ④ and ⑤ are repeated (2nd capture). "H" pulse width t1 of P0.0 input is determined by

$$t1 = (F002H - 5000H) \times t_{CLK} \qquad t_{CLK}: \text{TMCLK cycle}$$

⑦ Always remember that if the timer counter register overflows, TMINT is generated. The timer counter register returns from FFFFH to 0000H and continues counting.
⑧ If P0.0/CAP input changes, operations ④ and ⑤ are repeated (3rd capture). Since the counter overflows once between the 2nd and 3rd capture, "L" pulse width t2 of P0.0 input is determined by

$$t2 = (6000H - F002H + 10000H) \times t_{CLK}$$

⑨ Even if P0.0/CAP changes, capture does not occur if CAPF is "1".

Figure 8-7 shows operation timing during capture, and Figure 8-8 shows the capture signal (CAP) generation circuit.

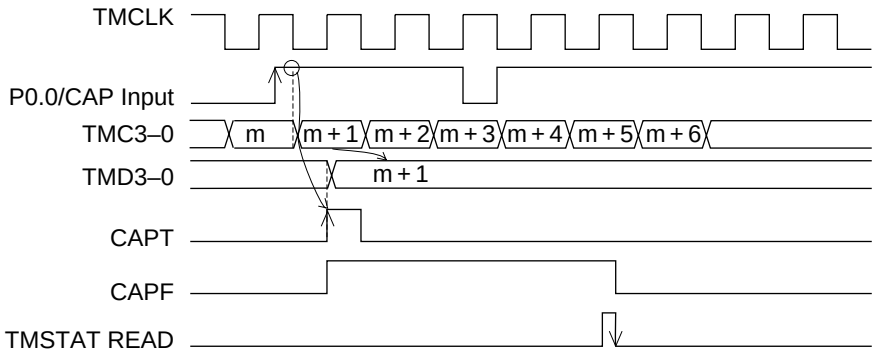


Figure 8-7 Operation Timing During Capture

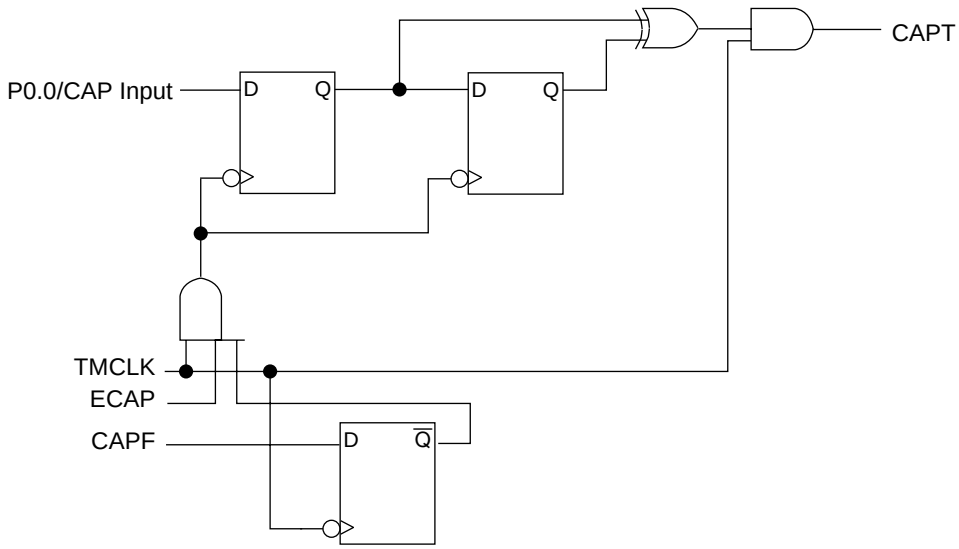


Figure 8-8 Capture Signal (CAPT) Generation Circuit

The maximum delay time from a P0.0/CAP input level change until capture is 1 cycle of the timer clock.

8.3.7 Operation in Clock Frequency Measurement Mode

If bit 1 of timer control register 0 (TMCON0) is set to "1", and bit 2 is set to "0", the timer enters clock frequency measurement mode. Clock frequency measurement mode allows the measurement of the frequency of the 700 kHz RC oscillation clock, which exhibits dispersion due to manufacturing. Based on the count value acquired by this measurement, the value to set to the timer data register in auto reload mode is determined, and the baud rate clock required for serial transmission is generated.

Figure 8-9 shows the operation timing in clock frequency measurement mode.

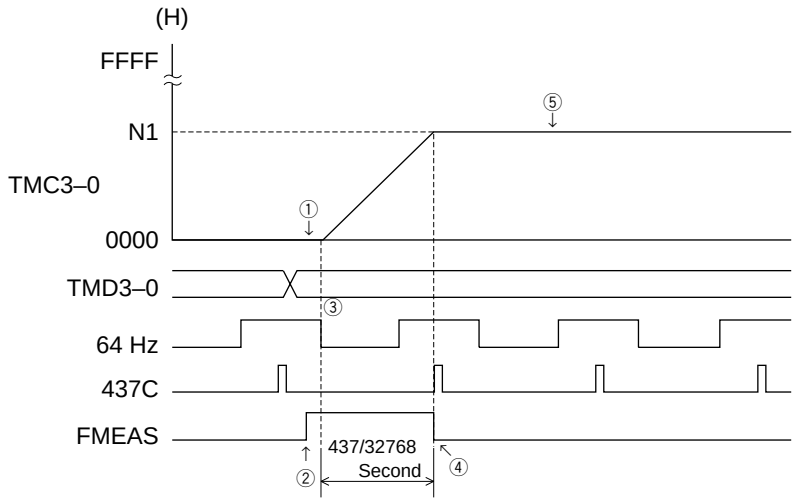


Figure 8-9 Operation Timing in Clock Frequency Measurement Mode

The operation procedure of Figure 8-9 follows.

① Clear all bits of the timer counter registers and the timer data registers to zero, and set TMCLK to 700 kHz.
② Set FMEAS to "1" to enter clock frequency measurement mode. (Do not set TMRUN to "1".)
③ If the fall of 64 Hz comes when FMEAS is "1", the counter starts.
④ If the 437C signal becomes "1", FMEAS is reset to "0", and the counter stops at the fall of the next TMCLK. The 437C signal is a pulse signal that rises at 437/32768 second after the fall of 64 Hz.
⑤ Read value N1 of TMC3–0.

If the 700 kHz RC oscillation clock is exactly 700 kHz, the count value N1 read from TMC3–0 becomes:

N1 = 700000 × 437/32768 = 9335 (Decimal)
= 2477 (Hexadecimal)
= 0010 0100 0111 0111 (Binary)
Round Down

Since 437/32768 second corresponds to 128 oscillations of the 9600 Hz (precisely 9598 Hz) clock, the dividing value N2 to generate 9600 Hz from 700 kHz is determined. When the count value is divided by 128 Since 128 is 2^7, N2 can be determined when the lower 7 digits of N1 (binary) are rounded down.

N2 = 9335/128 = 0010010000 (Binary)
= 48 (Hexadecimal)
= 72 (Decimal)

This indicates that 9600 Hz is about 72 times the cycle of 700 kHz. Therefore, if TMD3–0 are set to FFB8H so that the counter overflows every 72 counts of the 700 kHz clock and the timer is operated in auto reload mode, the cycle of TMINT (t_{TMINT}) generated by overflow becomes

t_{TMINT} = 1/700000 × 72 = 0.10286 ms (9722 Hz).

In the same way, if the 700 kHz RC oscillation clock is actually 600 kHz, due to dispersion by manufacturing, N1 becomes

N1 = 600000 × 437/32768 = 8001 (Decimal)
= 1F41 (Hexadecimal)
= 0001 1111 0100 0001 (Binary)
Round Down

If the lower 7 digits of N1 (binary) are rounded down,

N2 = 9335/128 = 000111110 (Binary)
= 3 E (Hexadecimal)
= 62 (Decimal)

If TMD3–0 are set to FFC2H so that the counter overflows every 62 counts of the 600 kHz clock and the timer is operated in auto reload mode, then the cycle of TMINT (t_{TMINT}) generated by overflow becomes

t_{TMINT} = 1/600000 × 62 = 0.10333 ms (9677 Hz).

Therefore, by the application of clock frequency measurement mode, a precision cycle of a TMINT signal can be generated from a 700 kHz RC oscillation clock that has a large dispersion. This TMINT signal can be supplied to serial ports as a baud rate clock. By changing N2, it is easy to generate 4800 Hz, 2400 Hz, and any other baud rate clock. The accuracy of a baud rate clock generated in this manner can be within ±2% for 9600 Hz, and ±1% for 4800 Hz or less.

Figure 8-10 shows the operation of baud rate clock generation when the RC oscillation clock frequency is 700 kHz.

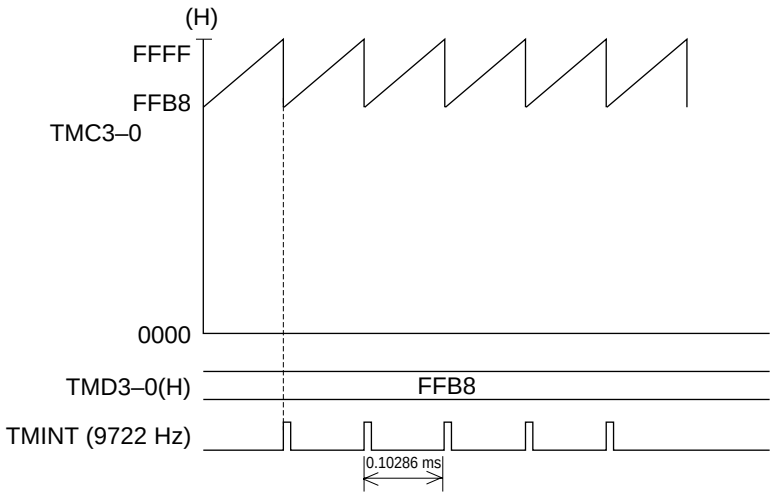
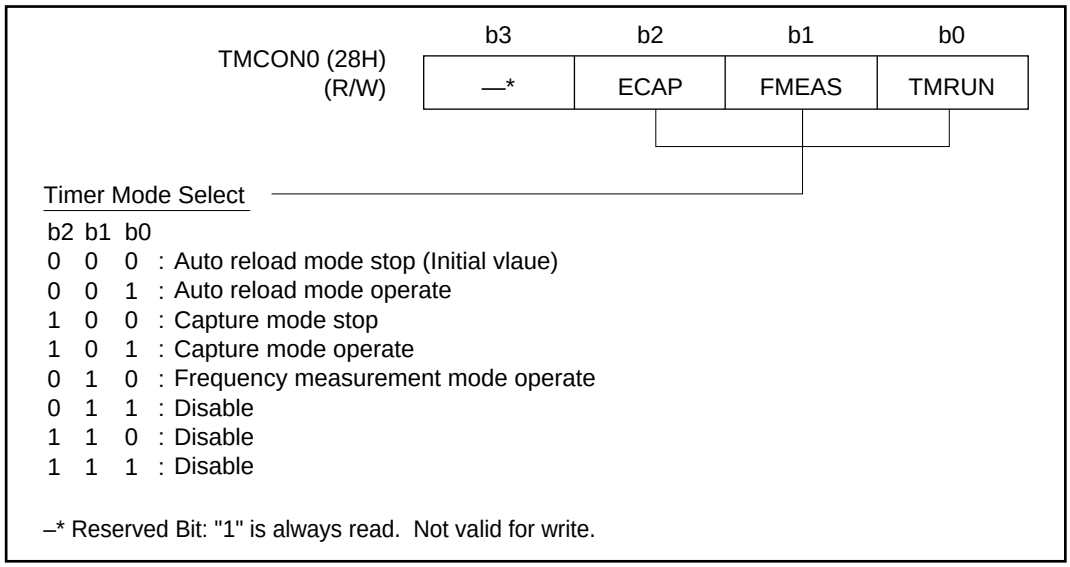


Figure 8-10 Operation of Baud Rate Clock Generation

8.4 Timer-Related Registers

(1) Timer Control Register 0 (TMCON0)
Timer control register 0 (TMCON0) is a 4-bit special function register that controls the operation mode of the timer.



b2	b1	b0	
0	0	0	: Auto reload mode stop (Initial vlaue)
0	0	1	: Auto reload mode operate
1	0	0	: Capture mode stop
1	0	1	: Capture mode operate
0	1	0	: Frequency measurement mode operate
0	1	1	: Disable
1	1	0	: Disable
1	1	1	: Disable

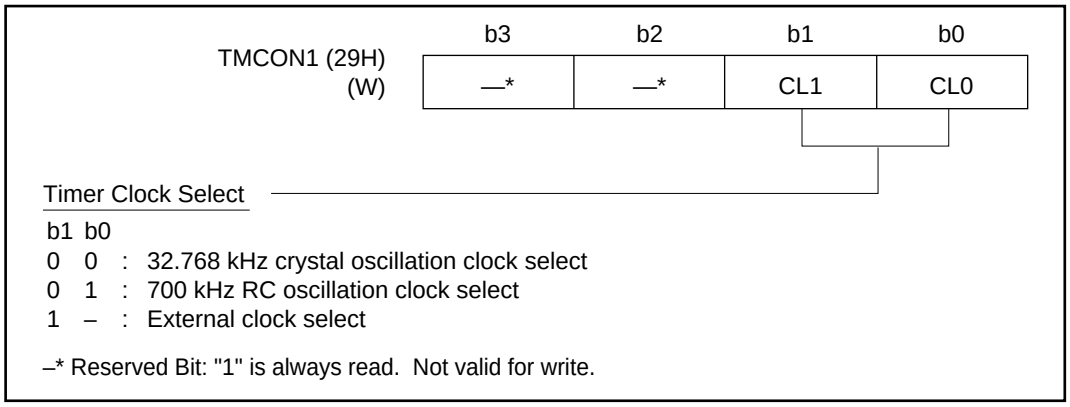
–* Reserved Bit: "1" is always read. Not valid for write.

Bits 2 to 0

ECAP, FMEAS and TMRUN are bits that control operation mode, and count operation stop/operate of each timer. In auto reload mode and in capture mode, count operation stop/operate is controlled by the TMRUN bit. In frequency measurement mode, if the FMEAS bit is set to "1", count operation is performed from the fall of the next 64 Hz to the rise of 437C. All 3 bits are reset to "0" at system reset. Do not set the FMEAS bit and other bits to "1" at the same time.

(2) Timer Control Register 1 (TMCON1)

Timer control register 1 (TMCON1) is a 4-bit special function register that selects the timer clock. Since TMCON1 is for writing only, bit operation instructions, and increment and decrement instructions cannot be used.



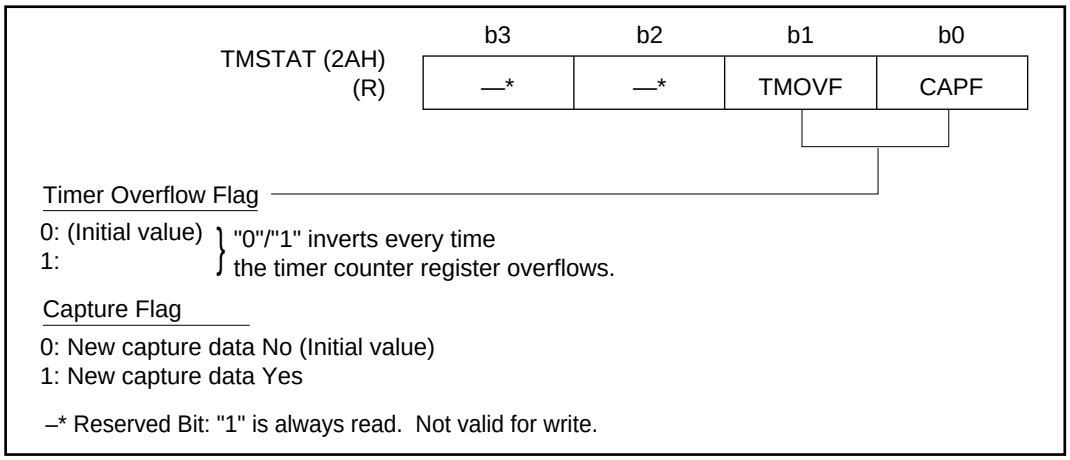
Bits 1, 0: CL1, CL0

CL1 and CL0 are bits that select the timer clock. Both are reset to "0" and the 32.768 kHz crystal oscillation clock is selected at system reset.

Note: If the 700 kHz RC oscillation clock is selected, set FCON (09H) to "1H" to enable 700 kHz RC oscillation.

(3) Timer Status Register (TMSTAT)

The timer status register (TMSTAT) is a 4-bit special function register (SFR) that indicates the status of the timer.



Bit 1: TMOVF

Flag that indicates a timer counter register overflow. "0"/"1" inverts every time an overflow occurs. TMOVF is reset to "0" at system reset.

Bit 0: CAPF

Bit that indicates new capture data yes/no. If CAPF is "0", it indicates that there is no new capture data after system reset or after CAPF was read the last time. If CAPF is "1", it indicates that there are new capture data. If CAPF is "1", the next capture is disabled. CAPF is reset to "0" at system reset. If the input level of P0.0 changes and capture occurred in capture mode, CAPF is automatically set to "1". CAPF is automatically reset to "0" if TMSTAT is read.

(4) Timer Data Registers 0 to 3 (TMD0 to 3)

Timer data registers (TMD0 to 3) are 4-bit special function registers (SFRs) that store reload values to timer counter registers 0 to 3 in auto reload mode, and store capture data of timer counter registers 0 to 3 in capture mode.

TMD0 (20H) (R/W)

b3	b2	b1	b0
TD3	TD2	TD1	TD0

Value of bits 3 to 0 of 16-bit data register

TMD1 (21H) (R/W)

b3	b2	b1	b0
TD7	TD6	TD5	TD4

Value of bits 7 to 4 of 16-bit data register

TMD2 (22H) (R/W)

b3	b2	b1	b0
TD11	TD10	TD9	TD8

Value of bits 11 to 8 of 16-bit data register

TMD3 (22H) (R/W)

b3	b2	b1	b0
TD15	TD14	TD13	TD12

Value of bits 15 to 12 of 16-bit data register

Bits 15 to 0

Bits 15 to 0 of a 16-bit data register. Bit 15 is MSB, bit 0 is LSB. Data is exchanged with the same bit number of the timer counter register. Since these bits are not reset at system reset, initial values are undefined. Even if data is written to TMD0 to 3, the values of TMC0 to 3 do not change. If data is written to TMD0 to 3 in capture register mode, the values of TMC0 to 3 are written to TMD0 to 3.

(5) Timer Counter Registers 0 to 3 (TMC0 to 3)

Timer counter registers (TMC0 to 3) are 4-bit special function registers (SFRs) that function as a 16-bit binary counter.

TMC0 (24H) (R/W)

b3	b2	b1	b0
TC3	TC2	TC1	TC0

Value of bits 3 to 0 of 16-bit binary counter.

TMC1 (25H) (R/W)

b3	b2	b1	b0
TC7	TC6	TC5	TC4

Value of bits 7 to 4 of 16-bit binary counter.

TMC2 (26H) (R/W)

b3	b2	b1	b0
TC11	TC10	TC9	TC8

Value of bits 11 to 8 of 16-bit binary counter.

TMC3 (27H) (R/W)

b3	b2	b1	b0
TC15	TC14	TC13	TC12

Value of bits 15 to 12 of 16-bit binary counter.

Bits 15 to 0

Bits 15 to 0 of the 16-bit binary counter. The counter is incremented at the fall of timer clock TMCLK. Bit 15 is MSB, bit 0 is LSB. Since these bits are not reset at system reset, initial values are undefined. If data is written to TMC0 to 3, the same values are written to the corresponding bits of TMD0 to 3.

Table 8-1 shows timer-related registers.

Table 8-1 Timer-Related Registers

Register Name	Symbol	Address	Read/Write	Value at System Reset
Timer Data Register 0	TMD0	20H	R/W	Undefined
Timer Data Register 1	TMD1	21H	R/W	Undefined
Timer Data Register 2	TMD2	22H	R/W	Undefined
Timer Data Register 3	TMD3	23H	R/W	Undefined
Timer Counter Register 0	TMC0	24H	R/W	Undefined
Timer Counter Register 1	TMC1	25H	R/W	Undefined
Timer Counter Register 2	TMC2	26H	R/W	Undefined
Timer Counter Register 3	TMC3	27H	R/W	Undefined
Timer Control Register 0	TMCON0	28H	R/W	8H
Timer Control Register 1	TMCON1	29H	W	0CH
Timer Status Register 0	TMSTAT	2AH	R	0CH
Interrupt Enable Register 1	IE1	32H	R/W	0H
Interrupt Request Register 1	IRQ1	33H	R/W	0H

Chapter 9

Serial Port (SIOP)

Chapter 9 Serial Port (SIOP)

9.1 Overview

The serial port (SIOP) is used for serial communication, and can select synchronous/asynchronous communication.

Since the transmit and receive parts of the serial port are independent circuit blocks, transmit and receive can be performed simultaneously.

Each transmit and receive mode has:

- UART mode (asynchronous communication mode)
- Synchronous mode (synchronous communication mode)

In UART mode, transmit baud rate can be set to any value up to 9600 bps by built-in timer and 700 kHz RC oscillation circuit. Receive baud rate can be set to any one value from 9600/4800/2400/1200 bps by program.

There are two clock modes in synchronous mode: internal clock mode generating shift clock internally and external clock mode receiving supply of shift clock externally. The baud rate of internal clock mode is fixed at 32.768 kHz. Maximum baud rate for external clock mode is 500 kHz.

Table 9-1 shows the serial port modes and baud rate.

Table 9-1 Modes of Serial Port and Baud Rate

		Mode		Baud Rate
Serial Port	Transmit	UART Mode		Any value up to 9600 bps can be set by timer (TM)
		Synchronous Mode	Internal Clock Mode	Fixed at 32.768 kHz
			External Clock Mode	By external clock (500 kHz Max.)
	Receive	UART Mode		① 9600 bps ② 4800 bps ③ 2400 bps ④ 1200 bps
		Synchronous Mode	Internal Clock Mode	Fixed at 32.768 kHz
			External Clock Mode	By external clock (500 kHz Max.)

Note: 32.768 kHz is the oscillation frequency of XTOSC.

9.2 Configuration of Serial Port

Figure 9-1 shows the configuration of the serial port.

The serial port is comprised of a transmit/receive clock generation circuit, a control register to control transmit/receive operations, a buffer register to store transmit/receive data, a shift register to transfer transmit/receive data, and a status register, to indicate transmit/receive operation status.

Table 9-2 shows serial port related registers.

Table 9-2 Serial Port Related Registers

Register Name	Symbol	Address	Bit Configuration				R/W	Value at System Reset
			b3	b2	b1	b1		
Transmit Control Register (L)	STCONL	60H	STSTB	STL1	STL0	STMOD	R/W	0H
Transmit Control Register (H)	STCONH	61H	STLMB	STPOE	STPEN	CLK	R/W	0H
Transmit Buffer Register (L)	STBUFL	62H	TB3	TB2	TB1	TB0	R/W	0H
Transmit Buffer Register (H)	STBUFH	63H	TB7	TB6	TB5	TB4	R/W	0H
Receive Control Register (L)	SRCONL	64H	SREN	SRL1	SRL0	SRMOD	R/W	0H
Receive Control Register (H)	SRCONH	65H	SRLMB	SRPOE	SRPEN	SRCLK	R/W	0H
Receive Buffer Register (L)	SRBUFL	66H	RB3	RB2	RB1	RB0	R	0H
Receive Buffer Register (H)	SRBUFH	67H	RB7	RB6	RB5	RB5	R	0H
Receive Baud Rate Setting Register	SRBRT	68H	–	–	BRT1	BRT0	R/W	0CH
Serial Port Status Register	SSTAT	69H	BFULL	PERR	OERR	FERR	R	0H

In Figure 9-1, P0.1/RXD is the receive serial data input pin, P2.2/TXD the transmit serial data output pin, P2.0/TXC the serial transmit clock I/O pin, and P2.1/RXC the serial receive clock I/O pin. For P2.0/TXC and P2.1/RXC, set input or output by the port control register according to the mode at synchronous communication (internal or external clock mode).

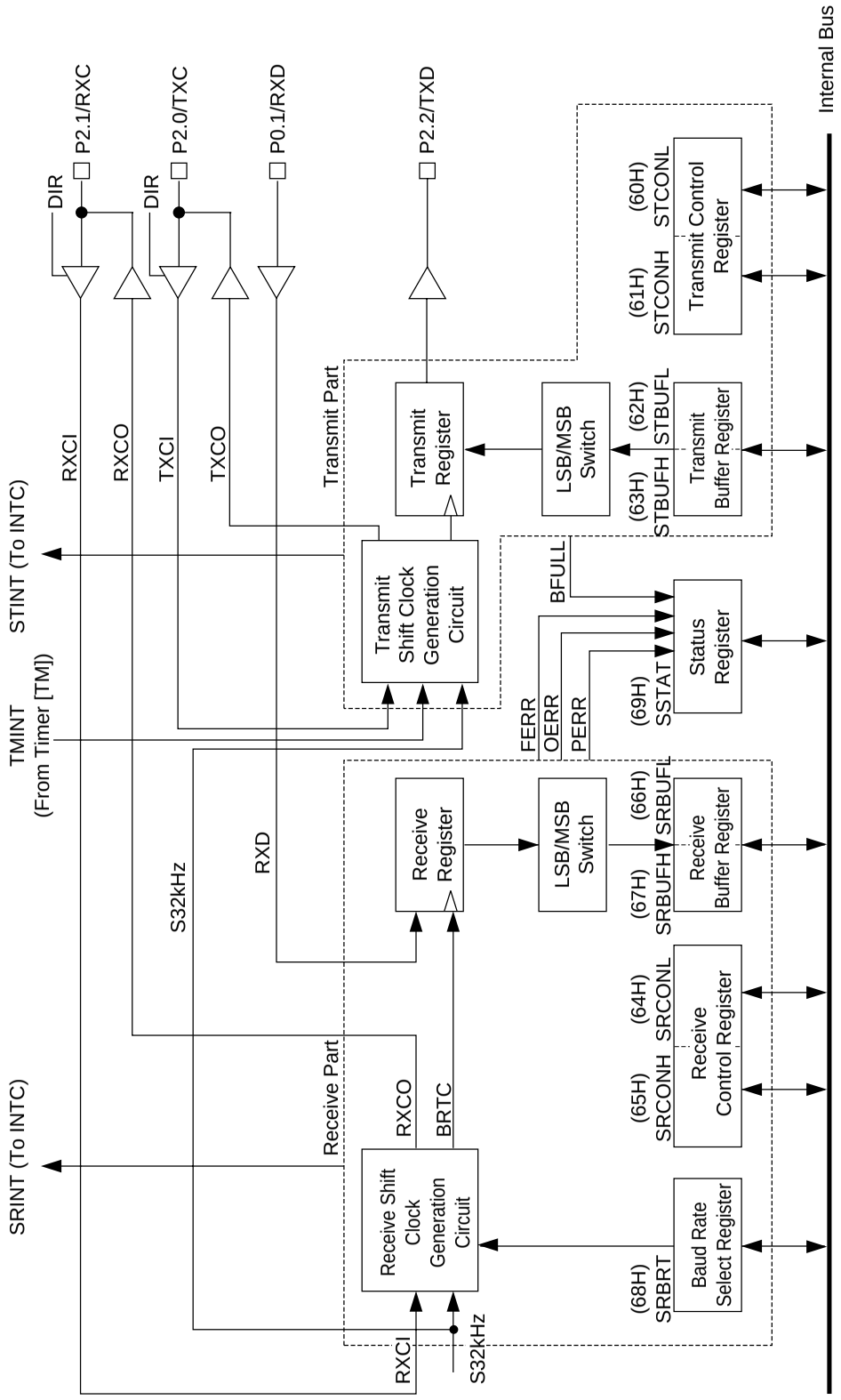


Figure 9-1 Configuration of Serial Port

9.3 Serial Port-Related Registers

9.3.1 Transmit Control Register (STCONL, STCONH)

STCONL and STCONH are 4-bit special function registers that control transmit operations of the serial port.

STCONL and STCONH are assigned to SFR addresses 60H and 61H, and both contents become 0H at system reset.

Figure 9-2 (a) shows the configuration of STCONL, and Figure 9-2 (b) shows the configuration of STCONH.

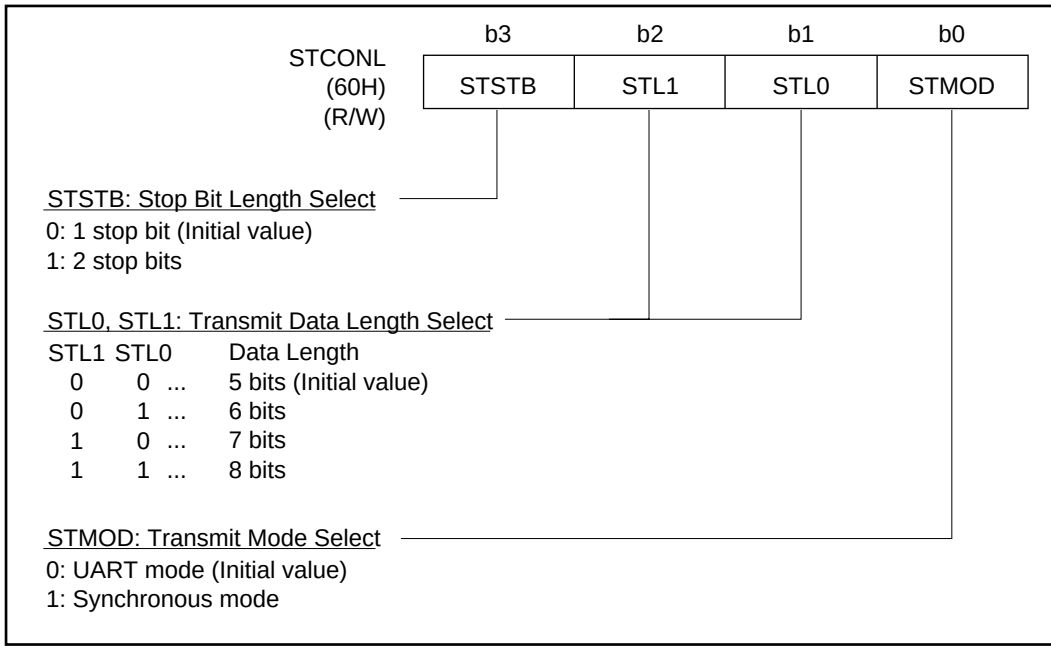


Figure 9-2 (a) Configuration of STCONL

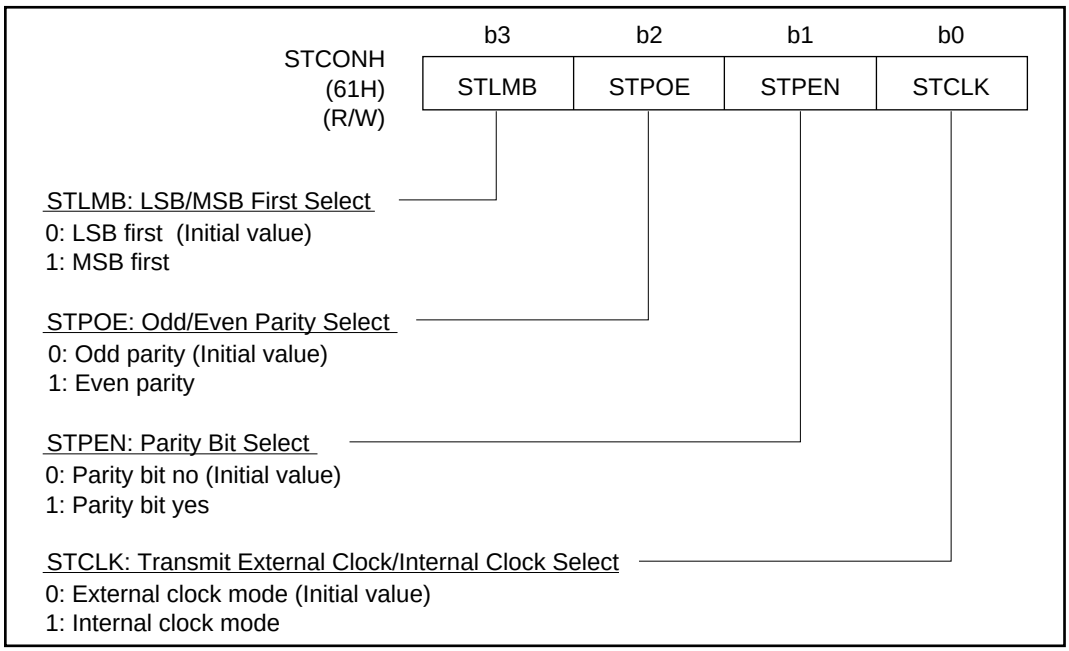


Figure 9-2 (b) Configuration of STCONH

<Description of Each Bit>

(1) STCONL (60H)
- Bit 0: STMOD
  Bit to specify transmit operation mode of serial port.
- Bit 2, 1: SRL0, SRL1
  Bits to specify transmit data length.
- Bit 3: STSTB
  Bit to specify length of stop bit. If bit 0 is "1" (in synchronous mode), bit 3 is meaningless (same operation, whether bit 3 is "0" or "1").

(2) STCONH (61H)
- Bit 0: STCLK
  Bit to specify external clock/internal clock for synchronous mode transmission. If bit 0 of STCONL is "0" (in UART mode), bit 0 of STCONH is meaningless (same operation whether bit 0 is "0" or "1").
- Bit 1: STPEN
  Bit to specify whether parity bit is added/not added.
- Bit 2: STPOE
  Bit to specify whether parity bit is odd/even. If bit 1 is "0", bit 2 is meaningless (same operation, whether bit 2 is "0" or "1").
- Bit 3: STLMB
  Bit to specify transmit direction of transmit data, LSB first/MSB first.

9.3.2 Transmit Buffer Register (STBUFL, STBUFH)

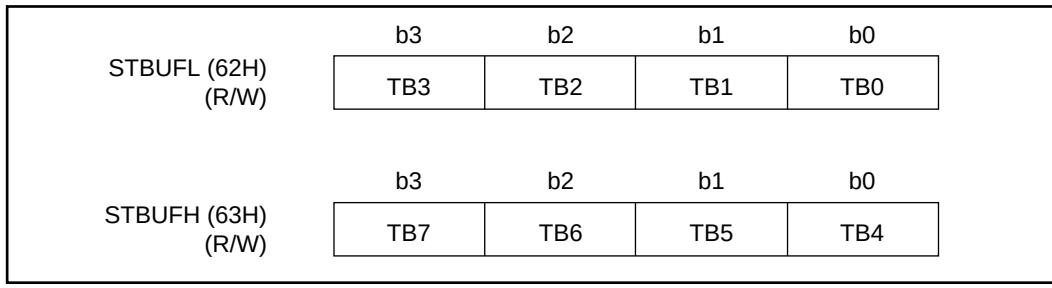


Figure 9-3 Configuration of STBUFL/H

STBUFL and STBUFH are a 4-bit register pair that sets data to transmit during a serial port transmit operation. By the LSB/MSB switch operator, mentioned later, the data transmit direction (LSB first or MSB first) can be changed. STBUFL and STBUFH are assigned to SFR addresses 62H and 63H, and both contents become 0H at system reset.

Since the transmit operation starts when transmit data is set to STBUFH, set the transmit data to STBUFL before that, or by byte writing with STBUFH. Set the baud rate and transmit mode before starting transmit operations.

If the transmit operation has already started when transmit data is set to STBUFH, the transmit of new transmit data is started when the previous transmit operation ends, and an interrupt request signal (STINT) is generated at that time. If an STINT interrupt routine is programmed so that data to transmit next is written to STBUFL and STBUFH, the transmit operation becomes continuous, without any idle time.

9.3.3 Transmit Register

Transmit register is a shift register that performs actual shift operations during transmit operation. The content becomes 00H at system reset. Transmit register cannot be directly accessed from the CPU.

Figure 9-4 shows the transmit operation flow (hardware), explaining transmit data transfer timing from STBUFL/H to transmit register. First transmit mode, baud rate, etc. are set. When transmit data is set to STBUFH, the buffer full flag (BFULL) of the status register (SSTAT) becomes "1", and if the transmit operation is not in progress, the content of STBUFL/H is transferred to the transmit register, and transmit starts. At this time the BFULL flag becomes "0", and the next transmit data can be set to STBUFL/H.

If the previous transmit operation is not yet finished (in transmission), transmit data is held at STBUFL/H until transmit ends. At this time the BFULL flag remains as "1", and when the previous transmit operation ends, transmit data of STBUFL/H is transferred to the transmit register, and transmit starts.

Note: It is possible to set transmit data to STBUFL/H when the BFULL flag is "1", but transmit data previously set and held at STBUFL/H is overwritten and erased. ALWAYS check that the BFULL flag is "0" before setting the next transmit data.

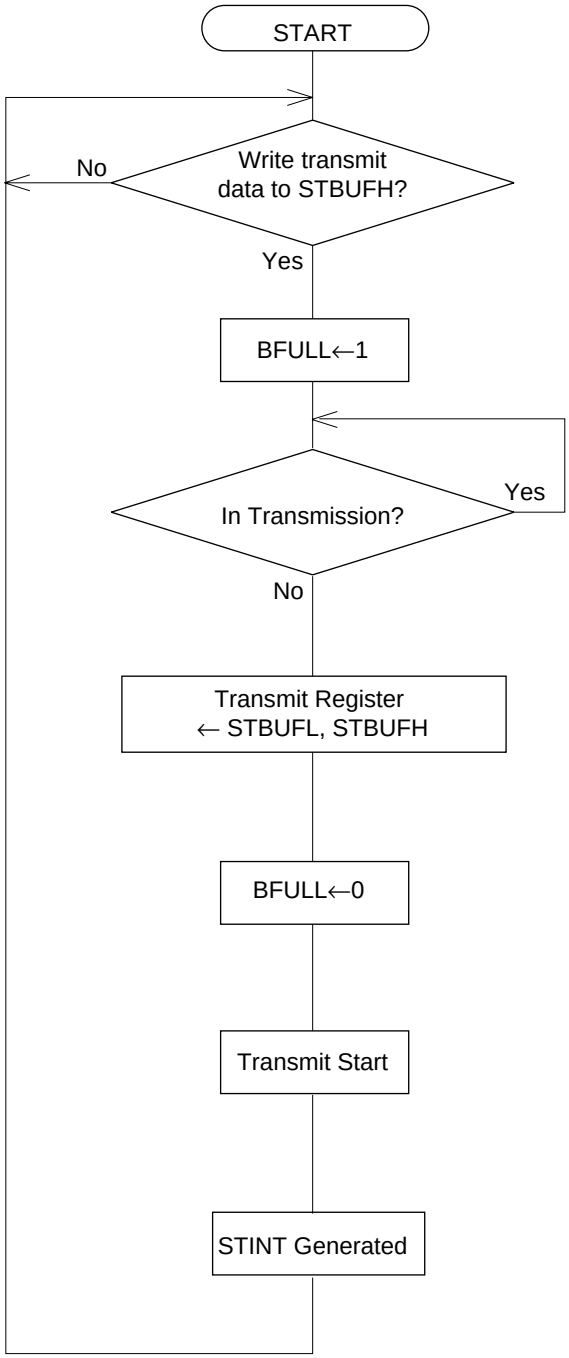


Figure 9-4 Transmit Operation Flow by Hardware

9.3.4 Receive Control Register (SRCONL, SRCONH)

SRCONL and SRCONH are 4-bit registers that control the receive operation of the serial port. SRCONL and SRCONH are assigned to SFR addresses 64H and 65H, and both contents become 0H at system reset.

Figure 9-5 (a) shows the configuration of SRCONL, and Figure 9-5 (b) shows the configuration of SRCONH.

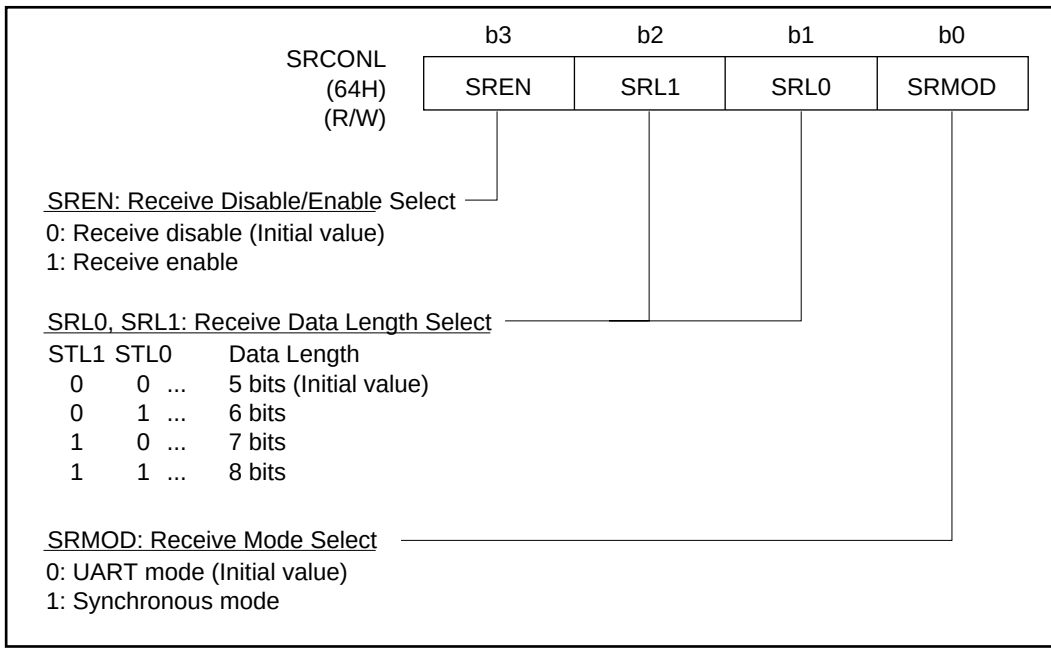


Figure 9-5 (a) Configuration of SRCONL

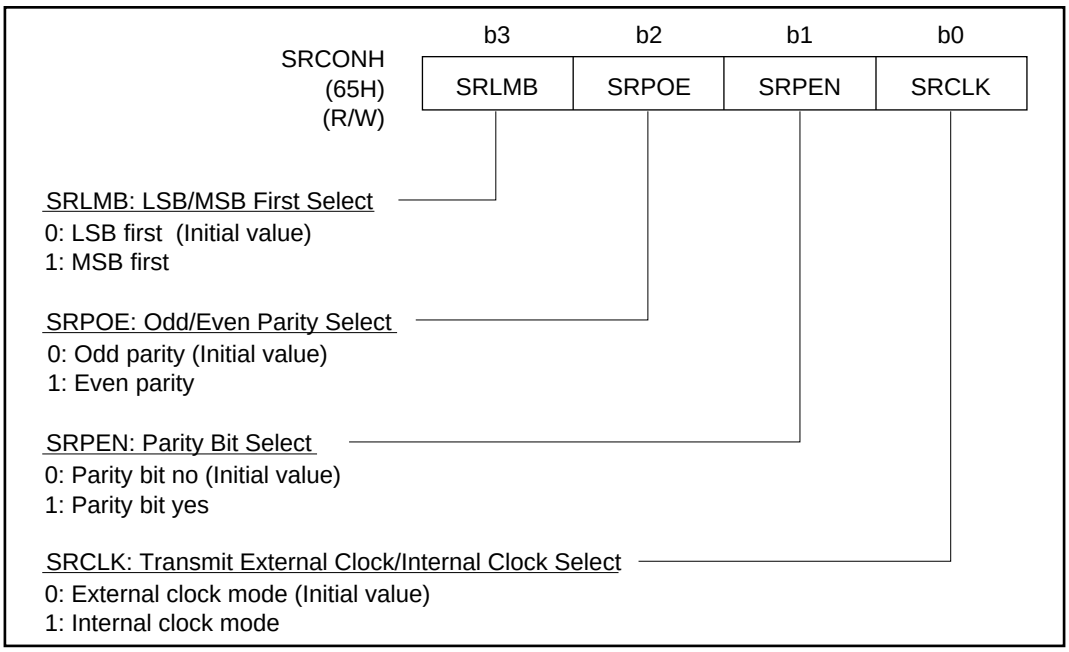


Figure 9-5 (b) Configuration of SRCONH

<Description of Each Bit>

(1) SRCONL (64H)
- Bit 0: SRMOD
  Bit to specify receive operation mode of serial port.
- Bits 2, 1: SRL0, SRL1
  Bits to specify receive data length.
- Bit 3: SREN
  Bit to specify receive operation enable/disable. After receive is enabled, bit 3 becomes "0" if 1 frame of receive data is received in synchronous mode. In UART mode, bit 3 does not change.

(2) SRCONH (65H)
- Bit 0: SRCLK
  Bit to specify external clock/internal clock for synchronous mode receive. If bit 0 of SCRONL is "0" (in UART mode), bit 0 is meaningless (same operation, whether bit 0 is "0" or "1").
- Bit 1: SRPEN
  Bit to specify whether parity bit is added/not added.
- Bit 2: SRPOE
  Bit to specify whether parity bit is odd/even. If bit 1 is "0", bit 2 is meaningless (same operation, whether bit 2 is "0" or "1").
- Bit 3: SRLMB
  Bit to specify receive direction of receive data, LSB first/MSB first.

9.3.5 Receive Register

Receive register is a shift register that performs an actual shift operation during receive operation. The content becomes 00H at system reset. The receive register cannot be directly accessed from the CPU. When a receive operation ends, data in receive register is transferred to SRBUFL/H, and at the same time a receive interrupt request signal (SRINT) is generated.

9.3.6 Receive Buffer Register (SRBUFL, SRBUFH)

Figure 9-6 Configuration of SRBUFL/H

SRBUFL and SRBUFH are a 4-bit register pair that holds data received in serial port receive operations. SRBUFL and SRBUFH are assigned to SFR addresses 66H and 67H, and both contents become 0H at system reset. When a receive operation ends, the content of the receive register is transferred to SRBUFL/H, and at the same time a receive interrupt request signal (SRINT) is generated. The content of SRBUFL/H is held until the next receive operation ends.

An overrun error occurs if previous data has not been read from SRBUFL/H when a receive operation ends. If an overrun error occurs, receive data is not captured to SRBUFL/H.

9.3.7 Receive Baud Rate Setting Register (SRBRT)

SRBRT is a 4-bit special function register that sets the receive baud rate in UART mode during a serial port receive operation. SRBRT is assigned to SFR address 68H, and the value becomes 0CH at system reset. Figure 9-7 shows the configuration of SRBRT.

Figure 9-7 shows Configuration of SRBRT.

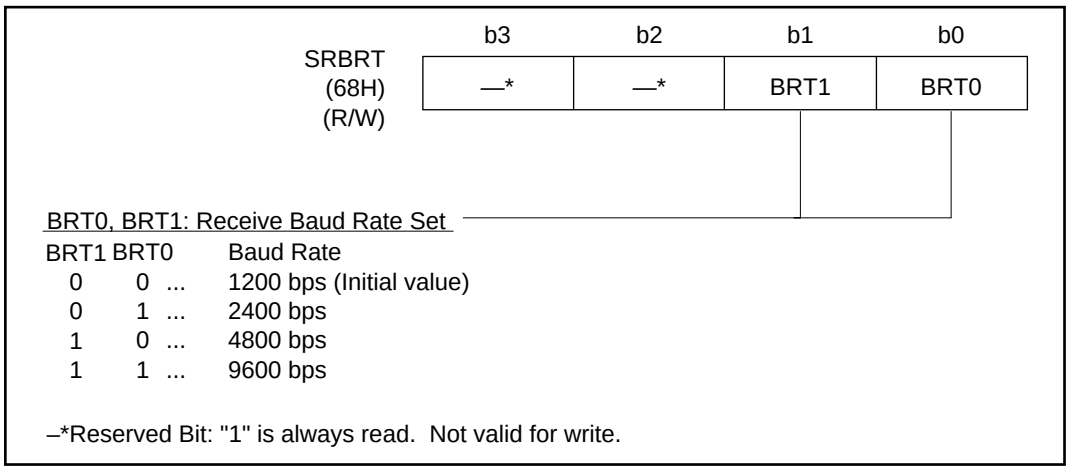


Figure 9-7 Configuration of SRBRT

<Configuration of Each Bit>

(1) SRBRT (68H)
- Bits 1, 0 (BRT0, BRT1)
  Bits to set the receive baud rate.

9.3.8 Serial Status Register (SSTAT)

SSTAT is a 4-bit special function register that indicates status in serial port transmit/receive operations. SSTAT is assigned to SFR address 69H, and the value becomes 0H at system reset. SSTAT is a read only register, and the content is reset everytime it is read.

Figure 9-8 shows the configuration of SSTAT.

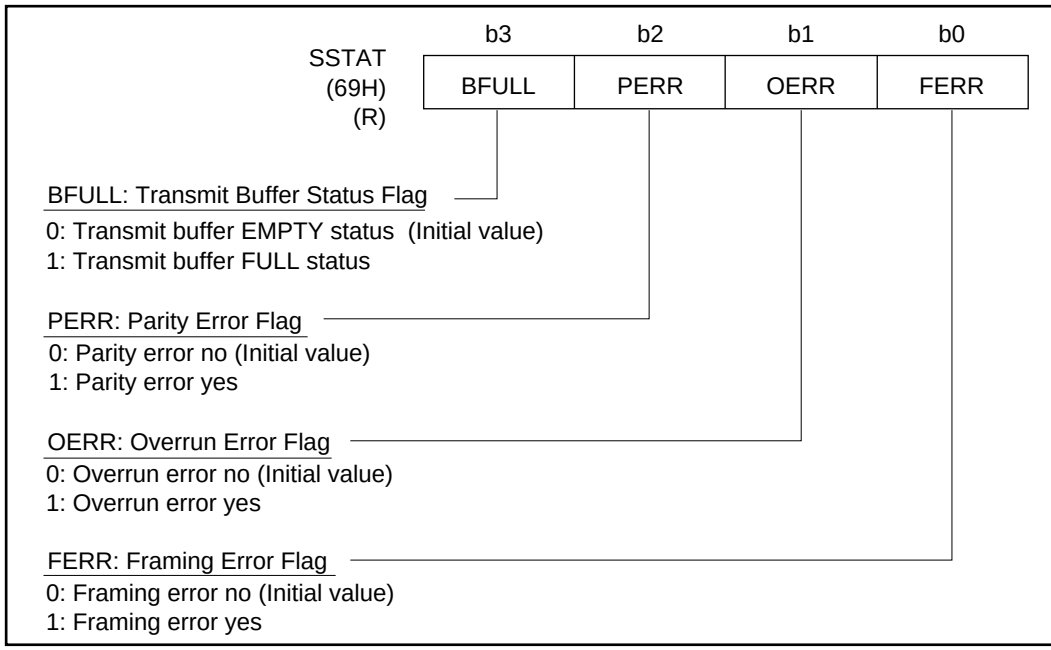


Figure 9-8 Configuration of SSTAT

<Configuration of Each Bit>

(1) SSTAT (69H)

- Bit 0: FERR (Framing Error)
  Bit 0 is valid only in UART mode, and is set ("1") in the following cases.

  (1) When "1" is detected at sampling of start bit,
  (2) When "0" is detected at sampling of stop bit.
  In both cases, a receive interrupt request signal (SRINT) is generated.

- Bit 1: OERR (Overrun Error)
  Bit 1 is valid in both UART and synchronous modes, and is set ("1") when a receive operation ends, and when previously received data has not been read to the CPU. In this case new data is not transferred to SRBUFL/H.

- Bit 2: PERR (Parity Error)
  Bit 2 is valid in both UART and synchronous modes, and is set ("1") when parity of received data and parity bit added to data do not match when compared.

- Bit 3: BFULL (Transmit Buffer Status Flag)
  Bit 3 is valid in both UART and synchronous modes. Bit 3 is set ("1") if transmit data is set (written) to STBUFL/H during a transmit operation, and is reset to "0" if transmit data is transferred to the transmit register.

If transmit data is set (written) to STBUFL/H when the BFULL flag is "1", transmit previously data set to STBUFL/H is overwritten and erased. Always check that the BFULL flag is "0" before setting the next transmit data.

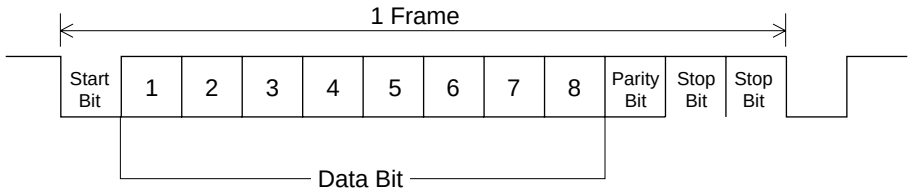
9.4 Operation of Serial Port

9.4.1 Data Format

(1) UART Mode

Figure 9-9 (a) shows the configuration of transmit/receive data frame in UART Mode.

By the setting of SRCONL/H and STCONL/H, the data bit length can be set to 5–8 bits. If parity bit yes is selected, odd/even parity can be set. For stop bit, 1 or 2 bits can be set. By a combination of the above settings, transmit/receive data frame configuration becomes a minimum of 7 bits and a maximum of 12 bits.



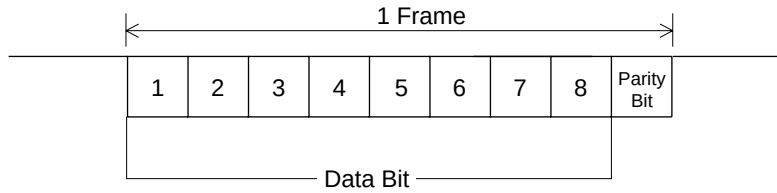
- 1 Frame
  Max.: 12 bits
  Min.: 7 bits
- Data Bit Length: 5–8 bits varialbe
- Parity Bit: Yes/No selectable
  Odd/Even parity selectable
- Stop Bit: 1/2 stop bits selectable

Figure 9-9 (a) Configuration of Transmit/Receive Data Frame in UART Mode

(2) Synchronous Mode

Figure 9-9 (b) shows the configuration of transmit/receive data frame in Synchronous Mode.

By setting SRCONL/H and STCONL/H, the data bit length can be set to 5–8 bits. If parity bit yes is selected, odd/even parity can be set. By a combination of the above settings, transmit/receive data frame configuration becomes a minimum of 5 bits and a maximum of 9 bits.



- 1 Frame
  Max.: 9 bits
  Min.: 5 bits
- Data Bit Length: 5–8 bits varialbe
- Parity Bit: Yes/No selectable
  Odd/Even parity selectable
- Stop Bit: 1/2 stop bits selectable

Figure 9-9 (b) Configuration of Transmit/Receive Data Frame in Synchronous Mode

9.4.2 Transmit Operation

Since the serial port transmit circuit has a transmit register and transmit buffer register (STBUFL/H), the next data can be set to STBUFL/H during transmit. However, if the BFULL flag of the serial status flag (SSTAT) is "1", transmit data at STBUFL/H is not yet transferred to the transmit register. Always check that the BFULL flag is "0" before writing new transmit data.

(1) UART Mode

UART mode is specified when bit 0 of STCONL is set to "0". Figure 9-10 shows the transmit timing chart in UART mode.

The transmit procedure in UART mode is shown below.

Determine the transmit baud rate, set the timer (see Chapter 8. Timer (TM)), and set the transmit format (data bit length, parity bit yes/no, etc.) at STCONL and STCONH. A TMINT signal supplied from the timer becomes the baud rate clock.

A. Set the transmit data at STBUFL/H.

B. The transmit data from STBUFL/H is transferred to the transmit register, and transmit operation starts. A serial port transmit interrupt request signal (STINT) is generated at the same time.

C. Check that BFULL = "0", and set the next transmit data at STBUFL/H.

D. If the transmit operation ended, the next transmit data set at STBULF/H is transferred to the transmit register, and transmit operation starts. A serial port transmit interrupt request signal (STINT) is generated at the same time.

Hereafter repeat step "C" as many times as necessary.

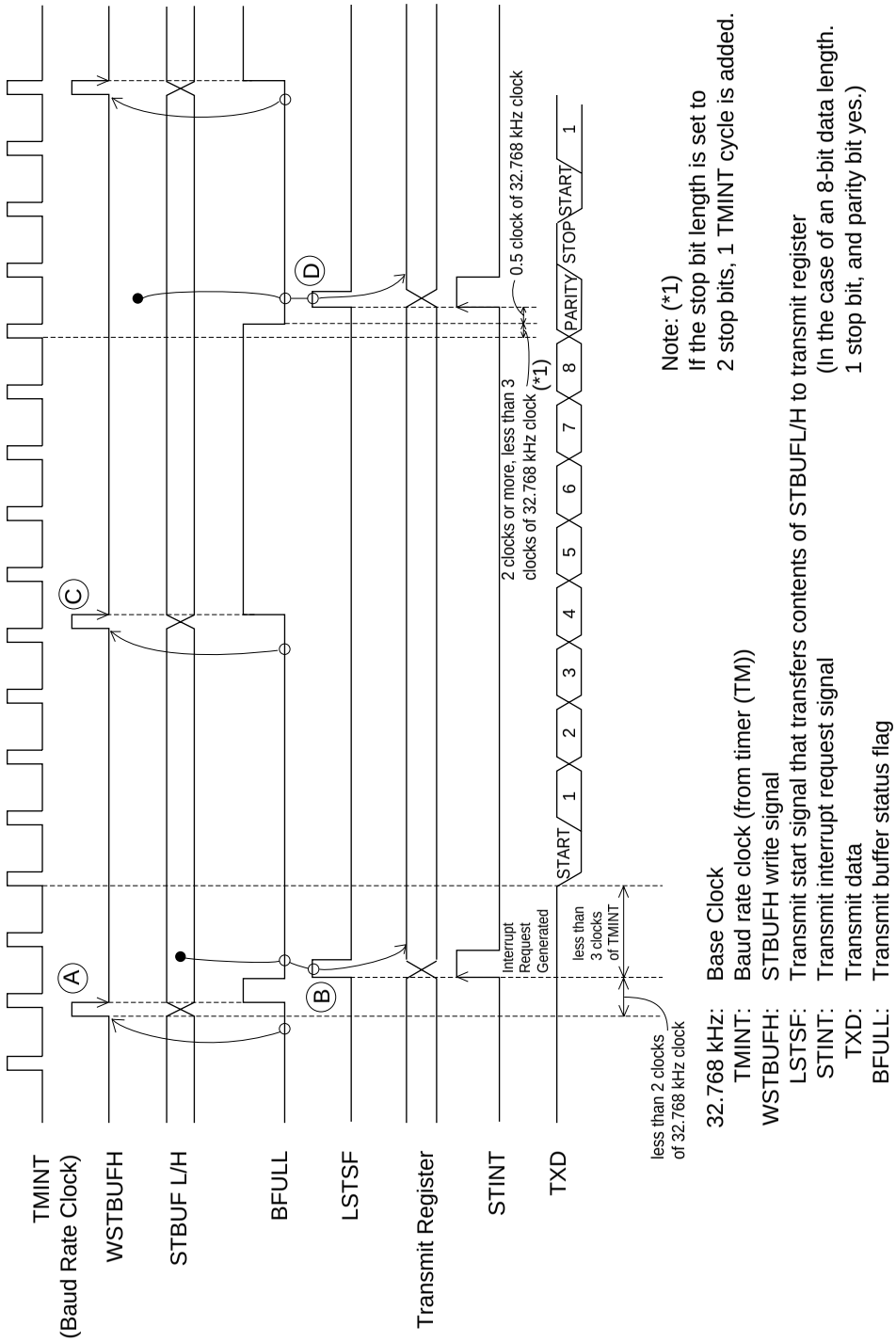


Figure 9-10 Transmit Timing Chart in UART Mode

(2) Synchronous Internal Clock Mode

Synchronous internal clock mode is specified when bit 0 of STCONL is set to "1", and bit 0 of STCONH to "1". Figure 9-11 shows the transmit timing chart in synchronous internal clock mode. The transmit procedure in synchronous internal clock mode is shown below.

Set the transmit format (data bit length, parity bit yes/no, etc.) at STCONL and STCONH.

A. Set the transmit data at STBUFL/H.

B. The transmit data from STBUFL/H is transferred to the transmit register, and transmit operation starts. A serial port transmit interrupt request signal (STINT) is generated at the same time.

C. Check that BFULL = "0", and set the next transmit data at STBUFL/H.

D. If the transmit operation ended, the next transmit data set at STBUFL/H is transferred to the transmit register, and transmit operation starts. A serial port transmit interrupt request signal (STINT) is generated at the same time.

   Hereafter, repeat step "C" as many times as necessary.

In synchronous internal clock mode, the transmit baud rate is fixed to 32.768 kHz. If the transmit data is set at STBUFH, the transmit clock (TXCO) is generated from that point for 2 or more clocks, and 3.5 or less clocks of 32.768 kHz, and transmit starts.

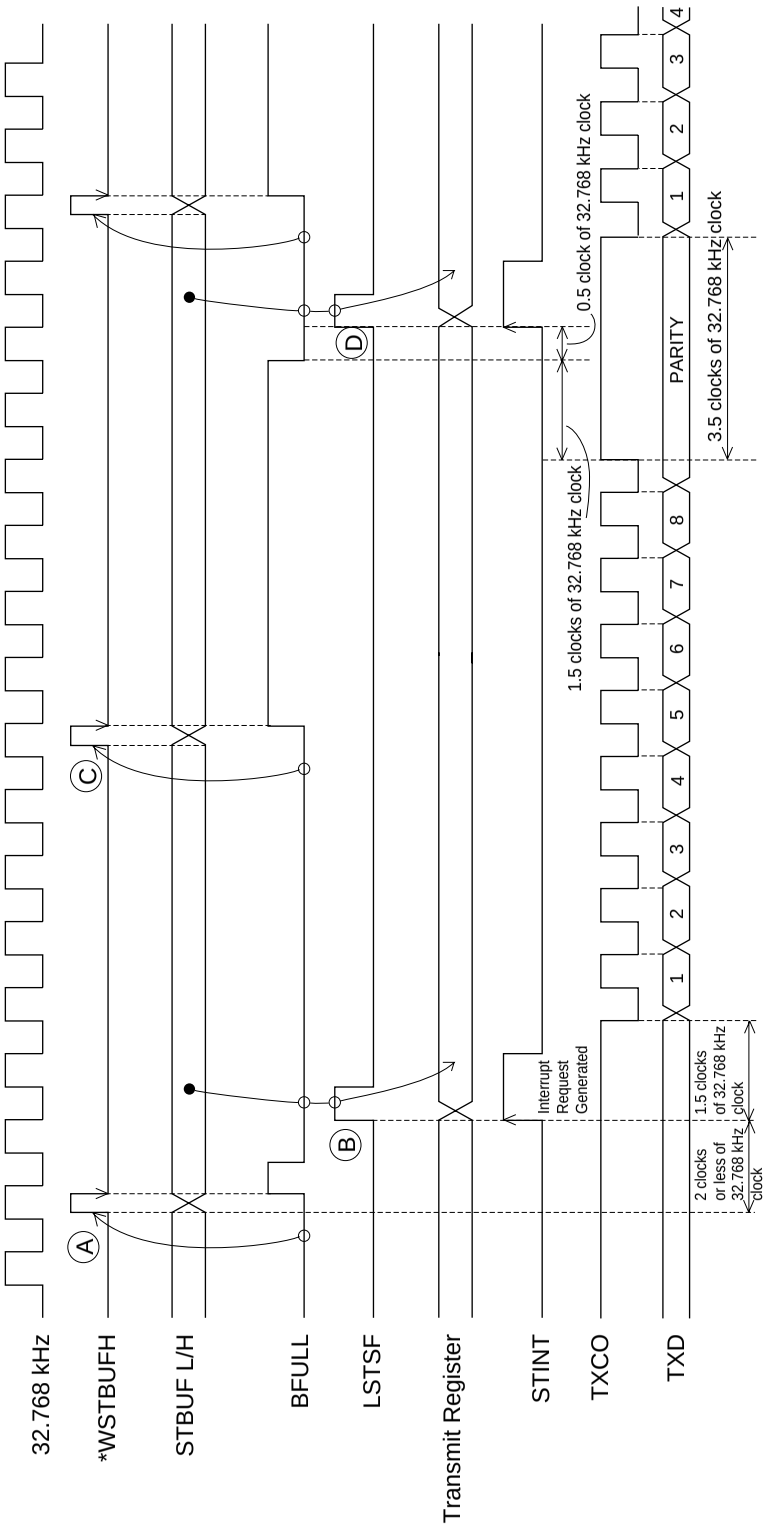


Figure 9-11 Transmit Timing Chart in Synchronous Internal Clock Mode

(3) Synchronous External Clock Mode

A synchronous external clock mode is specified when bit 0 of STCONL is set to "1", and bit 0 of STCONH to "0". Figure 9-12 shows the transmit timing chart in synchronous external clock mode. The transmit procedure in synchronous external clock mode is shown below.

Set the transmit format (data bit length, parity bit yes/no, etc.) at STCONL and STCONH.

A. Set the transmit data at STBUFL/H.

B. The transmit data from STBUFL/H is transferred to the transmit register. A serial port transmit interrupt request signal (STINT) is generated at the same time.

C. Transmit operation starts from the transmit shift clock (TXCI).

D. Check that BFULL = "0", and set the next transmit data at STBUFL/H.

E. If the transmit operation ended, the next transmit data set at STBUFL/H is transferred to the transmit register. A serial port transmit interrupt request signal (STINT) is generated at the same time.

Hereafter repeat step "D" as many times as necessary.

The transmit baud rate in synchronous external clock mode is determined by the input shift clock (TXCI).

If data is continuously transmitted, keep an interval of at least 3.5 clocks (about 107 μs) of 32.768 kHz clock for one frame of clocked (TXCI) transmit data.

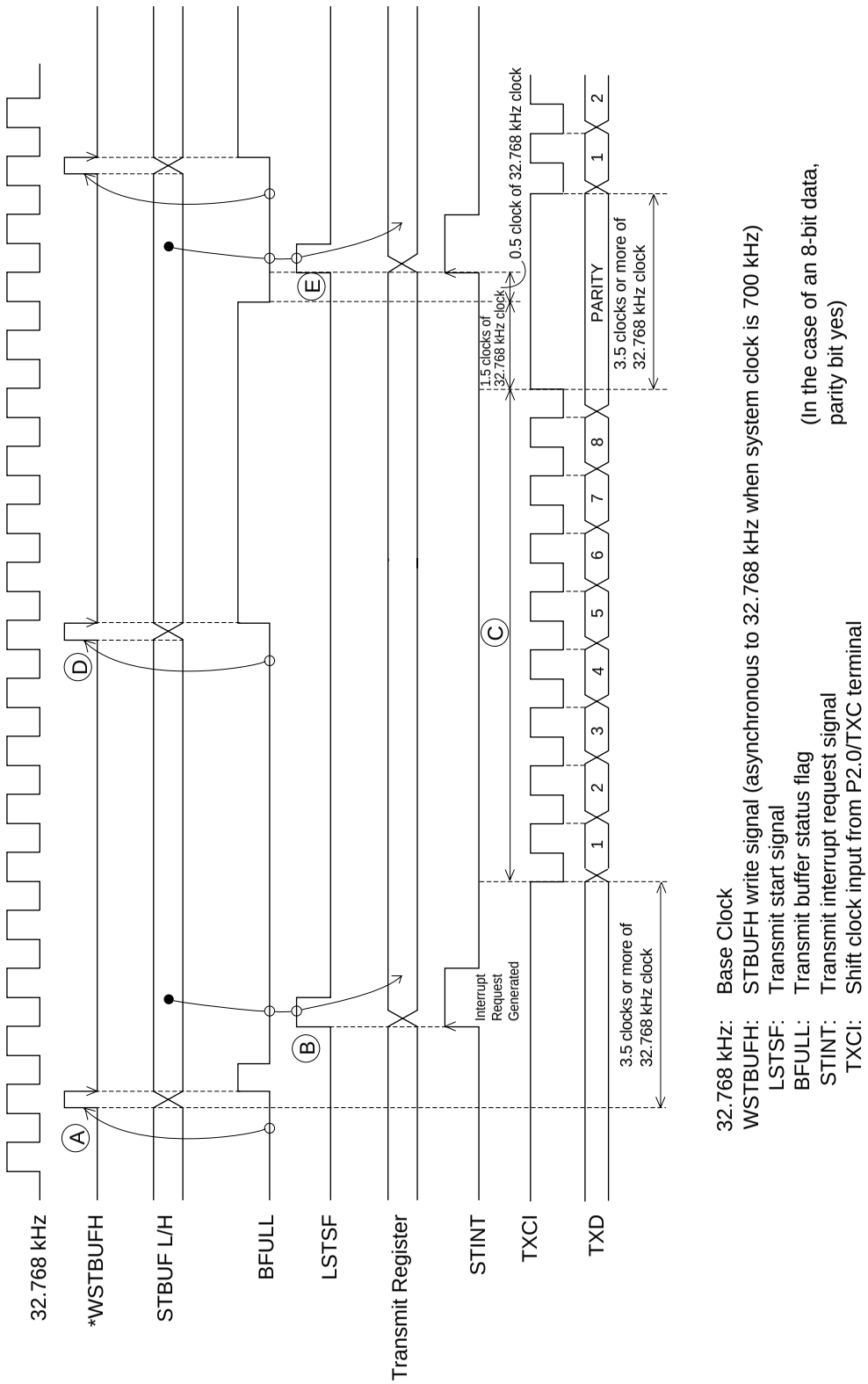


Figure 9-12 Transmit Timing Chart in Synchronous External Clock Mode

9.4.3 Receive Operation

(1) UART Mode

UART mode is specified when bit 0 of SRCONL is set to "0". Figure 9-13 shows the receive timing chart in UART mode.

The receive procedure in UART mode is shown below.

Set the receive baud rate to the receive baud rate setting register (SRBRT). The receivable baud rates in UART mode are 9600 bps, 4800 bps, 2400 bps, and 1200 bps.

Set the receive format (data bit length, parity bit yes/no, etc.) to SRCONL and SRCONH. A TMINT signal supplied from the timer becomes the baud rate clock.

A. Set the receive enable/disable flag (SREN) of the 3rd bit of SRCONL to "1" (receive enable).

B. Receive operation starts at the fall of the start bit of receive data (RXD).

C. Receive operation ends. If a framing error or an overrun error occurs, an FERR flag or OERR flag of the status register (SSTAT) is set ("1").

D. Received data is transferred to SRBUFL/H. If a parity error occurs, a PERR flag of the status register (SSTAT) is set ("1").

E. A serial port receive interrupt request signal (SRINT) is generated.

Receive data is received during a receive operation until the status changes to receive disable (SREN = "0"). To end receiving, reset ("0") the receive enable/disable flag (SREN).

Since the sampling clock (SRSMPL) of receive data is generated based on 32.768 kHz, without 700 kHz, a receive operation can be performed while low power consumption is maintained.

Take care that an overrun error does not occur while receiving data of two or more frames successively. Switch the system clock to its high-speed mode immediately upon receiving such data.

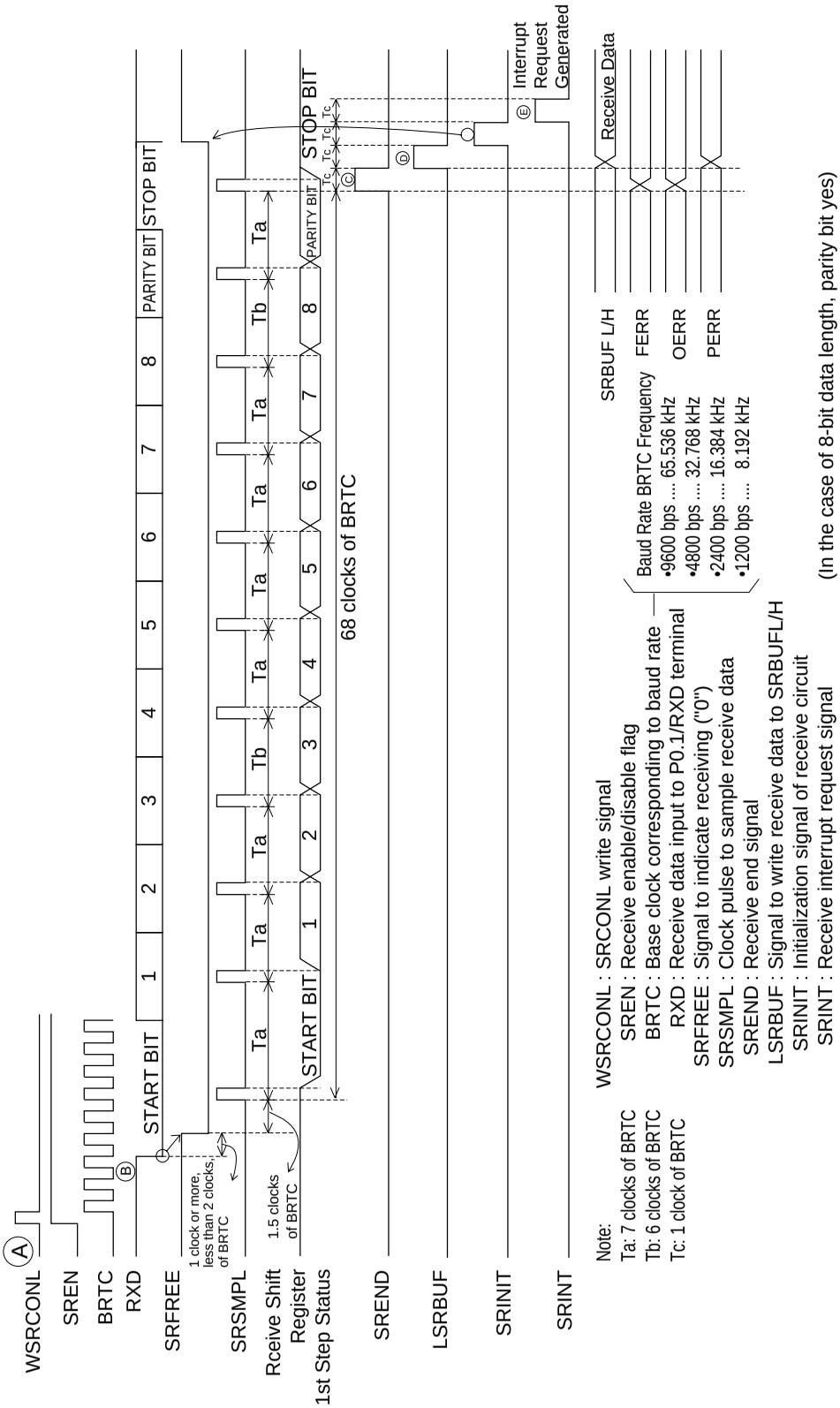


Figure 9-13 Receive Timing Chart in UART Mode

(2) Synchronous Internal Clock Mode

The synchronous internal clock mode is specified when bit 0 of SRCONL is set to "1", and bit 0 of SRCONH to "1".

Figure 9-14 shows the receive timing chart in synchronous internal clock mode.

The receive procedure in synchronous internal clock mode is shown below.

Set the receive format (data bit length, parity bit yes/no, etc.) at SRCONL and SRCONH.

A. Set the receive enable/disable flag (SREN) at the 3rd bit of SRCONL to "1" (receive enable).

B. A receive shift clock (RXCO) is generated at the 3 to 4 clocks of BRTC after the point A., and receive operation starts. (Shift clock is output from P2.1/RXC terminal)

C. Receive data input from P0.1/RXD terminal at the rise of RXCO is captured to the receive register.

D. Receive operation ends. If an overrun error occurs, the OERR flag of the status register (SSTAT) is set ("1").

E. Received data is transferred to SRBUFL/H. If a parity error occurs, a PERR flag of the status register (SSTAT) is set ("1").

F. A serial port receive interrupt request signal (SRINT) is generated.

G. SREN is reset ("0") at the fall of SRINT.

Hereafter, repeat step "A" as many times as necessary.

In synchronous internal clock mode, the receive baud rate is fixed to 32.768 kHz.

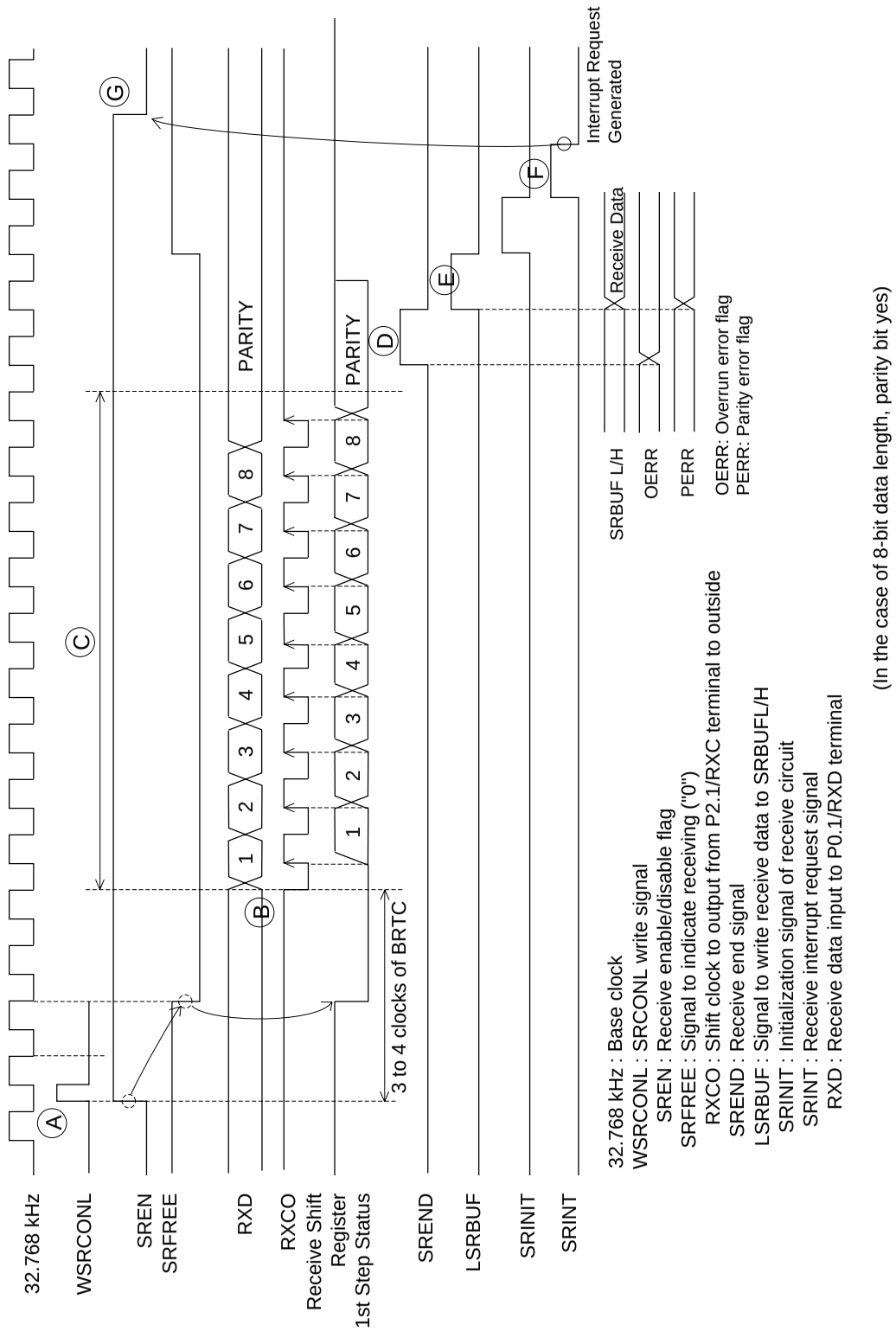


Figure 9-14 Receive Timing Chart in Synchronous Internal Clock Mode

(3) Synchronous External Clock Mode

Synchronous external clock mode is specified when bit 0 of SRCONL is set to "1", and bit 0 of SRCONH to "0".

Figure 9-15 shows the receive timing chart in synchronous external clock mode.

The receive procedure in synchronous external clock mode is shown below.

Set the receive format (data bit length, parity bit yes/no, etc.) at SRCONL and SRCONH.

A. Set the receive enable/disable flag (SREN) at the 3rd bit of SRCONL to "1" (receive enable).

B. Receive data input from P0.1/RXD terminal is captured to the receive register at the rise of the receive shift clock input from P2.1/RXC terminal.

C. Receive operation ends. If an overrun error occurs, the OERR flag of the status register (SSTAT) is set ("1").

D. Received data is transferred to SRBUFL/H. If a parity error occurs, the PERR flag of the status register (SSTAT) is set ("1").

E. An interrupt request signal (SRINT) is generated.

F. SREN is reset ("0") at the fall of SRINT.

Hereafter, repeat step "A" as many times as necessary.

For synchronous external clock receive, the baud rate can be set to any value by the external clock (RXCI), but take an interval for the five clocks (about 153 µs) of 32.768 kHz from where receive is enabled (SREN = "1") to where the external clock (RXCI) is input.

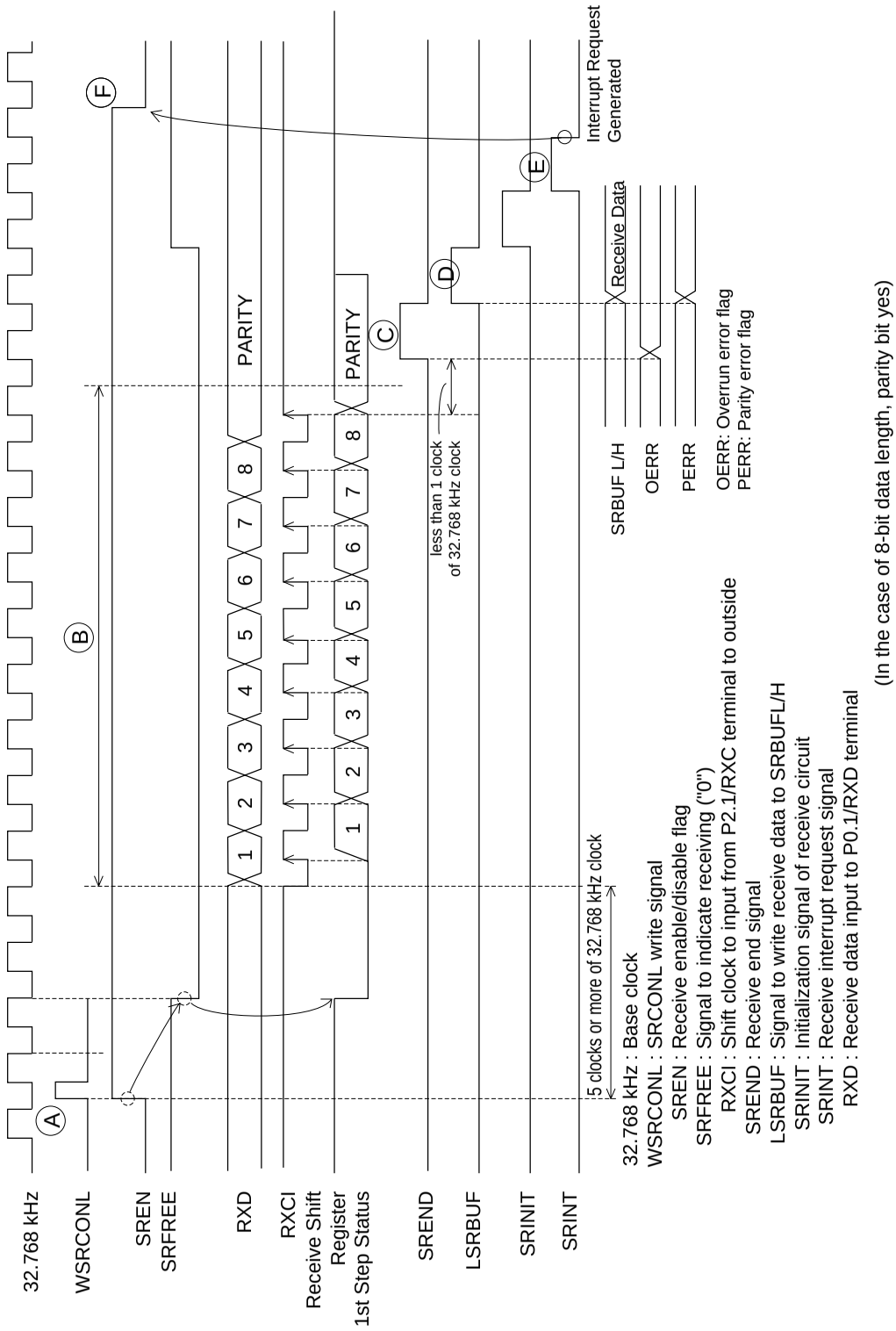


Figure 9-15 Receive Timing Chart in Synchronous External Clock Mode

9.5 LSB First/MSB First Switching of Transmit/Receive Data

LSB first/MSB first transmit can be switched by the setting of bit 3 (STLMB) of STCONH. LSB first/ MSB first receive can be switched by the setting of bit 3 (SRLMB) of SRCONH.

9.5.1 LSB First/MSB First Switching of Transmit Data

Figure 9-16 shows the content of the transmit buffer register (STBUFL/H).

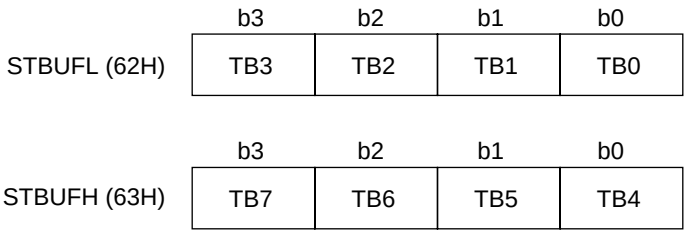


Figure 9-16 STBUFL/H

If bit 3 (STLMB) of STCONH is set to "0", data transmits with LSB firstly.

Figure 9-17 shows the correspondence between LSB first transmit data and each transmit buffer register bit. In this case, LSB is bit 0 (TB0) of STBUFL.

If STLMB is set to "1", data is transmits MSB firstly. Figure 9-18 shows the correspondence between MSB first transmit data and each transmit buffer register bit. In this case, MSB is bit 3 (TB7) of STBUFH.

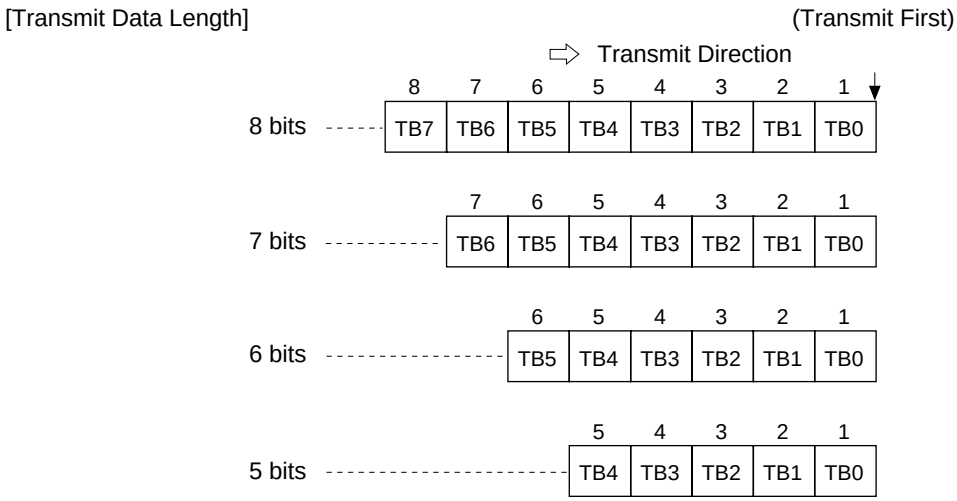


Figure 9-17 Correspondence between LSB First Transmit Data and Each Transmit Buffer Register Bit

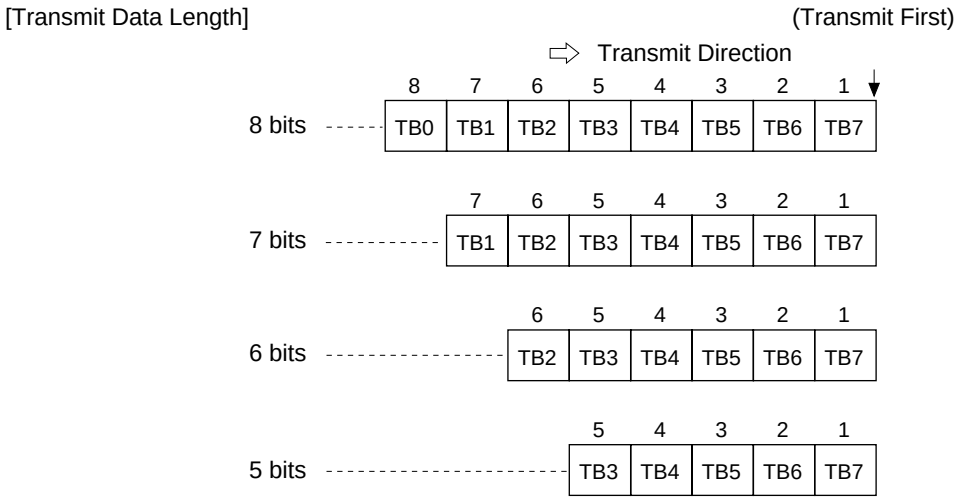


Figure 9-18 Correspondence between MSB First Transmit Data and Each Transmit Buffer Register Bit

9.5.2 LSB First/MSB First Switching of Receive Data

Figure 9-19 shows the content of the receive buffer register (SRBUFL/H).

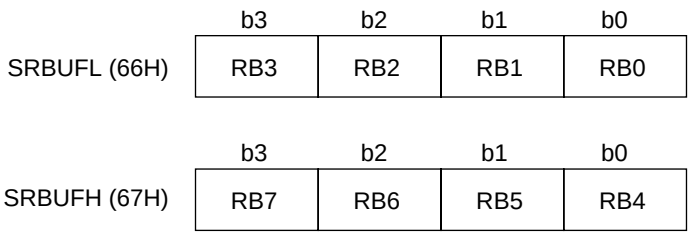


Figure 9-19 SRBUFL/H

If receive data is LSB first, data is received with the 3rd bit (SRLMB) of SRCONH as "0" (LSB first receive). If receive data is MSB first, data is received with SRLMB as "1" (MSB first receive).

Figure 9-20 shows the correspondence between LSB first receive data and each bit of SRBUFL/H.

Figure 9-21 shows the correspondence between MSB first receive data and each bit of SRBUFL/H.

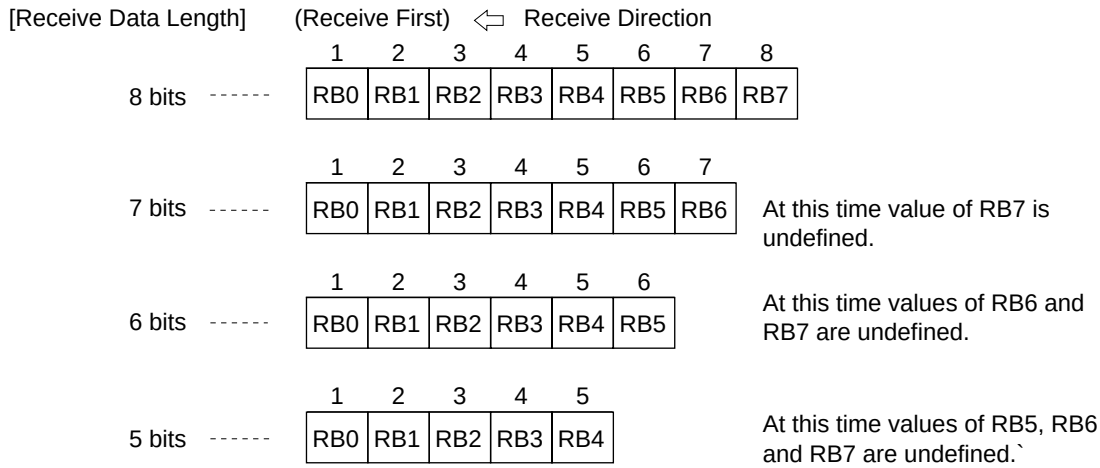


Figure 9-20 Correspondence between LSB First Receive Data and Each Receive Buffer Register Bit

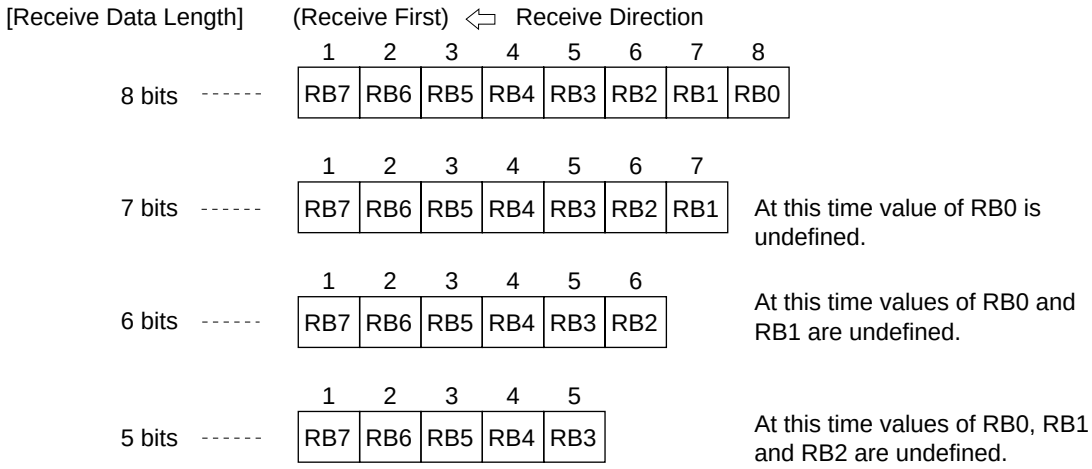


Figure 9-21 Correspondence between MSB First Receive Data and Each Receive Buffer Register Bit

Note:

1. To prevent an overrun error in the UART receive baud rate of 9,600 bps, be sure to set the receive data bit length to 8 bits and proceed as follows. (If the receive data bit length of 5 to 7 bits is selected, reception may fail.)

① Set the port P0.1 (RXD) to the external interrupt (XI0INT) enable and to the system clock sampling.

② Input the jump instruction to the jump address 038H of the external interrupt (XI0INT) of the port P0.1 (RXD).

③ Set at the jump address as follows.

VSSLH = 1 : Set VSSL = VSS2.
CPUCLK = 1: Set the system clock to 700 kHz.
EXI0 = 0 : Inhibit the external interrupt (XI0INT).
RTI : Return processing

④ Perform receive process with the receive interrupt (SRINT). Note that the receive data of the SRBOF L/H should be made first before making the setting so that the receive process can be ended within the period of one frame of the receive data.

Then, continue receiving with the receive interrupt.

Figure 9-22 shows a flow diagram illustrating the UART reception. Figure 9-23 shows a timing chart illustrating the UART reception.

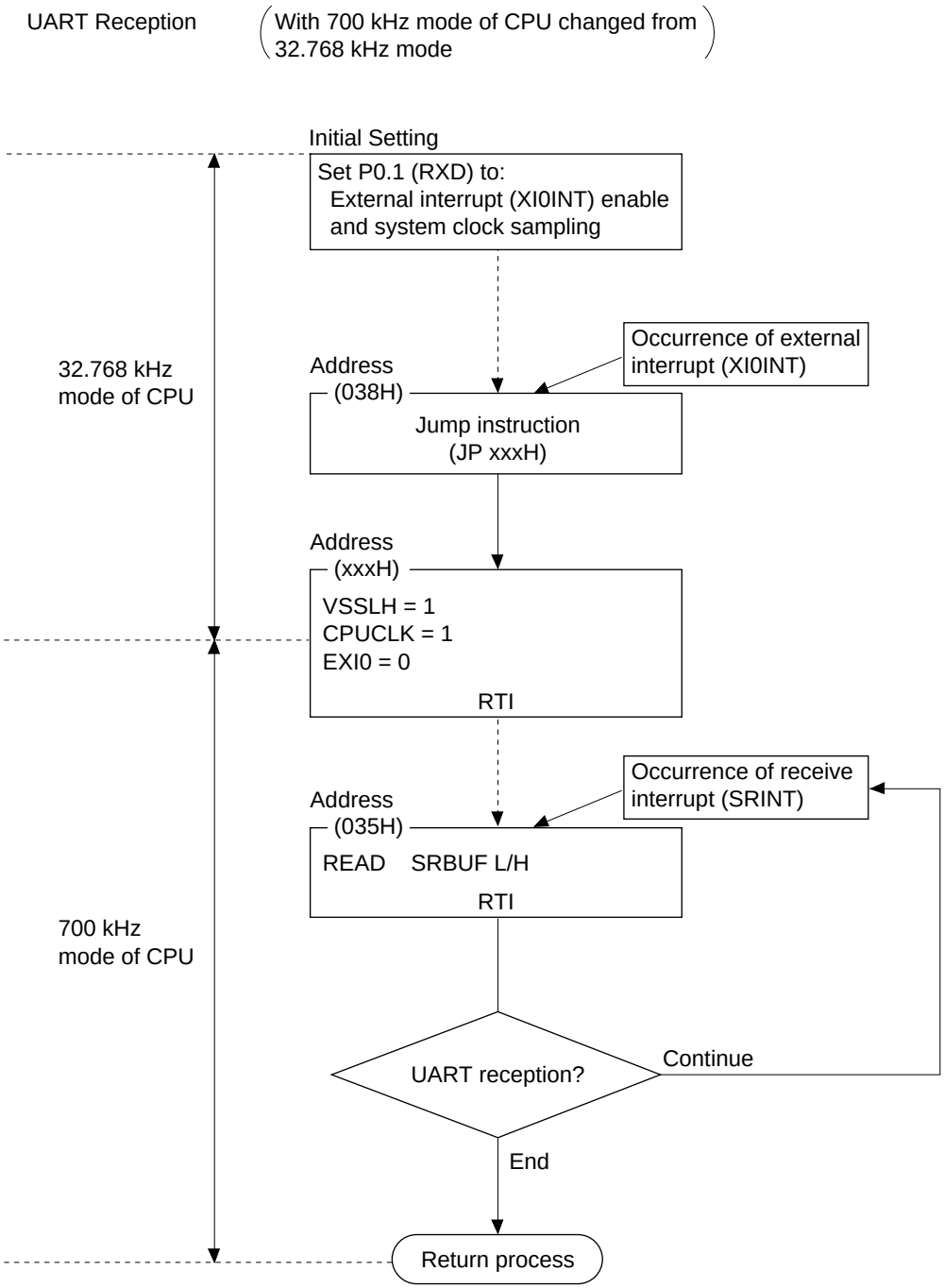


Figure 9-22 Flow Diagram for the UART Reception to Change the CPU Clock to 700 kHz

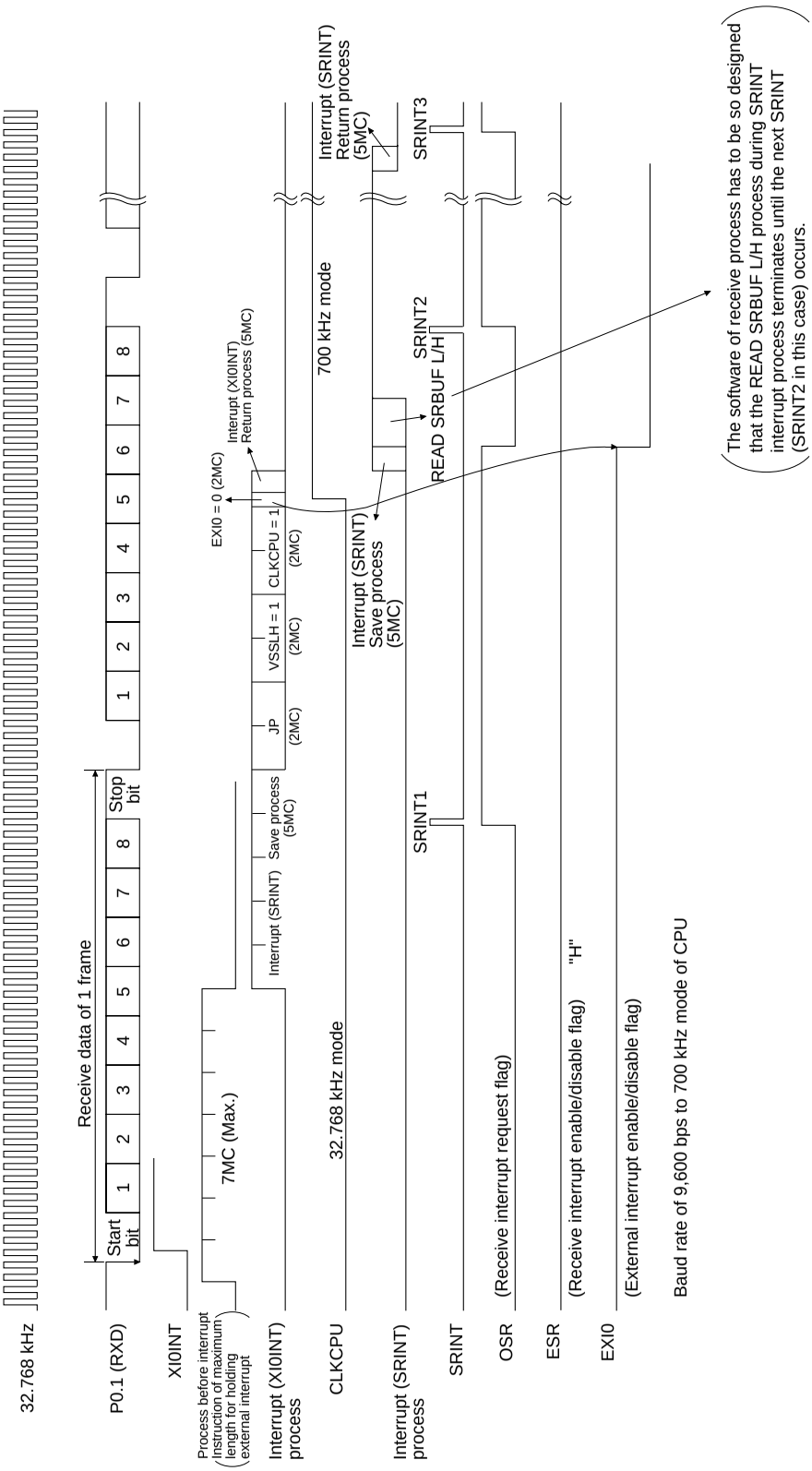


Figure 9-23 Timing Chart for the UART Reception to Change the System Clock to 700 kHz

2. Care should be taken in the UART reception with the system clock fixed at 32.768 kHz as follows.

   Table 9-3 shows a process machine cycle (MC) margin at the system clock of 32.768 kHz for the bit lengths of one receive frame (*) at the baud rates.

   Set a baud rate and bit lengths of one receive frame available in connection with the number of process machine cycles needed by software according to the table.

Table 9-3 Process Machine Cycle Margin at the CPU Clock of 32 kHz at the Baud Rates

Bit length of one receive frame / Baud rate	7 bits	8 bits	9 bits	10 bits	11 bits	12 bits
4800 bps	15MC	18MC	20MC	22MC	25MC	27MC
2400 bps	31MC	36MC	40MC	45MC	50MC	54MC
1200 bps	63MC	72MC	81MC	91MC	100MC	109MC

* Bit lengths of one receive frame = Start bit (1 bit) + data bit (5 to 8 bits) + parity bit (0 to 1 bit) + stop bit (1 to 2 bits).

For example, if an application needs 41MC (machine cycle) for "interrupt process + data process + return process" after occurrence of the receive interrupt (SRINT), reception can be made up to 10-bit length of one receive frame at the baud rate of 2,400 bps.

In the above example, to have receive data of 12-bit length of one receive frame at 4,800 bps baud rate, the system clock has to be switched to the 700 kHz mode right after the start of reception. This is similar to the selection of 9,600 bps baud rate. Note that the reception cannot be made with the system clock fixed 32.768 kHz.

Chapter 10

Buzzer Driver (BD)

Chapter 10 Buzzer Driver (BD)

10.1 Overview

The MSM64167E has a built-in buzzer driver that has 2 types of buzzer output frequencies and 4 types of buzzer output modes. Buzzer output is specified by the buzzer control register (BDCON) and the buzzer frequency control register (BFCON).

10.2 Configuration of Buzzer Driver

Figure 10-1 shows the configuration of the buzzer driver.

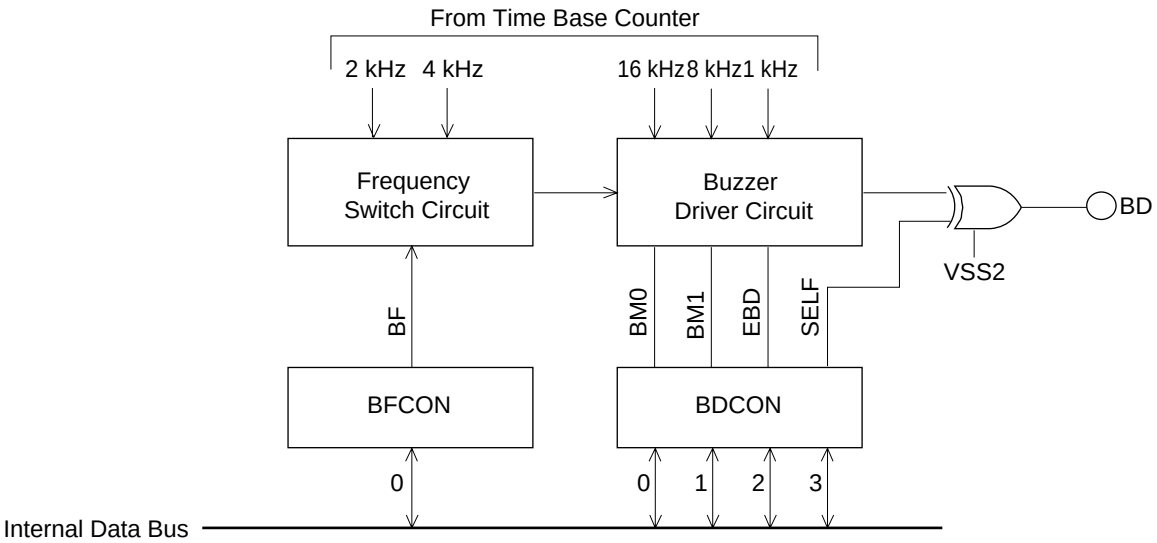


Figure 10-1 Configuration of Buzzer Driver

10.3 Operation of Buzzer Driver

If bit 2 (EBD) of buzzer control register (BDCON) is set to "1", a buzzer drive signal is output to the buzzer driver pin. For buzzer output frequency, either 4 kHz or 2 kHz can be selected by the buzzer frequency control register (BFCON). For buzzer output mode, 2 types of intermittent sound, single sound and continuous sound, totaling 4 types, can be selected by bit 1/0 (BM1/BM0) of buzzer control register (BDCON). Also the output logic of the BD pin can be selected by bit 3 (SELF) of BDCON. If SELF bit is reset to "0", positive logic output ("L" level output during output stop) is selected, and if set to "1", negative logic output ("H" level output during output stop) is selected. The buzzer output frequency signal has a 50% duty.

In intermittent sound 1 mode, a wave form synchronizing an 8 Hz output of the time base counter is output. In intermittent sound 2 mode, a wave form synchronizing the logical product signal of an 8 Hz and $\overline{1\ Hz}$ output of the time base counter is output. In single sound mode, output starts synchronizing to the rise of EBD, and stops at the fall of the 16 Hz output of the time base counter. In continuous sound mode, output continues while EBD is "1".

Figure 10-2 shows the output waveform in each output mode. The shaded portion of Figure 10-2 indicates the output frequency signal of each buzzer.

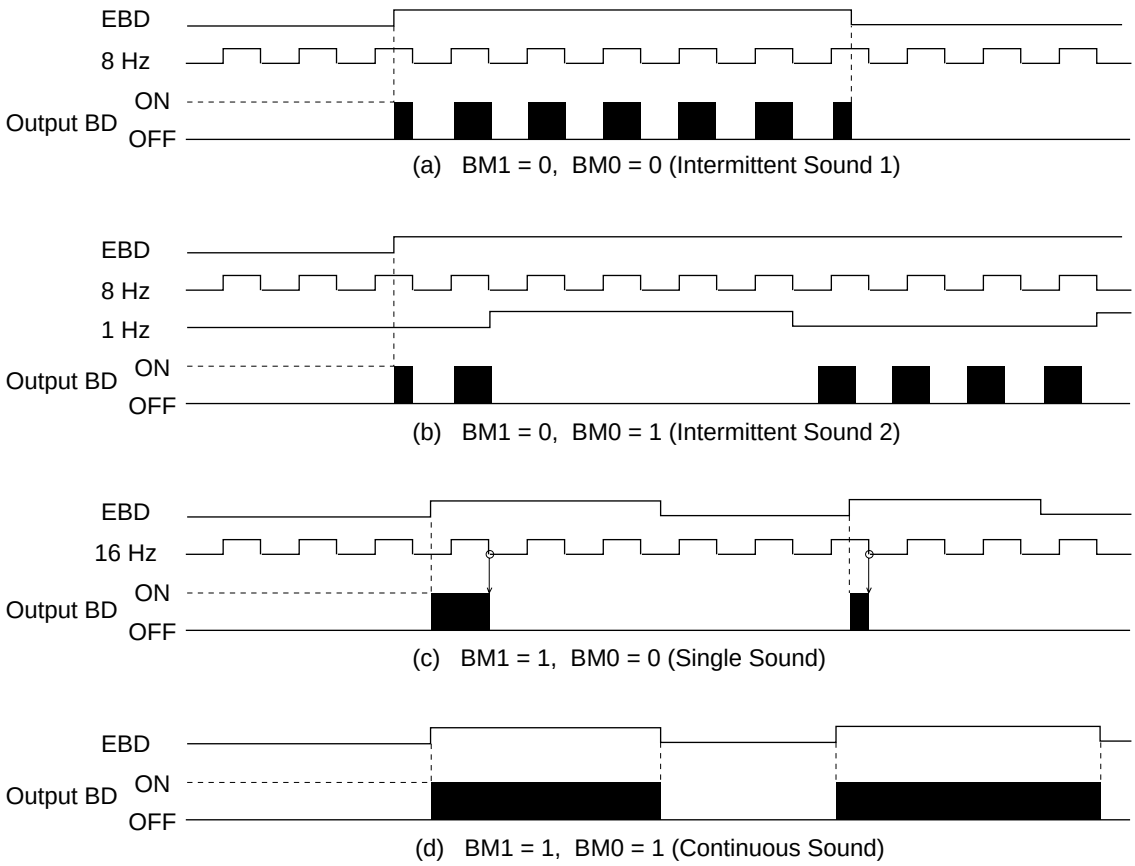
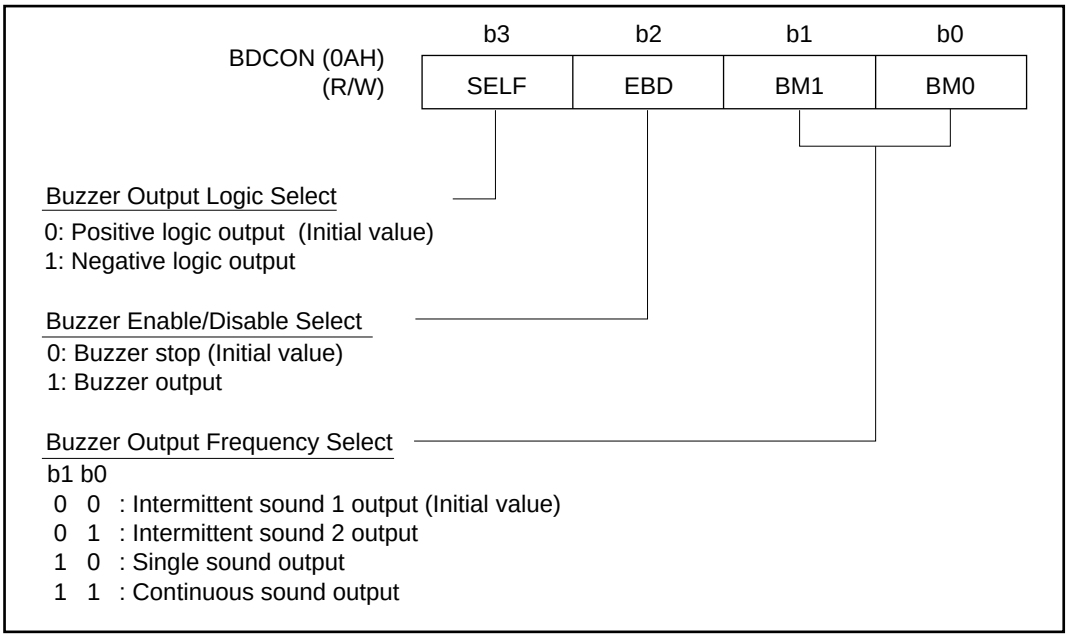


Figure 10-2 Buzzer Driver Output Waveform in Each Output Mode

10.4 Buzzer Driver-Related Registers

(1) Buzzer Control Register (BDCON)

Buzzer control register (BDCON) is a 4-bit special function register (SFR) that controls the output logic of the BD pin, 4 types of buzzer output modes, and buzzer output ON/OFF.



Bit 3: SELF

Bit to select the output logic of BD pin. If bit 3 is reset to "0", positive logic output ("L" level output during output stop) is selected, and if bits 3 is set to "1", negative logic output ("H" level output during output stop) is selected. Bit 3 is reset to "0", and positive logic output is selected at system reset.

Bit 2: EBD

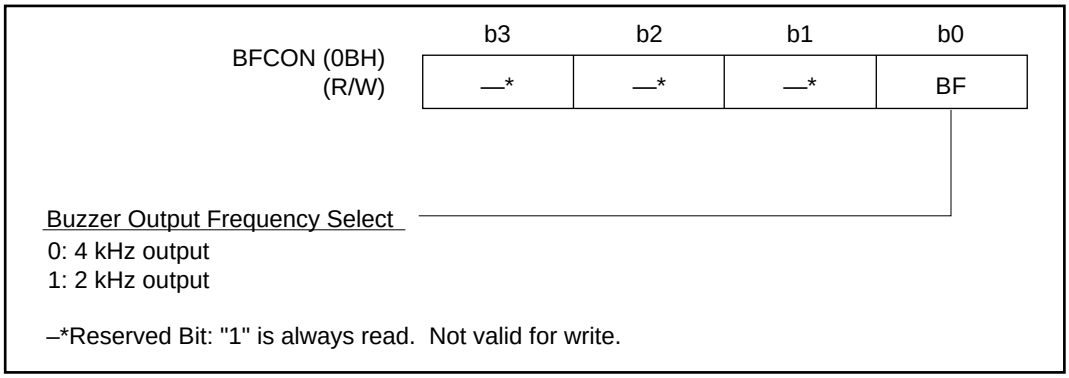
Bit to select buzzer driver output ON/OFF. Bit 2 is reset to "0" and buzzer is not output at system reset.

Bits 1, 0: BM1, BM0

Bits to select output mode of buzzer driver. Intermittent sounds 1, 2, single sound and continuous sound output can be selected. BM1 and BM0 are reset to "0", and intermittent sound 1 output is selected at system reset.

(2) Buzzer Frequency Control Register (BFCON)

Buzzer frequency control register (BFCON) is a 4-bit special function register (SFR) that controls buzzer output frequency.



Bit 0: BF

Bit to select buzzer output frequency. Bit 0 is reset to "0" and 4 kHz output is selected at system reset.

Each output frequency is output with a 50% duty.

Tables 10-1 and 10-2 show buzzer driver-related registers and related pins.

Table 10-1 Buzzer Driver-Related Registers

Register Name	Symbol	Address	Read/Write	Value at System Reset
Buzzer Driver Control Register	BDCON	0AH	R/W	0H
Buzzer Frequency Control Register	BFCON	0BH	R/W	0EH

Table 10-2 Buzzer Driver-Related Pins

Pin Name	Pin No.		Pad No.	Input/Output	Note
	GA	TB			
BD	40	38	40	Output	Buzzer driver pin

Note: Pin No. indicates the pin number of an 80QFP (80-pin package).

10.5 Difference of Output Logic Depending on SELF Bit and External Circuit

Figure 10-3 shows the output waveform of the buzzer driver depending on the SELF bit. "H" level of the BD pin becomes VDD, and "L" level becomes VSS2 output level.

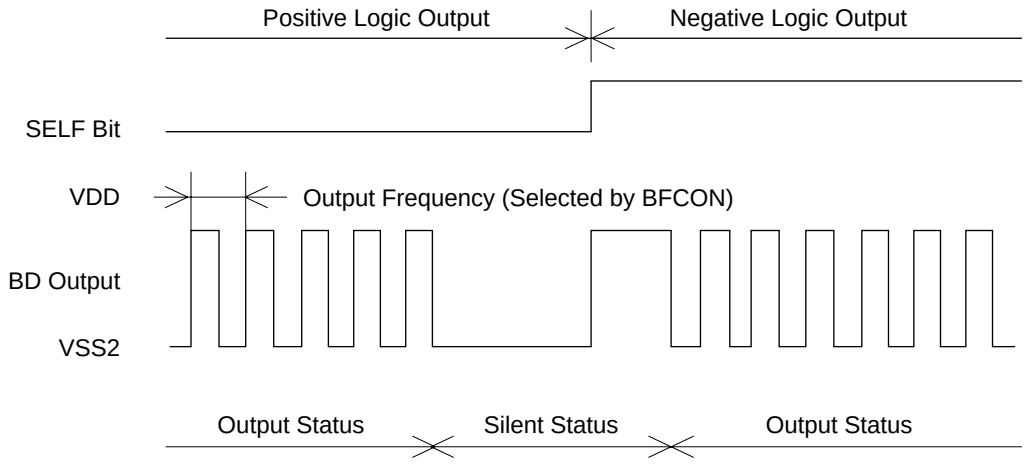
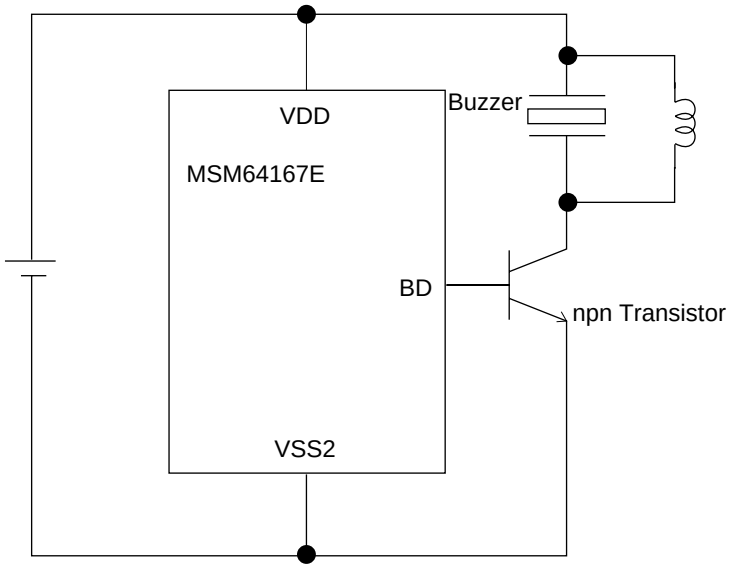


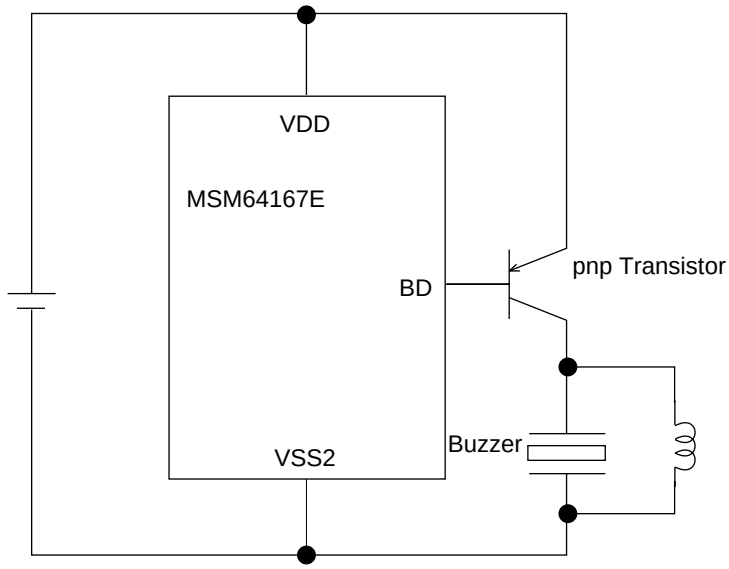
Figure 10-3 Output Waveform of BD Pin

Figure 10-4 shows an example of an external circuit of the buzzer driver.

As shown here, do not directly drive the buzzer with the BD pin, but via an external transistor.



(a) When SELF bit = "0"



(b) When SELF bit = "1"

Figure 10-4 Example of External Circuit of Buzzer Driver

Chapter 11

Watchdog Timer (WDT)

Chapter 11 Watchdog Timer (WDT)

11.1 Overview

The MSM64167E has a built-in watchdog timer (WDT) to detect CPU runaway.

WDT is comprised of a 6-bit watchdog timer counter (WDTC) to count the 16 Hz output of the time base counter, and the watchdog timer control register (WDTCON) to reset WDTC.

11.2 Configuration of Watchdog Timer

Figure 11-1 shows the configuration of the watchdog timer.

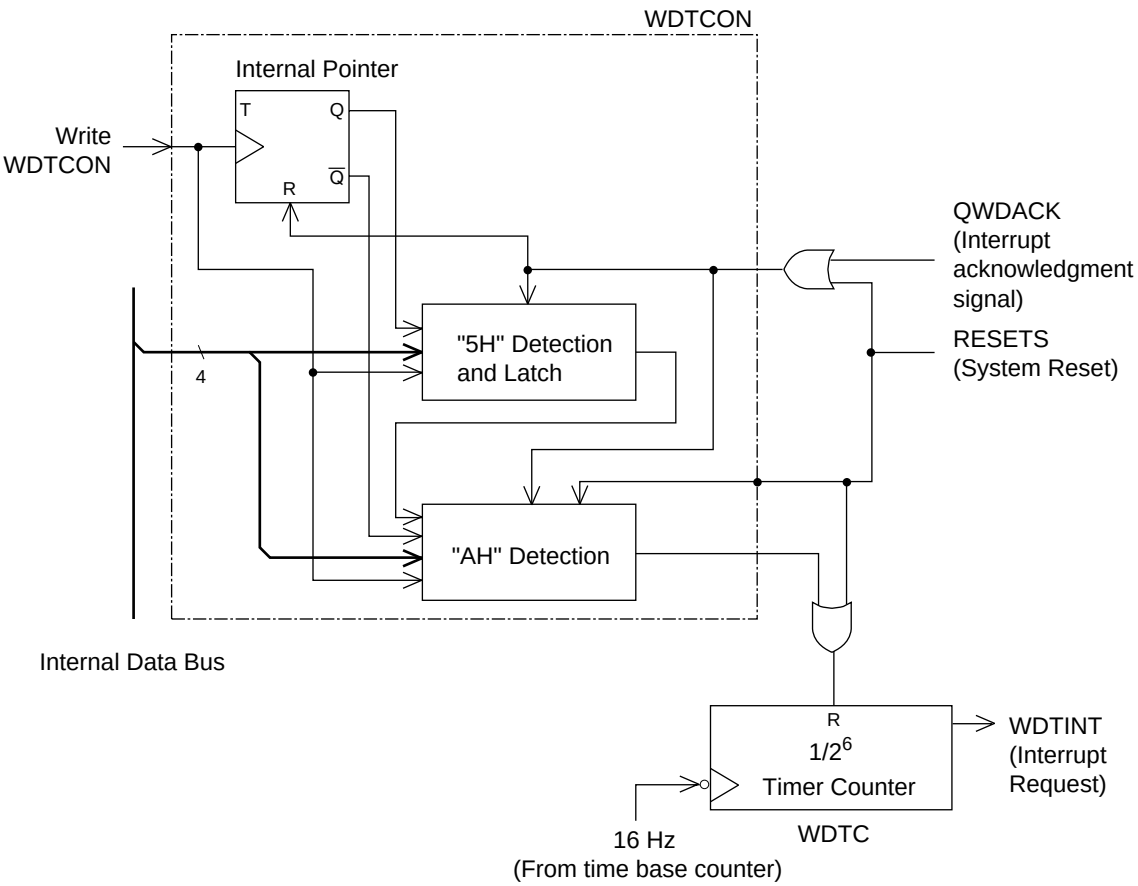


Figure 11-1 Configuration of Watchdog Timer

11.3 Operation of Watchdog Timer

If system reset is cleared, the watchdog timer (WDT) automatically starts and the watchdog timer counter (WDTC) starts countup. WDTC is not reset unless "5H" and "0AH" are alternately written to the watchdog timer control register (WDTCON).

If WDTC is not reset, WDTC overflows in 1.9 to 2.0 seconds, which generates a watchdog timer interrupt request (WDTINT). WDTINT is an interrupt that cannot be disabled by software (non-maskable interrupt), and is accepted with the highest priority.

As a consequence, the program must be written so that WDTC is reset every 1 second by software. If CPU runaway occurs and WDTC cannot be normally reset due to a power supply abnormality, etc., WDTC overflows and a watchdog timer interrupt is generated. In a watchdog timer interrupt routine, execute a return from abnormal status to a normal routine.

Note: The watchdog timer cannot detect all abnormal operations. Even if CPU runaway occurs, the watchdog timer cannot detect an abnormality if WDTC is reset.

Figure 11-2 shows the flow chart of resetting the watchdog timer. As Figure 11-2 shows, WDT is reset when "5H" is written if the internal pointer is "0", and when "0AH" is written if the internal pointer is "1". The internal pointer is reset to "0" at system reset and when WDTC overflows, and the internal pointer is inverted whenever it is written in WDTCON.

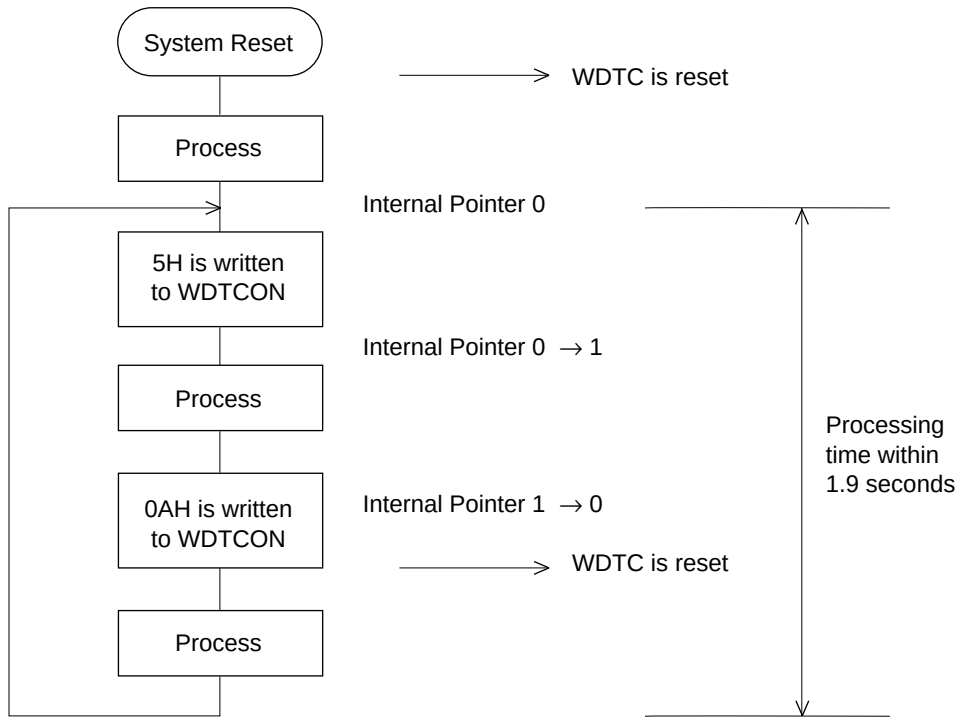


Figure 11-2 Flow Chart of Resetting Watchdog Timer

Figure 11-3 shows the time chart of the watchdog timer operation.

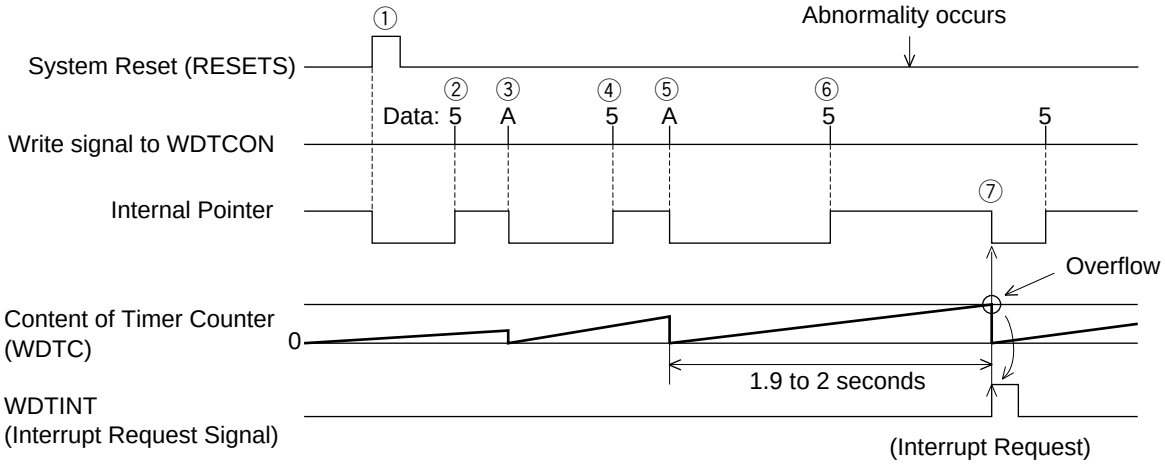


Figure 11-3 Timer Chart of Watchdog Timer Operation

The operation of the watchdog timer follows.

① Internal pointer and watchdog timer counter (WDTC) are reset by system reset.
② "5H" is written to WDTCON (internal pointer 0 → 1).
③ "0AH" is written to WDTCON, and WDTC is reset (internal pointer 1 → 0).
④ "5H" is written to WDTCON (internal pointer 0 → 1).
⑤ "0AH" is written to WDTCON, and WDTC is reset (internal pointer 1 → 0).
⑥ "5H" is written to WDTCON (internal pointer 0 → 1).
⑦ If "0AH" is not written to WDTCON when the internal pointer is "1", (if WDTC is not reset due to CPU runaway), a watchdog timer interrupt, WDTINT, is generated by an overflow of the timer counter. At this time, the internal pointer becomes "0".

11.4 Watchdog Timer Control Register (WDTCON)

Watchdog timer control register (WDTCON) is a 4-bit write only special function register (SFR) that resets the watchdog timer.

WDTCON (38H) (W)

b_3	b_1	b_1	b_0
d3	d2	d1	d0

Chapter 12

A/D Converter (ADC)

Chapter 12 A/D Converter (ADC)

12.1 Overview

The MSM64167E includes dual slope type A/D converter (ADC) that converts A/D for voltage input to analog input pins AIN0 to AIN3. Since the AD conversion counter uses a timer (see Chapter 8), AD conversion speed and resolution are programmable. Count values of the timer change in proportion to the input voltage.

12.2 Configuration of A/D Converter

Figure 12-1 shows the configuration of the A/D converter.

The A/D converter is configured with a dual slope circuit, a reference voltage generation circuit, a voltage amplification circuit, a constant-current generation circuit, and a control circuit.

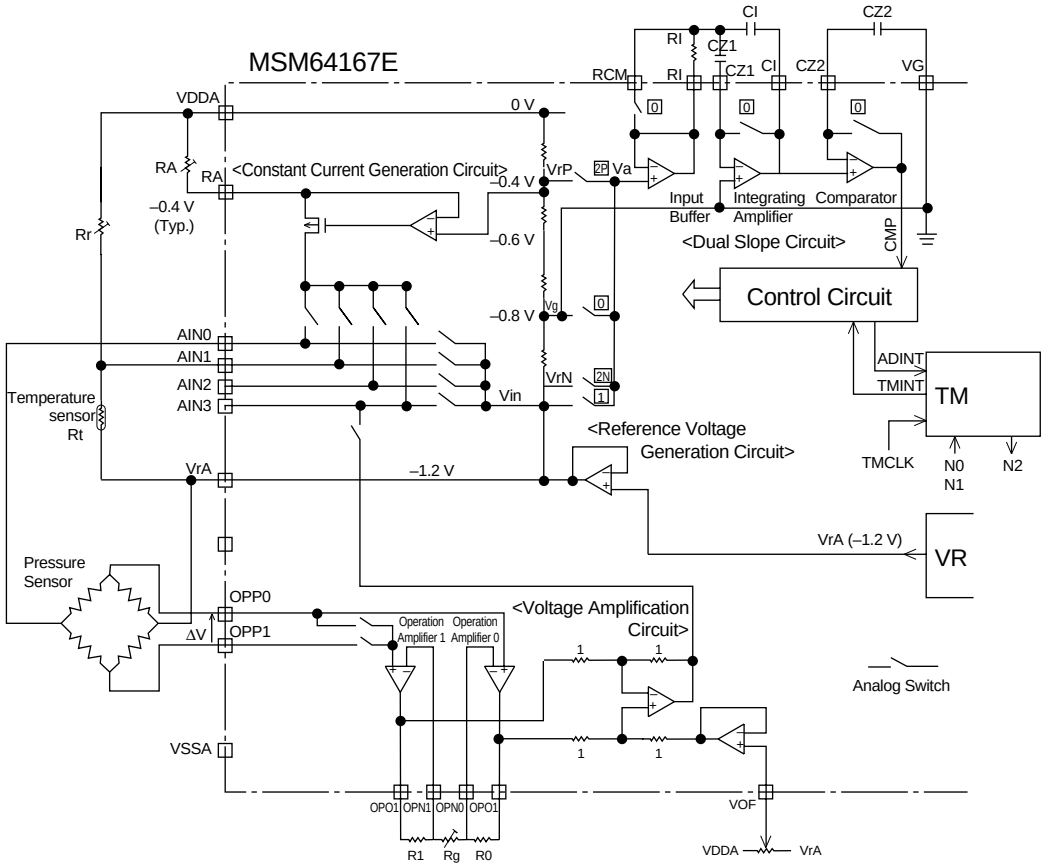


Figure 12-1 Configuration of A/D Converter

12.3 Operation of A/D Converter

12.3.1 AD Conversion Operation

Figure 12-2 shows the configuration of the dual slope circuit. Figure 12-3 shows a waveform diagram of the AD conversion operation. Figure 12-4 shows a flow diagram of the AD conversion operation.

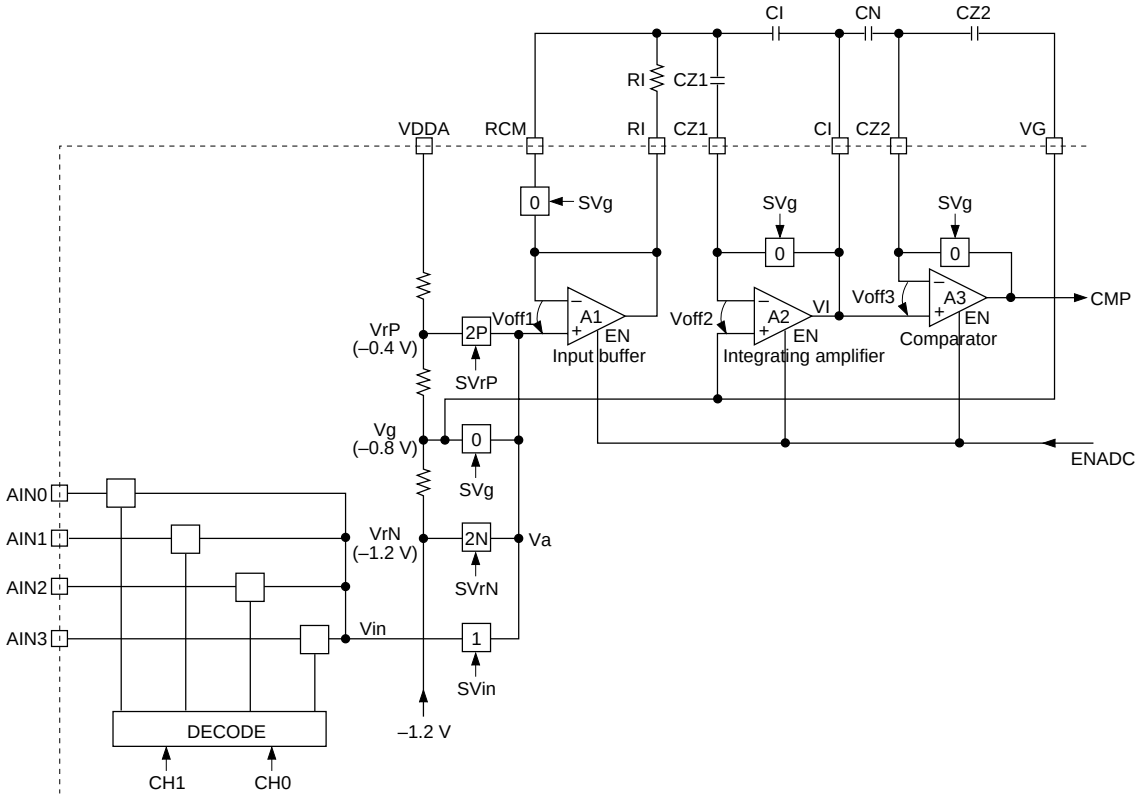


Figure 12-2 Configuration of the Dual Slope Circuit

Note: CN: Capacitor for noise reduction
For capacitors CI, CN, CZ1, and CZ2, select those that have a small amount of charge leakage. If a capacitor that has a large amount of charge leakage is used, the AD conversion accuracy will be deteriorated.

Recommended material for the capacitors: polypropylene or polystyrene

For the dual slope circuit, connect an integral resisance RI, an integral capacitor CI, and offset compensation capacitors CZ1 and CZ2.

Connect the sensors to a VrA pin. This can change input voltages in proportion to a reference voltage VrA generated inside the A/D converter so that AD conversion error due to production dispersion of VrA can be canceled.

When the sensors which require fixed current drive are used, fixed current can be output from AIN0–AIN3 by connecting current adjustment resistance to RA Pin.

A micro-voltage can be amplified by the built-in voltage amplification circuit once. The input voltage Δ V can be magnified by (R1 + Rg + R0)/Rg times and a value of inverted level shift based on the VOF pin can be input to the AIN3 pin by connecting resistances R1, Rg and R0 to the voltage amplification circuit.

Reference voltages VrP, Vg, and VrN needed for the AD conversion are generated internally based on the reference voltage VrA. They are made by dividing the voltage VrA through resistances such as VrP = 1/3 $\times$ VrA, Vg = 2/3 $\times$ VrA, and VrN = 3/3 $\times$ VrA. Because the voltage VrA itself is dispersed in a range of –1.2 $\pm$0.1 V, the voltages VrP, Vg, and VrN also are changed. In this chapter, however, the voltages are set to VrP = –0.4 V, Vg = –0.8 V, and VrN = –1.2 V for ease of description.

Note: If the absolute voltage is measured, errors caused by the dispersion of the reference voltage (internally generated) cannot be canceled.

If the absolute voltage is measured, it is required to externally apply a stable (accurate) reference voltage (to VrA pin). It should be noted that a range of the voltage externally applied has to be between VrA and VSSA + 1 V.

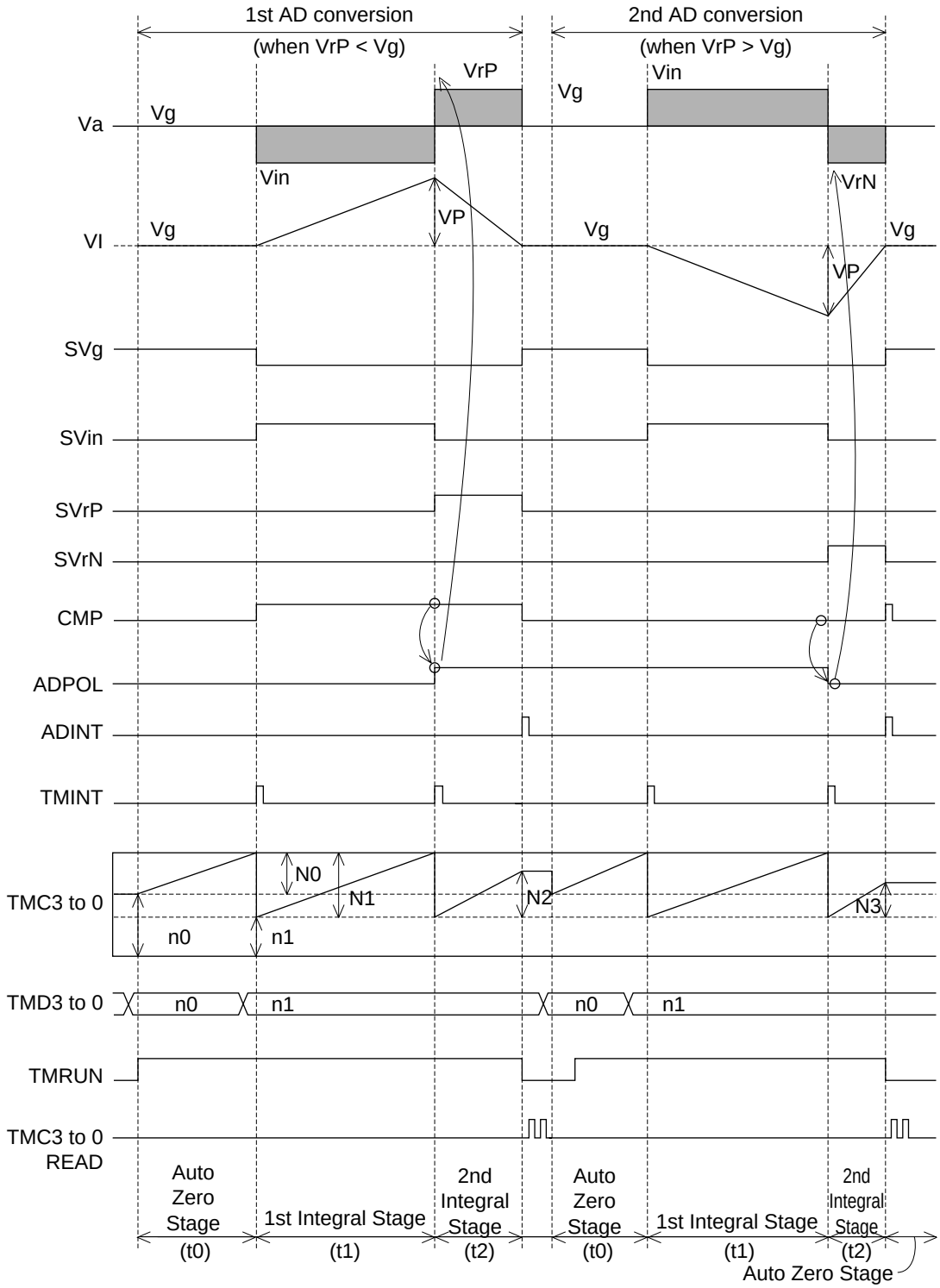
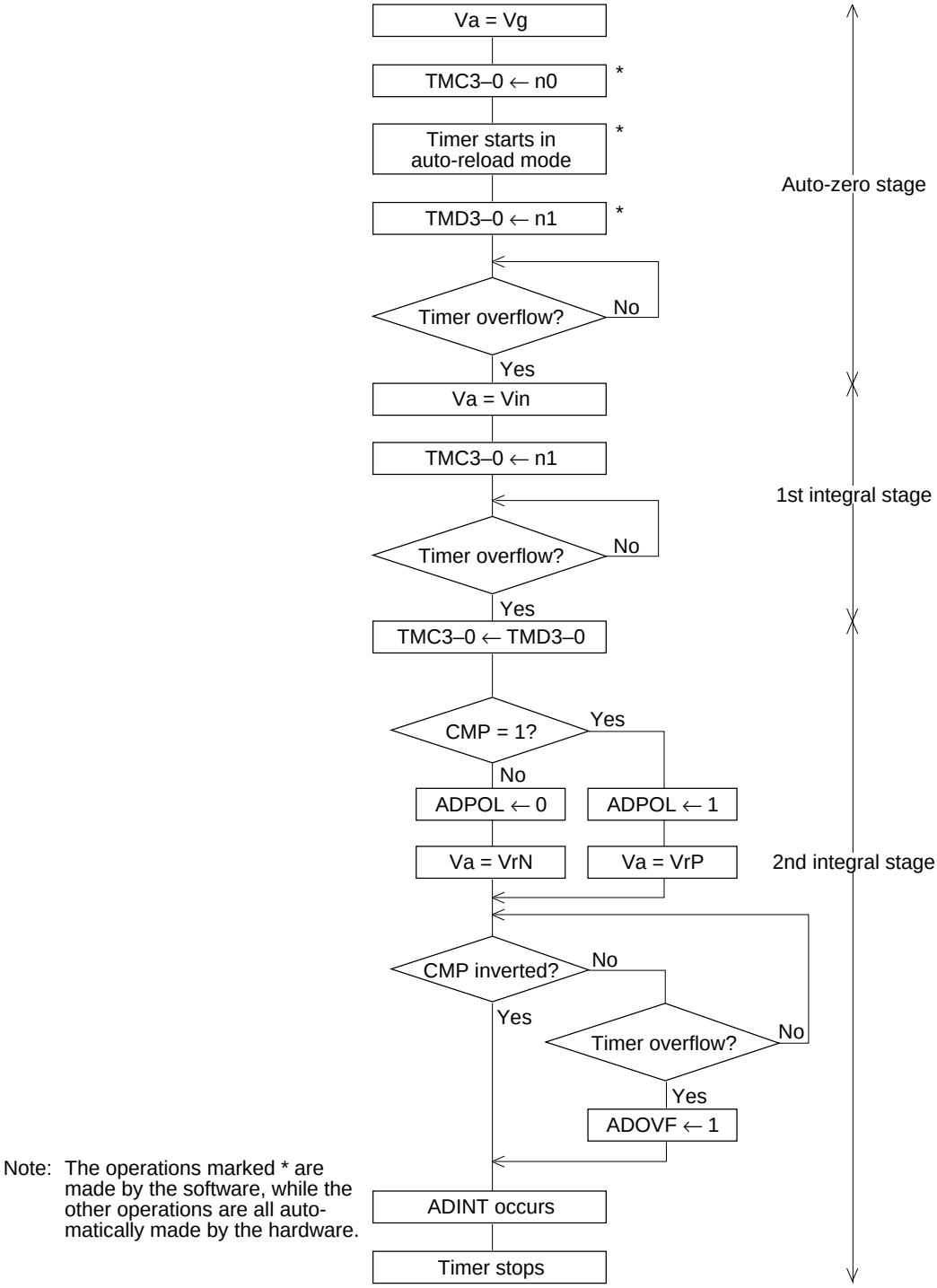


Figure 12-3 Waveform Diagram of the AD Conversion Operation



Note: The operations marked * are made by the software, while the other operations are all automatically made by the hardware.

Figure 12-4 Flow Diagram for the AD Conversion Operation

Note: See Section 12.3.8 for the difference between a timer overflow and ADOVF (an overflow resulting from AD conversion).

The A/D converter is activated by setting bit 2 (ENADC) of an AD control register 1 to "1".

There are four analog input channels, of AIN0 to AIN3. Any of them can be selected with the internal analog switch. Channel can be selected with bit 1 (CH1) and bit 2 (CH2) of an AD control register 0.

The AD conversion is made in consecutive operations of the auto-zero stage, the 1st integral stage, and the 2nd integral stage by combination of the A/D converter and the timer. The switching operation from stage to stage is automatically controlled by an overflow signal of the timer. The serial operation for the AD conversion is described in Figures 12-2 and 12-3. The guaranteed accuracy of the A/D converter is on the assumption that the timer frequency is 32.768 kHz. The converter can be operated at 700 kHz, but with low accuracy.

(1) Auto-zero Stage (t0)

The auto-zero stage is a stage for initializing voltage levels of the dual slope circuit.

In the auto-zero stage, all the analog switches 0 are turned on. The integral ground voltage Vg is selected for the integral input voltage Va. The integral capacitor CI is discharged. The offset compensation capacitors CZ1 and CZ2 are charged with offset voltages of the input buffer, integrating amplifier, and comparator. If all the offset voltages are (0), potentials at the RI, CI, RCM, CZ1, CZ2, and VG pins are set to Vg in the auto-zero stage.

A period of the auto-zero stage can be set with the timer. The offset compensation capacitors CZ1 and CZ2 are 0.1 μF, the auto-zero stage requires 30 msec or more in a 12-bit AD conversion. The timer should have n0 preset so that the timer will overflow in 30 msec. If the timer is started in the auto-reload mode, the auto-zero stage is automatically ended by the overflow signal TMINT of the timer in N0 count. Control moves to the next 1st integral stage. A value n1 reloaded for a period of the 1st integral stage should be set to TMD3–0 before the end of the auto-zero stage. For example, 0F000H should be preset for the 12-bit AD conversion.

(2) 1st Integral Stage (t1)

The 1st integral stage is a stage for integrating an analog value to be measured for a predetermined period of time before charging CI in proportion to the measured voltage.

In the 1st integral stage, the analog switch 1 is turned on. The analog input voltage Vin to be measured is selected for the integral input voltage Va to integrate. A voltage VI output of the integrating amplifier is increased if Vin < Vg or is decreased if Vin > Vg. Slant of the VI waveform is in proportion to difference of Vin – Vg. The timer continues counting from the value n1 reloaded when control was moved from the auto-zero stage to the 1st integral stage. In count of N1, the timer overflows before control is automatically moved from the 1st integral stage to the 2nd integral stage.

Let number of counts of the timer in the 1st integral stage and cycle of the timer clock be denoted by N1 and t00, respectively. A voltage Vp output of the integrating amplifier at the end of the 1st integral stage is

$$Vp = -(Vin - Vg) \times N1 \times t00/(CI \times RI) \quad \text{..... (Expression 12-1)}$$

Since t00 and N1 are constant, Vp is proportional to (Vin – Vg).

(3) 2nd Integral Stage (t2)

In movement to the 2nd integral stage, Vin polarity flag (ADPOL) is set. If the comparator output is "H", the ADPOL is set to "1". If the comparator output is "L", the ADPOL is set to "0".

In the 2nd integral stage, if ADPOL = "1", the analog switch 2P is turned on. If ADPOL = "0", the analog switch 2N is turned on. In other words, for the integral input voltage Va, the reference voltage VrP or VrN is selected so that the input voltage makes Vg opposite to that of the 1st integral stage, before being integrated. Therefore, direction of the voltage VI output of the integrating amplifier is opposite to the one in the 1st integral stage. If the voltage VI output of the integrating amplifier exceeds "0", the comparator inverts. An A/D converter interrupt request ADINT is generated to stop the timer automatically. The 2nd integral stage ends before control is returned to the auto-zero stage.

Since the reference voltage in the 2nd integral stage is integrated, the slant of the VI waveform is always constant. Therefore the period of time from the start to end of the 2nd integral stage is proportional to the voltage Vp output of the integrating amplifier. Let the number of counts of the timer in the 2nd integral stage be denoted by N2 if the reference voltage is VrP. The following equation is given.

$$0 = Vp - (VrP - Vg) \times N2 \times t00/(CI \times RI) \quad \text{..... (Expression 12-2)}$$

Solving Expressions 12-1 and 12-2, we obtain

$$N2/N1 = (Vg - Vin)/(VrP - Vg) \quad \text{..... (Expression 12-3)}$$

Since Vin, VrP, and Vg are based on VrA, dispersion of the value of VrA will not affect the result of the AD conversion.

Notes: 1. Be sure to stop the timer (TM) before setting ENADC to "1".

2. While ENADC is "1", the timer (TM) should not be used for the purposes other than AD conversion.

3. When AD conversion is forcibly ended by setting ENADC to "0" during the 2nd integral stage, ADINT may occur.

12.3.2 Input Voltage Overflow Flag (ADOVF)

Normally, TMINT is generated twice during AD conversion, when conntrol is moved from the auto-zero stage to the 1st integral stage and when control is moved from the 1st integral stage to the 2nd integral stage. If Vin > VrP or Vin < VrN (when the input voltage is out of the electrical standards), and if the same value is reloaded in the 1st integral stage and the 2nd integral stage, a third TMINT is generated before the comparator inverts in the 2nd integral stage, and then the input voltage overflow flag (ADOVF) is set to "1". In this event, also ADINT is generated to return control to the auto-zero stage. The timer stops after the reload operation is performed by the third overflow. Note that the timer does not operate in the state where the input voltage overflow flag (ADOVF) is set to "1". The ADOVF is reset to "0" if the A/D converter status register (ADSTAT) is read. While the input voltage overflow flag (ADOVF) is set to "1", the timer does not operate.

When the A/D converter status register (ADSTAT) is read, ADOVF is reset to "0".

12.3.3 Offset Compensation

Figure 12-5 shows an offset compensation waveform.

For explanatory purposes in subsection 12.3.1, the offset voltages of the input buffer, integrating amplifier, and comparator that configure the dual slope circuit were treated as "0". But, actually, they have respective input offset voltages applied to them. This A/D converter is devised to cancel the offset voltages of the input buffer, integrating amplifier, and comparator.

As shown in Figure 12-2, when the offset voltages based on negative input voltages of input buffer, integrating amplifier and comparator are Voff1, Voff2 and Voff3 respectively, voltages of pins in the auto-zero stage are as follows: RCM, RI = Voff1, CZ1, CI = –Voff2 and CZ2 = –Voff2 – Voff3. If the offset compensation capacitors CZ1 and CZ2 have no leakage, the voltges at the RCM and CZ2 pins maintain the above mentioned values even in the 1st integral stage and the 2nd integral stage.

On the other hand, the voltage at the RI pin during the period of integration is Va – Voff1. Hence, a voltage VRI applied across the integral resistance RI is

$$VRI = Va - Voff1 - (-Voff1) = Va.$$

As a result, an error due to Voff1 is canceled.

A voltage output of the integrating amplifier at the start of integration is –Voff.

The negative voltage input to the comparator is maintained at a value of –Voff2 – Voff3 that is a deviation by the offset voltage of the comparator itself from –Voff2. Because of this, the comparator output is inverted where the integral output voltage intersects –Voff2. In the end, the integration starts from –Voff2 and ends at –Voff2 so that errors of becoming Voff2 and Voff3 can be canceled.

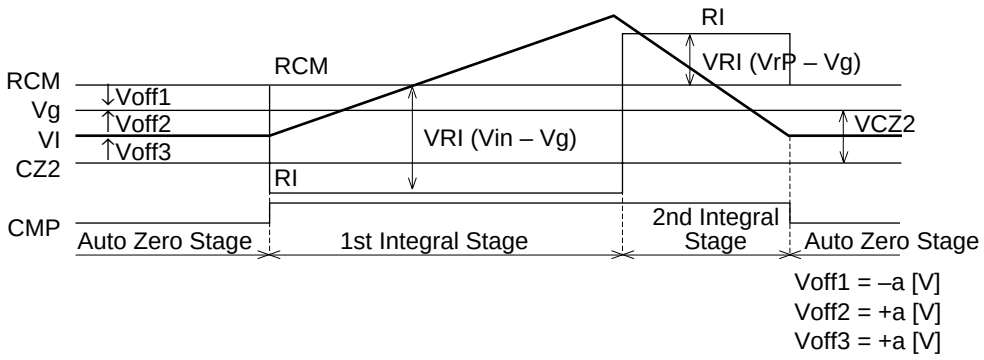


Figure 12-5 Offset Compensation Waveform

12.3.4 Reference Voltage Generation Circuit

Figure 12-6 shows the reference voltage generation circuit.

The reference voltage generation circuit outputs to the VrA pin the constant voltage of around –1.2 V generated by a constant voltage generation circuit VR. The reference voltage also is a reference voltage used for generating Vg, VrP, and VrN inside the A/D converter. Therefore, as shown in Figure 12-1, the sensor can be put in between the VDDA and VrA pins to affect dispersion of the voltage VrA to all of Vg, VrP, VrN, and Vin at an equal rate. This can cancel an error of the AD conversion. To eliminate the dispersion of the VrA output voltage, it is also possible to have an external accurate reference voltage entered to it. It should be noted that a range of the external input voltage has to be between VrA and VSSA + 1 V.

If the ENADC bit is set to "0", the VrA pin is internally pulled up to VDD.

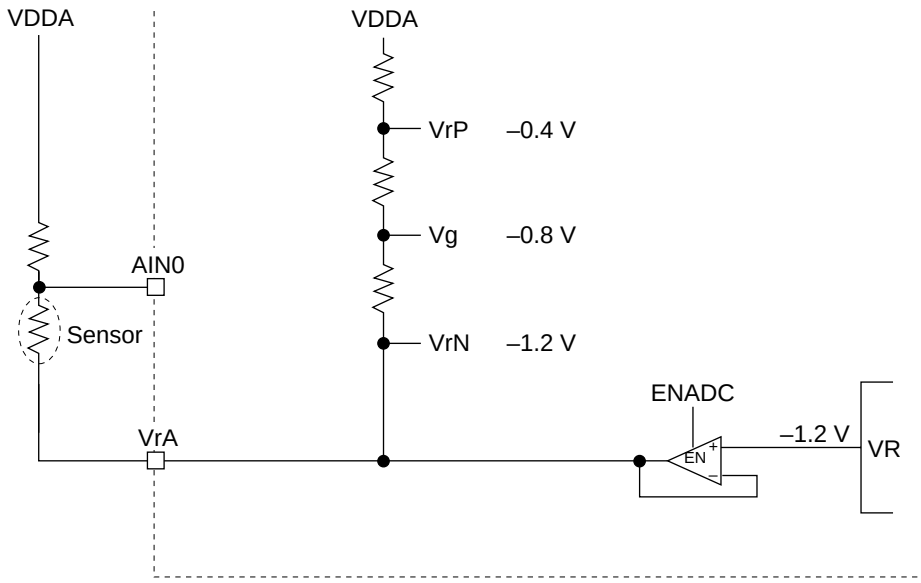


Figure 12-6 Configuration of the Reference Voltage Generation Circuit

12.3.5 Voltage Amplification Circuit

Figure 12-7 shows the configuration of the voltage amplification circuit.

The voltage amplification circuit is activated when bit 3 (ENOPA) of an AD control register 1 is set to "1". If ENOPA = "0", input pins OPP0, OPP1, OPN0, OPN1, and VOF of the voltage amplification circuit are internally pulled up to VDD. The current consumed in the voltage amplification circuit becomes zero.

Connect the external resistances R0, Rg and R1 to the voltage amplification circuit to multiply the voltage (Δ V) between the OPP0 and OPP1 by (R0 + Rg + R1)/Rg times. The voltage amplification circuit inverts and level-shifts the voltage to output to AIN3. They are based on VOF pin voltage. If the voltages of OPP0, OPP1, OPO0, OPO1 for VDD are denoted as VOPP0, VOPP1, VOPO0 and VOPO1 respectively, and if the voltage of VOF and voltage of AIN3 output are denoted as VVOF and VAIN3, then the voltage VAIN3 is

$$VAIN3 = (VOPP0 - VOPP1) \times (R0 + Rg + R1)/Rg + VVOF.$$

Figure 12-8 shows examples of the voltages of pins in operation. The multiplier of (R0 + Rg + R1)/Rg must be up to 40. However, VOPO0 and VOPO1 must be in a range of $2 \times VSSA + 4.0\ V < VOPO0, VOPO1 < -0.1\ V$, and VOPP0 and VOPP1 must be $VSSA + 1.4\ V < VOPP0, VOPP1 < -0.4\ V$, and VAIN3 must be in a range of $-0.4\ V < Vo < -1.2\ V$. Values of R0, Rg, R1, and VVOF should be determined so that the voltage can be in those ranges.

If bit 1 (SOPP0) of the AD control register 1 is set to "1", the voltage at the OPP0 pin is input to both operation amplifier 0 and 1. If the voltage at the AIN3 pin is measured, we can know of the offset of the voltage amplification circuit. In other words, offset can be canceled by adjusting VVOF in that state. Figure 12-9 shows examples of the voltages at the pins in the offset adjustment. In Figure 12-9, SOPP0 = 1, or the VAIN3 at the time when input voltage is 0 is adjusted to VG level. VAIN3 can be adjusted to desired level.

Note: Be sure that the amplified voltage to be output to AIN3 is in the range of VrA to VrP.

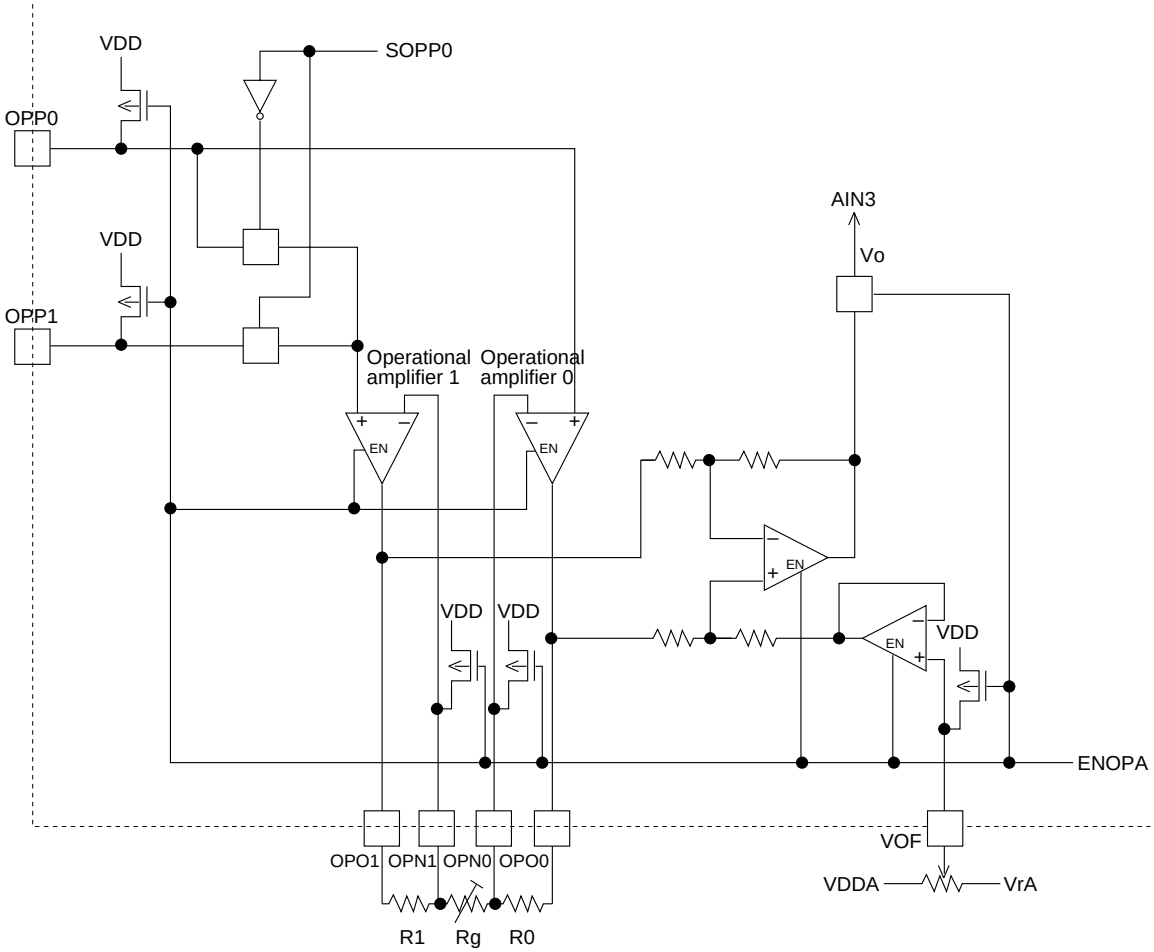


Figure 12-7 Configuration of the Voltage Amplification Circuit

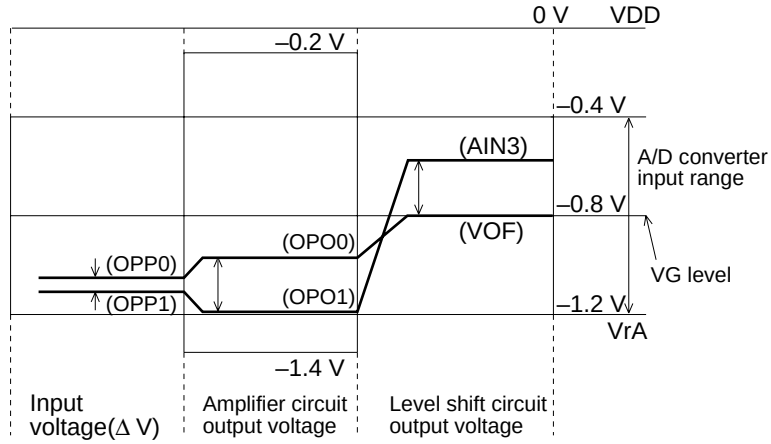


Figure 12-8 Examples of the Voltages at the Pins in Operation

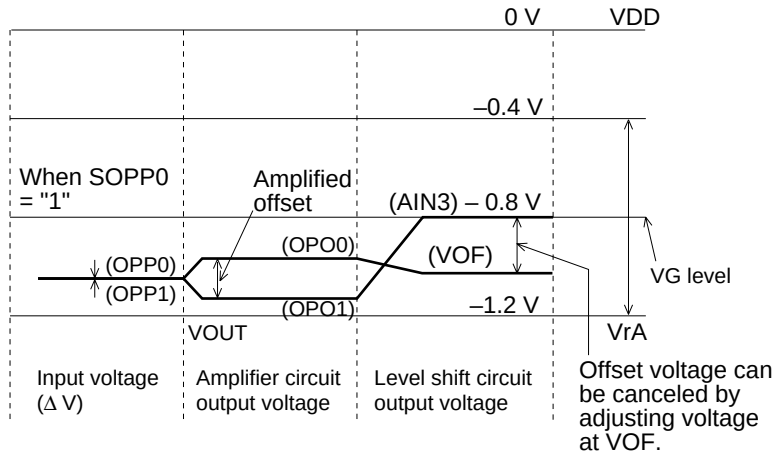


Figure 12-9 Examples of the Voltages at the Pins in the Offset Adjustment

12.3.6 Constant-Current Generation Circuit

Figure 12-10 shows the configuration of the constant-current generation circuit.

The constant-current generation circuit outputs a constant-current to a pin selected from AIN0 to AIN3 by connecting a constant-current adjusting resistance RA between the RA pin and VDDA. The RA pin has a voltage of around VDD – 0.4 V output to it. Channels outputting constant current can be selected by bit 3 (ICH1) and bit 2 (ICH0) of the AD control register. If no constant current is needed, keep the RA pin open.

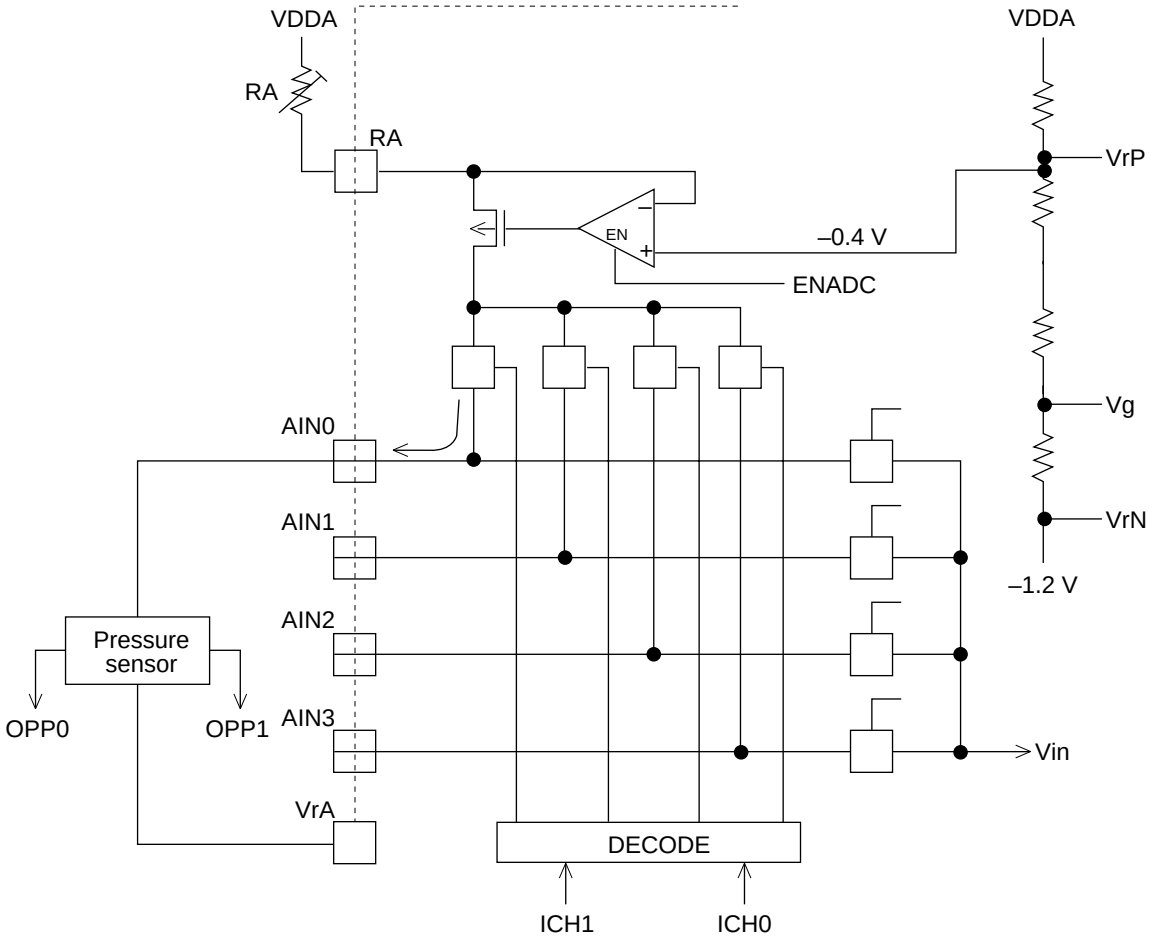


Figure 12-10 Configuration of the Constant-Current Generation Circuit

12.3.7 External Components

The dual slope circuit consists of external components, including the integrating resistance RI, integrating capacitor CI, offset compensation capacitors CZ1 and CZ2, and noise reducing capacitor CN (the capacitors may not be connected sometimes). Care should be taken in selecting types and values of the external components because these increase the performance of the A/D converter.

The A/D converter may involve an error due to deterioration of the linearity of the integral output voltage VI caused by leaking resistance and dielectric absorption of the integrating capacitor CI, offset compensation capacitors CZ1 and CZ2, and noise reducing capacitor CN. To reduce the error, the capacitors should be preferably made of polypropylene or polystyrene.

Also, error is caused when the peak value Vp of the voltage VI output of the integrating circuit is too low or high. Figure 12-11 shows a graph illustrating the output waveform VI of the integrating circuit. The VI is

$$VI = ((Vin - Vg) \times t00 \times N1)/(CI \times RI).$$

Error is caused if the integral constant CI × RI is too low, because of the output saturation in the first integral stage. This is indicated by ① in Figure 12-11. Also error occurs if the integral constant CI × RI is too high, because of the dead zone of comparator (input range where output becomes indeterminate). This is indicated by ③ in Figure 12-11. An optimum output range, as indicated by ②, is a range that the maximum value of VI should have a margin of 0.1 V to become around VDD – 0.1 V. The integral constant should be selected to make such an optimum output range.

Minimum value of RI should be 30 kΩ because the output current of the input buffer and the integrating amplifier are limited.

R0, Rg and R1 are connected to the amplification circuit externally. These three resistances determine the multiplier G. The multiplier G is given by

$$G = (R0 + Rg + R1)/Rg.$$

The multiplier G has to be in a range of 1 to 40. To avoid error in the multiplier G, it is recommended that Rg be made variable to adjust.

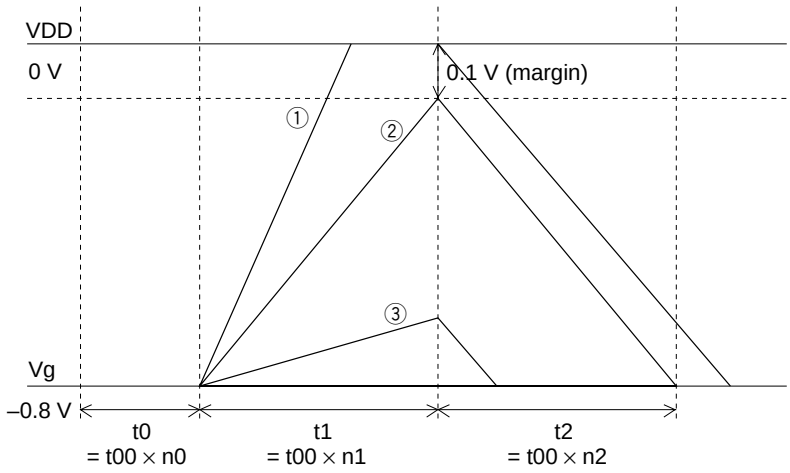


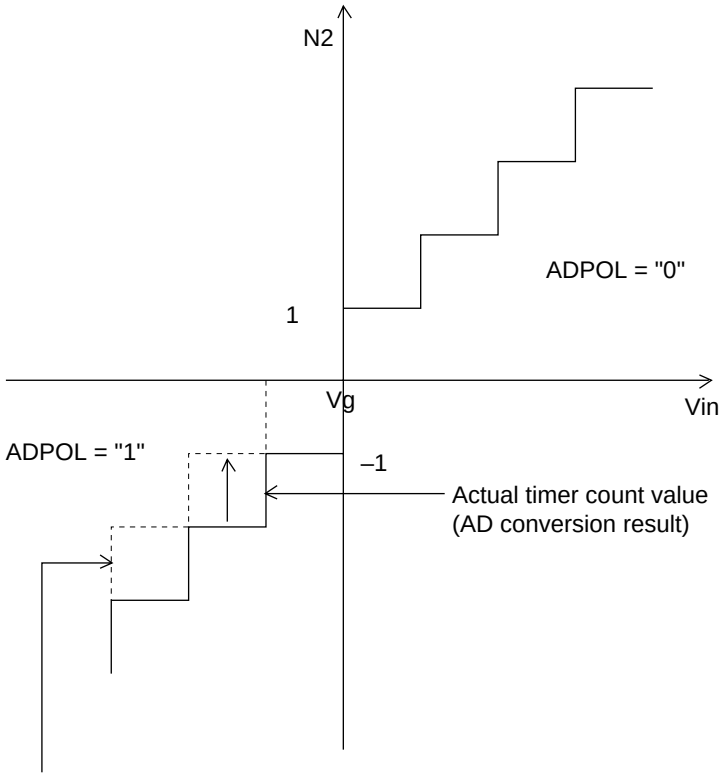
Figure 12-11 Output Waveform VI of the Integrating Circuit

The output currents of the operation amplifiers used in the voltage amplification circuit, like that of the integrating amplifier, are limited. Therefore , the sum of R0 + Rg + R1 has to be higher than 500 kΩ.

Note: When using a voltage amplification circuit, set the multiplier G considering the input offset volltage.

12.3.8 Precautions in Use of A/D Converter

The A/D converter has a minimum AD conversion count value set to "1", and not to "0". Therefore, a result of the AD conversion for the input around Vg is made as shown by a solid line in Figure 12-12. (In the figure, the result of the AD conversion with ADPOL = "1" is negative.) When AD conversion input is generated across Vg, and when continuous AD conversion output is necessary, add 1 to the result of ADPOL = "1" and deduct 1 from the result of ADPOL = "0" by software program. The dotted line in the figure has 1 added to ADPOL = "1".



Value of 1 added to the result of the AD converstion with ADPOL = "1" by software program

With the addition of 1 above, continuity can be obtained between the result of the AD conversion with ADPOL = "1" and that of the AD conversion with ADPOL = "0".

Figure 12-12 Result of the AD Conversion of the Input Around Vg

ADC Input (V)	TMC (16 bits) (Hex)		ADPOL	ADOVF	ADC Value (Dec)
	—		—	—	—
	F001	Saturation	0	1	avobe 4096
	F001	Count upward	0	1	avobe 4096
	F000	Overflow	0	0	4096
VrP (–0.4 V)*	FFFF	Count upward	0	0	4095
	FFFE	Count upward	0	0	4094
	FFFD	Count upward	0	0	4093
	⋮		⋮	⋮	⋮
	⋮	Count upward	⋮	⋮	⋮
	F002	Count upward	0	0	2
	F001		0	0	1
VrP (–0.8 V)	F001	Count upward	1	0	1
	F002	Count upward	1	0	2
	⋮		⋮	⋮	⋮
	⋮	Count upward	⋮	⋮	⋮
	FFFD	Count upward	1	0	4093
	FFFE	Count upward	1	0	4094
	FFFF	Count upward	1	0	4095
VrP (–1.2 V)*	F000	Overflow	1	0	4096
	F001	Count upward	1	1	avobe 4096
	F001	Saturation	1	1	avobe 4096

* The value of the analog input voltage that brings the TMC to "0000" (full-count value) depends on the characteristics of the integral capacitor used for AD conversion. Because of this, the value is not always equal to VrN or VrP.

Figure 12-13 (a) Timer Values and AD Conversion Results with the Setting of a 12-Bit (2^{12} = 4096) Precision

ADC Input (V)	TMC (16 bits) (Hex)		ADPOL	ADOVF	ADC Value (Dec)
	—		—	—	—
VrP (–0.4 V)*	FF01	Saturation	0	1	avobe 256
	FF01	Count upward	0	1	avobe 256
	FF00	Overflow	0	0	256
	FFFF	Count upward	0	0	255
	FFFE	Count upward	0	0	254
	FFFD	Count upward	0	0	253
	⋮		⋮	⋮	⋮
VrP (–0.8 V)	⋮	Count upward	⋮	⋮	⋮
	F002	Count upward	0	0	2
	F001		0	0	1
	F001	Count upward	1	0	1
	F002	Count upward	1	0	2
	⋮		⋮	⋮	⋮
VrP (–1.2 V)*	⋮	Count upward	⋮	⋮	⋮
	FFFD	Count upward	1	0	253
	FFFE	Count upward	1	0	254
	FFFF	Overflow	1	0	255
	FF00	Count upward	1	0	256
	FF01	Saturation	1	1	avobe 256
	FF01		1	1	avobe 256

* The value of the analog input voltage that brings the TMC to "0000" (full-count value) depends on the characteristics of the integral capacitor used for AD conversion. Because of this, the value is not always equal to VrN or VrP.

Figure 12-13 (b) Timer Values and AD Conversion Results with the Setting of an 8-Bit (2^8 = 256) Precision

Note: As seen in Figures 12-13 (a) and (b), the timer overflows differ from the overflows resulting from AD conversion.

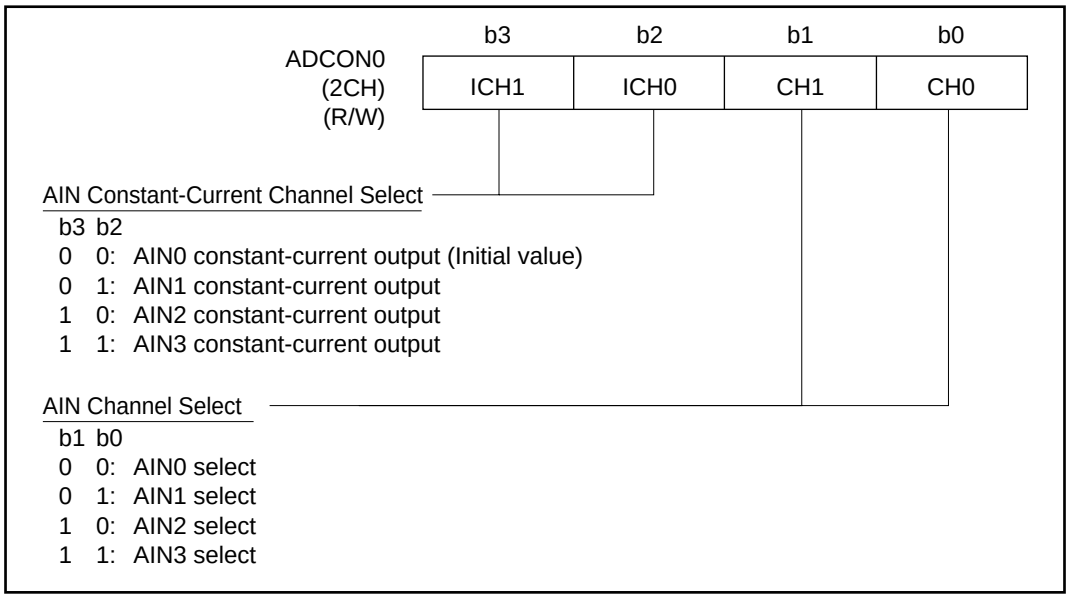
Care should be taken in that an error may occur if a CPU, buzzer driver, or similar devices are activated while the A/D converter is operating.

The guaranteed accuracy of the A/D converter is on the assumption that the timer frequency (TMCLK) is 32.768 kHz. The converter can be operated at 700 kHz, but will produce a large number of errors.

12.4 A/D Converter-Related Registers

(1) AD control register 0 (ADCON0)

The AD control register 0 (ADCON0) is a 4-bit special-function register (SFR) for controlling the A/D converter.



12

Bits 3 and 2: ICH1 and ICH0

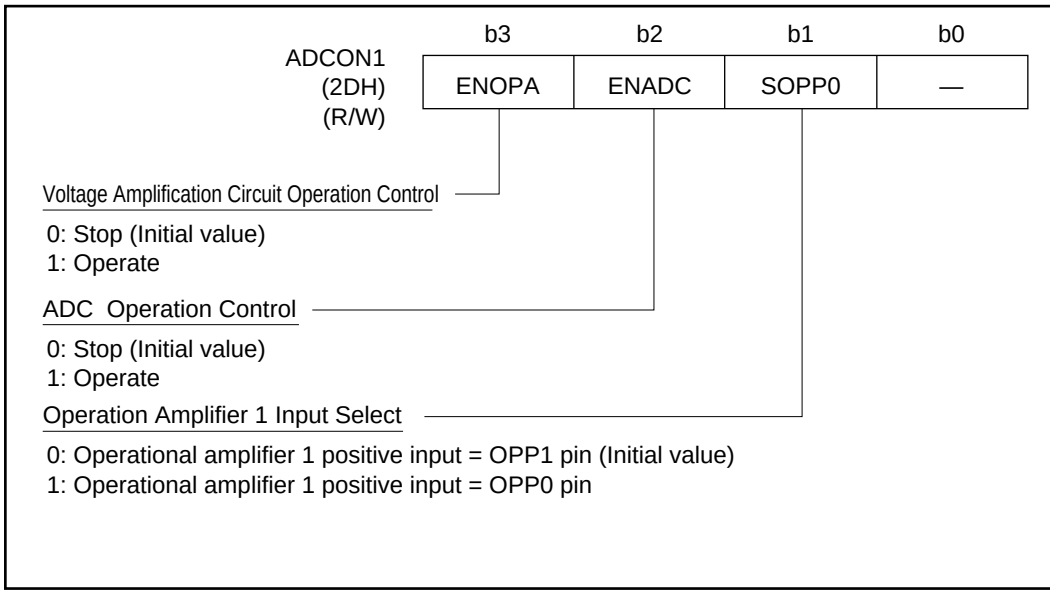
The ICH1 and ICH0 are bits that select a pin to make the constant-current output mode from the analog inplut pins AIN0 to AIN3. When the system is reset, the bits are all reset to "0" and the AIN0 pin goes into the constant-current output mode. If the constant-current output mode is not used, keep the RA pin open.

Bits 1 and 0: CH1 and CH0

The CH1 and CH0 are bits that select the channel (AIN0 to AIN3) of the analog input pins. At the system reset, the bits are all reset to "0" and the channel at the AIN0 pin is selected.

(2) AD control register 1 (ADCON1)

The AD control register 1 (ADCON1) is a 4-bit special-function register (SFR) for controlling the A/D converter.



Bit 3: ENOPA

Bit ENOPA places the voltage amplification circuit in the operation state. The bit is reset to "0" (stop state) when the system is reset. In the reset state, the input pins OPP0, OPP1, OPN0, OPN1, and VOF are internally pulled up to VDD, and the current consumption in the voltage amplification circuit becomes zero. When the voltage amplification circuit is in operation, the pull-up's are all released so that the output of the voltage amplification circuit is internally connected to the AIN3 pin.

Bit 2: ENADC

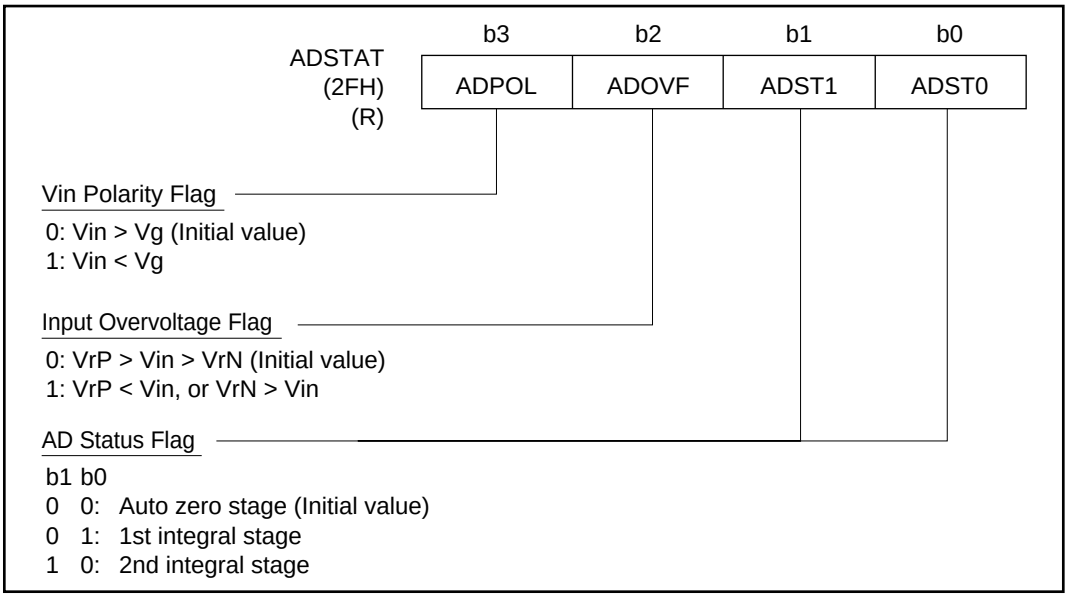
Bit ENADC places the A/D converter in the operation state. The bit is reset to "0" (stop state) when the system is reset. In the reset state, the current consumption in the voltage amplification circuit becomes zero. The input pins VrA, OPP0, OPP1, OPN0, OPN1, and VOF are internally pulled up to VDD.

Bit 1: SOPP0

Bit SOPP0 switches the positive input of the operational amplifier 1 of the voltage amplification circuit to the same OPP0 pin as the operational amplifier 0. The bit is reset to "0" when the system is reset. In the reset state, OPP1 pin is selected for the positive input of the operational amplifier 1. If SOPP0 is set to "1", input of operational amplifiers 0 and 1 become the same, therefore output of the voltage amplification circuit in this status becomes the amplified offset voltage of the circuit, and offset voltage can be easily adjusted.

(3) A/D converter status registance (ADSTAT)

The A/D converter status register (ADSTAT) is a 4-bit special-function register (SFR) that indicates the status of the A/D converter.



Bit 3: ADPOL

The ADPOL is a flag of sign bit that indicates the input polarity of Vin when Vg (–0.8 V) is used as a reference. The output level of the comparator is checked when control is moved to the 2nd integral stage. When the level is at "H", the flag becomes "1". When the level is at "L", the flag becomes "0". The flag is reset to "0" at the system reset.

Bit 2: ADOVF

Flag ADOVF indicates that the input voltage is out of the electrical standards. The input voltage is determined as overvoltage when the timer overflows before the comparator inverts in the 2nd integral stage, and the input overvoltage flag is reset to "1". The bit is reset to "0" at the system reset. This flag is set to "0" if the ADSTAT is read.

Bits 1 and 0: ADST1 and ADST0

The ADST1 and ADST0 are flags that indicate whether A/D converter is in auto zero stage, 1st integral stage or 2nd integral stage. These bits are reset to "0" at the system reset. They are always reset to "0" when the timer is stopped (TMRUN = 0).

Table 12-1 lists the A/D converter-related registers.

Table 12-1 A/D Converter-Related Registers

Register Name	Symbol	Address	Read/Write	Value at System Reset
A/D Converter Control Register 0	ADCON0	2CH	R/W	0H
A/D Converter Control Register 1	ADCON1	2DH	R/W	1H
(Disabled)		2EH	R/W	8H
A/D Converter Status Register	ADSTAT	2FH	R	0H
Timer Data Register 0	TMD0	20H	R/W	Undefined
Timer Data Register 1	TMD1	21H	R/W	Undefined
Timer Data Register 2	TMD2	22H	R/W	Undefined
Timer Data Register 3	TMD3	23H	R/W	Undefined
Timer Counter Register 0	TMC0	24H	R/W	Undefined
Timer Counter Register 1	TMC1	25H	R/W	Undefined
Timer Counter Register 2	TMC2	26H	R/W	Undefined
Timer Counter Register 3	TMC3	27H	R/W	Undefined
Timer Control Register 0	TMCON0	28H	R/W	8H
Timer Control Register 1	TMCON1	29H	W	0CH
Interrupt Enable Register 0	IE0	30H	R/W	0H
Interrupt Request Register 0	IRQ0	31H	R/W	0H

Note: The register at address 2EH is disabled.
Do not write "1" to any bit at address 2EH.
However, "0" can be written to the register bits upon initialization of the register.
(Writing "0" does not affect microcontroller operation.)

Chapter 13

LCD Driver (LCD)

Chapter 13 LCD Driver (LCD)

13.1 Overview

The MSM64167E has 31 internal output LCD drivers (LCD).

An LCD driver component is comprised of 31 × 4-bit display registers (DSPR0–30), a display control register (DSPCON), and LCD driver circuit and a bias generation circuit (BIAS) for 31 outputs.

LCD driving has three modes: 1/4 duty, 1/3 duty, and 1/2 duty. A maximum of 108 segments can be driven in 1/4 duty mode, a maximum of 84 segments in 1/3 duty mode, and a maximum of 58 segments in 1/2 duty mode. These modes can be selected by software.

The common driver and segment driver of each LCD driver are selected by mask option. Also display registers are freely assigned to the segment drivers of each bit by mask option.

A display register cannot be used unless selected by mask option. As a consequence, even if an open display register is used for a purpose other than display, that display register must be specified in the mask option table. See "Appendix F: Mask Options" on the mask option table.

L0 to L7 of LCD drivers can be output to a port by mask option.

The relationship between duty, bias method and maximum segments follows.

In 1/4 duty	1/3 bias method	108 segments
In 1/3 duty	1/3 bias method	84 segments
In 1/2 duty	1/2 bias method	58 segments

13.2 Configuration of LCD Driver

Figure 13-1 shows the configuration of an LCD driver. Figures 13-2 and 13-3 show an LCD driver and the peripheral circuits of a display register.

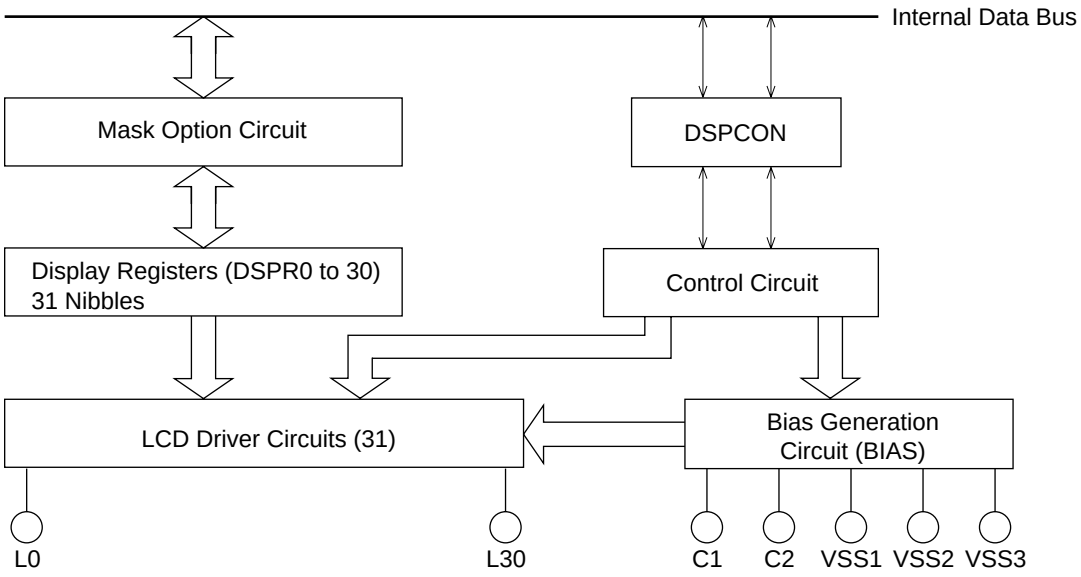


Figure 13-1 Configuration of LCD Driver

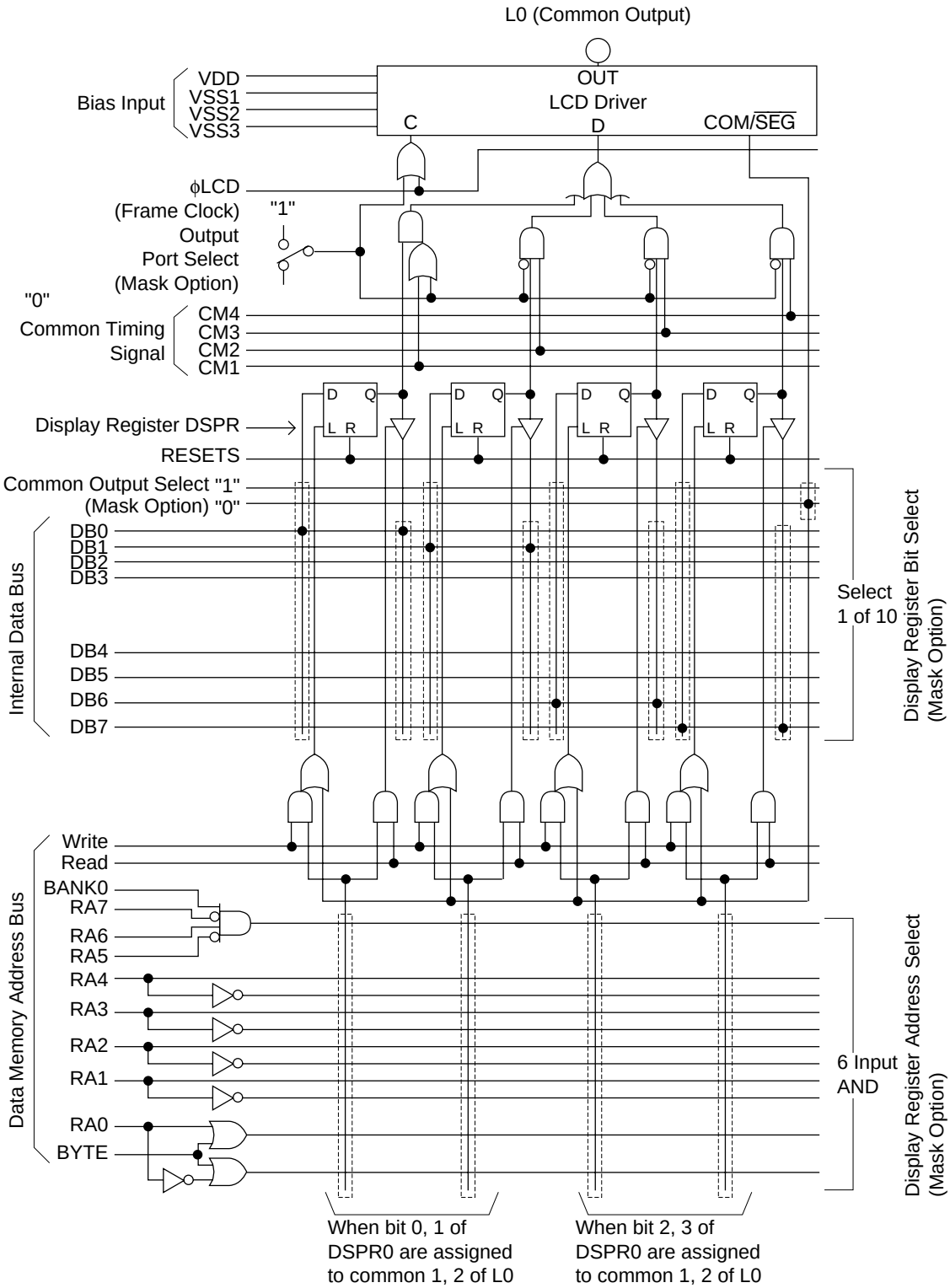


Figure 13-2 LCD Driver and Display Register (L0 to L7 Circuit Configuration: For 1 input)

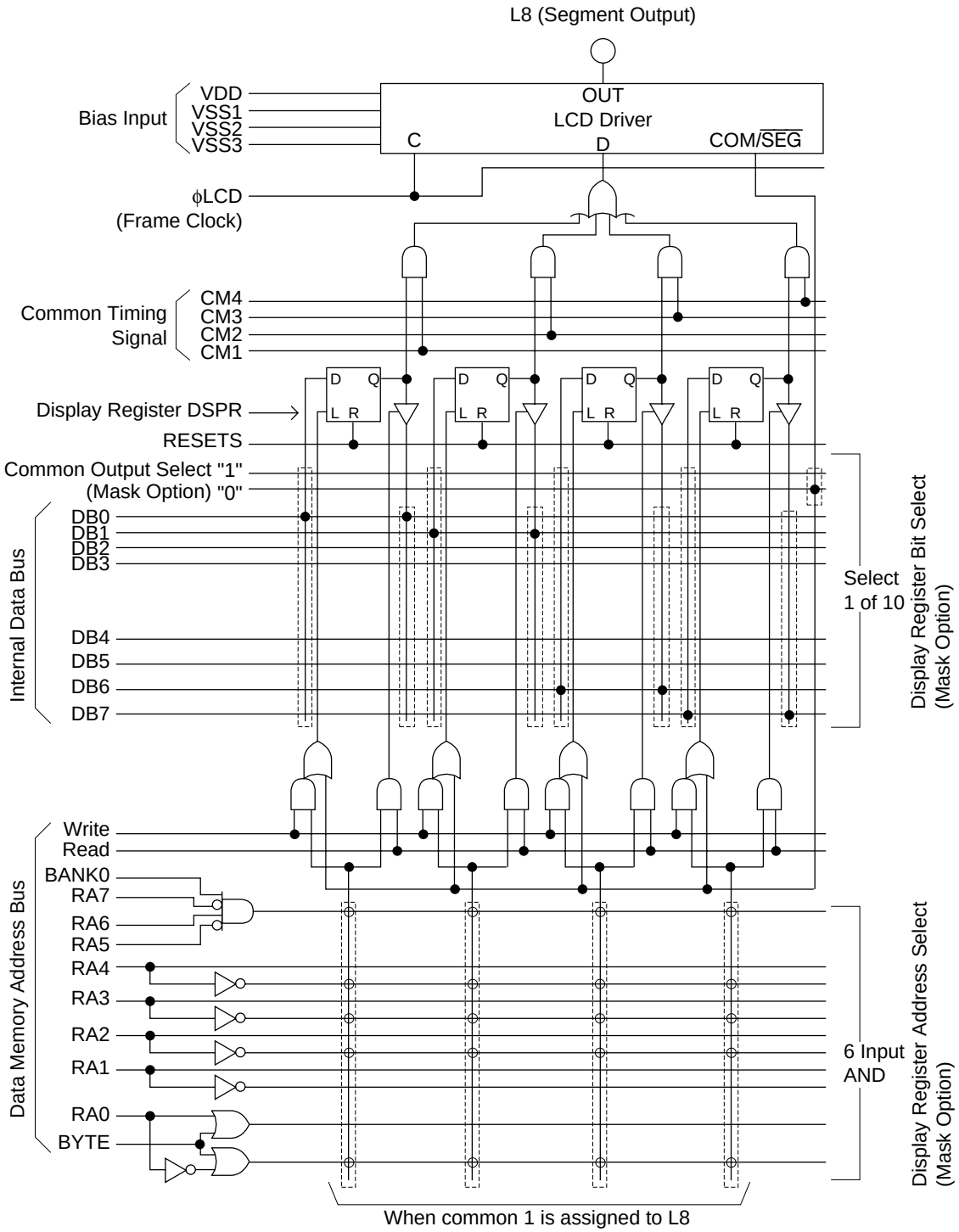


Figure 13-3 LCD Driver and Display Register (L8 to L30 Circuit Configuration: For 1 output)

13.3 Operation of LCD Driver

LCD driver outputs LCD driver waveforms based on data written to a display register.

The address of a display register, bit assignment, and the selection of segment drivers and common drivers are specified by mask option.

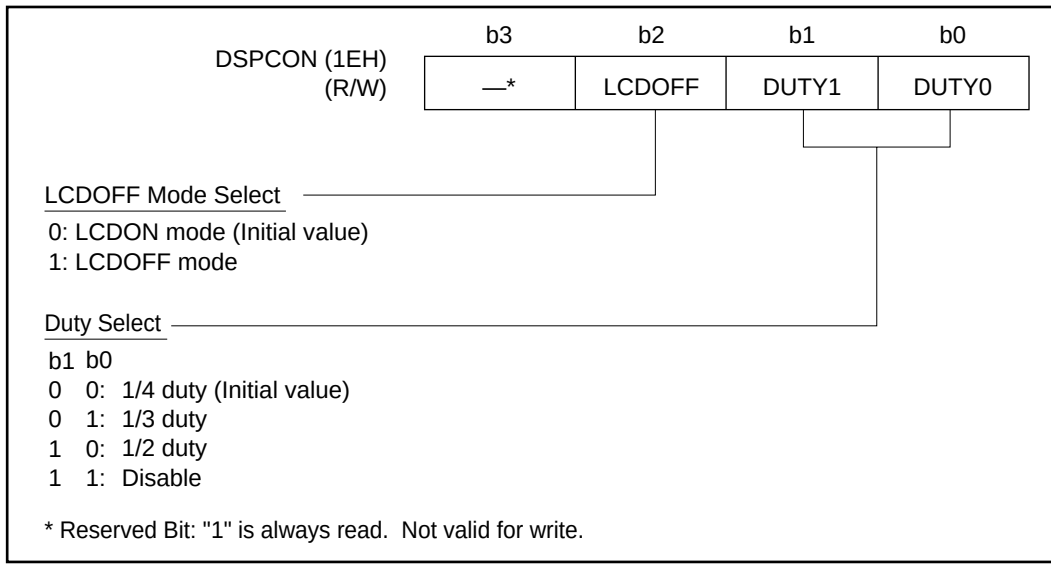
Four segments of a display register are assigned to each segment driver, and all four segments are used in 1/4 duty, three segments are used in 1/3 duty, and 2 segments are used in 1/2 duty.

In Figure 13-2, the L0 pin is a segment driver, and bits 0 and 1 of DSPR0 are assigned to the segments corresponding to common 1 and 2, and bits 2 and 3 of DSPR1 are assigned to the segments corresponding to commons 3 and 4. In Figure 13-3, L8 output is the common 1 driver. By mask option, any display register and bit can be assigned for any output.

The duty of an LCD driver is selected by the display control register (DSPCON).

13.4 Display Control Register (DSPCON)

The display control register (DSPCON) is a 4-bit special function register (SFR) that controls the duty ratio of an LCD driver, and LCD ON/OFF.



Bit 2: LCDOFF

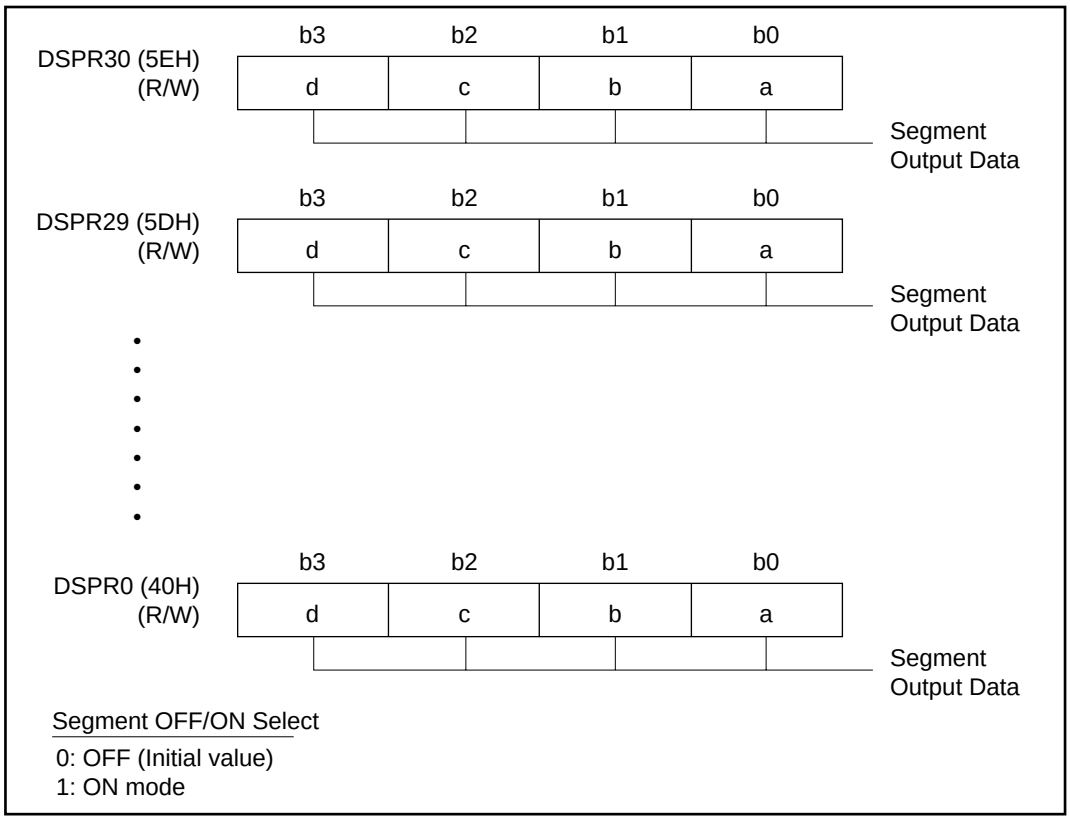
LCDOFF is a bit that selects ON/OFF mode of an LCD driver. It is reset to "0", and LCD mode is selected at system reset. In LCDON mode, an LCD driver outputs an LCD drive waveform depending on data written to the display register. If LCDOFF is set to "1", LCDOFF mode is selected. In LCDOFF mode, all LCD drivers output VDD level, and all drivers enter OFF mode. Even if LCDOFF mode is set, the value of the display register is not changed. This mode does not affect the pin set to the output ports of L0–L7.

Bits 1, 0: DUTY1, DUTY0

DUTY1 and DUTY0 are bits that select the duty ratio of an LCD driver. Both are reset to "0" and 1/4 duty is selected at system reset. It is disabled to set both DUTY1 and DUTY0 to "1".

13.5 Display Registers 0–30 (DSPR0–30)

Display registers 0 to 30 (DSPR0 to 30) are 4-bit special function registers (SFRs) to write segment output data of an LCD driver. Display registers are assigned to 40H–5EH of the bank 0.



Any bit of a display register can be assigned to any segment driver by mask option. All registers are reset to "0", and all LCD lights go out at system reset. All display register bits set to "1" light, and bits reset to "0" go out.

To determine the assignment of bits of a display register to a display segment, refer to the "LCD Driver Mask Option Table" in "Appendix F: Mask Options".

13.6 Output Port Selection by Mask Option

L0 to L7 of LCD drivers can be independently selected for output ports by the setting of mask options. When these pins are specified to an output port, 1 port pin is assigned to 1 bit of a display register. Figure 13-4 shows an equivalent circuit when display register DSPR0 is assigned to L0 to L4 as an output port. At this time "H" output is at VDD level, and "L" output is at VSS level.

The output format is a CMOS type.

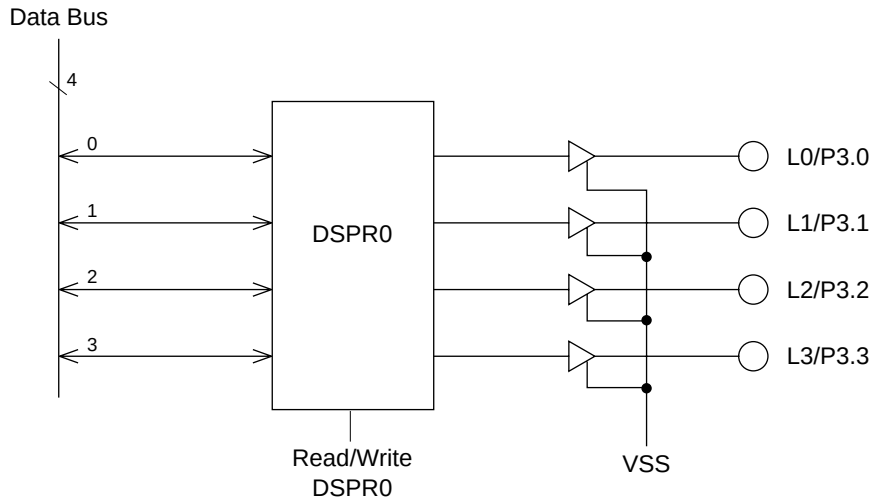


Figure 13-4 Equivalent Circuit when DSPR0 is Assigned to L0 to L3 as an Output Port

Only DSPR0 and DSPR1 can be used for the output port, other display registers cannot be used.

To determine the assignment of bits of a display register to an output pin, and for output port specifications, refer to "LCD Driver Mask Option Table", in "Appendix F: Mask Options".

13.7 Bias Generation Circuit for LCD Driver

The bias generation circuit for LCD raises or lowers the power voltage, and generates –1.5 V, –3.0 V and –4.5 V for an LCD driver by an external capacitor.

Figure 13-5 shows the configuration of a bias generation circuit.

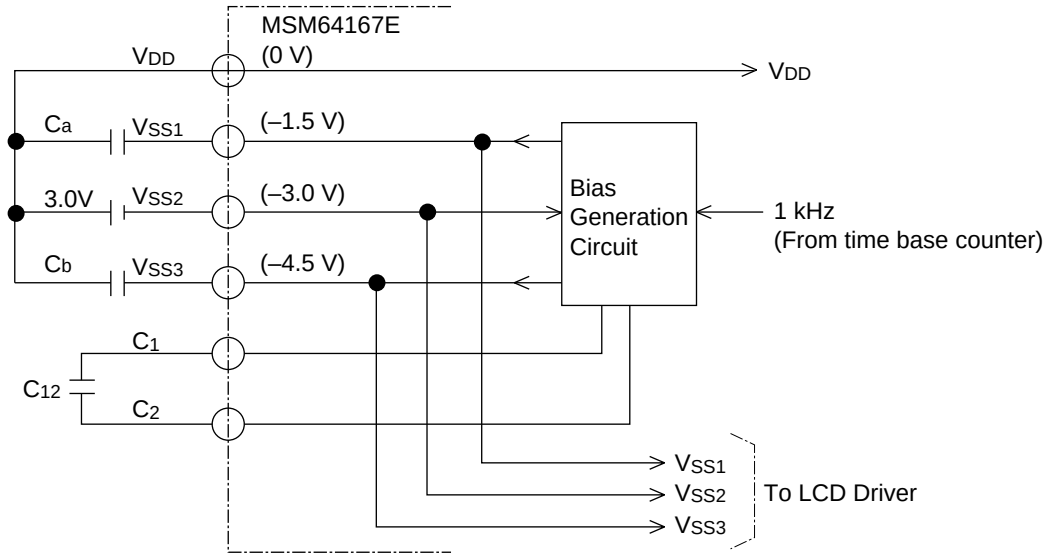


Figure 13-5 Configuration of Bias Generation Circuit (Ca, Cb, C12 = 0.1 μF)

13

Note: If an LCD driver is used at 1/2 duty, Cb is unnecessary. Set VSS3 to open.

13.8 LCD Driver Output Waveform

Figures 13-6 (a) to (c) show 1/4 duty. Figures 13-7 (a) and (b) show 1/3 duty, and Figures 13-8 (a) and (b) show 1/2 duty of an LCD driver output waveform.

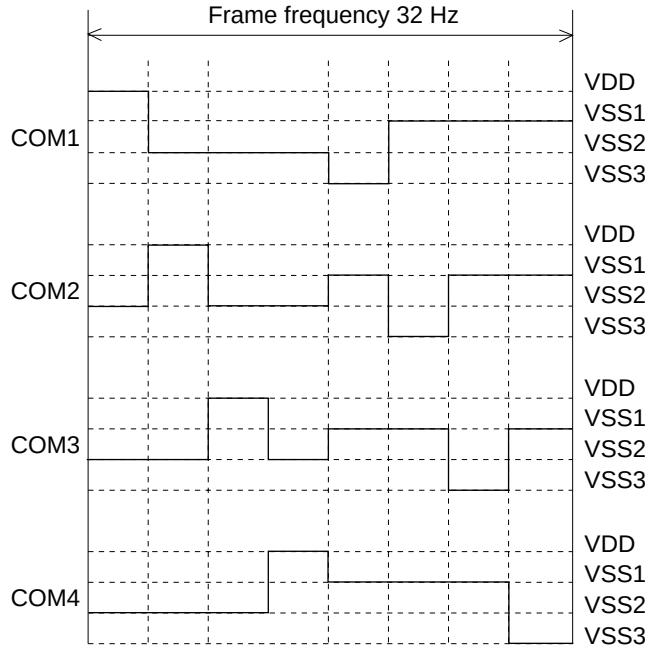


Figure 13-6 (a) 1/4 Duty Common Driving Waveforms (1/3 bias)

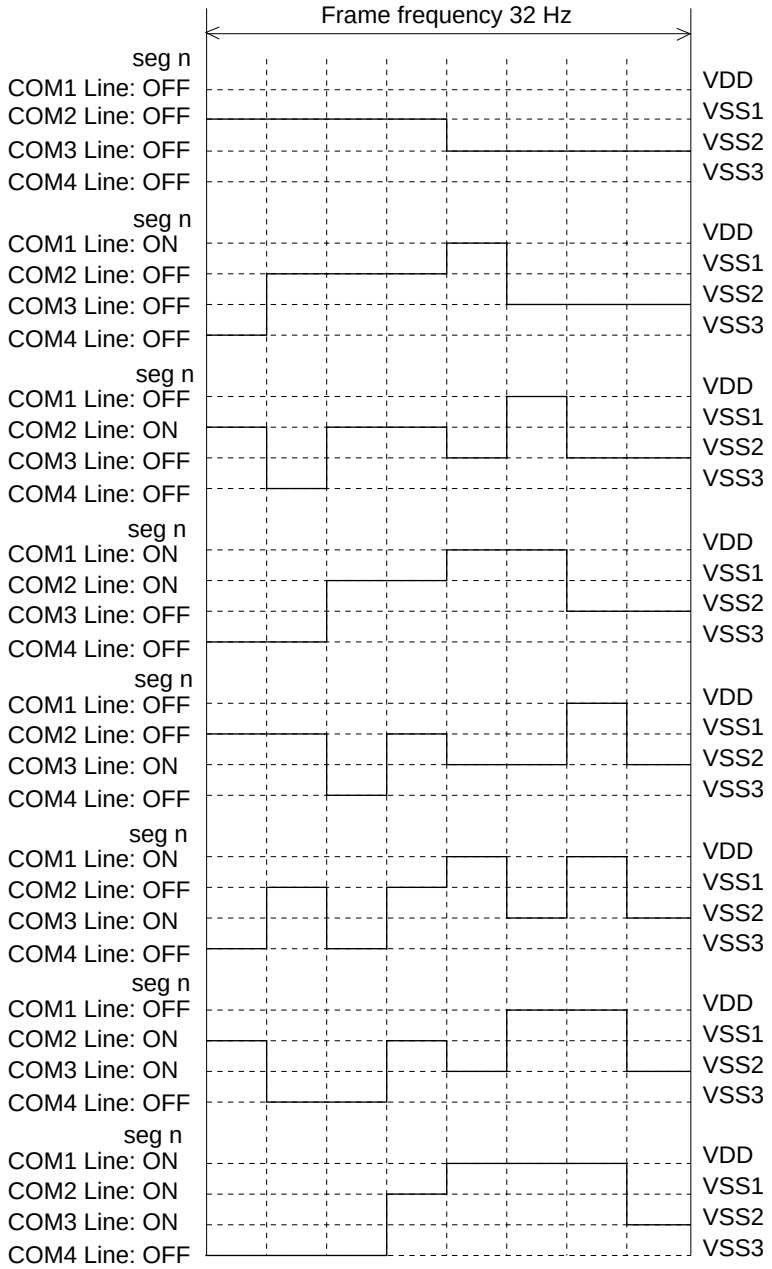


Figure 13-6 (b) 1/4 Duty Segment Driving Waveforms (1/3 bias)

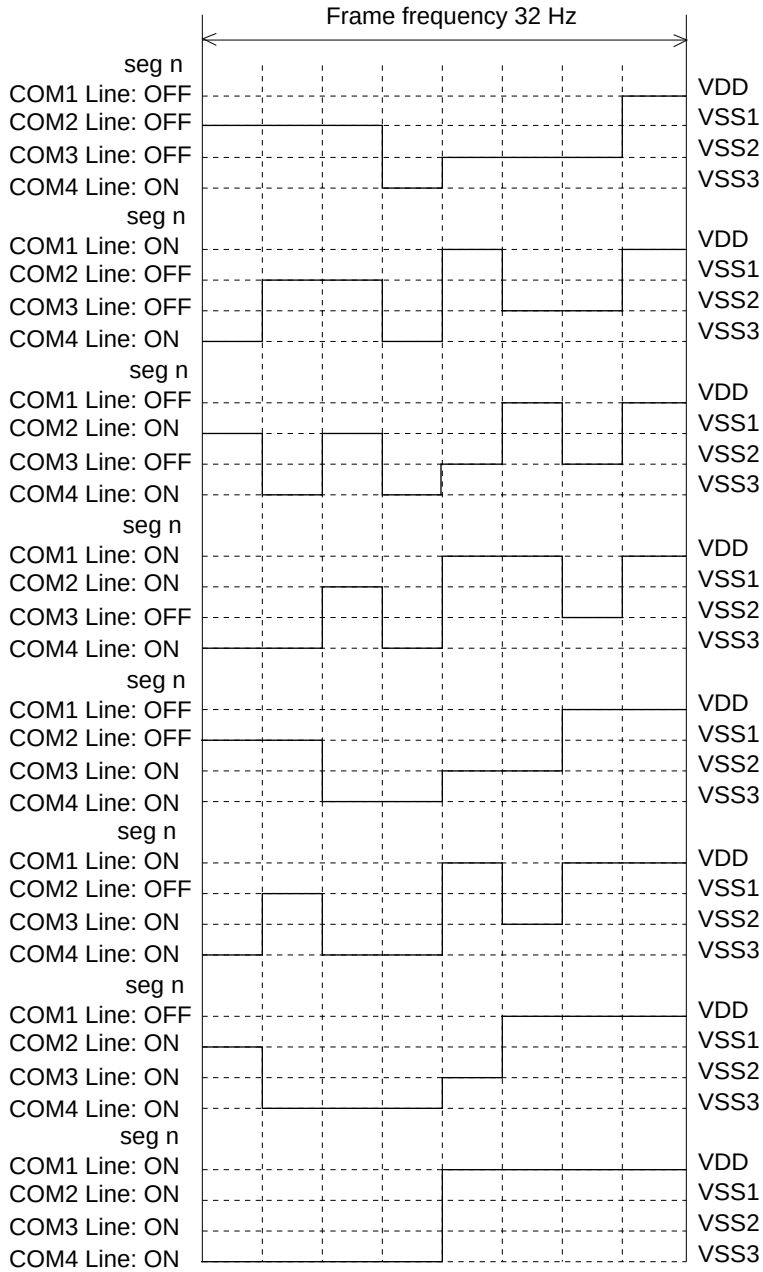


Figure 13-6 (c) 1/4 Duty Segment Driving Waveforms (1/3 bias)

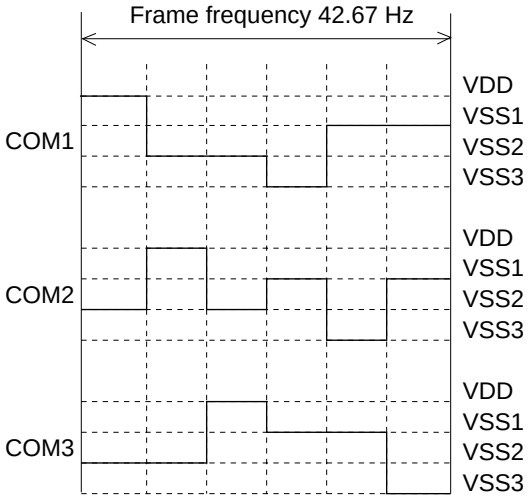


Figure 13-7 (a) 1/3 Duty Common Driving Waveforms (1/3 bias)

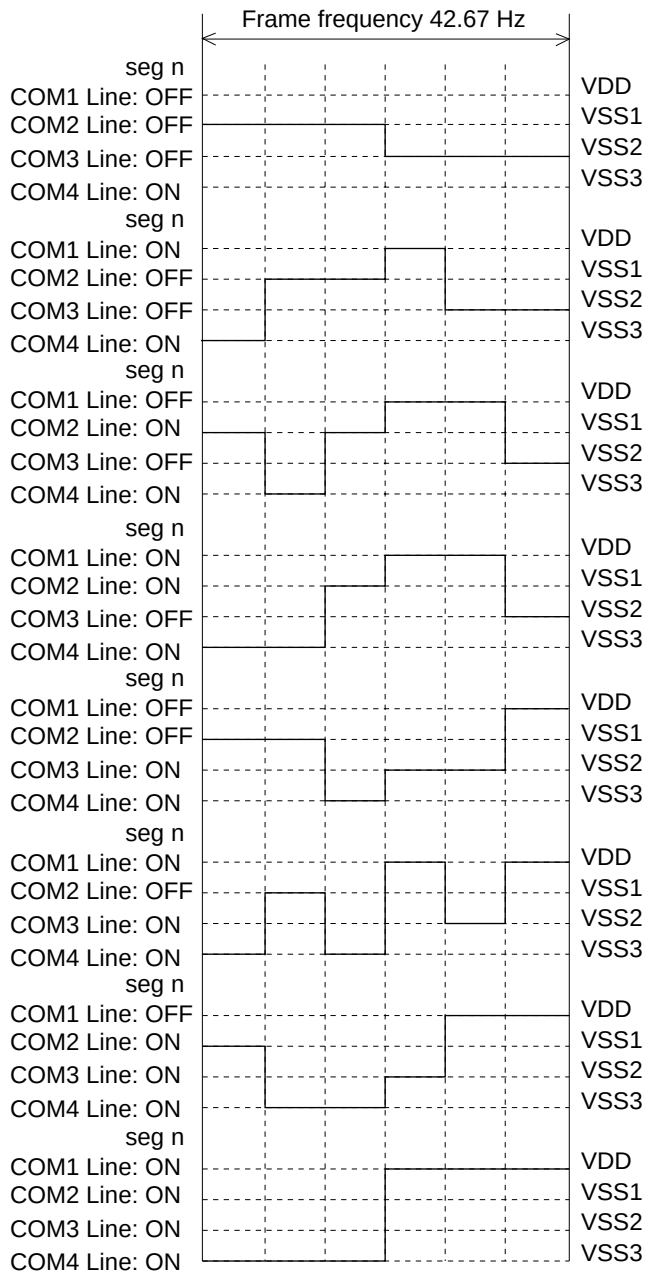


Figure 13-7 (b) 1/3 Duty Segment Driving Waveforms (1/3 bias)

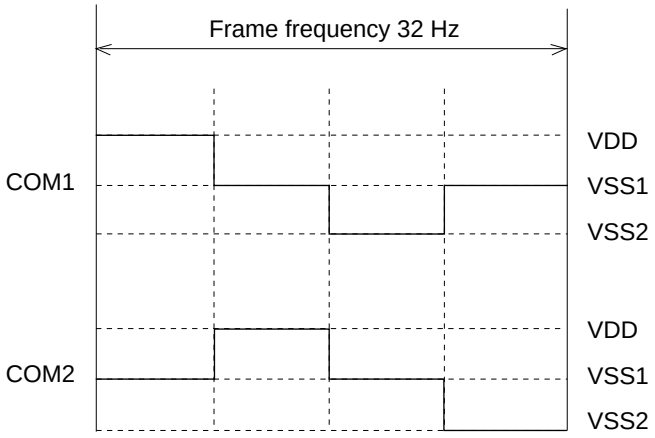


Figure 13-8 (a) 1/2 Duty Common Driving Waveforms (1/2 bias)

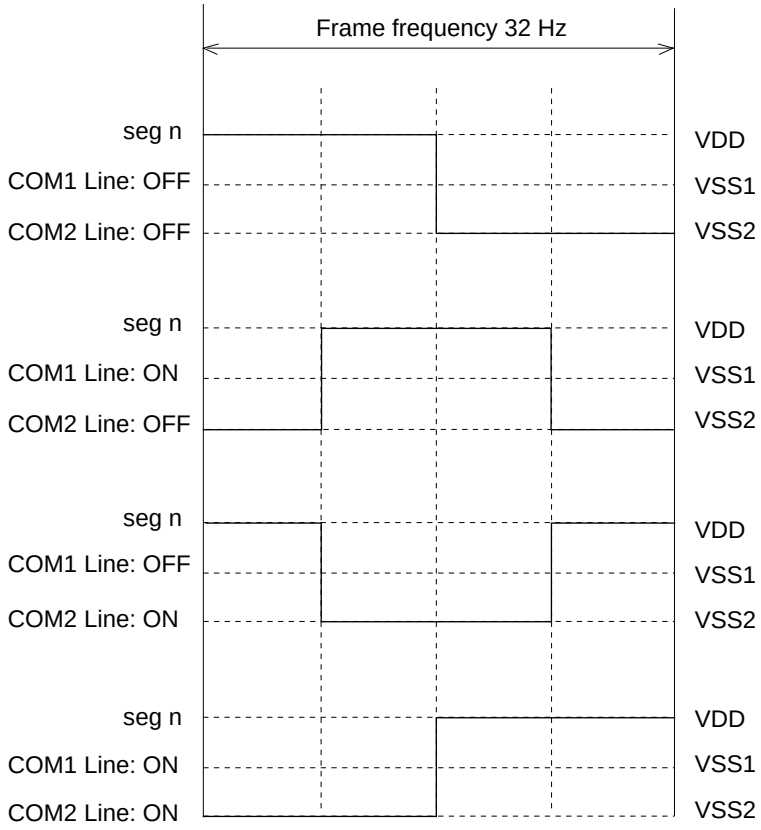


Figure 13-8 (b) 1/2 Duty Segment Driving Waveforms (1/2 bias)

Tables 13-1 and 13-2 (a), (b) show LCD driver-related registers and pins.

Table 13-1 LCD Driver-Related Registers

Register Name	Symbol	Address	R/W	Initial Value at System Reset
Display Control Register	DSPCON	1EH	R/W	8H
Display Register 0	DSPR0	40H	R/W	0H
Display Register 1	DSPR1	41H	R/W	0H
Display Register 2	DSPR2	42H	R/W	0H
Display Register 3	DSPR3	43H	R/W	0H
Display Register 4	DSPR4	44H	R/W	0H
Display Register 5	DSPR5	45H	R/W	0H
Display Register 6	DSPR6	46H	R/W	0H
Display Register 7	DSPR7	47H	R/W	0H
Display Register 8	DSPR8	48H	R/W	0H
Display Register 9	DSPR9	49H	R/W	0H
Display Register 10	DSPR10	4AH	R/W	0H
Display Register 11	DSPR11	4BH	R/W	0H
Display Register 12	DSPR12	4CH	R/W	0H
Display Register 13	DSPR13	4DH	R/W	0H
Display Register 14	DSPR14	4EH	R/W	0H
Display Register 15	DSPR15	4FH	R/W	0H
Display Register 16	DSPR16	50H	R/W	0H
Display Register 17	DSPR17	51H	R/W	0H
Display Register 18	DSPR18	52H	R/W	0H
Display Register 19	DSPR19	53H	R/W	0H
Display Register 20	DSPR20	54H	R/W	0H
Display Register 21	DSPR21	55H	R/W	0H
Display Register 22	DSPR22	56H	R/W	0H
Display Register 23	DSPR23	57H	R/W	0H
Display Register 24	DSPR24	58H	R/W	0H
Display Register 25	DSPR25	59H	R/W	0H
Display Register 26	DSPR26	5AH	R/W	0H
Display Register 27	DSPR27	5BH	R/W	0H
Display Register 28	DSPR28	5CH	R/W	0H
Display Register 29	DSPR29	5DH	R/W	0H
Display Register 30	DSPR30	5EH	R/W	0H

Note: Display registers 0 to 30 cannot be used unless selected by mask option.

Table 13-2 LCD Driver-Related Pins

Pin Name	Pin No.		Pad No.	Input/ Output	Remarks
	GA	TB			
VSS1	39	37	39	–	Bias output for LCD drive (–1.5 V)
VSS2	35	33	35	–	Negative power supply (–3.0 V)
VSS3	38	36	38	–	Bias output for LCD drive (–4.5 V)
C1	37	35	37	–	Capacitor connection pin for
C2	36	34	36	–	LCD drive bias generation
L0/P3.0	79	77	79	Output	LCD driver output pins.
L1/P3.1	80	78	80	Output	These becomes output port by mask
L2/P3.2	1	79	1	Output	option.
L3/P3.3	2	80	2	Output	
L4/P4.0	3	1	3	Output	
L5/P4.1	4	2	4	Output	
L6/P4.2	5	3	5	Output	
L7/P4.3	6	4	6	Output	
L8	7	5	7	Output	LCD driver output pins.
L9	8	6	8	Output	
L10	9	7	9	Output	
L11	10	8	10	Output	
L12	11	9	11	Output	
L13	12	10	12	Output	
L14	13	11	13	Output	
L15	14	12	14	Output	
L16	15	13	15	Output	
L17	16	14	16	Output	
L18	17	15	17	Output	
L19	18	16	18	Output	
L20	19	17	19	Output	
L21	20	18	20	Output	
L22	21	19	21	Output	
L23	22	20	22	Output	
L24	23	21	23	Output	
L25	24	22	24	Output	
L26	25	23	25	Output	
L27	26	24	26	Output	
L28	27	25	27	Output	
L29	28	26	28	Output	
L30	29	27	29	Output	

Chapter 14

Constant Voltage Generation Circuit (VR)

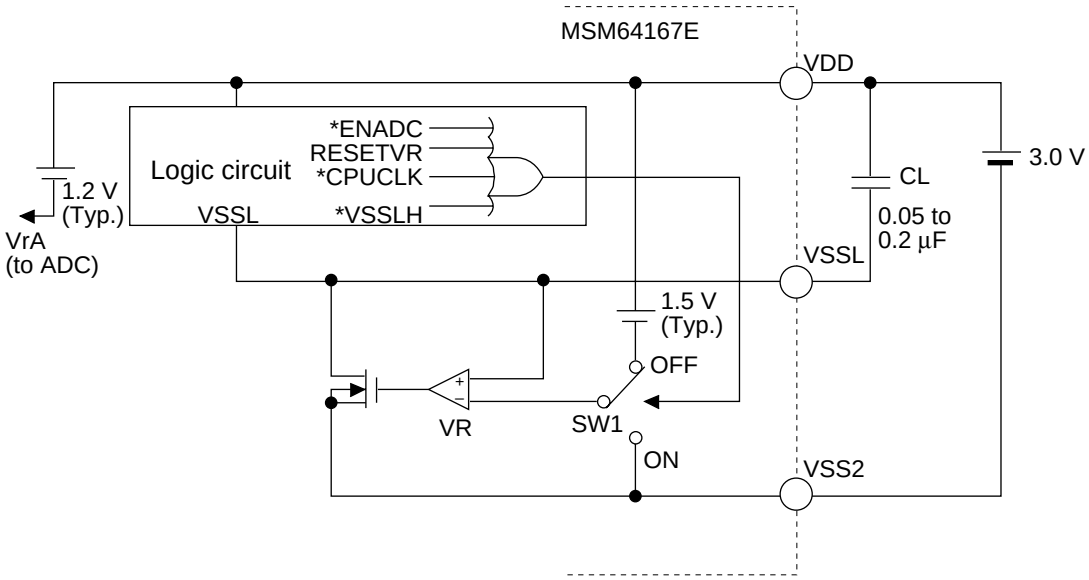
Chapter 14 Constant Voltage Generation Circuit (VR)

14.1 Overview

The MSM64167E has two built-in constant voltage generation circuits (VRs).

14.2 Configuration of Constant Voltage Generation Circuit

Figure 14-1 shows the configuration of the constant voltage generation circuit.



* ENADC, CPULCK and VSSLH indicate output of the SFR.

Figure 14-1 Constant Voltage Generation Circuit

In Figure 14-1, the "CL" capacitor is a noise smoothening capacitor on the VSSL line of the logic circuit and it is necessary to install the capacitor of 0.05 µF to 0.2 µF externally. SW1 in the figure becomes ON state when (1) CPUCLK bit of the frequency control register selection is set to "1", (2) $\overline{\text{RESET}}$ pin is set to "L" level, (3) the VSSLH bit of VSSL control register is set to "1", (4) the ENADC bit of AD control register 1 is set to "1" or (5) power ON is detected.

14.3 Operation of Constant Voltage Generation Circuit

The constant voltage generation circuit (VR) is generated when VDD – 1.5 V of constant voltage VSSL is used as the internal logic circuit. VDD – 1.2 V of constant voltage VrA is the reference power supply for the A/D converter.

VSSL level becomes VSS2 level if reset signal RESETVR of the constant voltage generation circuit is "1" (power ON detection signal is "1", or ($\overline{\text{RESET}}$) pin is "0"). It normally becomes VDD – 1.5 V if reset is cleared and RESETVR becomes "0", but becomes VSS2 level if the 700 kHz RC oscillation circuit is operated if CPUCLK is set to "1", if the VSSLH bit of the VSSL control register is set to "1", or if the ENADC bit of AD control register is set to "1".

VrA level becomes VDD – 1.2 V if the ENADC bit of the AD control register is set to "1", otherwise it becomes VDD level.

Table 14-1 shows the differences in power levels by RESETVR, CPUCLK, VSSLH and ENADC. Figure 14-2 shows the VSSL output status.

Table 14-1 Difference of Power Levels by RESETVR, CPUCLK, and VSSLH, and ENADC

RESETVR	ENADC	CPUCLK	VSSLH	Internal Logic Power Supply (VSSL)
1	–	–	–	VSS2
0	0	0	0	VDD – 1.5 V
0	–	–	1	VSS2
0	–	1	–	VSS2
0	1	–	–	VSS2

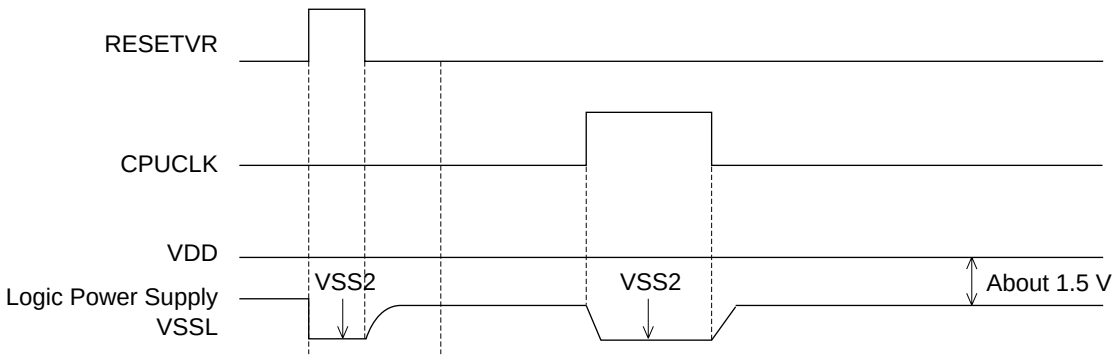
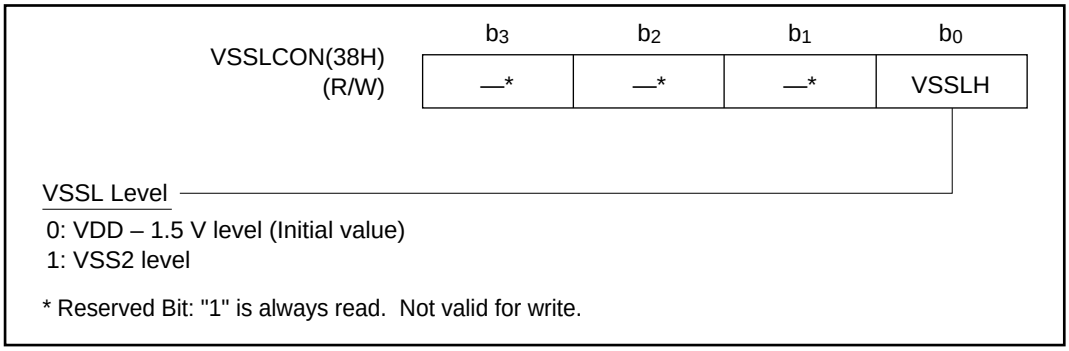


Figure 14-2 VSSL Output Status

14.4 VSSL Control Register (VSSLCON)

The VSSL control register (VSSLCON) is a 4-bit special function register (SFR) that controls the output voltage level of VSSL, an output of the constant voltage generation circuit.



Bit 0: VSSLH

Flag to select the output voltage level of VSSL, an output of the constant voltage generation circuit (VR). If VSSLH is reset to "0", VSSL output becomes VDD – 1.5 V, and if VSSLH is set to "1", VSSL output becomes VSS2 level. VSSLH is reset to "0" at system reset. However when the constant voltage generation circuit is reset, and when the system clock is set to 700 kHz, VSSL output becomes VSS2 level, regardless of the bit setting.

Chapter 15

Test Circuit (TST)

Chapter 15 Test Circuit (TST)

15.1 Overview

The MSM64167E has an internal test circuit (TST) that outputs CMP output of the A/D converter or the 700 kHz RC oscillation clock of the system clock generation part to the BD pin using test pins ($\overline{TST1}$) and ($\overline{TST2}$). With this test mode, the conversion characteristics of the A/D converter and the frequency of the RC oscillation clock can be checked.

15.2 Operation in ADC Test Mode

When "L" is input to $\overline{RESET}$ pin with $\overline{TST1}$ and VSS1 pins in "L" level, $\overline{TST2}$ pin in "H" level, and $\overline{RESET}$ pin connected to XT pin with the status enters system reset mode. Then when the $\overline{RESET}$ pin is set to "H" level, the status enters ADC test mode.

Figure 15-1 shows operation in ADC test mode

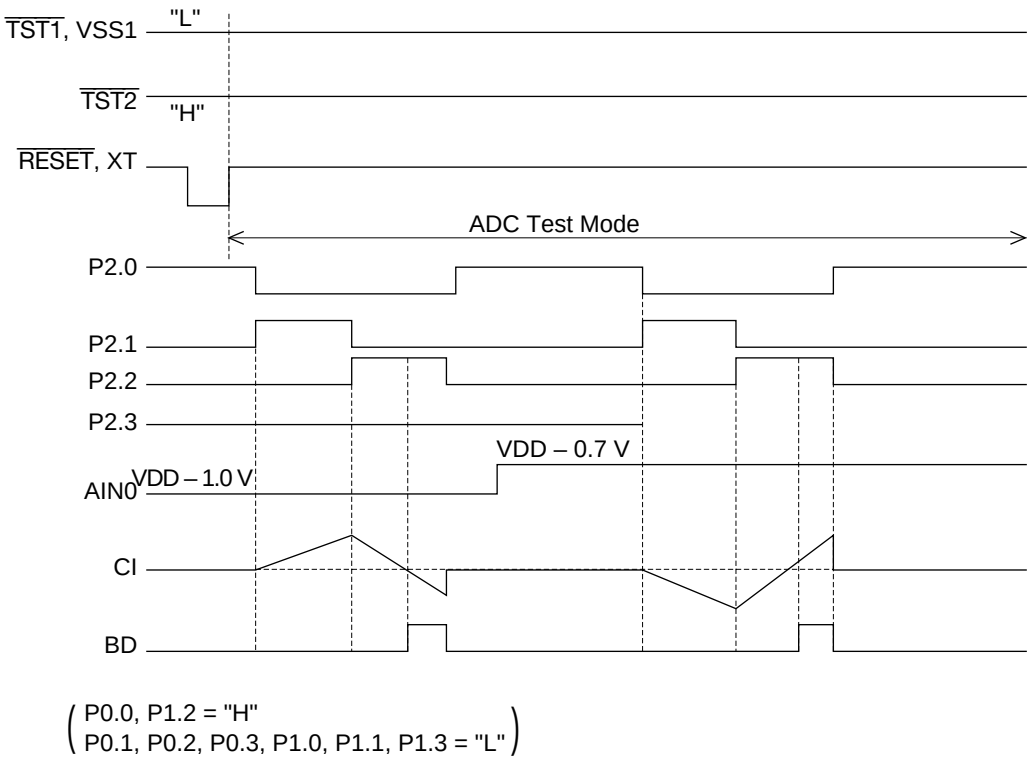


Figure 15-1 Operation in ADC Test Mode

In ADC test mode, the operation of the A/D converter is controlled by the 12 inputs of Ports 0–2. The comparator output (CMP) signal of the double integral circuit is output to the BD pin. Table 15-1 shows the function of each port in ADC test mode.

Table 15-1 Function of Each Port in ADC Test Mode

Pin Name	Pin No.		Pad No.	Input/Output	Remarks
	GA	TB			
P0.0	67	65	67	I	Same function of bit 0 of AD control register 0
P0.1	68	66	68	I	Same function of bit 1 of AD control register 0
P0.2	69	67	69	I	Same function of bit 2 of AD control register 0
P0.3	70	68	70	I	Same function of bit 3 of AD control register 0
P1.0	71	69	71	I	Same function of bit 0 of AD control register 1
P1.1	72	70	72	I	Same function of bit 1 of AD control register 1
P1.2	73	71	73	I	Same function of bit 2 of AD control register 1
P1.3	74	72	74	I	Same function of bit 3 of AD control register 1
P2.0	75	73	75	I	When "1" integral input voltage is Vg
P2.1	76	74	76	I	When "1" integral input voltage is Vin
P2.2	77	75	77	I	When "1" integral input voltage is VrP
P2.3	78	76	78	I	When "1" integral input voltage is VrN

Note: Do not set two pins or more of P2.0–P2.3 to "H" in ADC test mode.

15.3 Operation in RC Oscillation Test Mode

When "L**"** is input to $\overline{\text{RESET}}$ pin with $\overline{\text{TST1}}$, $\overline{\text{TST2}}$ and $\overline{\text{XT}}$ pins in "L", the status enters system reset mode. Then when the $\overline{\text{RESET}}$ is set to "H" level, the status enters RC oscillation test mode.

In RC oscillation test mode, the 700 kHz RC oscillation clock is output to the BD terminal without division. At this time it is not necessary to set the CPUCLK bit of the frequency control register to "1".

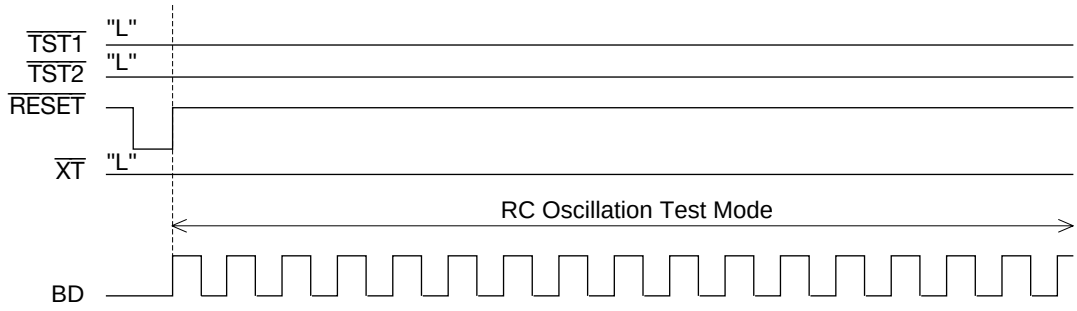


Figure 15-2 Operation in RC Oscillation Test Mode

Appendixes

Appendix A List of Special Function Registers

Register Name	Symbol	Address	Bit Configuration				R/W	Byte Access	Value at System Reset	Reference (Chapter)
			b3	b2	b1	b0				
Port 0 Register	P0	00H	P03	P01	P01	P00	R/W	Yes	0	See Chapter 7
Port 1 Register	P1	01H	P13	P12	P11	P10	R/W		0	See Chapter 7
Port 2 Register	P2	02H	P23	P22	P21	P20	R/W	Yes	0	See Chapter 7
		03H								
		04H								
		05H								
		06H								
		07H								
VSSL Control Register	VSSLCON	08H	—*	—*	—*	VSSLH	R/W	No	0EH	See Chapter 14
Frequency Control Register	FCON	09H	—*	—*	—*	CPUCLK	R/W		0EH	See Chapter 5
Buzzer Driver Control Register	BDCON	0AH	SELF	EBD	BM1	BM0	R/W	Yes	0H	See Chapter 10
Buzzer Frequency Control Register	BFCON	0BH				BF	R/W		0EH	See Chapter 10
		0CH								
		0DH								
		0EH						No		
Time Base Counter Register	TBCR	0FH	1 Hz	2 Hz	4 Hz	8 Hz	R/W		0H	See Chapter 6
Port 00 Control Register	P00CON	10H	P00IE	P00F	P00DIR	P00MOD	W	Yes	0	See Chapter 7
Port 01 Control Register	P01CON	11H	P01IE	P01F	P01DIR	P01MOD	W		0	See Chapter 7
Port 02 Control Register	P02CON	12H	P02IE	P02F	P02DIR	P02MOD	W	Yes	0	See Chapter 7
Port 03 Control Register	P03CON	13H	P03IE	P03F	P03DIR	P03MOD	W		0	See Chapter 7
Port 10 Control Register	P10CON	14H	P10IE	P10F	P10DIR	P10MOD	W	Yes	0	See Chapter 7
Port 11 Control Register	P11CON	15H	P11IE	P11F	P11DIR	P11MOD	W		0	See Chapter 7
Port 12 Control Register	P12CON	16H	P12IE	P12F	P12DIR	P12MOD	W	Yes	0	See Chapter 7
Port 13 Control Register	P13CON	17H	P13IE	P13F	P13DIR	P13MOD	W		0	See Chapter 7
Port 20 Control Register	P20CON	18H	P20IE	TXC	P20DIR	P20MOD	W	Yes	0	See Chapter 7
Port 21 Control Register	P21CON	19H	P21IE	RXC	P21DIR	P21MOD	W		0	See Chapter 7
Port 22 Control Register	P22CON	1AH	P21IE	TXD	P22DIR	P22MOD	W	Yes	0	See Chapter 7
Port 23 Control Register	P23CON	1BH	P23IE	TMO	P23DIR	P23MOD	W		0	See Chapter 7
Port Control Register	PCON	1CH				PUD	W	Yes	0EH	See Chapter 7
		1DH								
Display Control Register	DSPCON	1EH	—*	LCDOFF	DUTY1	DUTY0	R/W	Yes	8H	See Chapter 13
		1FH								

Register Name	Symbol	Address	Bit Configuration				R/W	Byte Access	Value at System Reset	Reference (Chapter)
			b3	b2	b1	b0				
Timer Data Register 0	TMD0	20H	TD3	TD2	TD1	TD0	R/W	Yes	Undefined	See Chapter 8
Timer Data Register 1	TMD1	21H	TD7	TD6	TD5	TD4	R/W		Undefined	See Chapter 8
Timer Data Register 2	TMD2	22H	TD11	TD10	TD9	TD8	R/W	Yes	Undefined	See Chapter 8
Timer Data Register 3	TMD3	23H	TD15	TD14	TD13	TD12	R/W		Undefined	See Chapter 8
Timer Counter Register 0	TMC0	24H	TC3	TC2	TC1	TC0	R/W	Yes	Undefined	See Chapter 8
Timer Counter Register 1	TMC1	25H	TC7	TC6	TC5	TC4	R/W		Undefined	See Chapter 8
Timer Counter Register 2	TMC2	26H	TC11	TC10	TC9	TC8	R/W	Yes	Undefined	See Chapter 8
Timer Counter Register 3	TMC3	27H	TC15	TC14	TC13	TC12	R/W		Undefined	See Chapter 8
Timer Control Register 0	TMCON0	28H	—*	ECAP	FMEAS	TMRUN	R/W	Yes	8H	See Chapter 8
Timer Control Register 1	TMCON1	29H	—*	—*	CL1	CL0	W		0CH	See Chapter 8
Timer Status Regiser	TMSTAT	2AH	—*	—*	TMOVF	CAPF	R	Yes	0EH	See Chapter 8
		2BH								
AD Control Register 0	ADCON0	2CH	ICH1	ICH0	CH1	CH0	R/W	Yes	0H	See Chapter 12
AD Control Register 1	ADCON1	2DH	ENOPA	ENADC	SOPP0		R/W		1H	See Chapter 12
(Disabled)		2EH	—*				R/W	Yes	8H	
AD Status Register	ADSTAT	2FH	ADPOL	ADOVF	ADST1	ADST0	R		0H	See Chapter 12
Interrupt Enable Register 0	IE0	30H	EAD	E32Hz	E16Hz	EIHZ	R/W	No	0H	See Chapter 4
Interrupt Request Register 0	IRQ0	31H	QAD	Q32Hz	Q16Hz	Q1Hz	R/W		0H	See Chapter 4
Interrupt Enable Register 1	IE1	32H	ESR	EST	EXI1	ETM	R/W	No	0H	See Chapter 4
Interrupt Request Register 1	IRQ1	33H	QSR	QST	QXI1	QTM	R/W		0H	See Chapter 4
Interrupt Enable Register 2	IE2	34H	—*	—*	—*	EXI0	R/W	No	0EH	See Chapter 4
Interrupt Request Register 2	IRQ2	35H	—*	—*	QWDT	QXI0	R/W		0CH	See Chapter 4
		36H								
		37H								
Watchdog Timer Control Register	WDTCON	38H	d3	d2	d1	d0	W	Yes		See Chapter 11
		39H								
		3AH								
		3BH								
		3CH								
		3DH								
		3EH								
		3FH								

Note: Address 2EH is disabled. Do not write "1" to any bit at address 2EH. However, "0" can be written to the register bits upon initialization of the register. (Writing "0" does not affect microcontroller operation.)

Register Name	Symbol	Address	Bit Configuration				R/W	Byte Access	Value at System Reset	Reference (Chapter)
			b3	b2	b1	b0				
Display Register 0	DSPR0	40H	d	c	b	a	R/W	Yes	0H	See Chapter 13
Display Register 1	DSPR1	41H	d	c	b	a	R/W		0H	See Chapter 13
Display Register 2	DSPR2	42H	d	c	b	a	R/W	Yes	0H	See Chapter 13
Display Register 3	DSPR3	43H	d	c	b	a	R/W		0H	See Chapter 13
Display Register 4	DSPR4	44H	d	c	b	a	R/W	Yes	0H	See Chapter 13
Display Register 5	DSPR5	45H	d	c	b	a	R/W		0H	See Chapter 13
Display Register 6	DSPR6	46H	d	c	b	a	R/W	Yes	0H	See Chapter 13
Display Register 7	DSPR7	47H	d	c	b	a	R/W		0H	See Chapter 13
Display Register 8	DSPR8	48H	d	c	b	a	R/W	Yes	0H	See Chapter 13
Display Register 9	DSPR9	49H	d	c	b	a	R/W		0H	See Chapter 13
Display Register 10	DSPR10	4AH	d	c	b	a	R/W	Yes	0H	See Chapter 13
Display Register 11	DSPR11	4BH	d	c	b	a	R/W		0H	See Chapter 13
Display Register 12	DSPR12	4CH	d	c	b	a	R/W	Yes	0H	See Chapter 13
Display Register 13	DSPR13	4DH	d	c	b	a	R/W		0H	See Chapter 13
Display Register 14	DSPR14	4EH	d	c	b	a	R/W	Yes	0H	See Chapter 13
Display Register 15	DSPR15	4FH	d	c	b	a	R/W		0H	See Chapter 13
Display Register 16	DSPR16	50H	d	c	b	a	R/W	Yes	0H	See Chapter 13
Display Register 17	DSPR17	51H	d	c	b	a	R/W		0H	See Chapter 13
Display Register 18	DSPR18	52H	d	c	b	a	R/W	Yes	0H	See Chapter 13
Display Register 19	DSPR19	53H	d	c	b	a	R/W		0H	See Chapter 13
Display Register 20	DSPR20	54H	d	c	b	a	R/W	Yes	0H	See Chapter 13
Display Register 21	DSPR21	55H	d	c	b	a	R/W		0H	See Chapter 13
Display Register 22	DSPR22	56H	d	c	b	a	R/W	Yes	0H	See Chapter 13
Display Register 23	DSPR23	57H	d	c	b	a	R/W		0H	See Chapter 13
Display Register 24	DSPR24	58H	d	c	b	a	R/W	Yes	0H	See Chapter 13
Display Register 25	DSPR25	59H	d	c	b	a	R/W		0H	See Chapter 13
Display Register 26	DSPR26	5AH	d	c	b	a	R/W	Yes	0H	See Chapter 13
Display Register 27	DSPR27	5BH	d	c	b	a	R/W		0H	See Chapter 13
Display Register 28	DSPR28	5CH	d	c	b	a	R/W	Yes	0H	See Chapter 13
Display Register 29	DSPR29	5DH	d	c	b	a	R/W		0H	See Chapter 13
Display Register 30	DSPR30	5EH	d	c	b	a	R/W	Yes	0H	See Chapter 13
		5FH								

Register Name	Symbol	Address	Bit Configuration				R/W	Byte Access	Value at System Reset	Reference (Chapter)
			b3	b2	b1	b0				
Transmit Control Register (L)	STCONL	60H	STSTB	STL0	STL1	STMOD	R/W	Yes	0H	See Chapter 9
Transmit Control Register (H)	STCONH	61H	STLMB	STPOE	STPEN	STCLK	R/W		0H	See Chapter 9
Transmit Buffer Register (L)	STBUFL	62H	TB3	TB2	TB1	TB0	R/W	Yes	0H	See Chapter 9
Transmit Buffer Register (H)	STBUFH	63H	TB7	TB6	TB5	TB4	R/W		0H	See Chapter 9
Receive Control Register (L)	SRCONL	64H	SREN	SRL0	SRL1	SRMOD	R/W	Yes	0H	See Chapter 9
Receive Control Register (H)	SRCONH	65H	SRLMB	SRPOE	SRPEN	SRCLK	R/W		0H	See Chapter 9
Receive Buffer Register (L)	SRBUFL	66H	RB3	RB2	RB1	RB0	R	Yes	0H	See Chapter 9
Receive Buffer Register (H)	SRBUFH	67H	RB7	RB6	RB5	RB4	R		0H	See Chapter 9
Receive Baud Rate Setting Register	SRBRT	68H	—*	—*	BRT0	BRT1	R/W	No	0CH	See Chapter 9
Serial Port Status Register	SSTAT	69H	BFULL	PERR	OERR	FERR	R		0H	See Chapter 9
		6AH								
		6BH								
		6CH								
		6DH								
		6EH								
		6FH								
		70H								
		71H								
		72H								
		73H								
		74H								
		75H								
		76H								
		77H								
		78H								
		79H								
		7AH								
		7BH								
Master Interrupt Enable Register	MIEF	7CH	—*	—*	—*	MI		No	0EH	See Chapter 4
Halt Mode Register	HALT	7DH	—*	—*	—*	HLT			0EH	See Chapter 3
Stack Pointer	SP	7EH	SP3	SP2	SP1	—*	R/W	Byte access only	0FFH	See Chapter 2
		7FH	—*	SP6	SP5	SP4				

Notes:

(1) A stack pointer can be byte accessed only.

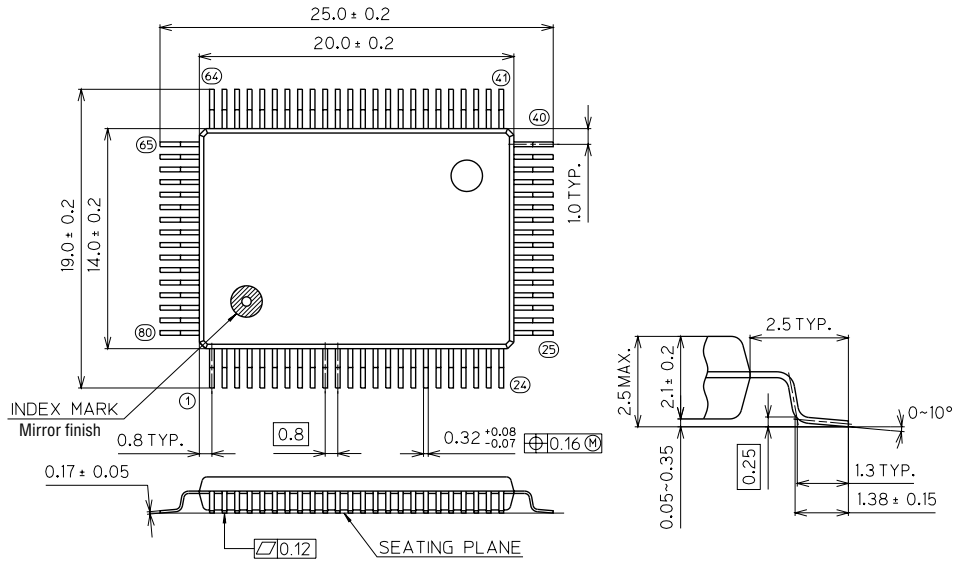
(2) "—*" in the table indicates a reserved bit. When it is read, "1" is always read. Writing is invalid.

(3) Display register DSPR0 to 30 cannot be used unless selected by mask option. When an open display register is used for a purpose other than display, specify the display register in the LCD mask option table. (See [Note] (5) in "Appendix F: Mask Options".)

Appendix B Package Dimensions

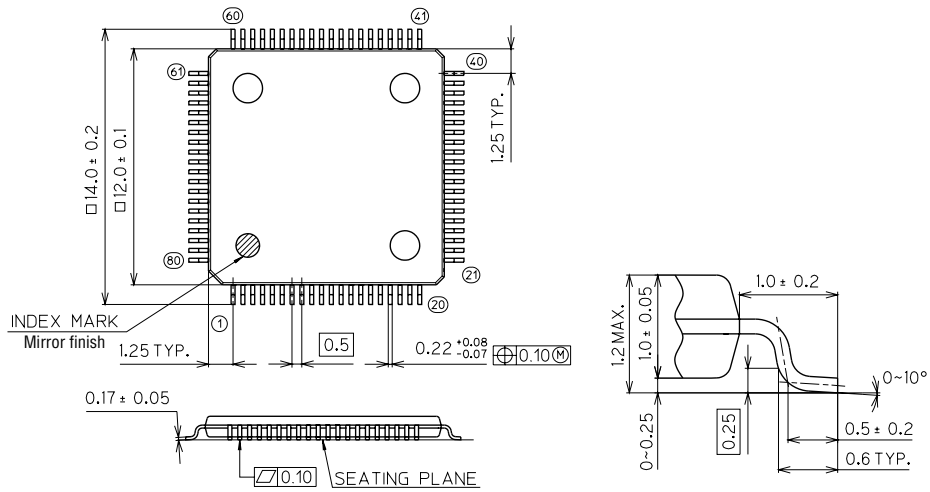
MSM64167E-xxxGA

(Unit: mm)



MSM64167E-xxxTB

(Unit: mm)



Appendix C Bonding Pad Coordinates

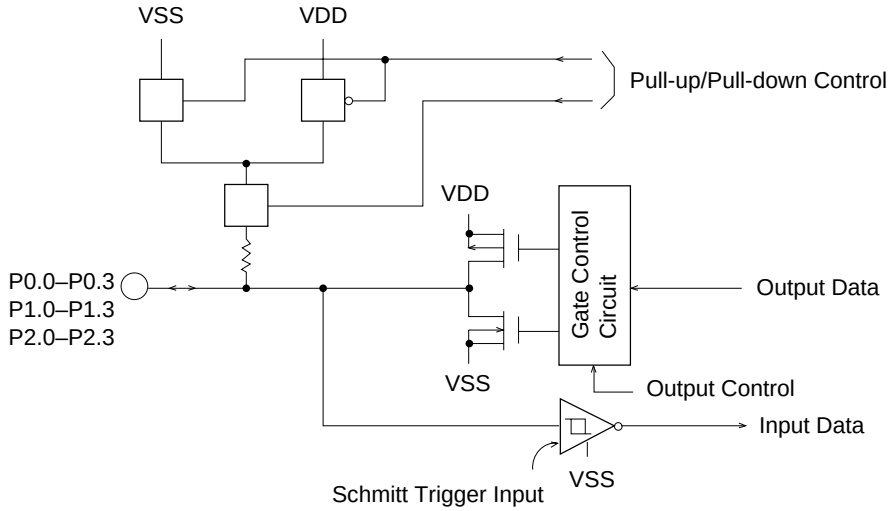
MSM64167E-xxx (Bonding pad size: 110 μm × 110 μm)

Center of chip: x = 0, y = 0

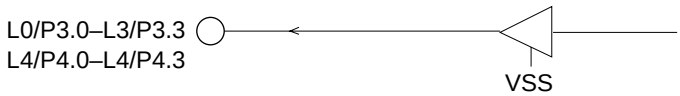
Pad No.	Pin Name	Coordinate (μm)		Pad No.	Pin Name	Coordinate (μm)	
		x	y			x	y
1	L2/P3.2	–2593	–2155	41	$\overline{TST1}$	2766	1946
2	L3/P3.3	–2304	–2155	42	$\overline{TST2}$	2660	2155
3	L4/P4.0	–1842	–2155	43	$\overline{RESET}$	2394	2155
4	L5/P4.1	–1626	–2155	44	VSSL	2211	2155
5	L6/P4.2	–1430	–2155	45	VOF	1899	2113
6	L7/P4.3	–1234	–2155	46	VDDA	1598	2113
7	L8	–1038	–2155	47	VrA	1294	2113
8	L9	–856	–2155	48	AIN0	991	2113
9	L10	–664	–2155	49	AIN1	688	2155
10	L11	–468	–2155	50	AIN2	506	2155
11	L12	–272	–2155	51	AIN3	324	2155
12	L13	–76	–2155	52	RA	142	2155
13	L14	143	–2155	53	RI	–40	2155
14	L15	367	–2155	54	RCM	–222	2155
15	L16	591	–2155	55	CZ1	–402	2155
16	L17	874	–2155	56	CI	–586	2155
17	L18	1056	–2155	57	CZ2	–768	2155
18	L19	1280	–2155	58	VG	–1016	2155
19	L20	1504	–2155	59	OPO0	–1246	2155
20	L21	1728	–2155	60	OPN0	–1498	2155
21	L22	1952	–2155	61	OPP0	–1749	2155
22	L23	2176	–2155	62	OPO1	–2001	2155
23	L24	2624	–2155	63	OPN1	–2253	2155
24	L25	2766	–1862	64	OPP1	–2625	2155
25	L26	2766	–1638	65	VSSA	–2766	1960
26	L27	2766	–1414	66	VSS	–2766	1708
27	L28	2766	–1190	67	P0.0	–2766	1456
28	L29	2766	–966	68	P0.1	–2766	1204
29	L30	2766	–742	69	P0.2	–2766	952
30	OSC2	2766	–518	70	P0.3	–2766	700
31	OSC1	2766	–336	71	P1.0	–2766	448
32	VDD	2766	–132	72	P1.1	–2766	196
33	$\overline{XT}$	2766	154	73	P1.2	–2766	–56
34	XT	2766	378	74	P1.3	–2766	–308
35	VSS2	2766	602	75	P2.0	–2766	–560
36	C2	2766	826	76	P2.1	–2766	–812
37	C1	2766	1050	77	P2.2	–2766	–1064
38	VSS3	2766	1232	78	P2.3	–2766	–1316
39	VSS1	2766	1456	79	L0/P3.0	–2766	–1568
40	BD	2766	1694	80	L1/P3.1	–2766	–1834

Appendix D Configuration of Input/Output Circuit

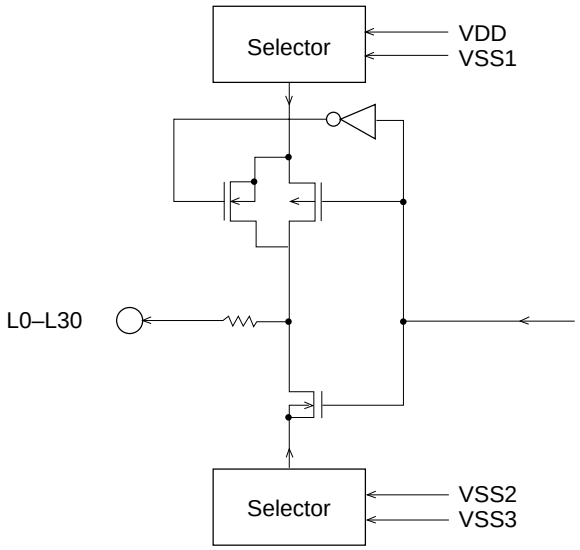
A. Input/Output Ports (P0.0–P0.3, P1.0–P1.3, P2.0–P2.3)



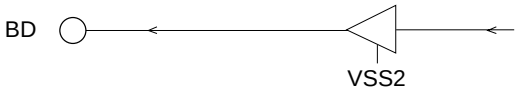
B. Output Ports: (L0/P3.0–L3/P3.3, L4/P4.0–L7/P4.3 terminals during mask option.)



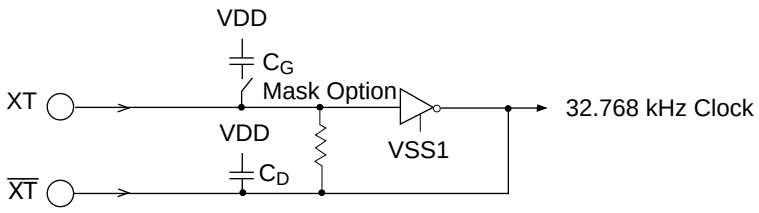
C. L0–L30 Output



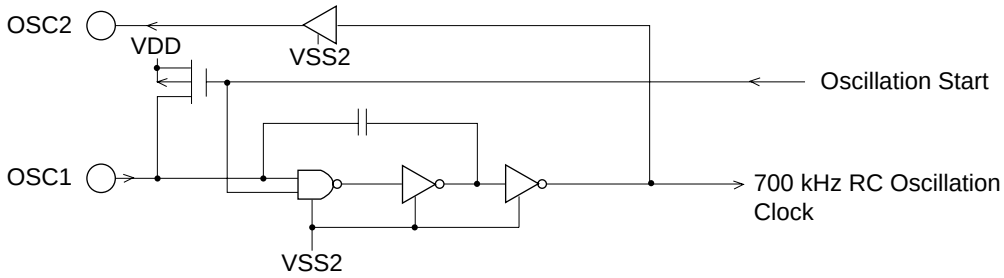
D. BD Output



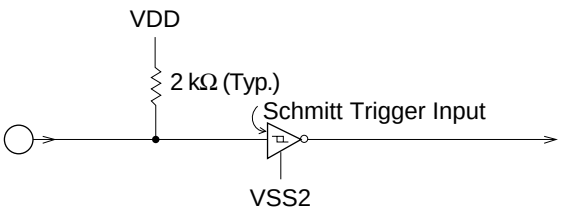
E. Crystal Oscillation Circuit



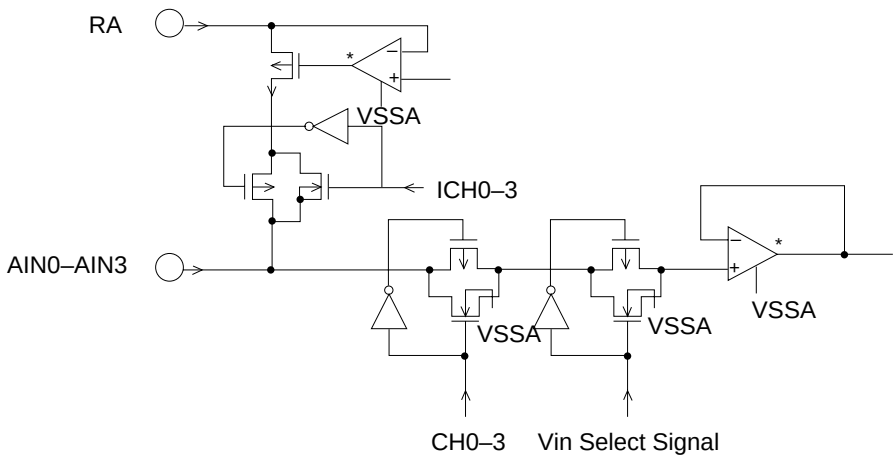
F. 700 kHz RC Oscillation Circuit



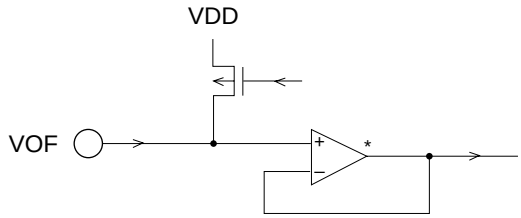
G. $\overline{RESET}$, $\overline{TST1}$, $\overline{TST2}$ Input



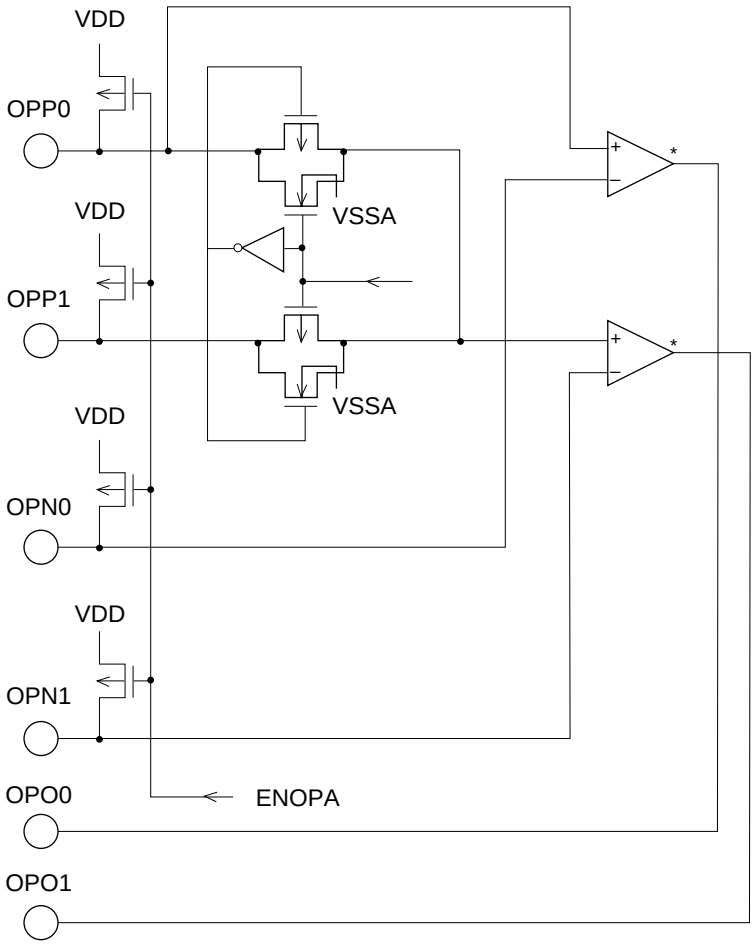
H. AIN0–AIN3, RA Input



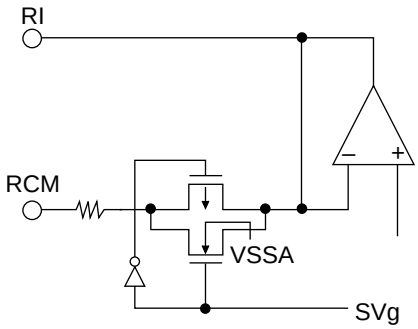
I. VOF Input



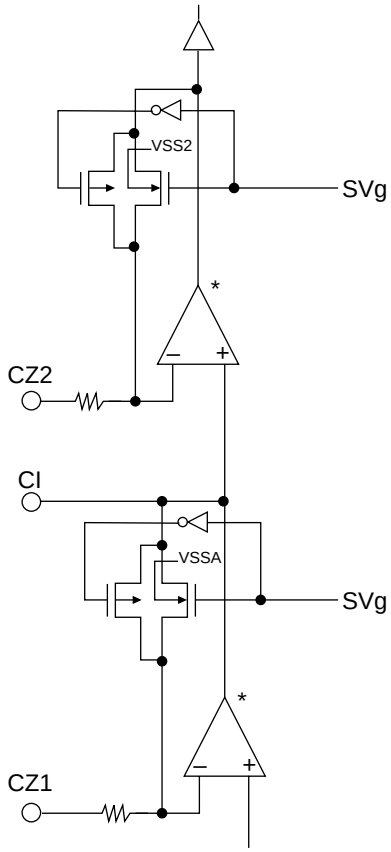
J. OPP0, OPP1, OPN0, OPN1, OPO0, OPO1



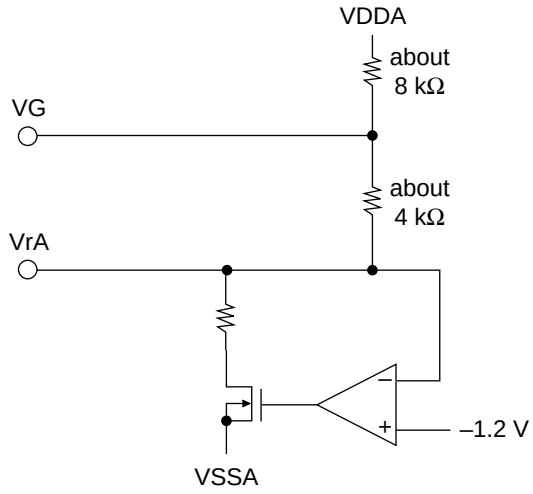
K. RCM, RI



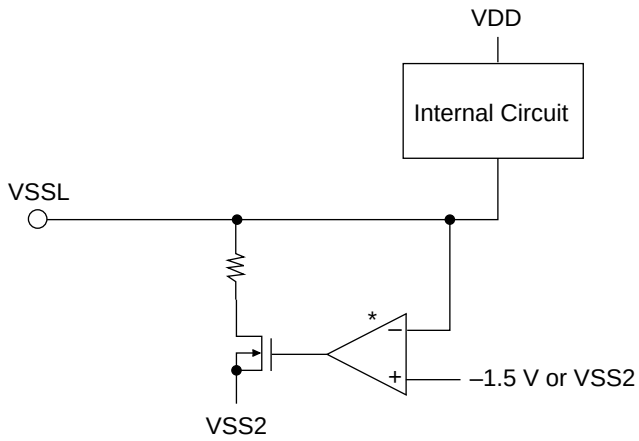
L. CZ1, CZ2, CI



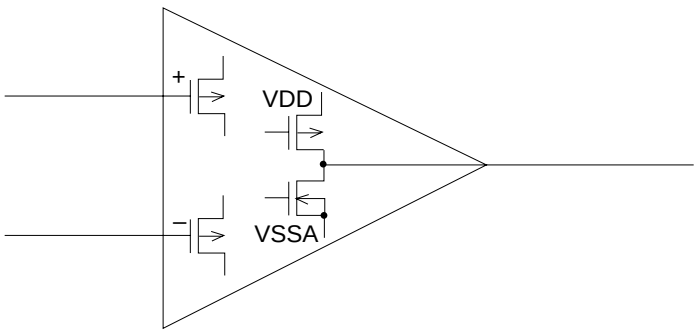
M. VrA, VG



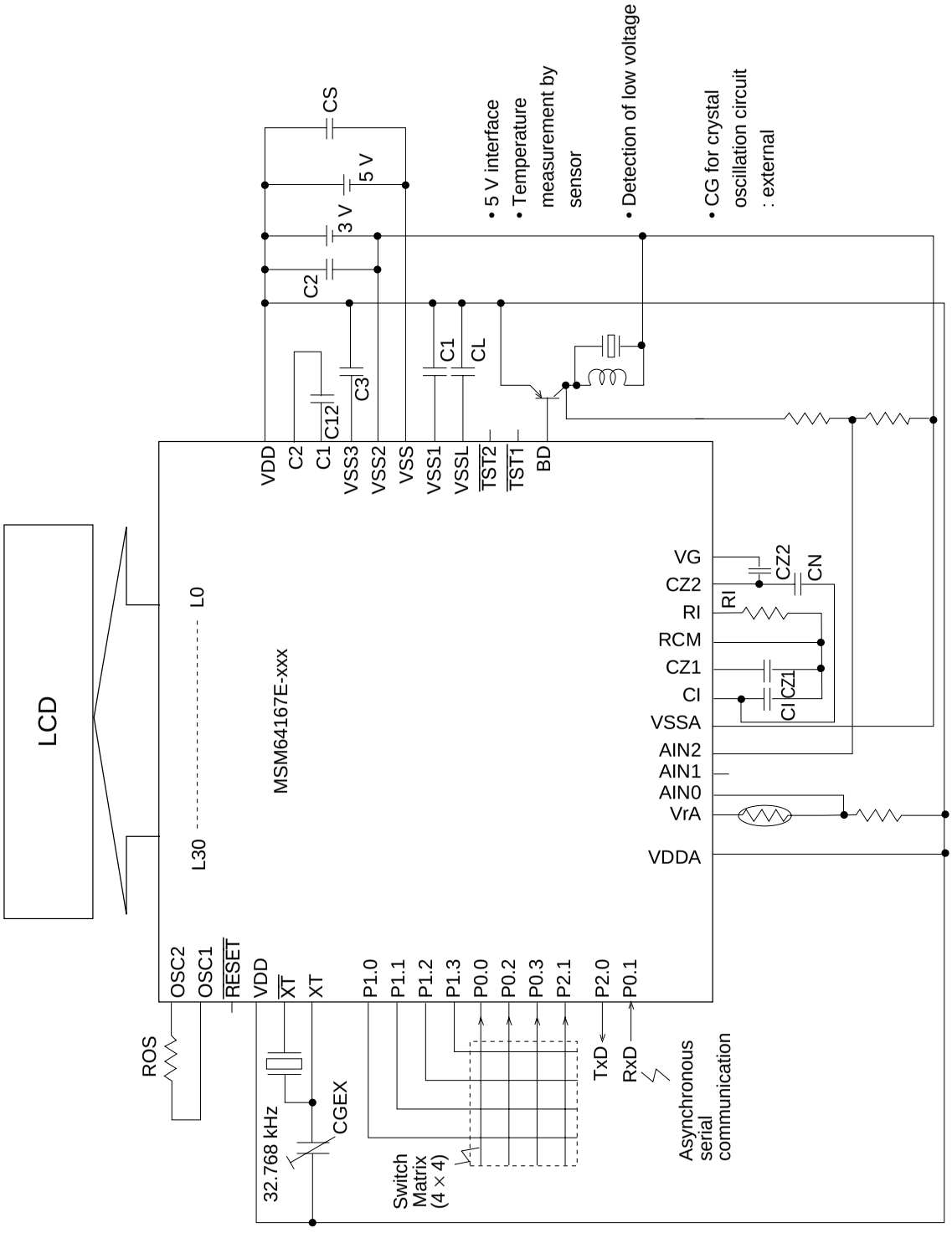
N. VSSL



Note:
Configuration of input/output circuit of amplifier indicated by "*" in above figures is shown below.



Appendix E Example of Applied Circuit



Appendix F Mask Options

- **CG Select Mask Option Table**

Item	Mask Specification	Select
CG of Crystal Oscillator	Internal	
	External	

- **LCD Driver Mask Option Table**

[Description of symbols used in LCD driver mask option table.]

SEG ..... LCD driver pin name

SIGNAL ..... Common signal name or each segment name. Write names corresponding to each common signal COM1, COM2, COM3 and COM4 from the left. If not used, leave the section blank.

C/S/P ..... If L0 to L30 of LCD driver are used as segment drivers, write "S", if used as common drivers, write "C", and if used as an output port, write "P". If not used leave the section blank.

DATA..... Write bit name (a, b, c, d) of display register for signal name. If not used leave the section blank.

DSPR ..... Write display register number (0 to 30).

Note:

(1) It is not necessary to use all display register numbers 0 to 30.

(2) It is acceptable to assign the same name (same display register number and bit name) for 2 or more segments.

(3) If "P" is selected, write 0 or 1 for DSPR. If "P" is selected, DATA and DSPR are assigned to the COM1 column. "P" can be selected only for L0 to L7 of the LCD driver.

(4) Create a mask option table using the MASK167 mask option generator. For details on input see the "MASK167 Mask Option Generator User's Manual".

(5) If a display register is used as a data register or flag, and not for display purposes, assign the display register to each bit using open segments in the LCD driver mask option table. If there are no open segments in the LCD mask option table, the display register cannot be used as a data register or flag.

[Example of LCD Driver Mask Option Table Creation]

1) When L0 is assigned to common 2, L1 to the segment, and L2 as the output port. (1/4 duty)

SEG	SIGNAL	C/S/P	COM1		COM2		COM3		COM4	
			DATA	DSPR	DATA	DSPR	DATA	DSPR	DATA	DSPR
L0	/COM2/ /	C								
L1	ALARM/MODE/ 4f / 4g	S	b	5	d	6	b	14	c	14
L2	OUT / / /	P	a	0						

2) When L27 is assigned to common 1, L28 to the segment, and L29 as unused. (1/4 duty)

SEG	SIGNAL	C/S/P	COM1		COM2		COM3		COM4	
			DATA	DSPR	DATA	DSPR	DATA	DSPR	DATA	DSPR
L27	COM1/ / /	C								
L28	1a / 1b / 1c / DP1	S	a	2	b	2	c	2	d	2
L29	/ / /									

Table of LCD Driver Mask Options (1/4 duty)

SEG	SIGNAL	C/S/P	COM1		COM2		COM3		COM4	
			DATA	DSPR	DATA	DSPR	DATA	DSPR	DATA	DSPR
L0	/ / /									
L1	/ / /									
L2	/ / /									
L3	/ / /									
L4	/ / /									
L5	/ / /									
L6	/ / /									
L7	/ / /									
L8	/ / /									
L9	/ / /									
L10	/ / /									
L11	/ / /									
L12	/ / /									
L13	/ / /									
L14	/ / /									
L15	/ / /									
L16	/ / /									
L17	/ / /									
L18	/ / /									
L19	/ / /									
L20	/ / /									
L21	/ / /									
L22	/ / /									
L23	/ / /									
L24	/ / /									
L25	/ / /									
L26	/ / /									
L27	/ / /									
L28	/ / /									
L29	/ / /									
L30	/ / /									

Table of LCD Driver Mask Options (1/3 duty)

SEG	SIGNAL	C/S/P	COM1		COM2		COM3	
			DATA	DSPR	DATA	DSPR	DATA	DSPR
L0	/ / /							
L1	/ / /							
L2	/ / /							
L3	/ / /							
L4	/ / /							
L5	/ / /							
L6	/ / /							
L7	/ / /							
L8	/ / /							
L9	/ / /							
L10	/ / /							
L11	/ / /							
L12	/ / /							
L13	/ / /							
L14	/ / /							
L15	/ / /							
L16	/ / /							
L17	/ / /							
L18	/ / /							
L19	/ / /							
L20	/ / /							
L21	/ / /							
L22	/ / /							
L23	/ / /							
L24	/ / /							
L25	/ / /							
L26	/ / /							
L27	/ / /							
L28	/ / /							
L29	/ / /							
L30	/ / /							

Table of LCD Driver Mask Options (1/2 duty)

SEG	SIGNAL	C/S/P	COM1		COM2	
			DATA	DSPR	DATA	DSPR
L0	/ / /					
L1	/ / /					
L2	/ / /					
L3	/ / /					
L4	/ / /					
L5	/ / /					
L6	/ / /					
L7	/ / /					
L8	/ / /					
L9	/ / /					
L10	/ / /					
L11	/ / /					
L12	/ / /					
L13	/ / /					
L14	/ / /					
L15	/ / /					
L16	/ / /					
L17	/ / /					
L18	/ / /					
L19	/ / /					
L20	/ / /					
L21	/ / /					
L22	/ / /					
L23	/ / /					
L24	/ / /					
L25	/ / /					
L26	/ / /					
L27	/ / /					
L28	/ / /					
L29	/ / /					
L30	/ / /					

Appendix G Electrical Characteristics

Absolute Maximum Ratings

(VDD = VDDA = 0 V)

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage 1	VSS1	Ta = 25°C	–2.0 to +0.3	V
Power Supply Voltage 2	VSS2	Ta = 25°C	–4.0 to +0.3	V
Power Supply Voltage 3	VSS3	Ta = 25°C	–5.5 to +0.3	V
Power Supply Voltage 4	VSSL	Ta = 25°C	–4.0 to +0.3	V
Power Supply Voltage 5	VSS	Ta = 25°C	–5.5 to +0.3	V
Power Supply Voltage 6	VSSA	Ta = 25°C	–4.0 to +0.3	V
Input Voltage 1	VIN1	VSS2 Input, Ta = 25°C	VSS2 – 0.3 to +0.3	V
Input Voltage 2	VIN2	VSS Input, Ta = 25°C	VSS – 0.3 to +0.3	V
Input Voltage 3	VIN3	VSS1 Input, Ta = 25°C	VSS1 – 0.3 to +0.3	V
Input Voltage 4	VIN4	VSSA Input, Ta = 25°C	VSSA – 0.3 to +0.3	V
Output Voltage 1	VOUT1	VSS2 Output, Ta = 25°C	VSS2 – 0.3 to +0.3	V
Output Voltage 2	VOUT2	VSS3 Output, Ta = 25°C	VSS3 – 0.3 to +0.3	V
Output Voltage 3	VOUT3	VSS Output, Ta = 25°C	VSS – 0.3 to +0.3	V
Output Voltage 4	VOUT4	VSS1 Output, Ta = 25°C	VSS1 – 0.3 to +0.3	V
Output Voltage 5	VOUT5	VSSA Output, Ta = 25°C	VSSA – 0.3 to +0.3	V
Storage Temperature	TSTG	—	–55 to +125	°C

Recommended Operating Conditions

(VDD = VDDA = 0 V)

Parameter	Symbol	Condition	Range	Unit
Operating Temperature	TOPE	—	–40 to +85	°C
Operating Voltage	VSS2 VSSA	VSS2 = VSSA	–3.6 to –2.6	V
	VSS	—	(Note) –5.25 to (0.8•VSS2 Max.–2.6)	V
700 kHz OSC External Resistance	ROS	—	90 to 300	kΩ
Crystal OSC Oscillation Frequency	fXT	—	30 to 66	kHz

Note: The upper limit of VSS should be 80% VSS2 and –2.6 V maximum.

DC Characteristics

(Unless otherwise specified, VDD = VDDA = 0 V, VSS2 = VSS = –3.0 V, Ta = –40 to +85˚C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
VSS1 Voltage	VSS1	Ca, Cb, C12 = 0.1 µF $^{+100\%}_{-50\%}$	–1.7	–1.5	–1.3	V	
VSS3 Voltage	VSS3	Ca, Cb, C12 = 0.1 µF $^{+100\%}_{-50\%}$	–4.7	–4.5	–4.3	V	
VSSL Voltage	VSSL		–2.1	–1.5	–0.6	V	
XTOSC Oscillation Start Voltage	VSTA	Oscillation start time: within 5 sec.	—	—	–2.6	V	
XTOSC Oscillation Holding Voltage	VHOLD	—	—	—	–2.6	V	
XTOSC Stop Detection Time	TSTOP	—	0.1	—	1000	ms	
XTOSC Internal Capacity	CG	—	10	15	20	pF	1
XTOSC External Capacity	CGEX	In the case of CG external option	10	—	30	pF	
XTOSC Internal Capacity	CD	—	10	15	20	pF	
700kOSC Internal Capacity	COS	—	8	12	16	pF	
700kOSC Oscillation Frequency	fOSC	External Resistance ROS = 100 kΩ VSS2 = –2.4 to +3.6 V	520	700	910	kHz	
POR Generated Voltage	VPOR1	POR is generated when VSS2 changes VPOR1 to –3.0 V	–0.7	—	0	V	
POR Non-generated Voltage	VPOR2	POR is not generated when VSS2 changes VPOR2 to –3.0 V	–3	—	–2	V	

Note: • "XTOSC" indicates 32.768 kHz oscillation circuit.
• "700kOSC" indicates 700 kHz RC oscillation circuit.
• "POR" indicates Power-On-Reset.
• "TSTOP" indicates that a system reset is generated if XTOSC stops oscillation for more than this duration.

DC Characteristics (continued)

(Unless otherwise specified, VDD = VDDA = 0 V, VSS2 = VSS = –3.0 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring Circuit
Current Consumption 1	IDD1	CPU in HALT state (700 kHz OSC stop)		—	1.2	4.5	µA	1
Current Consumption 2	IDD2	CPU in operation state (700 kHz OSC stop)		—	5	15	µA	
Current Consumption 3	IDD3	CPU in operation state (700 kHz OSC operation)		—	400	800	µA	
Current Consumption 4	IDD4	A/D converter in operation, CPU in HALT state (700 kHz OSC stop)	Voltage amplification circuit stop	—	200	300	µA	
			Voltage amplification circuit operation	—	400	600	µA	

DC Characteristics (continued)

(Unless otherwise specified, VDD = VDDA = 0 V, VSS1 = VSSL = –1.5 V, VSS2 = VSS = VSSA = –3.0 V, VSS3 = –4.5 V, Ta = –40 to +85°C)

Parameter (Pin Name)	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Output Current 1	IOH1	VOH1 = –0.5 V	–6	–2	–0.7	mA	
(P0.0 to P0.3)	IOL1	VOL1 = VSS + 0.5 V	0.7	2	6	mA	
(P1.0 to P1.3)	IOH1S	VSS = –5 V, VOH1S = –0.5 V	–9	–3	–1	mA	
(P2.0 to P2.3)	IOL1S	VSS = –5 V, VOL1S = VSS + 0.5 V	1	3	9	mA	
Output Current 2	IOH2	VOH2 = –0.7 V	–6	–2	–0.7	mA	
(BD)	IOL2	VOL2 = VSS2 + 0.7 V	0.7	2	6	mA	
Output Current 3	IOH3	VOH3 = –0.5 V	–3.0	–1.2	–0.2	mA	
(RI, CI, OPO0, OPO1)	IOL3	VOL3 = VSS + 0.5 V	15	30	100	µA	
Output Current 4	IOH4	VOH4 = –0.5 V	–1.5	–0.6	–0.15	mA	
(When L0 to L7 are	IOL4	VOH4 = VSS + 0.5 V	0.15	0.6	1.5	mA	
output ports)	IOH4S	VSS = –5 V, VOH4S = –0.5 V	–2	–0.7	–0.2	mA	2
	IOL4S	VSS = –5 V, VOL4S = VSS + 0.5 V	0.2	0.7	2.0	mA	
Output Current 5	IOH5	VOH5 = –0.5 V	–6	–2	–0.7	mA	
(OSC2)	IOL5	VOL5 = VSS2 + 0.5 V	0.7	2	6	mA	
Output Current 6	IOH6	VOH6 = –0.2 V (VDD level)	—	—	–4	µA	
(L0 to L30)	IOMH6	VOMH6 = VSS1 + 0.2 V (VSS1 level)	4	—	—	µA	
	IOMH6S	VOMH6S = VSS1 – 0.2 V (VSS1 level)	—	—	–4	µA	
	IOML6	VOML6 = VSS + 0.2 V (VSS2 level)	4	—	—	µA	
	IOML6S	VOML6S = VSS2 – 0.2 V(VSS2 level)	—	—	–4	µA	
	IOL6	VOL6 = VSS3 + 0.2 V (VSS3 level)	4	—	—	µA	
Output Leakage Current	IOOH	VOH = VDD	—	—	0.3	µA	
(P0.0 to P0.3)	IOOL	VOL = VSS2	–0.3	—	—	µA	
(P1.0 to P1.3)							
(P2.0 to P2.3)							

DC Characteristics (continued)

(Unless otherwise specified, VDD = VDDA = 0 V, VSS1 = VSSL = –1.5 V, VSS2 = VSS = VSSA = –3.0 V, VSS3 = –4.5 V, Ta = –40 to +85°C)

Parameter (Pin Name)	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Input Current 1	IIH1	VIH1 = VDD (During pulldown)	30	90	300	µA	3
(P0.0 to P0.3)	IIL1	VIL1 = VSS (During pullup)	–300	–90	–30	µA	
(P1.0 to P1.3)	IIH1S	VIH1 = VDD, VSS = –5 V (During pulldown)	80	250	800	µA	
(P2.0 to P2.3)	IIL1S	VIL1 = VSS = –5 V (During pullup)	–800	–250	–80	µA	
	IIH1Z	VIH1 = VDD (During high impedance)	0	—	1	µA	
	IIL1Z	VIL1 = VSS (During high impedance)	–1	—	0	µA	
Input Current 2	IIL2	VIL2 = VSSA (During pullup)	–300	–90	–30	µA	
(OPP0, OPP1, OPN0,	IIH2Z	VIH2 = VDD (During high impedance)	0	—	1	µA	
OPN1, VOF)	IIL2Z	VIL2 = VSSA (During high impedance)	–1	—	0	µA	
Input Current 3	IIL3	VIL3 = VSSA (ENADC = 0)	–375	–250	–125	µA	
(VrA)	IIH3	VIH3 = VrA + 30 mV (ENADC = 1)	0.6	1	—	mA	
Input Current 4	IIL4	VIL4 = VSS2 (During pullup)	–300	–110	–10	µA	
(OSC1)	IIH4Z	VIH4 = VDD (During high impedance)	0	—	1	µA	
	IIL4Z	VIL4 = VSS2 (During high impedance)	–1	—	0	µA	
Input Current 5	IIH5	VIH5 = VDD	0	—	1	µA	
($\overline{\text{RESET}}$, $\overline{\text{TST1}}$, $\overline{\text{TST2}}$)	IIL5	VIL5 = VSS2	–3	–1.5	–0.75	mA	
Input Current 6 (RCM, CZ1, CZ2 AIN0 to AIN3, RA)	IIH6Z	VIH6 = VDD (During high impedance)	0	—	1	µA	
	IIL6Z	VIL6 = VSSA (During high impedance)	–1	—	0	µA	
Input Voltage 1 (P0.0 to P0.3) (P1.0 to P1.3) (P2.0 to P2.3) (OSC1)	VIH1	—	–0.6	—	0	V	4
	VIL1	—	–3.0	—	–2.4	V	
	VIH1S	VSS = –5 V	–1	—	0	V	
	VIL1S	VSS = –5 V	–5	—	–4	V	
Input Voltage 2 (OSC1) ($\overline{\text{RESET}}$, $\overline{\text{TST1}}$, $\overline{\text{TST2}}$)	VIH2	—	–0.6	—	0	V	
	VIL2	—	–3.0	—	–2.4	V	

DC Characteristics (continued)

(Unless otherwise specified, VDD = VDDA = 0 V, VSS1 = VSSL = –1.5 V, VSS2 = VSS = VSSA = –3.0 V, VSS3 = –4.5 V, Ta = –40 to +85°C)

Parameter (Pin Name)	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Hysteresis Width (P0.0 to P0.3)	ΔVT1	—	0.2	0.5	1	V	4
(P1.0 to P1.3) (P2.0 to P2.3)	ΔVT1S	VSS = –5 V	0.25	1.0	1.5	V	
Hystereis Width ($\overline{\text{RESET}}$, $\overline{\text{TST1}}$, $\overline{\text{TST2}}$)	ΔVT2	—	0.2	0.5	1	V	
Input Capacitance (P0.0 to P0.3) (P1.0 to P1.3) (P2.0 to P2.3)	CIN	—	—	—	5	pF	1

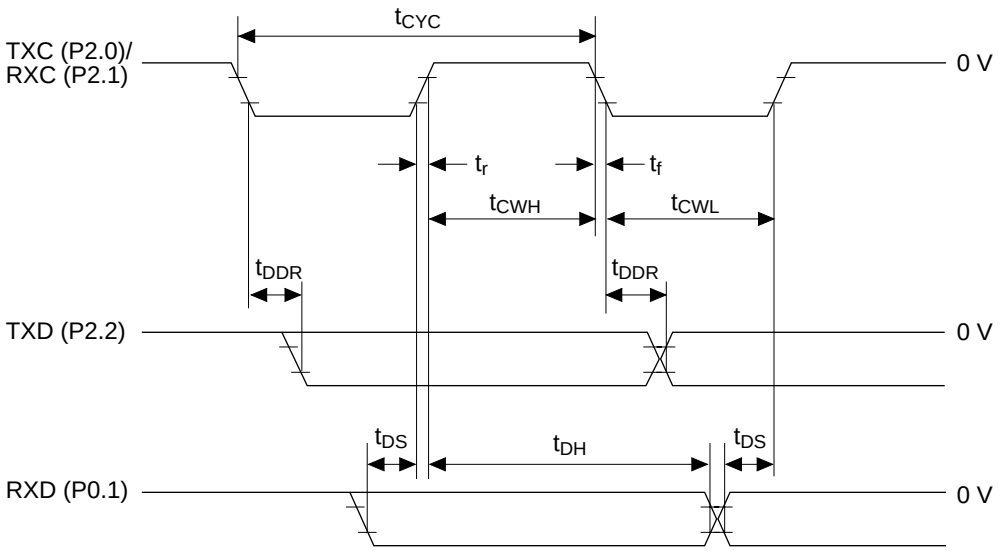
AC Characteristics (Serial Interface)

(Unless otherwise specified, VDD = 0 V, VSS2 = –3.0 V, VSS = –5 V, Ta = –40 to +85˚C)

(1) Synchronous communication

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
TXC/RXC Input Fall Time	t_f	—	—	—	1	µs
TXC/RXC Input Rise Time	t_r	—	—	—	1	µs
TXC/RXC Input "L" Level Pulse Width	t_{CWL}	—	0.8	—	—	µs
TXC/RXC Input "H" Level Pulse Width	t_{CWH}	—	0.8	—	—	µs
TXC/RXC Input Cycle Time	t_{CYC}	—	2.0	—	—	µs
TXC/RXC Output Cycle Time	$t_{CYC1(O)}$	CPU operating at 32 kHz	—	30.5	—	µs
TXD Output Delay Time	t_{DDR}	Output load capacitance = 10 pF	—	—	0.4	µs
RXD Input Setup Time	t_{DS}	—	0.5	—	—	µs
RXD Input Hold Time	t_{DH}	—	0.8	—	—	µs

Synchronous communication timing
("H" level = –1 V, "L" level = –4 V)



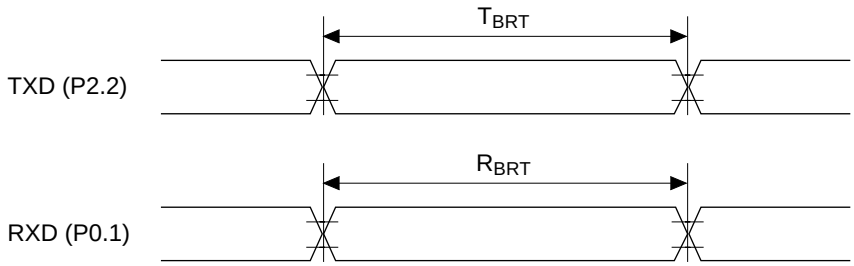
(2) UART communication

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Transmit Baud Rate	T_{BRT}	$T_{BRT} = 1/f_{BRT}$, $T_{CR} = 1/f_{OSC}$	$T_{BRT} - T_{CR}$	T_{BRT}	$T_{BRT} + T_{CR}$	s
Receive Baud Rate	R_{BRT}	$R_{BRT} = 1/f_{BRT}$	$R_{BRT} \times 0.97$	R_{BRT}	$R_{BRT} \times 1.03$	s

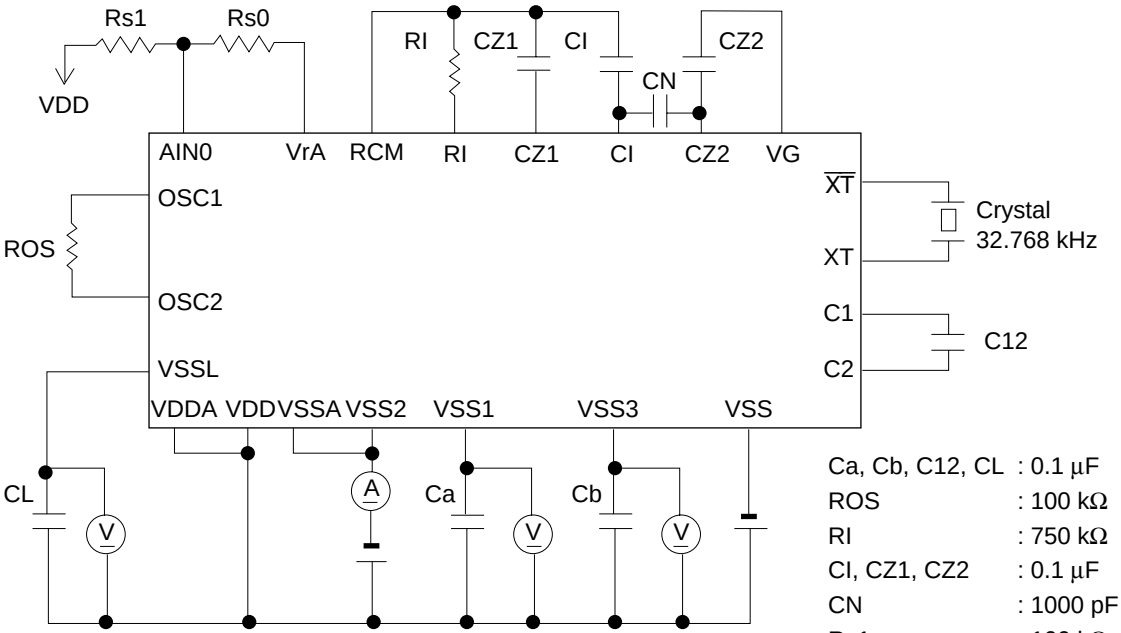
f_{BRT}: Baud rate (1200, 2400, 4800, 9600 bps)

UART communication timing

("H" level = –1 V, "L" level = –4 V)

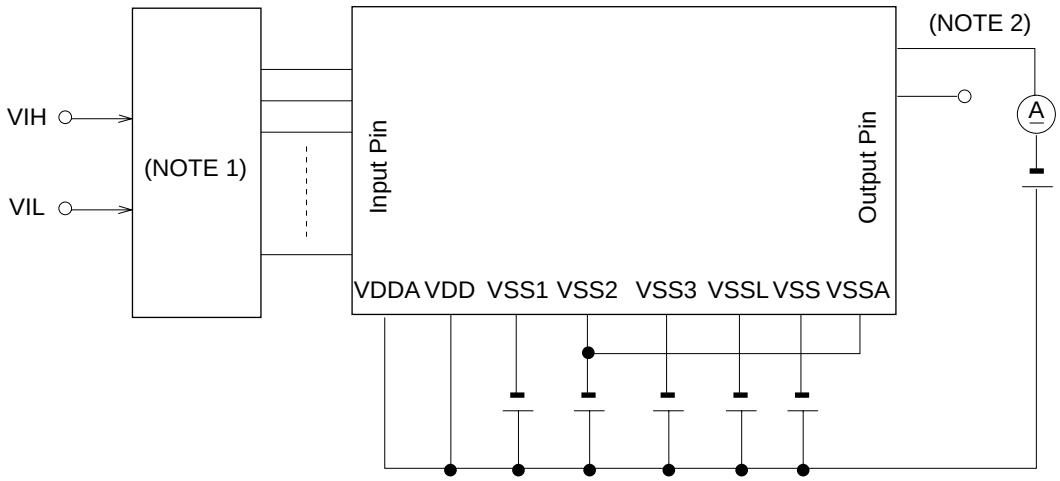


Measuring circuit 1

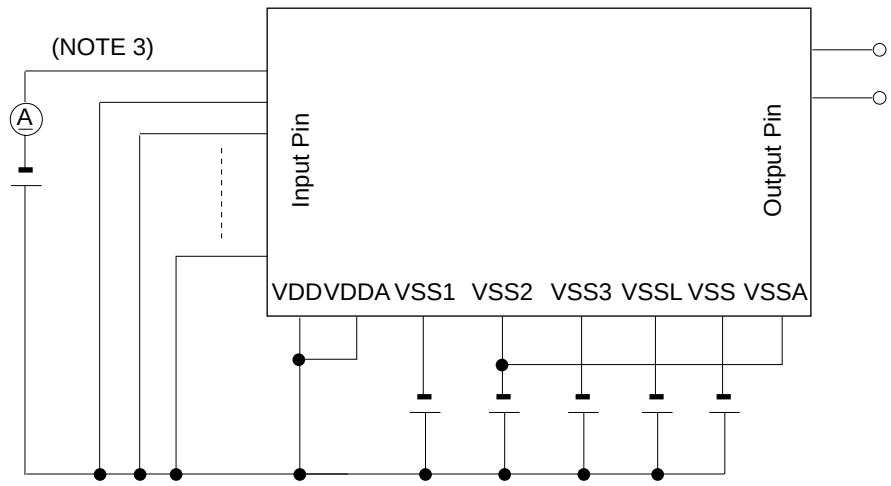


Ca, Cb, C12, CL	: 0.1 µF
ROS	: 100 kΩ
RI	: 750 kΩ
CI, CZ1, CZ2	: 0.1 µF
CN	: 1000 pF
Rs1	: 100 kΩ
Rs0	: 10 kΩ

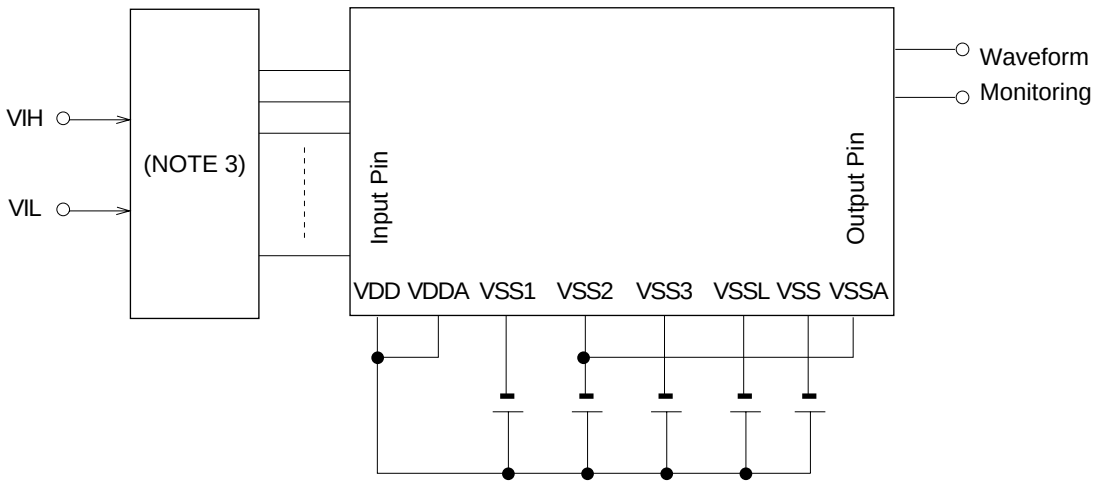
Measuring circuit 2



Measuring circuit 3



Measuring circuit 4



(NOTE 1) Input logic to set specified state.
(NOTE 2) Repeat for specified output pin.
(NOTE 3) Repeat for specified input pin.

A/D Converter Characteristics

(Unless otherwise specified, VDD = VDDA = 0 V, VSS2 = VSS = VSSA = –3 V, VrA = –1.2 V, Ta = –40 to +85°C, TMCLK = 32.768 kHz, at execution of 12-bit AD conversion)

Parameter (Pin Name)	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Resolution	n	—	—	—	12 + S	bits	5
Linearity Error I	EI1	Vin > VG	–1	—	+1	LSB	
Linearity Error II	EI2	Vin < VG	–1	—	+1	LSB	
Zero Scale Error	Ez	Vin = VG	–2	—	+2	LSB	
Full Scale Error I	EFS I	Vin > VG	–16	—	+16	LSB	
Full Scale Error II	EFS II	Vin < VG	–16	—	+16	LSB	
VrA Voltage	VrA	Ta = 25°C	–1300	–1200	–1100	mV	5
VG Voltage (VG)	VG	Ta = 25°C	–867	–800	–733	mV	
RA Voltage (RA)	VRA	Ta = 25°C	–440	–400	–360	mV	
VrA Temperature Coefficient	ΔVrA/ΔT	—	–8	0	+2	mV/°C	

Note: "S" indicates a sign bit.

Voltage Amplification Circuit Characteristics

(Unless otherwise specified, VDD = VDDA = 0 V, VSS2 = VSS = VSSA = –3 V, VrA = –1.2 V, Ta = –40 to +85°C)

Parameter (Pin Name)	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Amplifier Gain Error (*1)	Eg (*2)	VOOP1 – VOPP0 = 10 mV, Gain = 40 $Eg = \frac{(VOPO1 - VOPO0)/(VOPP1 - VOPP0)}{Gain} - 1$	–3.0	–1.5	0	%	5
Level Shift Error (*1)	EI	$EI = \frac{(VAIN3 - VVOF)}{(VOPO1 - VOPO0)} - 1$	–4	—	+4	%	
Amplifier Offset Voltage	VoffA	OPP0 = OPP1 = VOF = –0.8 V, OPO0 = OPN0, OPO1 = OPN1, VoffA = VOPO1 – VOPO0	–20	—	+20	mV	
Level Shift Offset Voltage	VoffL	OPO0 = OPO1 = VOF = –0.8 V VoffL = VAIN3 – VVOF	–30	—	+30	mV	

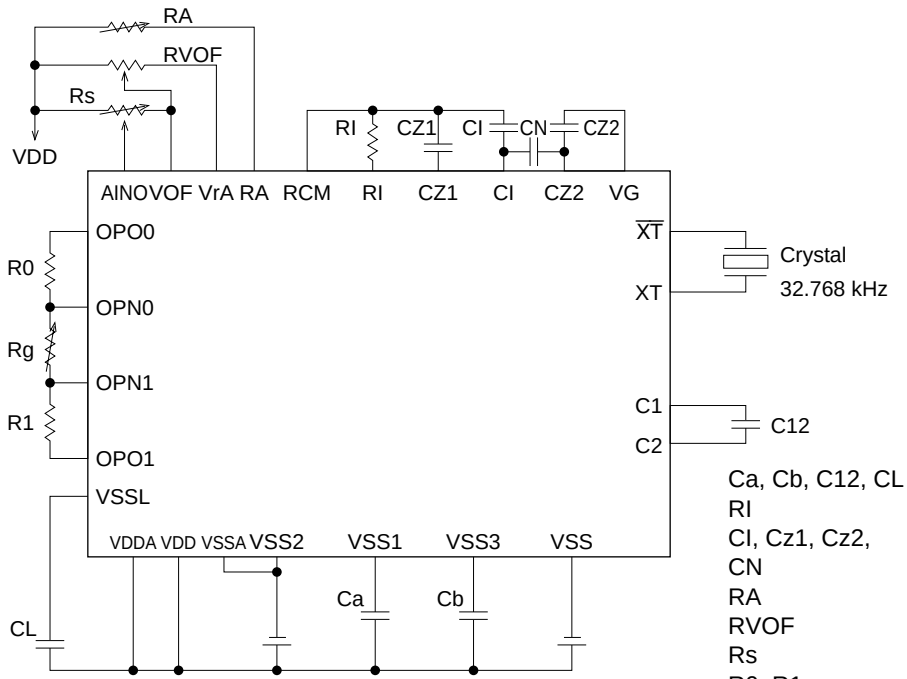
*1 Errors caused by offset voltage are excluded.
*2 Errors decrease in proportion to gain.
Note: VOPP0, VOPP1, and VVOF represent voltages between OPP0 and VDD pins, OPP1 and VDD pins, and VOF and VDD pins, respectively.

Recommended Operating Conditions for A/D Converter and Voltage Amplification Circuit

(Unless otherwise specified, VDD = VDDA = 0 V, VSS2 = VSS = VSSA = –3 V, VrA = –1.2 V, Ta = –40 to +85°C, at execution of 12-bit AD conversion)

Parameter (Pin Name)	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Analog Input Voltage Range (AIN0 to AIN3)	VAIN	—	–1.2	—	–0.4	V	5
Analog Input Voltage Range (OPP0, OPP1) (VOF)	VOPP	—	–1.6	—	–0.4	V	
Auto Zero Stage Time	t0	CI = CZ1 = CZ2 = 0.1 µF, RI = 750 kΩ TMCLK = 32.768 kHz	25	—	—	ms	
VrA Output Current	IVrA	—	—	—	0.6	mA	
Amplifier Output Voltage Range (OPO0, OPO1)	VOPO	—	–2.0	—	–0.1	V	
External Integral Resistance	RI	—	30	—	—	kΩ	
External Amplifier Resistance	RE	RE = R0 + Rg + R1	500	—	—	kΩ	
Amplifier Gain	Gain	$\text{Gain} = \frac{R0 + Rg + R1}{Rg}$	1	—	40	—	

Measuring circuit 5



Ca, Cb, C12, CL : 0.1 µF
RI : 750 kΩ
CI, Cz1, Cz2, : 0.1 µF
CN : 1000 pF
RA : 10 kΩ
RVOF : 10 kΩ max
Rs : 10 kΩ max
R0, R1 : 270 kΩ
Rg : 100 kΩ max

Difinition of Precision of AD Conversion

① Resolution

Definition: Distinguishable minimum input analog value.
For n bit(s), the resolution is (VrA × 1/3)/2^n.

② Linearity error

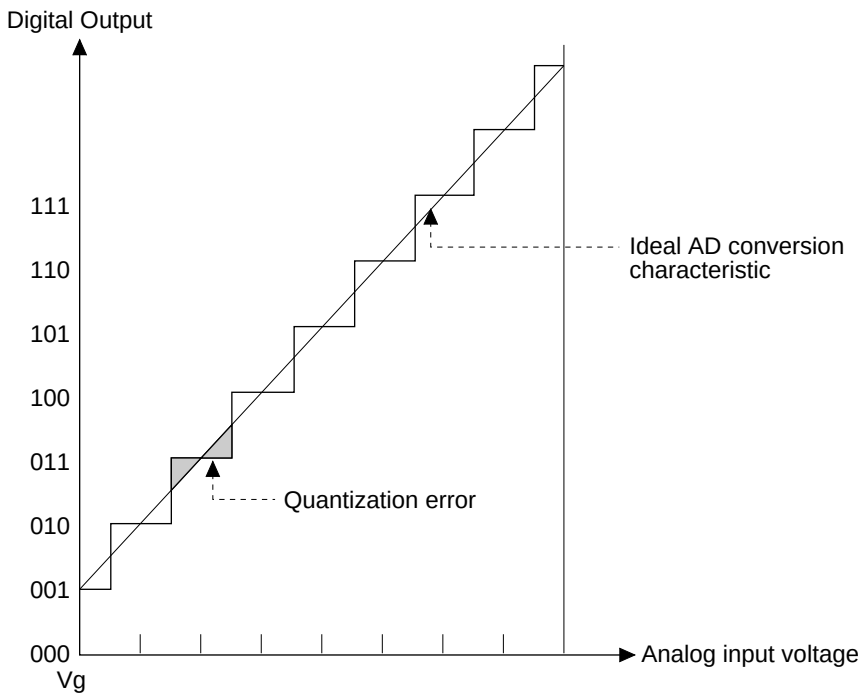
Definition: Deviation between ideal conversion characteristic and actual conversion characteristic. (Quantization error is therefore not included.)
The ideal conversion characteristic is represented by each step obtained by dividing the voltage between VrP or VrN and Vg into 2^n equal divisions.
However, the zero scale error, full scale error, and quantization error are excluded.

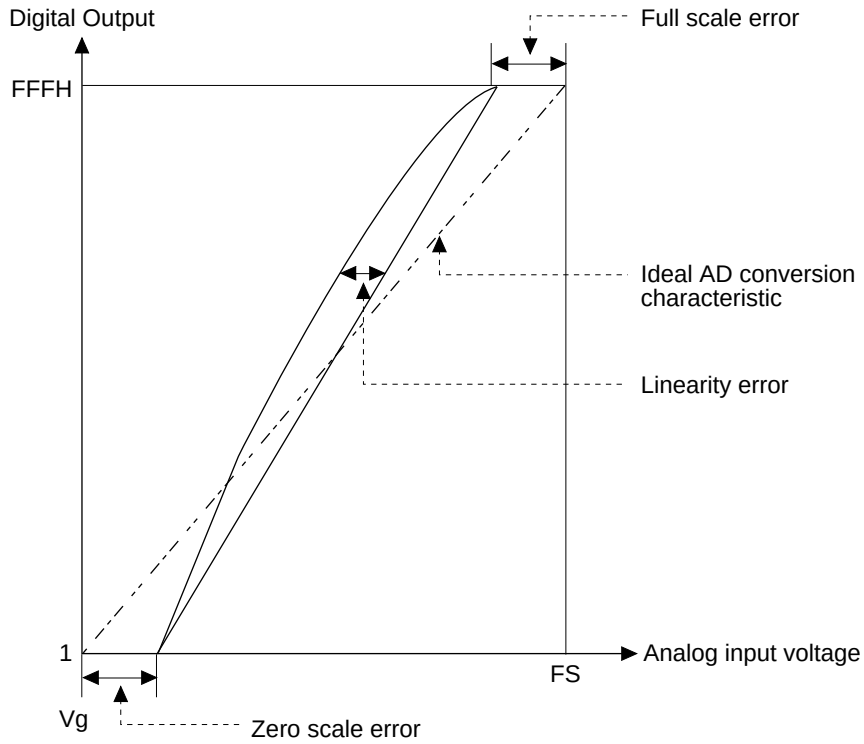
③ Zero scale error

Definition: Deviation between the ideal conversion characteristic at the point where digital output is switched from 1 to 2 and actual conversion characteristic.

④ Full scale error

Definition: Deviation between the ideal conversion characteristic at the point where digital output is switched from 2^n – 2 to 2^n – 1 and actual conversion characteristic.




Digital Output
Full scale error
FFFH
Ideal AD conversion characteristic
Linearity error
1
Analog input voltage
FS
Vg
Zero scale error

Appendix H Instruction List

"B" indicates the byte length of an instruction.
"C" indicates the execution machine cycle number of an instruction.

Mnemonic	Op-code	B	C	Operation
ADC		1	1	A, C $\leftarrow$ A + M (HL) + C
ADC	@XY	2	2	A, C $\leftarrow$ A + M (XY) + C
ADCB		1	2	BA, C $\leftarrow$ BA + M_b (HL) + C
ADCB	@XY	2	3	BA, C $\leftarrow$ BA + M_b (XY) + C
ADCS		1	1	A, C $\leftarrow$ A + M (HL) + C, Skip if Carry = 1
ADCS	@XY	2	2	A, C $\leftarrow$ A + M (XY) + C, Skip if Carry = 1
ADS		1	1	A $\leftarrow$ A + M (HL), Skip if Carry = 1
ADS	@XY	2	2	A $\leftarrow$ A + M (XY), Skip if Carry = 1
ADSB		1	2	BA $\leftarrow$ BA + M_b (HL), Skip if Carry = 1
ADSB	@XY	2	3	BA $\leftarrow$ BA + M_b (XL), Skip if Carry = 1
AIS	n_4	1	1	A $\leftarrow$ A + n_4, Skip if Carry = 1
AND		1	1	A $\leftarrow$ A $\wedge$ M (HL)
AND	@XY	2	2	A $\leftarrow$ A $\wedge$ M (XY)
ANDI	n_4	2	2	A $\leftarrow$ A $\wedge$ n_4
CAB		1	1	Skip if A = B
CAI	n_4	2	2	Skip if A = n_4
CAL	a_{11}	2	4	ST $\leftarrow$ PC + 2, $PC_{10\ to\ 0}$ $\leftarrow$ a_{11}, SP $\leftarrow$ SP – 2
CAM		1	1	Skip if A = M (HL)
CAM	@XY	2	2	Skip if A = M (XY)
CAMB		1	2	Skip if BA = M_b (HL)
CAMB	@XY	2	3	Skip if BA = M_b (XY)
CAMD	m_8	2	2	Skip if A = M (m_8)
CLI	n_4	2	2	Skip if L = n_4
CMA		2	2	A $\leftarrow$ $\overline{A}$
CMI	n_4	2	2	Skip if M (HL) = n_4
CZP	a_5	1	4	ST $\leftarrow$ PC + 1, $PC_{4\ to\ 0}$ $\leftarrow$ a_5, $PC_{11\ to\ 5}$ $\leftarrow$ 0 SP $\leftarrow$ SP – 2 (Even numbers of 10_H to $1E_H$ are indicated by a_5.)

Mnemonic	Op-code	B	C	Operation
DCA		1	1	A $\leftarrow$ A – 1, Skip if A = $0F_H$
DCH		1	1	H $\leftarrow$ H – 1, Skip if H = $0F_H$
DCL		1	1	L $\leftarrow$ L – 1, Skip if L = $0F_H$
DCM		1	1	M (HL) $\leftarrow$ M (HL) – 1, Skip if M (HL) = $0F_H$
DCM	@XY	2	2	M (XY) $\leftarrow$ M (XY) – 1, Skip if M (XY) = $0F_H$
DCMD	m_8	2	2	M (m_8) $\leftarrow$ M (m_8) – 1, Skip if M (m_8) = $0F_H$
DCX		1	1	X $\leftarrow$ X – 1, Skip if X = $0F_H$
DCY		1	1	Y $\leftarrow$ Y – 1, Skip if Y = $0F_H$
EOR		1	1	A $\leftarrow$ A $\forall$ M (HL)
EOR	@XY	2	2	A $\leftarrow$ A $\forall$ M (XY)
EORI	n_4	2	2	A $\leftarrow$ A $\forall$ n_4
INA		1	1	A $\leftarrow$ A + 1, Skip if A = 0
INH		1	1	H $\leftarrow$ H + 1, Skip if H = 0
INL		1	1	L $\leftarrow$ L + 1, Skip if L = 0
INM		1	1	M (HL) $\leftarrow$ M (HL) + 1, Skip if M (HL) = 0
INM	@XY	2	2	M (XY) $\leftarrow$ M (XY) + 1, Skip if M (XY) = 0
INMD	m_8	2	2	M (m_8) $\leftarrow$ M (m_8) + 1, Skip if M (m_8) = 0
INX		1	1	X $\leftarrow$ X + 1, Skip if X = 0
INY		1	1	Y $\leftarrow$ Y + 1, Skip if Y = 0
JA		1	1	$PC_{5\ to\ 0}$ $\leftarrow$ BA (bit 0 to bit 5)
JCP	a_6	1	1	$PC_{5\ to\ 0}$ $\leftarrow$ a_6
JM		1	3	$PC_{10\ to\ 0}$ $\leftarrow$ M_b, HL, BA PC_{11} $\leftarrow$ Mb (HL), BA
JP	a_{11}	2	2	$PC_{10\ to\ 0}$ $\leftarrow$ a_{11}
LAB		2	2	A $\leftarrow$ B
LAH		1	1	A $\leftarrow$ H
LAI	n_4	1	1	A $\leftarrow$ n_4 (Vertical Stack Instruction)
LAL		1	1	A $\leftarrow$ L
LALB		2	2	BA $\leftarrow$ HL
LAM		1	1	A $\leftarrow$ M (HL)
LAM	@XY	2	2	A $\leftarrow$ M (XY)

Mnemonic	Op-code	B	C	Operation
LAMB		1	2	BA $\leftarrow$ M_b (HL)
LAMB	@XY	2	3	BA $\leftarrow$ M_b (XY)
LAMD	m_8	2	2	A $\leftarrow$ M (m_8)
LAMDB	m_8	2	2	BA $\leftarrow$ M_b (m_8)
LAMM	n_2	1	1	A $\leftarrow$ M (HL), H $\leftarrow$ H $\forall$ n_2
LAM+		1	2	A $\leftarrow$ M (HL), L $\leftarrow$ L + 1, Skip if L = 0
LAM–		1	2	A $\leftarrow$ M (HL), L $\leftarrow$ L – 1, Skip if L = $0F_H$
LAX		1	1	A $\leftarrow$ X
LAY		1	1	A $\leftarrow$ Y
LAYB		2	2	BA $\leftarrow$ XY
LBA		2	2	B $\leftarrow$ A
LBAI	n_8	2	2	BA $\leftarrow$ n_8
LBS0I	n_3	2	2	BSR0 $\leftarrow$ n_3
LBS1I	n_3	2	2	BSR1 $\leftarrow$ n_3
LCAL	a_{12}	3	5	ST $\leftarrow$ PC + 3, PC $\leftarrow$ a_{12}, SP $\leftarrow$ SP – 2
LHA		1	1	H $\leftarrow$ A
LHI	n_4	2	2	H $\leftarrow$ n_4
LHLI	n_8	2	2	HL $\leftarrow$ n_8
LJP	a_{12}	3	5	PC $\leftarrow$ a_{12}
LLA		1	1	L $\leftarrow$ A
LLAB		2	2	HL $\leftarrow$ BA
LLI	n_4	1	1	L $\leftarrow$ n_4 (Vertical Stack Instruction)
LMA		1	1	M (HL) $\leftarrow$ A
LMA	@XY	2	2	M (XY) $\leftarrow$ A
LMAB		1	2	M_b (HL) $\leftarrow$ BA
LMAB	@XY	2	3	M_b (XY) $\leftarrow$ BA
LMAD	m_8	2	2	M (m_8) $\leftarrow$ A
LMADB	m_8	2	2	M_b (m_8) $\leftarrow$ BA
LMA+		1	2	M (HL) $\leftarrow$ A, L $\leftarrow$ L + 1, Skip if L = 0
LMA–		1	2	M (HL) $\leftarrow$ A, L $\leftarrow$ L – 1, Skip if L = $0F_H$

Mnemonic	Op-code	B	C	Operation
LMBI	n_8	2	2	M_b (HL) $\leftarrow$ n_8
LMBI	@XY, n_8	3	3	M_b (XY) $\leftarrow$ n_8
LMI	n_4	2	2	M (HL) $\leftarrow$ n_4
LMTB	a_4	2	3	M_b (HL) $\leftarrow$ T (a_4, XY)
LXA		1	1	X $\leftarrow$ A
LXI	n_4	2	2	X $\leftarrow$ n_4
LXYI	n_8	2	2	XY $\leftarrow$ n_8
LYA		1	1	Y $\leftarrow$ A
LYAB		2	2	XY $\leftarrow$ BA
LYI	n_4	2	2	Y $\leftarrow$ n_4
NOP		1	1	No operation
OR		1	1	A $\leftarrow$ A $\vee$ M (HL)
OR	@XY	2	2	A $\leftarrow$ A $\vee$ M (XY)
ORI	n_4	2	2	A $\leftarrow$ A $\vee$ n_4
POP	BA	1	2	SP $\leftarrow$ SP + 1, BA $\leftarrow$ ST
POP	HL	1	2	SP $\leftarrow$ SP + 1, HL $\leftarrow$ ST
POP	BSR	1	2	SP $\leftarrow$ SP + 1, BSR $\leftarrow$ ST
PUSH	BA	1	2	ST $\leftarrow$ BA, SP $\leftarrow$ SP – 1
PUSH	HL	1	2	ST $\leftarrow$ HL, SP $\leftarrow$ SP – 1
PUSH	BSR	1	2	ST $\leftarrow$ BSR, SP $\leftarrow$ SP – 1
RAL		1	1	C $\leftarrow$ A_3 $\leftarrow$ A_2 $\leftarrow$ A_1 $\leftarrow$ A_0 $\leftarrow$ C
RAR		1	1	C $\rightarrow$ A_3 $\rightarrow$ A_2 $\rightarrow$ A_1 $\rightarrow$ A_0 $\rightarrow$ C
RBC		1	1	BCF $\leftarrow$ 0
RBE		1	1	BEF $\leftarrow$ 0
RC		1	1	C $\leftarrow$ 0
RMB	n_2	1	1	M (HL) [n_2] $\leftarrow$ 0
RMB	@XY, n_2	2	2	M (XY) [n_2] $\leftarrow$ 0
RMBD	m_8, n_2	2	2	M (m_8) [n_2] $\leftarrow$ 0
RT		1	3	PC $\leftarrow$ ST, SP $\leftarrow$ SP + 2
RTI		1	5	PC•C•HL•BA $\leftarrow$ ST, SP $\leftarrow$ SP + 4, MI $\leftarrow$ 1
RTS		1	3	PC $\leftarrow$ ST, SP $\leftarrow$ SP + 2, Then skip

Mnemonic	Op-code	B	C	Operation
SBC		1	1	BCF $\leftarrow$ 1
SBE		1	1	BEF $\leftarrow$ 1
SC		1	1	C $\leftarrow$ 1
SMB	n_2	1	1	M (HL) [n_2] $\leftarrow$ 1
SMB	@XY, n_2	2	2	M (XY) [n_2] $\leftarrow$ 1
SMBD	m_8, n_2	2	2	M (m_8) [n_2] $\leftarrow$ 1
SUBC		1	1	A, C $\leftarrow$ A – M (HL) – C
SUBC	@XY	2	2	A, C $\leftarrow$ A – M (XY) – C
SUBCB		1	2	BA, C $\leftarrow$ BA – M_b (HL) – C
SUBCB	@XY	2	3	BA, C $\leftarrow$ BA – M_b (XY) – C
SUBCS		1	1	A, C $\leftarrow$ A – M (HL) – C, Skip if Borrow = 0
SUBCS	@XY	2	2	A, C $\leftarrow$ A – M (XY) – C, Skip if Borrow = 0
SUBS		1	1	A $\leftarrow$ A – M (HL), Skip if Borrow = 1
SUBS	@XY	2	2	A $\leftarrow$ A – M (XY), Skip if Borrow = 1
SUBSB		1	2	BA $\leftarrow$ BA – M_b (HL), Skip if Borrow = 1
SUBSB	@XY	2	3	BA $\leftarrow$ BA – M_b (XY), Skip if Borrow = 1
TAB	n_2	1	1	Skip if A [n_2] = 1
TC		1	1	Skip if C = 1
TMB	n_2	1	1	Skip if M (HL) [n_2] = 1
TMB	@XY, n_2	2	2	Skip if M (XY) [n_2] = 1
TMBD	m_8, n_2	2	2	Skip if M (m_8) [n_2] = 1
XAB		1	2	A $\leftrightarrow$ B
XAM		1	1	A $\leftrightarrow$ M (HL)
XAM	@XY	2	2	A $\leftrightarrow$ M (XY)
XAMB		1	2	BA $\leftrightarrow$ M_b (HL)
XAMB	@XY	2	3	BA $\leftrightarrow$ M_b (XY)
XAMD	m_8	2	2	A $\leftrightarrow$ M (m_8)
XAMDB	m_8	2	2	BA $\leftrightarrow$ M_b (m_8)
XAMM	n_2	1	1	A $\leftrightarrow$ M (HL), H $\leftarrow$ H $\forall$ n_2
XAM+		1	2	A $\leftrightarrow$ M (HL), L $\leftarrow$ L + 1, Skip if L = 0
XAM–		1	2	A $\leftrightarrow$ M (HL), L $\leftarrow$ L – 1, Skip if L = $0F_H$

[Explanation of Symbols]

The meaning of the symbols used in the following sections are explained below.

- A ..... Accumulator
- C ..... Carry flag
- B, H, L, X, Y ..... Working registers
- BA ..... Indicates 8-bit data contents of registers B (B3 to B0), and accumulators (A3 to A0), with registers B at the MSB side

	7	6	5	4	3	2	1	0
BA:	B3	B2	B1	B0	A3	A2	A1	A0

- HL ..... Indicates 8-bit data contents of registers H and L, with register H at the MSB side

	7	6	5	4	3	2	1	0
HL:	H3	H2	H1	H0	L3	L2	L1	L0

- XY ..... Indicates 8-bit data contents of registers X and Y, with register X at the MSB side

	7	6	5	4	3	2	1	0
XY:	X3	X2	X1	X0	Y3	Y2	Y1	Y0

- BSR ..... Indicates bank select registers (BSR1, BSR0), bank common flag (BCF) and bank enable flag (BEF)

	7	6	5	4	3	2	1	0
BSR:	BEF	BSR1			BCF	BSR0		

- M (y) ..... Indicates 4-bit data memory contents in address indicated by y

	3	2	1	0
M(y):	M(y)			

- Mb (y) ..... Indicates 8-bit data memory contents in address indicated by y. The data configuration is shown below. The LSB is always an even address.

	7	6	5	4	3	2	1	0
Mb(y):	M(y + 1)				M(y)			
	(Odd Address)				(Even Address)			

- T (y) ..... Indicates 8-bit program memory (ROM) content in address indicated by y (for ROM table data).

	7	6	5	4	3	2	1	0
T(y)	T(y)							

- PC ..... Indicates contents of program counter (max. 12 bits). The PC value is the program memory address.

- SP ..... Indicates contents of stack pointer (8-bit). SP value is the stack address in data memory. SP is allocated to $7F_H$ and $7E_H$ addresses of data memory bank0.

	7	6	5	4	3	2	1	0
SP:	1	SP6	SP5	SP4	SP3	SP2	SP1	1
	($07F_H$ Address)				($07E_H$ Address)			

- ST ..... Indicates 8-bit stack content. This is 8-bit data indicated by SP in data memory. The configuration is shown below.

	7	6	5	4	3	2	1	0
ST:	(SP)				(SP – 1)			
	(Odd Address)				(Even Address)			

- MI ..... Indicates the master interrupt enable flag. MI is allocated to $7C_H$ address, bit 0 of data memory bank0.

- @XY ..... Indicates XY indirect addressing mode instruction. An indirect address mode instruction without this symbol is HL indirect addressing.

- nx ..... Indicates x-bit of immediate data.

- In ..... Indicates n-bit of immediate data. (n = 0, 1, 2 • • •)

- ax ..... Indicates immediate data to be loaded to PC as an x-bit program memory (ROM) address. The "x-bit" is usually from bit 0, but in the table address it is from bit 8.

- m_8 ..... Indicates immediate data to be the low order 8-bit address for direct addressing to data memory.

- r [n_2] ..... Indicates value of bit shown as n_2 (see the Fig. below) in content of r (data memory, working registers, accumulators, etc.).

n_2:	11	10	01	00
	↓	↓	↓	↓
r:	r3	r2	r1	r0

- $\vee$ ..... Indicates OR.
- $\wedge$ ..... Indicates AND.
- $\forall$ ..... Indicates exclusive-OR (EOR).
- X_H ..... "H" indicates that "X" is a hexadecimal value.

- Skip if ..... If condition is formed, next instruction is skipped, that is, the machine cycle time of the next instruction is spent and the instruction is not executed.
- Carry ..... Indicates the carry of operation results.
- Borrow ..... Indicates the borrow of operation results.

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