FEDL6696-02

OKI Semiconductor

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MSM6696

LCD Active Matrix Gate Driver

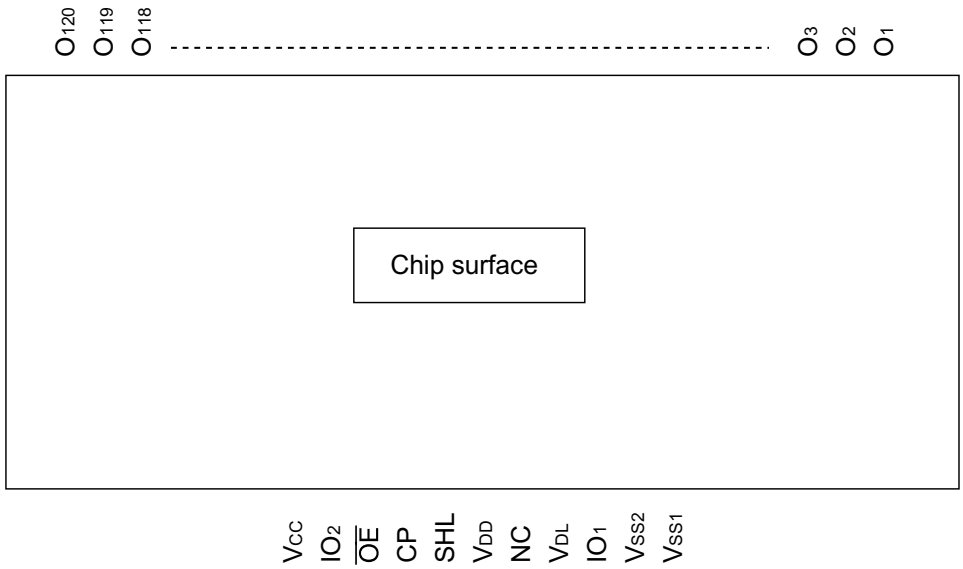
GENERAL DESCRIPTION

The MSM6696 is an LCD active matrix gate driver fabricated in CMOS technology.The device is composed of a 120-bit bi-directional shift register circuit, input level shifter circuits, etc. High voltage operation at 40 V has been realized using high breakdown voltage CMOS process.

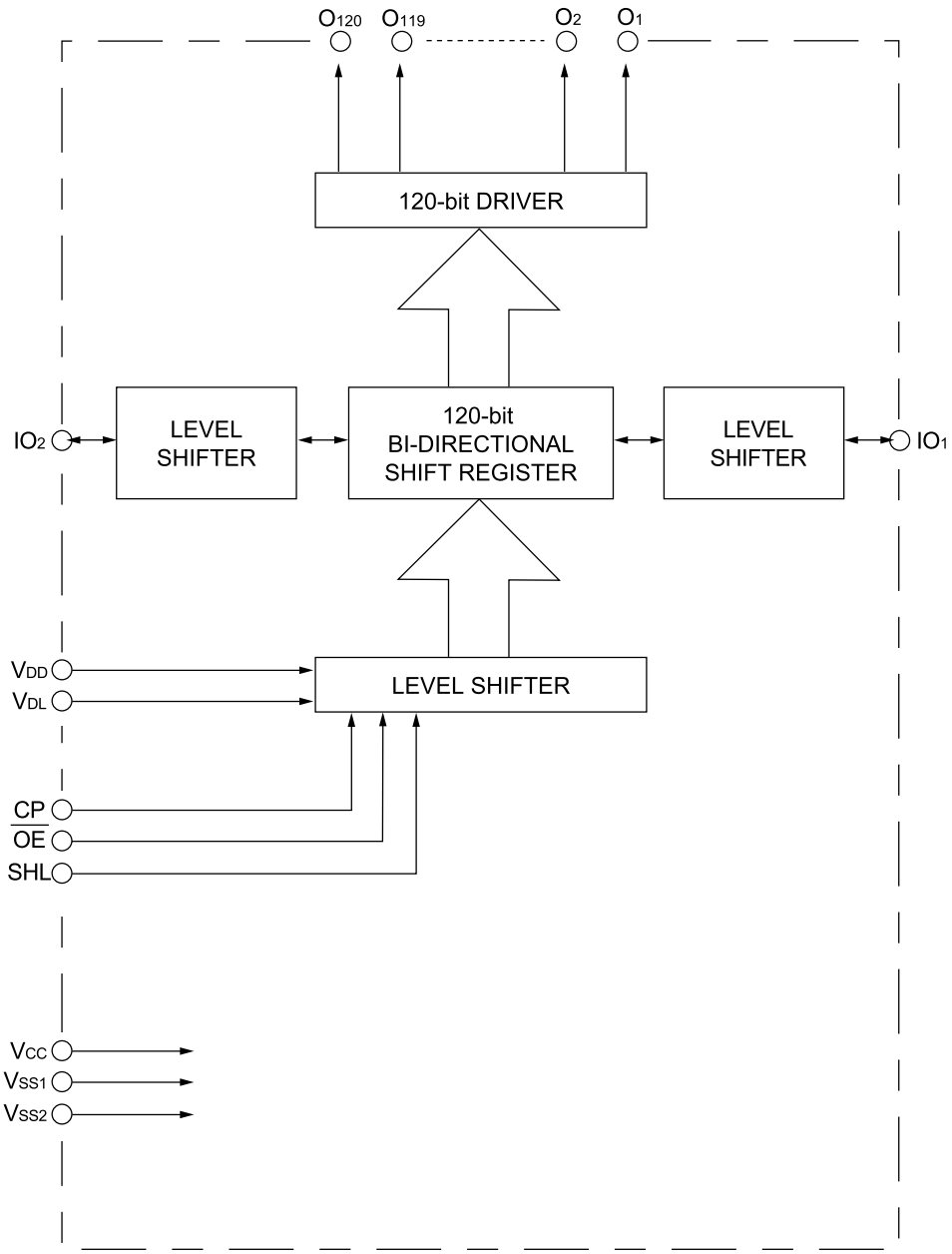
FEATURES

- Number of gate drive outputs: 120.
- Gate drive signal amplitude: 40 V (max.).
- Gate drive signal voltage: Positive voltage/negative voltage outputs can be made.
- Variable shift register scanning direction.
- Package: Bump chip, TCP.

PIN CONFIGURATION (TOP VIEW)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Conditions	Rating	Unit
Power Supply Voltage (1)	V_{CC}	Ta = 25°C	–0.3 to + 42.0	V
Power Supply Voltage (2)	V_{DL}	Ta = 25°C	– 0.3 to V_{DD} + 0.3	V
Power Supply Voltage (3)	V_{DD}	Ta = 25°C	–0.3 to + 27.0	V
Input Voltage	V_I	Ta = 25°C	– 0.3 to V_{DD} + 0.3	V
Storage Temperature Range	T_{Stg}	—	–30 to + 85	°C

RECOMMENDED OPERATING CONDITIONS

When using with V_{ss1} and V_{ss2} shorted together

(V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Conditions	Range	Unit
Power Supply Voltage (1)	V_{CC}	—	20 to 40	V
Power Supply Voltage (2)	V_{DL}	—	0 to 20	V
Power Supply Voltage (3)	V_{DD}	—	V_{DL} + 3 to V_{DL} + 5.5	V
Power Supply Voltage (4)	V_{CC} –V_{DL}	—	10 to 40	V
Operating Temperature Range	T_{op}	—	–20 to + 75	°C

When using with V_{ss1} and V_{ss2} separated

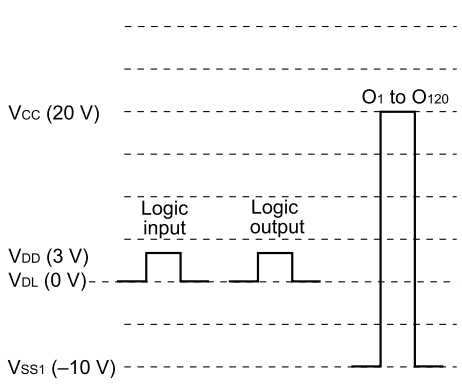
(V_{SS2} = 0 V)

Parameter	Symbol	Conditions	Range	Unit
Power Supply Voltage (1)	V_{CC}	—	20 to 40	V
Power Supply Voltage (2)	V_{DL}	—	0 to 20	V
Power Supply Voltage (3)	V_{DD}	—	V_{DL} + 3 to V_{DL} + 5.5	V
Power Supply Voltage (4)	V_{CC} –V_{DL}	—	10 to 40	V
Power Supply Voltage (5)	V_{SS1}	—	0 to 10	V
Power Supply Voltage (6)	V_{DL} –V_{SS1}	—	0 to 20	V
Operating Temperature Range	T_{op}	—	–20 to + 75	°C

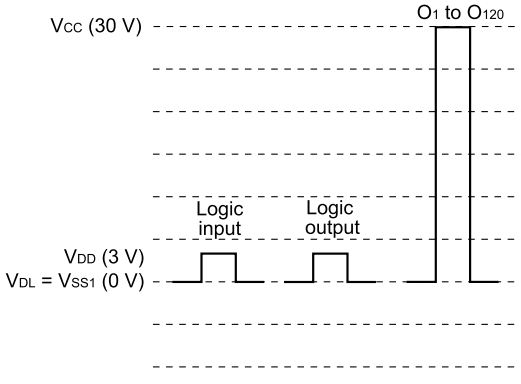
Voltage Settings

1) The MSM6696 can be set to give positive voltage or negative voltage gate drive outputs.
An example of negative voltage output is shown in 1-1), and an example of positive voltage output is shown in 1-2).
Input the logic input signals (CP, SHL, $\overline{OE}$, IO_1, and IO_2) with an amplitude of either V_{DD}–V_{DL} or V_{DD}–V_{ss2}.

1-1) Example of negative voltage output
($V_{SS1} = V_{SS2} = -10$ V, $V_{DL} = 0$ V)

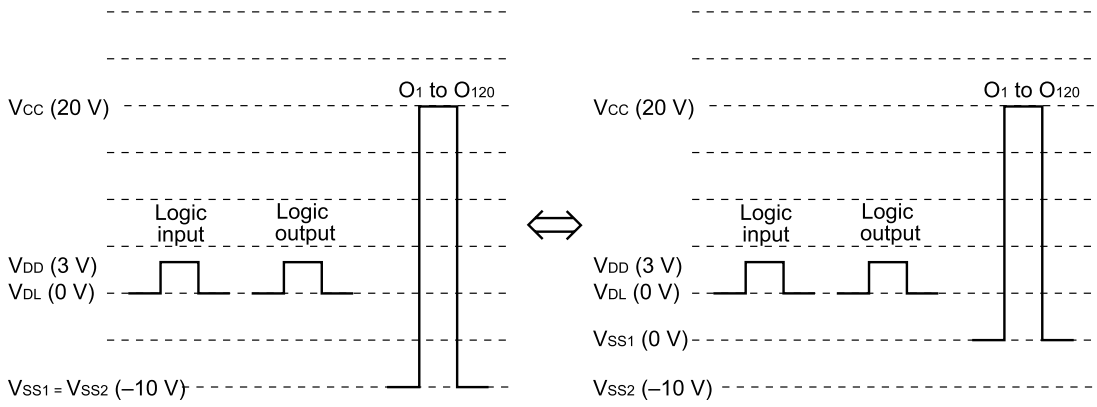


1-2) Example of positive voltage output
($V_{SS1} = V_{SS2} = V_{DL} = 0$ V)



2) In the MSM6696, since different voltages can be applied to V_{SS1} and V_{SS2}, it is possible to change the "L" level of the gate drive signals during operation.
An example of using with V_{ss1} and V_{ss2} separated is shown in 2-1) when giving negative voltage outputs. The voltage change of V_{ss1} directly corresponds as it is to the change in the gate drive signal "L" level. Use so that the voltage relationships among the power supplies other than Vss1 (those are, V_{CC}, V_{DD}, V_{DL}, and V_{ss2}) are kept fixed.
Input the logic input signals (CP, SHL, $\overline{OE}$, IO_1, and IO_2) with an amplitude of either V_{DD}-V_{DL} or V_{DD}-V_{ss2}.

2-1) Example of using with Vss_1 and Vss_2 separated during negative voltage outputs
($V_{SS} = -10$ V, $V_{DL} = 0$ V)



ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{CC} = 20 V, V_{DD} = 3 to 5.5 V, V_{DL} = 0 V, V_{SS1} = V_{SS2} =–10 V, T_A =–20 to + 75°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
"H" Input Voltage	V_{iH} *1	—	0.7× (V_{DD} –V_{DL}) +V_{DL}	—	V_{DD}	V
"L" Input Voltage	V_{IL} *1	—	V_{SS2}	—	0.3× (V_{DD} –V_{DL}) + V_{DL}	V
"H" Output Voltage	V_{OH} *2	I_O =–40 μ A	V_{DD} – 0.4	—	V_{DD}	V
"L" Output Voltage	V_{OL} *2	I_O = 40 μ A	V_{DL}	—	V_{DL} + 0.4	V
Input Current	I_I *1		–5.0	—	+5.0	μ A
"H" Output Resistance	R_{OH} *3	V_O = V_{CC} –0.5 V	—	—	1500	Ω
"L" Output Resistance	R_{OL} *3	V_O = V_{SS1} + 0.5 V	—	—	1500	Ω
Supply Current	I_{DD} *4	No load,	—	30	50	μ A
	I_{CC} *5	f_{CP} = 50 kHz 1/480 duty	—	350	600	μ A

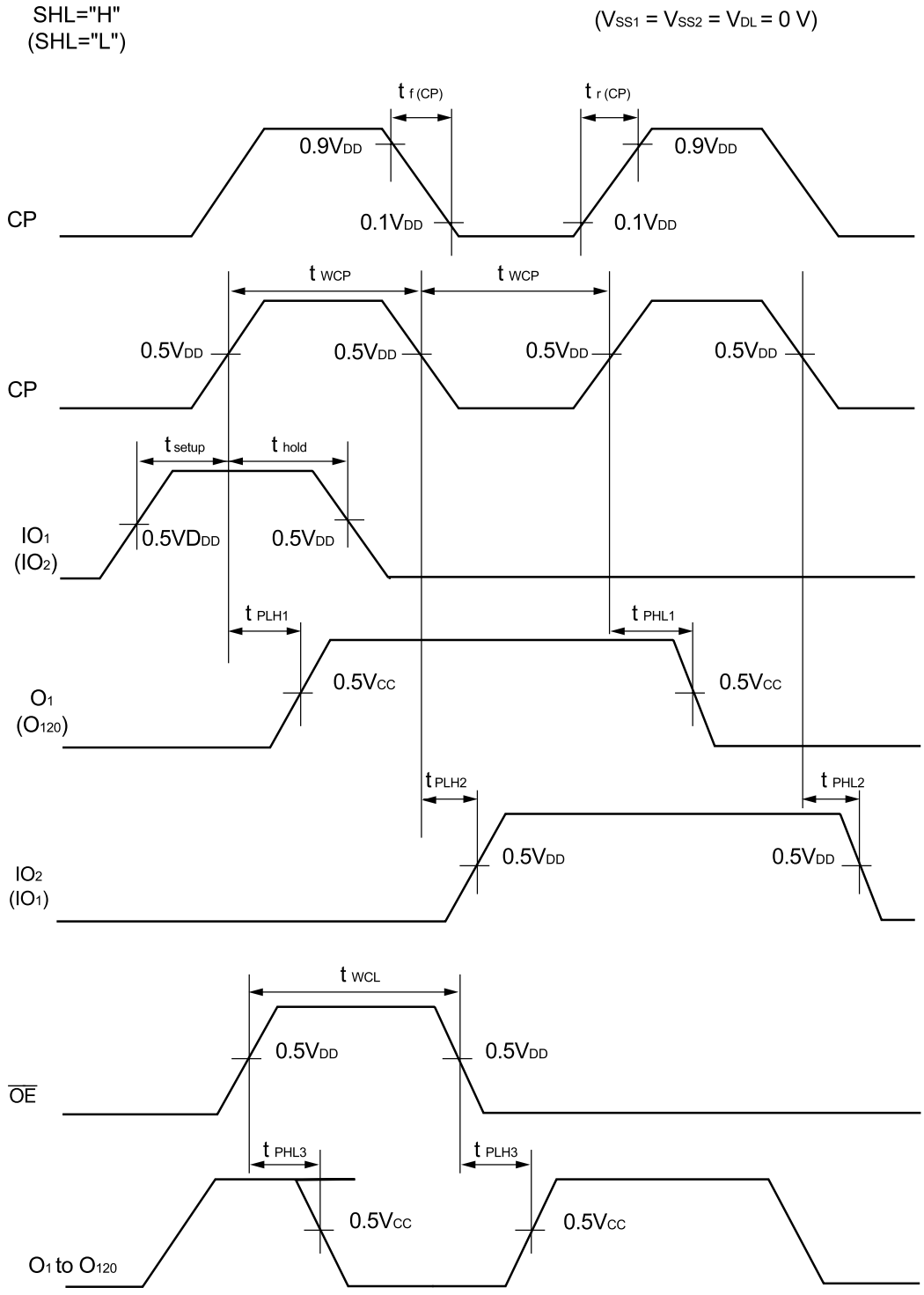
*1) Applicable to input pins (SHL, CP, $\overline{OE}$) and I/O pins (IO_1, IO_2).
*2) Applicable to I/O pins (IO_1, IO_2).
*3) Applicable to output pins (O_1 to O_{120}).
*4) Applicable to power supply pin V_{DD}.
*5) Applicable to power supply pin Vcc.

Switching Characteristics

(V_{CC} = 20 V, V_{DD} = 5 V, V_{DL} = 0 V, V_{SS1} = V_{SS2} = –10 V, T_A = –20 to + 75°C)

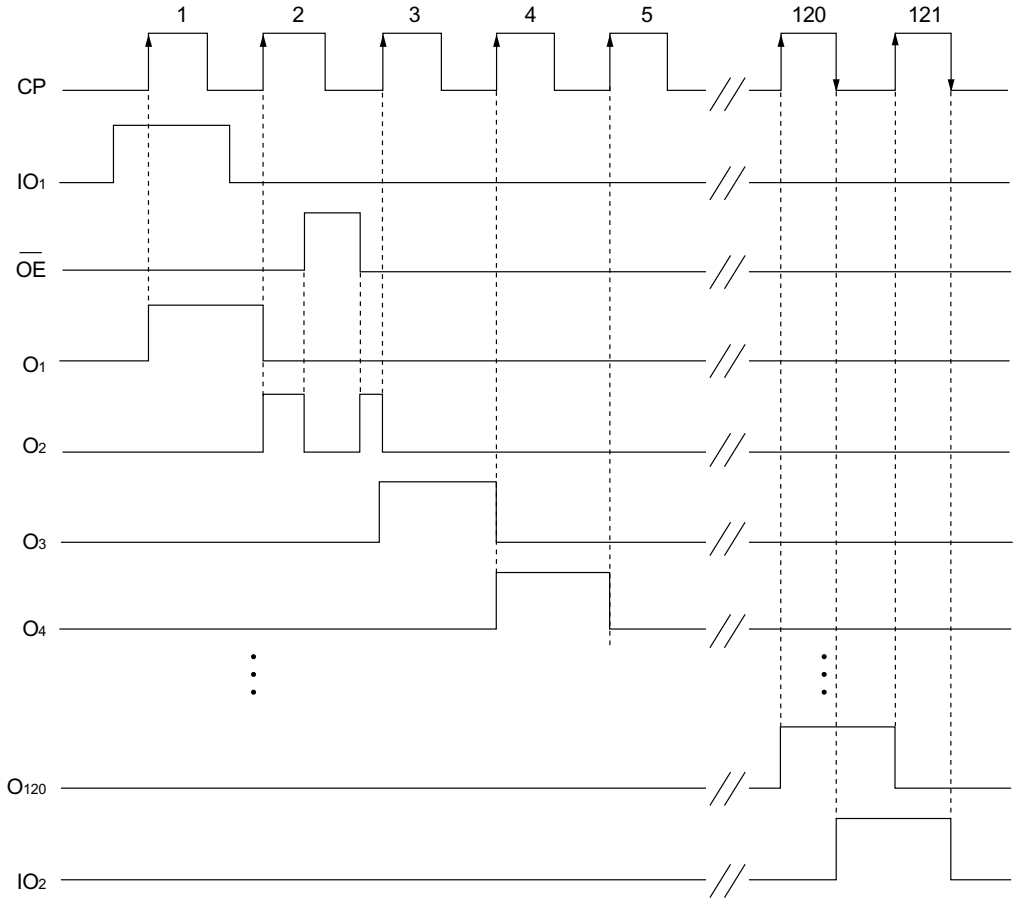
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Clock Frequency	f_{CP}	—	—	—	100	kHz
CP Pulse Width	t_{WCP}	—	400	—	—	ns
Clear Enable Time	T_{WCL}	—	1	—	—	μ s
Data Setup Time	t_{setup}	—	300	—	—	ns
Data Hold Time	t_{hold}	—	300	—	—	ns
CP Rise Time	$t_{r\,(cp)}$	—	—	—	30	ns
CP Fall Time	$t_{f\,(cp)}$	—	—	—	30	ns
Delay Time	t_{PLH1} (t_{PHL1})	C_L = 300pF	—	—	700	ns
	t_{PLH2} (t_{PHL2})	C_L = 30pF	—	—	400	ns
	t_{PLH3} (t_{PHL3})	C_L = 300pF	—	—	700	ns

TIMING DIAGRAM



FUNCTIONAL DESCRIPTION

The MSM6696 generates signals to drive 120-bit TFT gate using the 120-bit bi-directional shift register circuit and outputs them after level conversion.
The input signal for the shift register circuit is input at the rising edge of the clock pulse from the data input/output pin IO_1 (or IO_2). This signal is shifted at the rising edge of the clock pulse and is output at the falling edge of the clock pulse from the data input/output pin IO_2 (or IO_1). The TFT gate drive signals generated in the shift register circuit are output via the output pins O_1 to O_{120} in parallel after level conversion.
The direction of shifting the data can be selected by the input given to the shifting direction selection pin SHL. If the input to SHL is fixed at the "H" level, data will be shifted successively in the direction IO_1 to O_1 ... O_{120} to IO_2. If the input to SHL is fixed at the "L" level, data will be shifted successively in the direction IO_2 to O_{120} ... O_1 to IO_1. When an "H" level input is given to the clear input pin $\overline{OE}$, the outputs at all the output pins O_1 to O_{120} go to the "L" level irrespective of the shift data.
The timings of operations are shown below when an "H" level input is given to SHL.



Pin Functional Description

- IO_1, IO_2
  These are the data input/output pins for the 120-bit bi-directional shift register.
  The input data is read in from the pin IO_1 (or IO_2) at the rising edge of the clock pulse CP, and is output from the pin IO_2 (or IO_1) at the falling edge of CP after a shift register delay corresponding to 120 bits.

- SHL
  This is the input pin for selecting the shifting direction of the 120-bit bi-directional shift register.
  The functions of IO_1, IO_2, and SHL are given in the following table.

SHL	Shifting direction	Data input/output pin
"H"	O_1 to O_{120}	Input IO_1
		Output IO_2
"L"	O_{120} to O_1	Input IO_2
		Output IO_1

- CP
  This is the clock pulse input pin for the 120-bit bi-directional shift register.
  The input data is read in from the pin IO_1 (or IO_2) at the rising edge of the clock pulse CP, and is output from the pin IO_2 (or IO_1) at the falling edge of CP after a shift register delay corresponding to 120 bits.

- $\overline{OE}$
  This is the CLEAR input pin that fixes all gate drive signal outputs to the "L" level irrespective of the data stored in the shift register.
  The function of the $\overline{OE}$ pin is given in the following table.

$\overline{OE}$	Gate drive signals
"H"	All gate drive signals are tied to "L".
"L"	Correspond to the data in the shift register.

- O_1 to O_{120}
  These are the output pins for the gate drive signals.
  These pins correspond directly to each of the bits in the shift register.

- V_{DD}, V_{DL}
  These are the bias power supply pins for the level shifter.
  Always input a level lower than V_{DD} to the pin V_{DL} in accordance with the recommended operating conditions. ($V_{DD}>V_{DL}$)

- V_{CC}, V_{SS1}, V_{SS2}
  These are the power supply pins for this IC.
  V_{CC} determines the "H" level of the gate drive signals and V_{SS1} determines the "L" level of the gate drive signals.
  V_{SS2} is the reference level for the operations of this IC. Always input a level lower than the other power supply pins to the pin V_{ss2} in accordance with the recommended operating conditions. ($V_{CC}>V_{DD}>V_{DL}\geq V_{SS1}\geq V_{SS2}$)

CAUTIONS

- Since the power supply voltage of the gate driving section is high in this IC, applying a high voltage to the gate driving section with the logic section power supply left in the floating condition can cause excessive currents to flow thereby destroying the IC.
  Always adhere to the following sequences when switching ON and OFF the power supply to this IC.

  Power Supply Sequence 1
  At the time of power ON V_{DL}, $V_{DD} \rightarrow$ Logic inputs, V_{SS2} $V_{SS1} \rightarrow V_{CC}$
  At the time of power OFF $V_{CC} \rightarrow V_{SS1}$, V_{SS2}, Logic inputs $\rightarrow V_{DD}$, V_{DL}

  Power Supply Sequence 2
  At the time of power ON V_{DL}, V_{DD}, V_{SS2}, $V_{SS1} \rightarrow$ Logic inputs $\rightarrow V_{CC}$
  At the time of power OFF $V_{CC} \rightarrow$ Logic inputs $\rightarrow V_{SS1}$, V_{SS2}, V_{DD}, V_{DL}

- The output pins O_1 to O_{120} repeat switching of high voltage levels at high speed. Using this IC either with a short between the output pins or with a short between the output pins and other pins (input pins, input/output pins, power supply pins) can cause excessive currents to flow thereby destroying the IC. Never use the IC with any output pin shorted to other pins.

- This IC is provided with dummy pads other than the pads for making interconnections to the input pins, input/output pins, output pins, and power supply pins. Since some of the dummy pads are being fed with specific power supply voltages from inside the IC, interconnecting the dummy pads to the input pads, input/output pads, output pads, or power supply pads can cause excessive currents to flow thereby destroying the IC.
  Always keep the dummy pads open.

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