OKI OKI Semiconductor **MSM9888L/9889L**



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3V, Serial Voice Flash Memory-driving Recording and Playback IC

GENERAL DESCRIPTION

The MSM9888L/9889L are recording and playback ICs that are controlled by a microcontroller in serial mode, compress voice with the OKI ADPCM system with high tone quality, and directly store voice data in the serial voice flash momory. These ICs can operate in the range of 2.7 to 3.6 V and contain a mask ROM. Since the package is small and backup is not needed, these recording and playback ICs are suitable for voice systems such as handy terminals.

FEATURES

- Serial microcontroller interface
- Direct driving of serial voice flash memory
- 2-Mbit (MSM9892L), 4-Mbit (MSM9893L), 8-Mbit (MSM9894AL)
- Built-in mask ROM for fixed message
- Recording time (When the 2-Mbit serial voice flash memory is used)
 - : Approximately 65 seconds (Fsam=8.0 kHz)
 - : Approximately 81 seconds (Fsam=6.4 kHz)
 - : Approximately 130 seconds (Fsam=4.0 kHz)
- Playback time for fixed message
 - MSM9888L : Approximately 15 seconds (Fsam=8.0 kHz)
 - (Built-in 512-Kbit mask ROM) : Approximately 20 seconds (Fsam=6.4 kHz)
 - : Approximately 31 seconds (Fsam=4.0 kHz)
 - MSM9889L: Approximately 30 seconds (Fsam=8.0 kHz)(Built-in 1-Mbit mask ROM): Approximately 40 seconds (Fsam=6.4 kHz)
 - : Approximately 62 seconds (Fsam=4.0 kHz)
- Any data can be written to and read from the serial voice flash memory.
- Voice analyzing and synthesizing system
 - : 4-bit OKI ADPCM system, 8-bit OKI non-linear PCM system (for ROM playback only)
- Sampling frequency (for 4.096 MHz of master oscillation frequency)
- : 2.0 kHz, 2.7 kHz, 3.2kHz, 4.0 kHz, 5.3 kHz, 6.4 kHz, 8.0 kHz
- Built-in 12-bit A/D converter and 12-bit D/A converter
- Built-in LPF : Attenuation rate of -40 dB/oct
 Master oscillation frequency : 4 MHz to 6 MHz
 Supply voltage : 2.7 V to 3.6 V
 Operating temperature : -10°C to +70°C
 Operating current : Up to 15 mA (master oscillation frequency : 6 MHz, supply voltage : 3.6V)
 Number of phrases
 Variable message : 63 phrases
 Find means an example : 255 phrases
- Fixed message : 255 phrases • General-purpose message Japanese : MSM988L-820 English : MSM988L-819

• Package :

MSM9888L	: 30-pin plastic SSOP (SSOP30-P-56-0.65-K) (MSM9888L-xxxGS-AK)
MSM9889L	: 32-pin plastic TSOP (TSOP(1)32-P-0814-0.50-1K) (MSM9889L-xxxTA)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)

SG T	30 AGND
AMON 2	29 LOUT
FIN 3	28 LIN
ADIN 4	27 FRESET
FOUT 5	26 FPRT
AOUT 6	25 FCS
AVDD 7	24 FSCK
DVDD 8	23 FDI
CS 9	22 FDO
XT 10	21 DGND
XT 11	20 BUSY
SCK 12	19 TEST2
D0 13	18 TEST1
DI 14	17 TEST0
MON 15	16 RESET

MSM9888L (Built-in 512-Kbit Mask ROM)

30-Pin Plastic SSOP







32-Pin Plastic TSOP

PIN DESCRIPTION

MesselMesselMessel143DII132DOO143DII132DOO14SCKIInputs the 8-bit status data.124SCKIInputs the data transfer clock for the DI and DO pins.124SCKIInputs the data transfer clock for the DI and DO pins.95 \overline{CS} IAccepts the SCK pulse, when \overline{CS} is "L" level. Does not accept the SCK pulse201BUSYOOutputs "H" level during command execution. When driven high, do not input a command from the external micro-controller.1531MONOOutputs "H" level during recording or playback.2325FDIOConnected to the D pin of the serial voice flash memory.2426FSCKOConnected to the D pin of the serial voice flash memory.2527FCSOConnected to the REST pin of the serial voice flash memory.2628FPRTOConnected to the REST pin of the serial voice flash memory.2729FRESETOConnected to the REST pin of the serial voice flash memory.1119 \overline{XT} OScillator connecting pins. When using an external clock, input the clock from the XT pin and keep the \overline{XT} pin open.1119 \overline{XT} OAnalog reference voltage (Signal Ground) output pin.1118SGOAnalog reference voltage (Signal Ground) output pin.12	Pin D. H. T. D. H.									
13 2 D0 0 Outputs the 8-bit status data. 12 4 SCK 1 Inputs the data transfer clock for the D1 and D0 pins. 9 5 CS 1 Accepts the SCK pulse, when CS is "L" level. Does not accept the SCK pulse when CS is "L" level. 20 1 BUSY 0 Outputs "H" level during command execution. When driven high, do not input a command from the external micro-controller. 15 31 MON 0 Outputs "H" level during recording or playback. 22 24 FD0 1 Connected to the D pin of the serial voice flash memory. 22 24 FD0 1 Connected to the DX pin of the serial voice flash memory. 25 FZ FCS 0 Connected to the PRT pin of the serial voice flash memory. 26 RESET 0 Connected to the PRT pin of the serial voice flash memory. 27 29 FRESET 0 Connected to the ZS pin of the serial voice flash memory. 10 20 XT 1 Oscillator connecting pins. When using an external clock, input the clock from the XT pin and keep the XT pin open. 11 19 XT 0 Set the XT pin to the GND level in powe	M9888L	M9889L	Symbol	Туре	Description					
12 4 SCK I Inputs the data transfer clock for the DI and D0 pins. 9 5 CS I Accepts the SCK pulse, when CS is "L" level. Does not accept the SCK pulse when CS is "L" level. 20 1 BUSY 0 Outputs "H" level during command execution. When driven high, do not input a command from the external micro-controller. 15 31 MON 0 Outputs "H" level during recording or playback. 22 24 FD0 I Connected to the D0 pin of the serial voice flash memory. 24 26 FSCK 0 Connected to the SCK pin of the serial voice flash memory. 25 27 FCS 0 Connected to the RSC pin of the serial voice flash memory. 26 28 FPRT 0 Connected to the RESET pin of the serial voice flash memory. 10 20 XT I Oscillator connecting pins. When using an external clock, input the clock from the XT pin and keep the XT pin open. 11 19 XT 0 Set the XT pin to the GND level in power-down mode. 11 19 XT 0 Scillation stabilization time. Set to "H" level after oscillation stabilizea at 2.7V or more. 1 8 <td< td=""><td>14</td><td>3</td><td>DI</td><td>I</td><td>Inputs the 8-bit command data.</td></td<>	14	3	DI	I	Inputs the 8-bit command data.					
9 5 CS I Accepts the SCK pulse, when CS is "L" level. Does not accept the SCK pulse when CS is "L" level. 20 1 BUSY 0 Outputs "H" level during command execution. When driven high, do not input a command from the external micro-controller. 15 31 MON 0 Outputs "H" level during recording or playback. 23 25 FDI 0 Connected to the DI pin of the serial voice flash memory. 24 26 FSCK 0 Connected to the CS pin of the serial voice flash memory. 26 27 FCS 0 Connected to the BT pin of the serial voice flash memory. 27 29 FRESET 0 Connected to the REST pin of the serial voice flash memory. 20 XT 1 Oscillator connecting pins. When using an external clock, input the clock from the XT pin and keep the XT pin open. 11 19 XT 0 St the XT pin to the Sol Ti open. 16 6 RESET 1 Oscillator stabilization time. Set to "H" level after oscillation stabilizes. "L" level should be input to this pin until power supply voltage is stabilized at 2.7V or more. 1 8 SG	13	2	DO	0	Outputs the 8-bit status data.					
9 5 CS 1 when CS is 'H' level. 20 1 BUSY 0 Outputs 'H' level during command execution. When driven high, do not input a command from the external micro-controller. 15 31 MON 0 Outputs 'H' level during recording or playback. 22 25 FDI 0 Connected to the DI pin of the serial voice flash memory. 22 24 FDO 1 Connected to the CS pin of the serial voice flash memory. 25 27 FCS 0 Connected to the RESET pin of the serial voice flash memory. 26 28 FPRT 0 Connected to the RESET pin of the serial voice flash memory. 10 20 XT 1 Oscillator connecting pins. When using an external clock, input the clock from the XT pin and keep the XT pin open. 11 19 XT 0 Set the XT pin to the GND level in power-down mode. 16 6 RESET 1 oscillator stabilization time. Set to 'H' level si pin util power supply voltage is stabilized at 2.''V or orrore. 1 8 SG 0 Analog reference voltage (Signal Ground) output pin. Insert an electrolytic capacitor of 1µF between this pin and AGND pin. 28	12	4	SCK	I	•					
20 1 BUSY 0 command from the external micro-controller. 15 31 MON 0 Outputs 'H' level during recording or playback. 23 25 FDI 0 Connected to the DI pin of the serial voice flash memory. 24 26 FSCK 0 Connected to the CS pin of the serial voice flash memory. 25 27 FCS 0 Connected to the CS pin of the serial voice flash memory. 26 28 FPRT 0 Connected to the RESET pin of the serial voice flash memory. 26 28 FPRT 0 Connected to the RESET pin of the serial voice flash memory. 10 20 XT 1 Oscillator connecting pins. When using an external clock, input the clock from the XT pin to the GND level in power-down mode. 11 19 XT 0 Set the XT pin to the GND level in power-down mode. 16 6 RESET 1 Oscillation stabilization time. Set to 'H' level after oscillation stabilizes. 'L' level should be input to this pin until power supply voltage is stabilized at 2.7V or more. 1 8 SG 0 Analog reference voltage (Signal Ground) output pin. Insert an electrolytic capacitor of 1µF between this pin and AGND pin.	9	5	CS	I						
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22 24 FD0 1 Connected to the D0 pin of the serial voice flash memory. 24 26 FSCK 0 Connected to the SCK pin of the serial voice flash memory. 25 27 FCS 0 Connected to the CS pin of the serial voice flash memory. 26 28 FPRT 0 Connected to the RESET pin of the serial voice flash memory. 27 29 FRESET 0 Connected to the RESET pin of the serial voice flash memory. 10 20 XT 1 Oscillator connecting pins. When using an external clock, input the clock from the XT pin and keep the XT pin open. 11 19 XT 0 Set the XT pin to the GND level in power-down mode. 16 6 RESET 1 Oscillation stabilization time. Set to "H" level after oscillation stabilized at 2.7V or more. 1 8 SG 0 Analog reference voltage (Signal Ground) output pin. 18 9 LIN 1 Built-in OP amplifier's invention input pin 4 13 ADIN 1 Built-in OP amplifier's output pin 2 11 AMON 0 Connected to the LOUT pin when recording mode, and to the DA converter's output pin	15	31	MON	0	Outputs "H" level during recording or playback.					
24 26 FSCK 0 Connected to the SCK pin of the serial voice flash memory. 25 27 FCS 0 Connected to the CS pin of the serial voice flash memory. 26 28 FPRT 0 Connected to the PRT pin of the serial voice flash memory. 27 29 FRESET 0 Connected to the RESET pin of the serial voice flash memory. 10 20 XT 1 Oscillator connecting pins. When using an external clock, input the clock from the XT pin and keep the XT pin open. 11 19 XT 0 Set the XT pin to the GND level in power-down mode. 16 6 RESET 1 oscillation stabilization time. Set to "H" level after oscillation stabilizes. 1 8 SG 0 Analog reference voltage (Signal Ground) output pin. 1 8 SG 0 Analog reference voltage (Signal Ground) output pin. 28 9 LIN 1 Built-in OP amplifier's invention input pin. 4 13 ADIN 1 Built-in OP amplifier's output pin 2 11 AMON 0 <td< td=""><td>23</td><td>25</td><td>FDI</td><td>0</td><td>Connected to the DI pin of the serial voice flash memory.</td></td<>	23	25	FDI	0	Connected to the DI pin of the serial voice flash memory.					
25 27 FCS 0 Connected to the CS pin of the serial voice flash memory. 26 28 FPRT 0 Connected to the PRT pin of the serial voice flash memory. 10 20 XT 1 Oscillator connecting pins. When using an external clock, input the clock from the XT pin and keep the XT pin open. 11 19 XT 0 Set the XT pin to the GND level in power-down mode. 16 6 RESET 1 The LS1 is reset and starts oscillation when "L" level is input, keep "L" level during oscillation stabilization time. Set to "H" level after oscillation stabilizes. "L" level should be input to this pin until power supply voltage is stabilized at 2.7V or more. 1 8 SG 0 Insert an electrolytic capacitor of 1µF between this pin and AGND pin. 28 9 LIN 1 Built-in OP amplifier's invention input pin. The non-invention input pin is internally connected to SG. 29 10 LOUT 0 Built-in 12-bit AD converter's input pin Connected to the LOUT pin when playback mode. Connected to the DA converter's output pin when playback mode. Connected to the AD converter's input (FIN pin) 3 12 FIN 1 Built-in LPF's output pin. This is the output pin the played back waveform and connected to the speaker driving amplifier.	22	24	FD0	I	Connected to the DO pin of the serial voice flash memory.					
26 28 FPRT 0 Connected to the PRT pin of the serial voice flash memory. 27 29 FRESET 0 Connected to the RESET pin of the serial voice flash memory. 10 20 XT I Oscillator connecting pins. When using an external clock, input the clock from the XT pin and keep the XT pin open. 11 19 XT 0 Set the XT pin to the GND level in power-down mode. 16 6 RESET I The LSI is reset and starts oscillation when "L" level is input, keep "L" level during oscillation stabilization time. Set to "H" level after oscillation stabilizes. 1 8 SG 0 Analog reference voltage (Signal Ground) output pin. 18 SG 0 Analog reference voltage (Signal Ground) output pin. 19 1 8 SG 0 10 LOUT 0 Built-in OP amplifier's invention input pin. The non-invention input pin is internally connected to SG. 29 10 LOUT 0 Built-in 12-bit AD converter's input pin 2 11 AMON 0 Connected to the LOUT pin when recording mode, and to the DA converter's output pin when playback mode. Connected to the AD converter's input (FIN pin). 3 12	24	26	FSCK	0	Connected to the SCK pin of the serial voice flash memory.					
27 29 FRESET 0 Connected to the RESET pin of the serial voice flash memory. 10 20 XT 1 Oscillator connecting pins. When using an external clock, input the clock from the XT pin and keep the XT pin open. Set the XT pin to the GND level in power-down mode. 11 19 XT 0 The LSI is reset and starts oscillation when "L" level is input, keep "L" level during oscillation stabilization time. Set to "H" level after oscillation stabilizes. "L" level should be input to this pin until power supply voltage is stabilized at 2.7V or more. 1 8 SG 0 Analog reference voltage (Signal Ground) output pin. Insert an electrolytic capacitor of 1µF between this pin and AGND pin. 28 9 LIN 1 Built-in OP amplifier's invention input pin. Internally connected to SG. 29 10 LOUT 0 Built-in OP amplifier's output pin 4 13 ADIN 1 Built-in DP's output pin. On the LOUT pin when recording mode, and to the DA converter's output pin when playback mode. Connected to the AD converter's input (ADIN pin). 3 12 FIN 1 Built-in LPF's output pin. On the speaker driving amplifier. 17-19/21-23 TEST0-2 1 LSI testing pins. Fix to "L". Built-in LPF's output pin. This is the output pin the played back waveform and connected to the speaker	25	27	FCS	0	Connected to the CS pin of the serial voice flash memory.					
10 20 XT I Oscillator connecting pins. When using an external clock, input the clock from the XT pin and keep the XT pin open. Set the XT pin and keep the XT pin open. 11 19 XT 0 Set the XT pin to the GND level in power-down mode. 16 6 RESET 1 The LSI is reset and starts oscillation when "L" level is input, keep "L" level during oscillation stabilization time. Set to "H" level after oscillation stabilizes. "L" level should be input to this pin until power supply voltage is stabilized at 2.7V or more. 1 8 SG 0 Analog reference voltage (Signal Ground) output pin. Insert an electrolytic capacitor of 1μF between this pin and AGND pin. 28 9 LIN I Built-in OP amplifier's invention input pin. The non-invention input pin is internally connected to SG. 29 10 LOUT 0 Built-in 12-bit AD converter's input pin 2 11 AMON 0 Connected to the LOUT pin when recording mode, and to the DA converter's output pin when playback mode. Connected to the built-in LPF's input (FIN pin). 3 12 FIN I Built-in LPF's output pin. Connected to the AD converter's input (ADIN pin). 6 15 AOUT 0 Built-in LPF's output pin. This is the output pin the played back waveform and connected to the speaker driving amplifier.	26	28	FPRT	0	Connected to the PRT pin of the serial voice flash memory.					
10 20 XT I Oscillator connecting pins. When using an external clock, input the clock from the XT pin and keep the XT pin open. Set the XT pin to the GND level in power-down mode. 11 19 XT 0 The LSI is reset and starts oscillation when "L" level is input, keep "L" level during oscillation stabilization time. Set to "H" level after oscillation stabilizes. "L" level should be input to this pin until power supply voltage is stabilized at 2.7V or more. 1 8 SG 0 Analog reference voltage (Signal Ground) output pin. Insert an electrolytic capacitor of 1μF between this pin and AGND pin. 28 9 LIN I Built-in OP amplifier's invention input pin. The non-invention input pin is internally connected to SG. 29 10 LOUT 0 Built-in OP amplifier's output pin 2 11 AMON 0 Connected to the LOUT pin when recording mode, and to the DA converter's output pin when playback mode. Connected to the built-in LPF's input (FIN pin) 3 12 FIN I Built-in LPF's output pin. This is the output pin the played back waveform and connected to the speaker driving amplifier. 17:19:21-23 TESTO-2 I LSI testing pins. Fix to "L". 8 18 DV _{DD} Digital power supply pin. Insert a bypass capacitor of 0.1µF or higher between this pin and AGND pin. <	27	29	FRESET	0	Connected to the RESET pin of the serial voice flash memory.					
11 19 XI 0 Set the XT pin to the GND level in power-down mode. 16 6 RESET I The LSI is reset and starts oscillation when "L" level is input, keep "L" level during oscillation stabilization time. Set to "H" level after oscillation stabilizes. 1 8 SG 0 Analog reference voltage (Signal Ground) output pin. 1 8 SG 0 Insert an electrolytic capacitor of 1μF between this pin and AGND pin. 28 9 LIN I Built-in OP amplifier's invention input pin. The non-invention input pin is internally connected to SG. 29 10 LOUT 0 Built-in OP amplifier's output pin 2 11 AMON 0 Connected to the LOUT pin when recording mode, and to the DA converter's output pin when playback mode. Connected to the built-in LPF's input (FIN pin). 3 12 FIN I Built-in LPF's output pin. 5 14 FOUT 0 Built-in LPF's output pin. This is the output pin the played back waveform and connected to the speaker driving amplifier. 17-19/21-23 TESTO-2 I LSI testing pins. Fix to "L". Built-in LPF's output pin. Insert a bypass capacitor of 0.1µF or higher between this pin and DGND pin. 21 </td <td>10</td> <td>20</td> <td>XT</td> <td>1</td> <td></td>	10	20	XT	1						
Set the XT pin to the GND level in power-down mode. 16 6 RESET 1 The LSI is reset and starts oscillation when "L" level is input, keep "L" level during oscillation stabilization time. Set to "H" level after oscillation stabilized at 2.7V or more. 1 8 SG 0 Analog reference voltage (Signal Ground) output pin. Insert an electrolytic capacitor of 1µF between this pin and AGND pin. 28 9 LIN 1 Built-in OP amplifier's invention input pin. The non-invention input pin is internally connected to SG. 29 10 LOUT 0 Built-in 12-bit AD converter's input pin 2 11 AMON 0 Connected to the LOUT pin when recording mode, and to the DA converter's output pin when playback mode. Connected to the built-in LPF's input (FIN pin). 3 12 FIN 1 Built-in LPF's output pin. Connected to the AD converter's input (ADIN pin). 6 15 AOUT 0 Built-in LPF's output pin. This is the output pin the played back waveform and connected to the speaker driving amplifier. 17:19:21-23 TESTO-2 1 LSI testing pins. Fix to "L". 8 18 DV _{DD} — Digital power supply pin. Insert a bypass capacitor of 0.1µF or higher between this pin and AGND pin. 21 30 DGND					the XT pin and keep the \overline{XT} pin open.					
166RESETIThe LSI is reset and starts oscillation when "L" level is input, keep "L" level during oscillation stabilization time. Set to "H" level after oscillation stabilizes. "L" level should be input to this pin until power supply voltage is stabilized at 2.7V or more.18SG0Analog reference voltage (Signal Ground) output pin. Insert an electrolytic capacitor of 1μF between this pin and AGND pin.289LINIBuilt-in OP amplifier's invention input pin. The non-invention input pin is internally connected to SG.2910LOUTOBuilt-in OP amplifier's output pin413ADINIBuilt-in 12-bit AD converter's input pin211AMON0Connected to the LOUT pin when recording mode, and to the DA converter's output pin when playback mode. Connected to the built-in LPF's input (FIN pin).312FINIBuilt-in LPF's output pin.514FOUTOBuilt-in LPF's output pin.615AOUT0Built-in LPF's output pin.17-19/21-23TESTO-2ILSI testing pins. Fix to "L".818DV _{DD} —Digital power supply pin.2130DGND—Digital power supply pin.716AV _{DD} —Analog power supply pin.716AV _{DD} —Analog power supply pin.716AV _{DD} —Analog power supply pin.	11	19	XI	0	Set the XT pin to the GND level in power-down mode.					
1 8 SG 0 Insert an electrolytic capacitor of 1μF between this pin and AGND pin. 28 9 LIN I Built-in OP amplifier's invention input pin. The non-invention input pin is internally connected to SG. 29 10 LOUT 0 Built-in OP amplifier's output pin 4 13 ADIN I Built-in 12-bit AD converter's input pin 2 11 AMON 0 Connected to the LOUT pin when recording mode, and to the DA converter's output pin when playback mode. Connected to the built-in LPF's input (FIN pin) 3 12 FIN I Built-in LPF's input pin 5 14 FOUT 0 Built-in LPF's output pin. Connected to the AD converter's input (ADIN pin). 6 15 AOUT 0 Built-in LPF's output pin. This is the output pin the played back waveform and connected to the speaker driving amplifier. 17-1921-23 TESTO-2 I LSI testing pins. Fix to "L". 8 18 DV _{DD} — Digital power supply pin. Insert a bypass capacitor of 0.1µF or higher between this pin and DGND pin. 7 16 AV _{DD} — Analog power supply pin. Insert a bypass capacitor of 0.1µF or higher between this pin and AGND pin. <	16	6	RESET	I	"L" level should be input to this pin until power supply voltage is stabilized at					
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28 9 LIN 1 internally connected to SG. 29 10 LOUT 0 Built-in OP amplifier's output pin 4 13 ADIN I Built-in 12-bit AD converter's input pin 2 11 AMON 0 Connected to the LOUT pin when recording mode, and to the DA converter's output pin when playback mode. Connected to the built-in LPF's input (FIN pin). 3 12 FIN I Built-in LPF's input pin 5 14 FOUT 0 Built-in LPF's output pin. Connected to the AD converter's input (ADIN pin). 6 15 AOUT 0 Built-in LPF's output pin. This is the output pin the played back waveform and connected to the speaker driving amplifier. 17-19/21-23 TEST0-2 I LSI testing pins. Fix to "L". 8 18 DV _{DD} — Digital power supply pin. Insert a bypass capacitor of 0.1µF or higher between this pin and DGND pin. 7 16 AV _{DD} — Analog power supply pin. Insert a bypass capacitor of 0.1µF or higher between this pin and AGND pin.		Ŭ	04		Insert an electrolytic capacitor of $1\mu F$ between this pin and AGND pin.					
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615AOUT0Built-in LPF's output pin. This is the output pin the played back waveform and connected to the speaker driving amplifier.17-1921-23TEST0-2ILSI testing pins. Fix to "L".818DV_DDDigital power supply pin. Insert a bypass capacitor of 0.1µF or higher between this pin and DGND pin.2130DGNDDigital DGND pin716AV_DDAnalog power supply pin. Insert a bypass capacitor of 0.1µF or higher between this pin and AGND pin.	3	12	FIN	I	Built-in LPF's input pin					
6 15 AOU1 0 connected to the speaker driving amplifier. 17-19 21-23 TEST0-2 I LSI testing pins. Fix to "L". 8 18 DV _{DD} — Digital power supply pin. Insert a bypass capacitor of 0.1µF or higher between this pin and DGND pin. 21 30 DGND — Digital DGND pin 7 16 AV _{DD} — Analog power supply pin. Insert a bypass capacitor of 0.1µF or higher between this pin and AGND pin.	5	14	FOUT	0	Built-in LPF's output pin. Connected to the AD converter's input (ADIN pin).					
8 18 DV _{DD} — Digital power supply pin. Insert a bypass capacitor of 0.1μF or higher between this pin and DGND pin. 21 30 DGND — Digital DGND pin. 7 16 AV _{DD} — Analog power supply pin. Insert a bypass capacitor of 0.1μF or higher between this pin and AGND pin.	6	15	AOUT	0						
8 18 DV _{DD} — this pin and DGND pin. 21 30 DGND — Digital DGND pin 7 16 AV _{DD} — Analog power supply pin. Insert a bypass capacitor of 0.1µF or higher between this pin and AGND pin.	17-19	21-23	TEST0-2	1	LSI testing pins. Fix to "L".					
7 16 AV _{DD} — Analog power supply pin. Insert a bypass capacitor of 0.1μF or higher between this pin and AGND pin.	8	18	DV _{DD}	_						
7 16 AV _{DD}	21	30	DGND	_	Digital DGND pin					
	7	16	AV _{DD}	_						
	30	7	AGND	_	Analog GND pin					

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V _{DD}	Ta=25°C	-0.3 to +7.0	V
Input Voltage	VIN	Ta=25°C	-0.3 to V _{DD} +0.3	V
Storage Temperature	T _{STG}	—	-55 to +150	٥C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Power Supply Voltage	V _{DD}	DGND=AGND=0V	2.7 to 3.6	V
Operating Temperature	T _{op}	—	-40 to +85	°C
Master Clock Frequency	fosc	—	4.0 to 6.5	MHz

ELECTRICAL CHARACTERISTICS

DC Characteristics

Parameter	Parameter Symbol Condition		Min.	Тур.	Max.	Unit	
High-level Input Voltage	V _{IH}	_	_	V _{DD} ×0.85			V
Low-level Input Voltage	VIL	-	_		_	V _{DD} ×0.15	V
High-level Output Voltage	V _{OH}	I _{0H} =-	40μΑ	V _{DD} -0.3	—	—	V
Low-level Output Voltage	V _{OL}	I _{OL} =	2mA		_	0.45	V
High-level Input Current (*1)	I _{IH1}	V _{IH} =V _{DD}			_	10	μA
High-level Input Current (*2)	I _{IH2}	V _{IH} =	V _{DD}		_	20	μA
Low-level Input Cerrent (*1)	I _{IL1}	V _{IL} =	GND	-10	_	_	μA
Low-level Input Current (*2)	I _{IL2}	V _{IL} =	GND	-20	_	—	μA
Operating Current	I _{DD}	f _{OSC} =6.5MHz, without load		_	4	15	mA
Standby Current	IDDS	At power down,	MSM9888L		1	10	μΑ
	פטטי	without load	MSM9889L	—	1	Undefined	μA

*1 Applies to input pins excluding XT pin.*2 Applies to XT pin.

Analog Characteristics

Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
D/A Output Relative Error	V _{DAE}	No load	—	—	5	mV
FIN Allowable Input	V		$\frac{1}{4} \times V_{DD}$		$\frac{3}{4} \times V_{DD}$	V
Voltage Range	V _{FIN}		$\overline{4}^{\times VDD}$		$\overline{4}^{\times VDD}$	v
FIN Input Impedance	R _{FIN}	No load	1		—	MΩ
ADIN Allowable Input	V		1		$\frac{3}{4} \times V_{DD}$	V
Voltage Range	Vadin		$\frac{1}{4} \times V_{DD}$		$\overline{4}^{\times VDD}$	V
ADIN Input Impedance	R _{ADIN}	—	1	_	—	MΩ
OP Amplifier Open Loop Gain	G _{OP}	f _{IN} =0 to 4kHz	10		—	dB
OP Amplifier Input Impedance	R _{INA}	—	1		—	MΩ
OP Amplifier Load	р		100			ko
Resistance	R _{OUTA}		100	_		kΩ
AOUT Load Resistance	R _{AOUT}	_	50		—	kΩ
FOUT Load Resistance	R _{FOUT}	_	50		—	kΩ

MSM9888L/9889L

AC Characteristics

			-	_{DD} =AV _{DD} =2.7 to +85°C, f ₀			
P	arameter		Symbol	-	Typ.	Max.	Unit
Oscillation duty cycle			f _{duty}	40	50	60	%
RESET pulse width			t _{RST}	1µs or longer than when oscillation is stabilized	_	_	
RESET execution time		Note 1	t _{REX}		_	35	ms
Setup and hold time of SCI	K for CS		t _{скс}	200		_	ns
Setup and hold time of $\overline{\text{CS}}$	for SCK		t _{CCK}	200	_	_	ns
SCK pulse width "H"			t _{СКН}	500	_	_	ns
SCK pulse width "L"			t _{CKL}	500	—	—	ns
Setup time of DI to SCK ris	е		t _{DS}	200	_	—	ns
Hold time of DI to SCK rise			t _{DH}	200			ns
Data definition time to $\overline{\text{CS}}$ f	all		t _{CSE}			200	ns
Data float time to $\overline{\text{CS}}$ fall			t _{CSF}			200	ns
Data definition time to SCK	fall		t _{DD}			200	ns
Delay time of BUSY rise to	8th SCK bit rise		t _{BSY}			200	ns
BUSY time at input of com	mand (normal)	Note 1	t _{BR}		100	300	μs
BUSY time at input of REC	command (2)	Note 1	t _{RECB}	—		1	ms
Time from input of REC co	mmand (2) to MON rise		t _{RECM}	—		1	ms
Time from input of REC co	mmand (2) to PRM bit rise		t _{RECR}	—		3	ms
BUSY time at input of PLY	command (2)	Note 1	t _{PLYB}	—		1	ms
Time from input of PLY co	mmand (2) to MON rise		t _{PLYM}	—		1	ms
Time from input of PLY co	mmand (2) to RPM rise		t _{PLYR}			3	ms
Time from input of STOP	During recording		t _{SPCB}	—	40	65	ms
command to BUSY fall	During Flash playback	Note 2	t _{SPCB}	—		500	μs
	During ROM playback	Note 2	t _{SPCB}	—		500	μs
Time from input STOP	During recording		t _{SPCM}	—	40	65	ms
command to MON fall	During Flash playback	Note 2	tspcm	—	_	500	μs
	During ROM playback	Note 2	t _{SPCM}	—	_	500	μs
Time from input STOP	During recording	Note 2	t _{SPCR}	—	—	1	ms
command to RPM bit fall	During Flash playback	Note 2	t _{SPCR}	—	—	500	μs
	During ROM playback	Note 2	t _{SPCR}	—		500	μs

Note 1: Proportional to the period of oscillation frequency f_{OSC} .

Note 2: Proportional to the period of sampling frequency f_{SAM}.

$\mathsf{DV}_{\mathsf{DD}}\text{=}\mathsf{AV}_{\mathsf{DD}}\text{=}2.7$ to 3.6 V, <code>DGND=AGND=0</code> V,

			Ta=-40	to +85°C, f _C	_{SC} =4.096	MHz, f _{SAN}	=8.0 kHz
Parameter				Min.	Тур.	Max.	Unit
Time from input of PAUSE	During recording	Note 2	t _{PSCB}		—	500	μs
command to BUSY fall	During Flash playback	Note 2	t _{PSCB}			500	μs
	During ROM playback	Note 2	t _{PSCB}			500	μs
Time from input of PAUSE	command to VPM bit rise	Note 2	t _{PSCP}	_	—	500	μs
Time from input of STOP c reset of VPM bit	ommand during pause to	Note 2	t _{PSCP}	—	_	500	μs
Time from input of STOP c reset of RPM bit	ommand during pause to	Note 2	tpscr			1	ms
Time from input of STOP c reset of VPM bit	ommand during pause to	Note 2	t _{PSCP}			1	ms
Time from input of STOP	During recording		t _{SPCB}		40	65	ms
command durig pause to	During Flash playback	Note 2	t _{SPCB}		_	500	μs
reset of BUSY	During ROM playback	Note 2	tspcb			500	μs
Time from input of STOP	During recording		t _{SPCM}		40	65	ms
command during pause to	During Flash playback	Note 2	t _{SPCM}	_		500	μs
reset of MON	During ROM playback	Note 2	t _{SPCM}	_		500	μs
BUSY time at input of INIT	command		t _{INIB}		40	100	ms
BUSY time at input of BLK	RD command (2)		t _{BRD}			500	μs
BUSY time at input of BLK	WR command (3)		t _{BWR}			500	μs
BUSY time at input of DTR	W command (2)		t _{DRW}			2	ms
BUSY time at input of BYT	EW command (3)		t _{WBW}			300	μs
BUSY time at input of BYT	ER command (2)		t _{WBR}	—		300	μs
BUSY time at input of WEN	ID command		t _{WWN}		10	21	ms
BUSY time at input of END	command		t _{WEN}			300	μs
	During recording		t _{PDM}		40	85	ms
Time from input of PDWN	During Flash playback	Note 2	t _{PDM}			1	ms
command to BUSY rise	During ROM playback	Note 2	t _{PDM}			1	ms
	During standby mode	Note 1	t _{PDM}			1	ms
Address control time durin	g ROM playback		t _{AD}			2	ms
Time for delection of phras	e by DEL command		t _{DEL}		40	50	ms
BUSY time after input of S	TATUS command		t _{STA}			10	μs
Time from BUSY being "L"	During Flash playback	Note 2	t _{PXT}	_	—	1	ms
to stop of external crystal	During Flash playback	Note 2	t _{PXT}	_	_	1	ms
clock after input of PDWN	During ROM playback	Note 2	t _{PXT}	_	_	1	ms
command	During standby mode	Note 1	t _{PXT}			100	μs

Ta=-40 to +85°C. fosc=4.096 MHz. fsam=8.0 kHz

Note 1: Proportional to the period of oscillation frequency f_{OSC}.

Note 2: Proportional to the period of sampling frequency f_{SAM} .

TIMING DIAGRAMS

Reset Function

<When the M9888L/M9889L and M989x share the same power supply source>
<u>After powering on the M9888L/M9889L</u>, input "L" level to the M9888L/M9889L's <u>RESET pin</u>.
Then, after M9888L/M9889L's V_{DD} level stabilizes at 2.7 V or higher, and after t_{RST} time has passed, input "H" level to the M9888L/M9889L's <u>RESET pin</u>.

<When the M9888L/M9889L and M989xL each use an independent power supply source> Bring the M9888L/M9889L's RESET pin up to "H" level after satisfying the above timing requirements and after stabilizing the power supply of M989xL at 2.7 V or higher.



Note: If the above timing requirements are not properly satisfied, M9888L/M9889L's operation may become unstable due to mal-functionality of internal reset function, which may cause incorrect data write to M989xL. This may also cause such symptoms as "unable to record/playback", "message data is missing", etc.

Power-down by the PDWN command (while in "Ready")



MSM9888L/9889L

MCU I/f Control Timings

<Timing for Data Write>



<Timing for Data Read>



<Timing for Data Write>



<Timing for Data Read>





Recording by the REC command

Playback by the PLY command



End Recording/Playback without the STOP command



Number of recording blocks

FEDL9888L-9889L-01

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End Recording/Playback by the STOP command



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Transfer data by the DTRW command



MSM9888L/9889L

End DTRW mode by the END command



End DTRW mode by the WEND command



Initialize Flash Memory by the INIT command



MSM9888L/9889L

Erase a Phrase by the DEL command



Output Status Data by the STATUS command



DI (I) BLKRW command (1) BLKRW command (2) SCK (I) CS (I) BUSY (0) Ready Ready Ready Ready Ready

Setup Recording Time by the BLKRW command

Output the Number of Recording Blocks by the BLKRW command



Timing for Continuous ROM Playback by PLY Command



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FUNCTIONAL DESCRIPTION

Serial Voice Flash Memory Configuration

The external serial voice Flash memory consists of the voice control area, voice data area, and user data area. The desired user data area can be secured by specifying the memory capacity before recording.

The user data area and recording time are specified for each block. Each block has a size that is 1/256 of the memory capacity of external serial voice Flash memory.

The serial voice Flash memory consists of pages each has 264 bytes.

Before transfering data that is in the user area specified with the INIT command, specify its page address with the DTRW command. Transfer data with the BYTEW and BYTER commands while specifying the byte address.

Serial voice Flash memory	y model	MSM9892L	MSM9893L	MSM9894AL
			MSM9893AL	
Serial voice Flash memory	y capacity	2M bits	4M bits	8M bits
Number of pages		1024 pages	2048 pages	4096 pages
[Page address]		[000h to 3FFh]	[000h to 7FFh]	[000h to FFFh]
Number of usable blocks		255 blocks	255 blocks	255 blocks
Memory capacity per bloc	k			
Voice data area	No. of bits	8192 bits	16384 bits	32768 bits
No. of bits		8448 bits	16896 bits	33792 bits
User data area No. of bytes		1056 bytes	2112 bytes	4224 bytes
	No. of pages	4 pages	8 pages	16 pages

Shown below is an example of space allocation when a single block of the 4-Mbit serial voice Flash memory is used for the user data area.



Recording/Playback Time

The recording/playback time is determined by the memory capacity, sampling frequency and coded bit length, and is calculated by the following equation.

Recording/playback time = <u>Memory capacity [bits]</u> [sec] sampling frequency [Hz] × bit length [bits]

For example, if recording is performed at 6.4 kHz sampling frequency after connecting the 4-Mbit serial voice Flash memory, the maximum recording time is calculated as shown below. In this case, the user data area is not specified and all the 255 blocks are used for the voice data area.

Recording/playback time = $\frac{255 \text{ blocks} \times 16384 \text{ bits}}{6.4 \text{ kHz} \times 4 \text{ bits}}$ = 163 seconds

1. Maximum time for recording variable message (recording/playback when serial voice Flash memory is used)

Serial voice Flash memory	model	MSM9892L	MSM9893L	MSM9894AL
			MSM9893AL	
Memory capacity		2M bits	4M bits	8M bits
Memory capacity per block	κ	8192 bits	16384 bits	32768 bits
Maximum recording time	f _{SAM} =4.0 kHz	130 seconds	261 seconds	522 seconds
(255 blocks)	f _{SAM} =5.3 kHz	97 seconds	195 seconds	391 seconds
	f _{SAM} =6.4 kHz	81 seconds	163 seconds	326 seconds
	f _{SAM} =8.0 kHz	65 seconds	130 seconds	261 seconds

Note) A sampling frequency can be specified for each phrase.

2. Maximum time for recording fixed message (ROM playback with internal ROM)

Model name		MSM	9888L	MSM9889L		
Internal ROM	memory capacity	512	(bits	1M bits		
Voice data area	memory capacity	496	K bits	1008	K bits	
Maximum play	Maximum playback time		8-bit PCM	4-bit ADPCM	8-bit PCM	
	f _{SAM} =4.0 kHz	31.7 seconds	15.8 seconds	65.5 seconds	32.2 seconds	
	f _{SAM} =5.3 kHz	23.8 seconds	11.9 seconds	43.8 seconds	24.1 seconds	
f _{SAM} =6.4 kHz		19.8 seconds	9.9 seconds	40.3 seconds	20.1 seconds	
	f _{SAM} =8.0 kHz	15.8 seconds	7.9 seconds	32.2 seconds	16.1 seconds	

Note 1) The sampling frequency and voice synthesis algorithm can be specified for each phrase. Note 2) 16 Kbits of the internal ROM is used for the voice control area.

The internal ROM capacity minus 16 Kbits is the voice data area.

Connection of an Oscillator

Connect a ceramic oscillator or a crystal oscillator to XT and $\overline{\text{XT}}$ pins as shown below. The optimal load capacities when connecting ceramic oscillators from MURATA MFG., KYOCERA CORPORATION, and TDK CORPORATION are shown below for reference.



Supplier	Туре	Freq. (MHz)	C1 (pF)	C2 (pF)	Applicable IC	
	CSTLS4M00G56-B0 (with capacitor) CSTCR4M00G55-R0 (with capacitor)	- 4.0			M9888L	
A MFG.	CSTLS4M00G53-B0 (with capacitor) CSTCR4M00G53-R0 (with capacitor)	4.0			M9889L	
MURATA MFG.	CSTLS6M00G56-B0 (with capacitor) CSTCR6M00G55-R0 (with capacitor)	- 6.0			M9888L	
	CSTLS6M00G53-B0 (with capacitor) CSTCR6M00G53-R0 (with capacitor)	0.0			M9889L	
ATION	KBR-4.0MSA/MSB PBRC4.00A	- 4.0	33	33		
KYOCERA CORPORATION	KBR-4.0MKC (with capacitor) PBRC4.00B (with capacitor)	- 4.0		_	M9888L	
KYOCEF	KBR-4.0MKD (with capacitor) KBR-4.0MKS (with capacitor))	6.0		_		
TDK CORPORATION	FCR4.0MC5 (with capacitor)	4.0			M9888L	
CORPC	FCR6.0MC5 (with capacitor)	6.0			M9889L	

Power Supply Wiring

As shown in the following diagram, supply the power from the same power source, but separate the power supply wiring to the analog portion from that to the logic portion.



The analog section and logic section must share the same power. Otherwise, a latch-up may occur.



SG Pin

Connect a 1µF electrolytic capacitor to the SG pin as shown below. After reset or after the PDWN mode is released, do playback after the voltage level on the SG pin is stabilized. The voltage level is stabilized at $1/2 V_{DD}$.



Analog Input Amplifier Circuit

The device has two built-in operational amplifiers for amplifying the microphone output. Each OP amplifier is provided with the inverting input pin and output pin. The analog circuit reference voltage SG (signal ground) is connected internally to the non-inverting input of each OP amplifier.

For amplification, form an inverting amplifier circuit and adjust the amplification ratio by using external resistors as shown below.



During recording, the output V_{LO} of OP amp is connected to the input FIN of the LPF. Adjust the amplification ratio by using the external resistors so that the V_{LO} amplitude is within the LOUT admissible input voltage (V_{FIN}) range.

If V_{LO} exceeds the V_{FIN} range, the LPF output waveform will be distorted.

The table below shows an example of the FIN admissible input voltage range for the MSM9888L and MSM9889L.

Parameter	Power Supply	FIN admissible inpu	FIN admissible	
	Voltage V _{DD}	min.	max.	input Voltage
MSM9888L	3V	0.75V	2.25V	1.5V _{P-P}
MSM9889L	3V	0.75V	2.25V	1.5V _{P-P}

The value of the OP amp load resistance R_{OUTA} is 100 k Ω minimum. Therefore the values of the inverting amplifier circuit feedback resistors R2 should be 100 k Ω or more.

Connection of LPF Circuit Peripherals

The AMON pin is connected internally to the output of the amplifier circuit (LOUT pin) in the recording mode and to the output of the built-in DA converter in the playback mode. Therefore, connect the AMON pin directly to the input (FIN pin) of the built-in LPF.

Both the FOUT and AOUT pins are the output pins of the built-in LPF. Connect the FOUT pin to the input (ADIN pin) of the built-in AD converter and connect the AOUT pin to an external speaker through an external speaker drive amplifier.

In the MSM9888L/9889L, the connection of each of the FOUT and AOUT pins is changed to one of the output of the LPF, GND(ground) level, and SG (signal ground) level, depending on the operation status as shown below.

Analog pin	Power down and RESET	During operation (RESET pin = "H")				
		Recording mode/Standby	Playback mode			
FOUT pin	GND level	LPF Output (recording waveform)	LPF Output			
AOUT pin	GND level	SG level	LPF Output (playback waveform)			



Note: This diagram shows the state of each switch during the recording operation.

MSM9888L/9889L

LPF Characteristics

This MSM9888L/9889L contains a fourthorder switched-capacitor LPF.

The attenuation characteristic of this LPF is -40 dB/oct. The cut-off frequency and frequency characteristics of this LPF vary in proportion to the sampling frequency (fsamp). The cut-off frequency is preset to 0.4 times the sampling frequency. The following graph depicts the frequency characteristics of the LPF at fsamp = 8 kHz.



LPF Frequency Characteristics (f_{SAM}=8.0kHz)

Full Scale of A/D and D/A Converters

Parameter	Full	Full scale of A/D and D/A converters										
	min (V)	max (V)	Amplitude (Vp-p)									
MSM9888L	$\frac{1}{4} \times V_{DD}$	$\frac{3}{4} \times V_{DD}$	$\frac{1}{2} \times V_{DD}$									
MSM9889L	$\frac{1}{4} \times V_{DD}$	$\frac{3}{4} \times V_{DD}$	$\frac{1}{2} \times V_{DD}$									



Command Description

This IC is controlled with the following commands via control pins such as \overline{CS} , SCK, DI. DO and BUST (if necessary).

1. Command List

Command	D7	D6	D5	D4	D3	D2	D1	D0	Function
NOP	0	0	0	0	0	0	0	0	No function
REC	0	0	0	1	0	S2	S1	S0	Starts recording
RE6	0	0	C5	C4	C3	C2	C1	CO	
PLY	0	0	1	0	0	0	0	M0	Starts playback
PLI	C7	C6	C5	C4	C3	C2	C1	CO	
STOP	0	0	1	1	0	0	0	0	Terminates recording/playback.
PAUSE	0	1	0	0	0	0	0	0	Pauses or resets pause.
BLKRW	0	1	0	1	0	0	0	M1	Sets and reads the recording time.
DLKNVV	D7	D6	D5	D4	D3	D2	D1	D0	
DTRW	0	1	1	0	Pb	Ра	P9	P8	Reads data from or writes data to the flash memory
DIRV	P7	P6	P5	P4	P3	P2	P1	P0	
DEL	0	1	1	1	0	0	0	0	Erases phrases.
DEL	0	0	C5	C4	C3	C2	C1	CO	
PDWN	1	0	0	0	0	0	0	0	Stops the clock to select the power-down mode.
	1	0	0	1	0	0	0	B8	Writes the data written with W7 to 0 to the address
BYTEW	B7	B6	B5	B4	B3	B2	B1	B0	indicated by B8 to 0 to the flash memory buffer.
	W7	W6	W5	W4	W3	W2	W1	W0	
BYTER	1	0	1	0	0	0	0	B8	Reads data inside the buffer at the address
BYIER	B7	B6	B5	B4	B3	B2	B1	B0	indicated by B8 to 0.
WEND	1	0	1	1	0	0	0	0	Writes buffer data to the flash memory then quits.
END	1	1	0	0	0	0	0	0	Quits without writing buffer data to hte flash memory.
	1	1	1	0	1	0	1	0	Initializes the voice area part of the flash memory.
INIT	0	0	0	0	0	0	F1	F0	
	U7	U6	U5	U4	U3	U2	U1	U0	
STATUS	1	1	1	1	1	1	1	1	Outputs the status.

C7 to C0 : Phrase No.

S2 to S0 : Sampling frequency

Pb to P0 : Page address on the flash memory

B8 to B0 : Block address on the flash memory

F1 to F0 : Type of flash memory connected

U7 to U0 : Number of user data blocks

			Sampling frequency	Dividing
S2	S1	S 0	(Note 1)	ratio
0	0	0	2.0kHz	f _{0SC} /2048
0	0	1	2.7kHz	f _{OSC} /1536
0	1	0	3.2kHz	f _{0SC} /1280
0	1	1	4.0kHz	f _{0SC} /1024
1	0	1	5.3kHz	f _{0SC} /768
1	1	0	6.4kHz	f _{0SC} /640
1	1	1	8.0kHz	f _{0SC} /512

Sampling frequency

(Note 1) f_{OSC}=4.096MHz

Phrase designation

MODE0 Setting

MO	Function
0	Flash playback
1	ROM playback

MODE1 Setting

M1	Function
0	Sets the number of blocks to be recorded
	or played back with D7 to D0.
1	Sets the channel recorded with D7 to D0
	and outputs the recording time.

								Phrase No.	Flash memory	Flash memory	ROM
C7	C6	C5	C4	C3	C2	C1	C0	(HEX)	recording	playback	playback
0	0	0	0	0	0	0	0	Phrase 0 (00h)	Unavailable	Unavailable	Unavailable
0	0	0	0	0	0	0	1	Phrase 1 (01h)			
0	0	0	0	0	0	1	0	Phrase 2 (02h)			
•	•	•	•	•	•	•••	•	•	Available (63 phrases)	Available (63 phrases)	
0	0	1	1	1	1	1	0	Phrase 62 (3Eh)			
0	0	1	1	1	1	1	1	Phrase 63 (3Fh)			Available
0	1	0	0	0	0	0	0	Phrase 64 (40h)			(255 phrases)
0	1	0	0	0	0	0	1	Phrase 65 (41h)			
• • •	•	• •	•	• •	•	• •	•	•	Unavailable	Unavailable	
1	1	1	1	1	1	1	0	Phrase 254 (FEh)]		
1	1	1	1	1	1	1	1	Phrase 255 (FFh)			

Page address designation

Pb	Ра	P 9	P 8	P7	P6	P5	P4	P3	P2	P1	P0	Page address in Flash memory
0	0	0	0	0	0	0	0	0	0	0	0	Page 000h
0	0	0	0	0	0	0	0	0	0	0	1	Page 001h
0	0	0	0	0	0	0	0	0	0	1	0	Page 002h
0	0	0	0	0	0	0	0	0	0	1	1	Page 003h
									•			
			•			•			•			•
		•	•		•	•			•			•
1	1	1	1	1	1	1	1	1	1	0	1	Page FFDh
1	1	1	1	1	1	1	1	1	1	1	0	Page FFEh
1	1	1	1	1	1	1	1	1	1	1	1	Page FFFh

OKI Semiconductor

	Flash memory recording/playback	ROM playback	Flash memory data transfer
NOP	—	—	—
REC	0	—	—
PLY	0	0	
STOP	0	0	_
PAUSE	0	0	_
BLKRW	0	—	—
DTRW	—	_	0
DEL	0	_	_
PDWN	0	0	
BYTEW	—	—	0
BYTER	—	—	0
WEND	—	—	0
END	—	—	0
INIT	0	_	0
STATUS	0	0	

2. Relationship between Recording/Playbakc, data transfer, and commands

◎ : Necessary

 \bigcirc : Effective

— : Unnecessary

3. Command Descriptions

1.NOP

• Command	0	0	0	0	0	0	0	0
-----------	---	---	---	---	---	---	---	---

• Description: Non-operation No function available.

2.REC

• Command

d	0	0	0	1	0	S2	S1	S0
	0	0	C5	C4	C3	C2	C1	C0

- Description: Records the phrases designated by C7 to C0 with the sampling frequency designated by S2 to S0.
- Others

Sampling frequency

S2	S1 S0		Sampling frequency	Dividing
32	31	30	(Note 1)	ratio
0	0	0	2.0kHz	f _{0SC} /2048
0	0	1	2.7kHz	f _{OSC} /1536
0	1	0	3.2kHz	f _{0SC} /1280
0	1	1	4.0kHz	f _{0SC} /1024
1	0	1	5.3kHz	f _{0SC} /768
1	1	0	6.4kHz	f _{0SC} /640
1	1	1	8.0kHz	f _{0SC} /512

Note 1: Source frequency f_{OSC}=4.096 Hz

Phrase designation (phrases 1 to 63)

C5	C4	C3	C2	C1	C0	Phrase No. (HEX)
0	0	0	0	0	1	Phrase 1 (01h)
0	0	0	0	1	0	Phrase 2 (02h)
0	0	0	0	1	1	Phrase 3 (03h)
		•	• •			
1	1	1	1	1	0	Phrase 62 (3Eh)
1	1	1	1	1	1	Phrase 63 (3Fh)

3.PLY

• Cor

mmand	0	0	1	0	0	0	0	M0
	C7	C6	C5	C4	C3	C2	C1	CO

• Description:	M0	Description
	0	Plays phrases recorded in Flash memory. Designate the phrases
		to be played with C5 to C0 (phrases 1 to 63). Set C7 and C6 to "0".
	1	Plays a fixed message that is in internal ROM. Designate the
		phrase to be played with C7 to C0 (phrases 1 to 255).

4.STOP

• Command	0	0	1	1	0	0	0	0	
-----------	---	---	---	---	---	---	---	---	--

• Description: Quits recording or playback.

5. PAUSE

• Command

0	1	0	0	0	0	0	0

• Description: Pauses recording or plyaback. Restarts recording or playback if the PAUSE command is input again.

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6. BLKRW

• Com

ommand	0	1	0	1	0	0	0	M1
	D7	D6	D5	D4	D3	D2	D1	D0
Output	07	06	05	04	03	02	01	00

• Note: Outputs O7-O0 only when M1 is "1".

• Description: 1. BLKWR command When M1 is "0" Designates the number of blocks in which phrases are to be recorded.

D7	D6	D5	D4	D3	D2	D1	D0	Number of blocks (HEX)
0	0	0	0	0	0	0	0	Records phrases until memory is full (Remaining block is zero)
0	0	0	0	0	0	0	1	Records 1 (01h) block.
0	0	0	0	0	0	1	0	Records 2 (02h) blocks.
•	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	0	Records 254 (FEh) blocks.
1	1	1	1	1	1	1	1	Records 255 (FFh) blocks.

2. BLKRD command When M1 is "1" Outputs the number of blocks in which the phrase (phrases 1 to 63) designated by D7 to D0 was recorded.

If the number of designated phrases is zero, output the number of the remaining recordable blank blocks with O7 to O0.

D7	D6	D5	D4	D3	D2	D1	D0	Data output with O7 to O0
0	0	0	0	0	0	0	0	Outputs the number of the remaining recordable blank blocks.
0	0	0	0	0	0	0	1	Outputs the number of blocks of phrase 1 (01h).
0	0	0	0	0	0	1	0	Outputs the number of blocks of phrase 2 (02h).
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
0	0	1	1	1	1	1	0	Outputs the number of blocks of phrase 62 (3Eh).
0	0	1	1	1	1	1	1	Outputs the number of blocks of phrase 63 (3Fh).

Flash Memory Devices and Memory Capacity per Block

Shown below is the relationship between Flash memory devices and memory capacity per block. The memory capacity per block is 1/256 of memory capacity irrespective of the model of memory.

Medel nome	Memory	No. of blocks available	Memory capacity	Memory capacity per block used
Model name	capacity	for recording/playback	per block (bits)	for recording/playback (bits)
MSM9892L	2Mbit	255	8448	8192
MSM9893L	4Mbit	255	16896	16384
MSM9894L	8Mbit	255	33792	32768

Relationship between Blocks and Recording Time

The recording time is determined by the memory capacity per block used for recording/ playback, number of blocks used for recording, and sampling frequency. The recording time can be calculated by the following equation.

 $\frac{\text{Memory capacity per block used for recording/playback} \times \text{Number of blocks used}}{\text{Sampling frequency (kHz)} \times 4\text{-bit ADPCM}}$

For example, when 4-Mbit serial voice Flash memory is used, the recording time if voice data is recorded in 10 blocks at a 6.4 kHz sampling frequency is calculated as shown below.

Where the memory capacity per block used for recording/playback is 16384 bits,

Recording time (seconds) = $\frac{16384 \text{ bits} \times 10 \text{ blocks}}{6.4 \text{kHz} \times 4 \text{-bit ADPCM}}$

= 6.4 seconds
MSM9888L/9889L

7. DTRW

• Command

0	1	1	0	Pb	Ра	P9	P8
P7	P6	P5	P4	P3	P2	P1	P0

• Description: Selects the DTRW mode. Inputs data to or outputs data from the flash memory page designated with Pb to P0. To release the DTRW mode, input the WEND command or END command. The flash memory consists of 264 bytes per page.

MSM9892L MSM9893L MSM9894L 2M 4M 8M Memory size bits bits bits 32768 8192 16384 One-block size bits bits bits 1024 2048 4096 Number of pages Pages Pages Pages

0

C0

The number of pages on each flash memory is as follows:

8.DEL

- Command 0 1 1 1 0 0 0 0 0 C5 C4 C3 C2 C1
- Description: Erases the phrases designated with C5 to C0. Applied to recording playback using the flash memory and not applied to ROM playback.

9.PDWN

Command

1 0	0 0	0 0	0	0
-----	-----	-----	---	---

• Description: Stops the clock and sets the power-down mode after teh command is input. To release the power-down mode, input RESET.

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10. BYTEW

• Command

1	0	0	1	0	0	0	B8
B7	B6	B5	B4	B3	B2	B1	B0
W7	W6	W5	W4	W3	W2	W1	W0

- Note: This command is valid only in DTRW mode.
- Description: Rewrites the content of the page designated with the DTRW command in units of bytes. Designate the address in the page with B8 to B0 and input data with W7-W0.

11. BYTER

• Comma

ommand	1	0	1	0	0	0	0	B8
	B7	B6	B5	B4	B3	B2	B1	B0
Output	07	06	05	04	03	02	01	00

- Note: This command is valid only in DTRW mode.
- Reads the contents of the page designated with the DTRW command in units • Description: of byte. When the address in the page is designated with B8-B0, data is output after the command input.

12. WEND

- Command 1 0 1 1 0 0 0 0
- Note: This command is valid only in DTRW mode.
- Description: Writes the content of the page designated with the DTRW command to the flash memory then exits the DTRW mode.

13. END

- Command 1 1 0 0 0 0 0 0
- Note: This command is valid only in DTRW mode.
- Exits the DTRW mode without writing the content of the page designated • Description: with the DTRW command to the flash memory.

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14. INIT

• Command

1	1	1	0	1	0	1	0
0	0	0	0	0	0	F1	F0
U7	U6	U5	U4	U3	U2	U1	U0

• Description: Initializes the area that excludes the number of blocks designated with U7 to U0 from the end of the flash memory blocks as the recording/playback area. Also, selects the model of the flash memory with F1 and F0.

All voice data recorded in Flash memory can be erased by entering the INIT command.

Also use the INIT command to erase all phrases.

F1	F0	Flash memory size	Model name			
0	1	2M bits MSM9892L				
1	0	4M bits	MSM9893L			
1	1	8M bits	MSM9894L			

U7	U6	U5	U4	U3	U2	U1	U0	Setting of number of user blocks
0	0	0	0	0	0	0	0	The number of blocks designated as a user block is zero.
•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	0	254 blocks are designated as user blocks.
1	1	1	1	1	1	1	1	255 blocks are designated as user blocks.

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Flash memory allocation after input of INIT command

Example: The user data area is divided into two blocks.



15. STATUS

• Command

ommand	1	1	1	1	1	1	1	1
Output	07	06	05	04	03	02	01	00

• Description: Outputs the M9888 status.

07	MON	Outputs "1" during execution of the REC or PLY command.
		It includes the memory management time in addition to the
		recording/playback time. Also, outputs the same value as
		that of the MON pin.
06	VPM	Outputs "1" during pause.
05	RPM	Outputs "1" during acrual recording by the REC command
		or during voice output by the PLT command.
		Otherwise, "O" is output.
04	_	No function
03	MEMFUL	Outputs "1" when there is no space in the voice area on the
		flash memory.
02	NAR	Outputs "1" when the next phrase can be input during
		continuous voice playback of the fixed message in the
		internal ROM.
01	_	No function
00	_	No function

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Flowcharts

1. Flowchart of recording



2. Flowchart of playback



3. Flowchart of continuous ROM playback



This flowchart cannot be used for Flash memory playback.

4. Flowchart of Data Transfer



Writing to or Reading from Flash Memory

Data can be written or read in byte units by using both the MSM9888L and MSM989x series (serial voice Flash memory).

1. DTRW command

This command is used to transfer a page of data from the Flash memory to the 2112-bit buffer. When using this command, it is required to specify the address of a page to be transfered to the buffer.



2. BYTEW command and BYTER command

The BYTEW command is used to write in byte units the contents of a 2112-bit buffer transfered with the DTRW command. The BYTER command is used to read them.



3. WEND command

This command is used to write the contents of a 2112-bit buffer to the Flash memory. It takes about 21 msec for writing.



Flash Memory Devices and Memory Capacity per Block

Shown below is the relationship between Flash memory devices and memory capacity per block. The memory capacity per block is 1/256 of memory capacity irrespective of the model of memory.

Product name	-			Memory capacity per block used for recording/playback (bits)
MSM9892L	2Mbit	255	8448	8192
MSM9893L	4Mbit	255	16896	16384
MSM9894AL	8Mbit	255	33792	32768

Information on Voice Control of M9888L/M9889L

User-unavailable area of internal ROM of M9888L/M9889L

 $Voice \, control \, area \, and \, user-unavailable \, area \, of \, M989xL$





MSM9888L/9889L

NOTE ON USE

When you design a power supply circuit

The instantaneous current, though it is within the rated value, flows to the MSM989xL series product (serial voice Flash memory) when data is written in the product. See the following figure. When voice data is written to the MSM989xL series product during recording operation, the power supply voltage fluctuated by the instantaneous current may cause noises to be recorded. You should design a power supply circuit considering the above instantaneous current. It is recommended to use a regulator that can regulate the fluctuated voltage due to the instantaneous current.

The instantaneous current flows every $512/f_{SAM}$ [sec].

For example, if the sampling frequency $\rm f_{SAM}$ is 8 kHz, the instantaneous current flows every 64 ms.





APPLICATION CIRCUIT



MSM9888L/9889L

PACKAGE DIMENSIONS



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.

Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

MSM9888L/9889L

(Unit : mm)



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REVISION HISTORY

Descurrent		Pa	ge	
Document No.	Date	Previous Edition	Current Edition	Description
E2D0083-29-94	Sep. 1999	—	_	Preliminary edition
FEDL9888L-9889L-01	Feb. 27, 2002	25	25	Changed contents of the table for ceramic oscillators
		—	53	Addition of Revision History

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