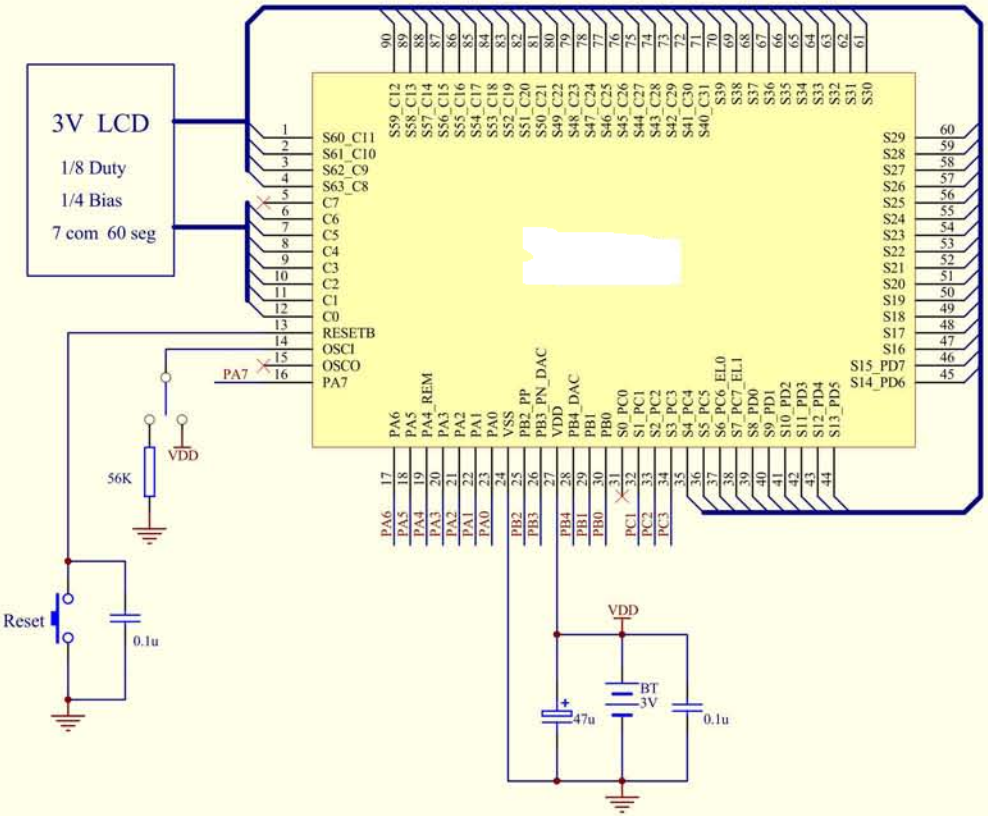


	PA0	PA1	PA2	PA3	PA4	PA5	PA6	PA7	
	MC AC								
	ALPHA	Shift	Left	Right	Mode	Off			PB2
	sqrtX G Xy	sqrt3 H sqrt	NORM g FIX	ENG Na SCI	DRG-K DRG	BLOCK Vm DHBO			PB3
	hpy	d/c h ab/c	G FMLA	IN e CALC	RANDOM 8 (-)	INSERT u BS			PB4
	Sin-1 A sin	Cos-1 B Cos	Tan-1 C Tan	DEG D D'M'S	10x E log	Ex F ln	r8 , 0		PB1
	X-1 X2	NEG O (	NOP P)	RCL J STO	CD K DATA	M- MR M+	xy : •		PB0
	n! L 7	n M 8	x N 9	C			Pai C EXP		PC1
	nPr Q 4	Σx R 5	Σx2 S 6	AND T *	XOR U /		PDEL me DEL		PC2
	nCr V 1	n W 2	n-1 X 3	OR Y +	XNOR Z -	% =			PC3

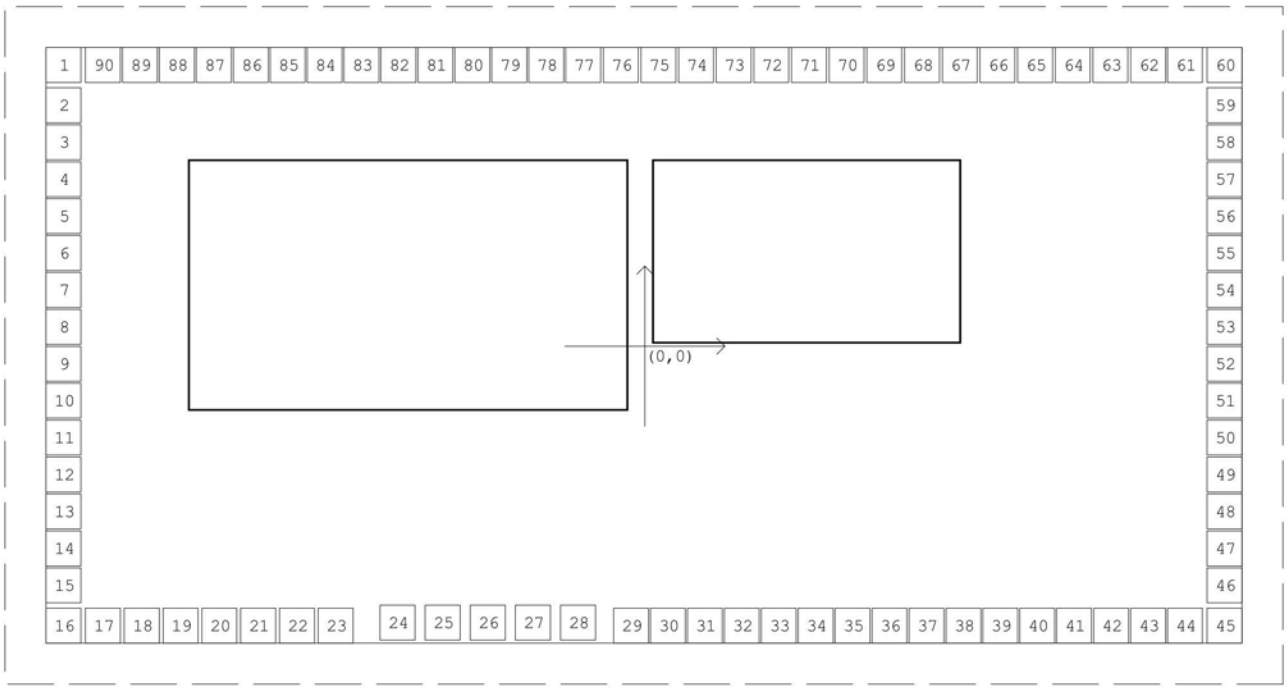
Title	application circuit	
Size: B	Number:	Revision: V1.2
Date: 20-Jan-2011	Sheet of 1/1	
File: X:\EL0280A\SCH\EL0280A.SCH	Drawn By: Dick	

PAD

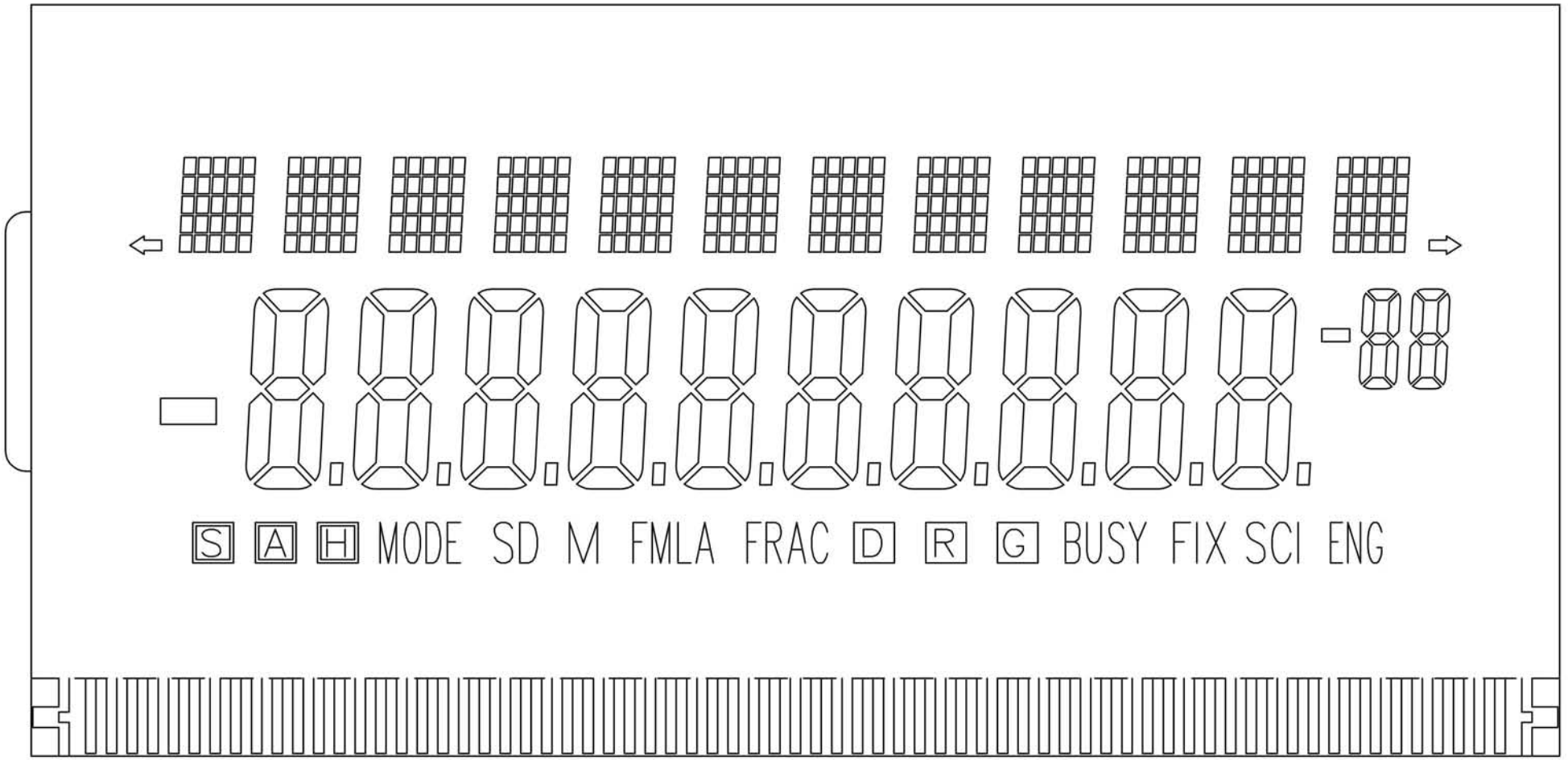
Pad Assignment:

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1	S60_C11	-1414.8	683.1	26	PB3	-380.9	-675.65	51	S20	1414.8	-135	76	S45_C26	-56.7	683.1
2	S61_C10	-1414.8	585	27	VDD	-270.9	-675.65	52	S21	1414.8	-45	77	S46_C25	-148.5	683.1
3	S62_C9	-1414.8	495	28	PB4	-160.9	-675.65	53	S22	1414.8	45	78	S47_C24	-238.5	683.1
4	S63_C8	-1414.8	405	29	PB1	-31.5	-683.1	54	S23	1414.8	135	79	S48_C23	-328.5	683.1
5	C7	-1414.8	315	30	PB0	58.5	-683.1	55	S24	1414.8	225	80	S49_C22	-418.5	683.1
6	C6	-1414.8	225	31	S0	148.5	-683.1	56	S25	1414.8	315	81	S50_C21	-508.5	683.1
7	C5	-1414.8	135	32	S1	238.5	-683.1	57	S26	1414.8	405	82	S51_C20	-598.5	683.1
8	C4	-1414.8	45	33	S2	328.5	-683.1	58	S27	1414.8	495	83	S52_C19	-688.5	683.1
9	C3	-1414.8	-45	34	S3	418.5	-683.1	59	S28	1414.8	585	84	S53_C18	-778.5	683.1
10	C2	-1414.8	-135	35	S4	508.5	-683.1	60	S29	1414.8	683.1	85	S54_C17	-868.5	683.1
11	C1	-1414.8	-225	36	S5	598.5	-683.1	61	S30	1318.5	683.1	86	S55_C16	-958.5	683.1
12	C0	-1414.8	-315	37	S6	688.5	-683.1	62	S31	1228.5	683.1	87	S56_C15	-1048.5	683.1
13	RESETB	-1414.8	-405	38	S7	778.5	-683.1	63	S32	1136.7	683.1	88	S57_C14	-1138.5	683.1
14	OSCI	-1414.8	-495	39	S8	868.5	-683.1	64	S33	1044.9	683.1	89	S58_C13	-1228.5	683.1
15	OSCO	-1414.8	-585	40	S9	958.5	-683.1	65	S34	953.1	683.1	90	S59_C12	-1318.5	683.1
16	PA7	-1414.8	-683.1	41	S10	1048.5	-683.1	66	S35	861.3	683.1				
17	PA6	-1318.5	-683.1	42	S11	1138.5	-683.1	67	S36	769.5	683.1				
18	PA5	-1224	-683.1	43	S12	1228.5	-683.1	68	S37	677.7	683.1				
19	PA4	-1129.5	-683.1	44	S13	1318.5	-683.1	69	S38	585.9	683.1				
20	PA3	-1035	-683.1	45	S14	1414.8	-683.1	70	S39	494.1	683.1				
21	PA2	-940.5	-683.1	46	S15	1414.8	-585	71	S40_C31	402.3	683.1				
22	PA1	-846	-683.1	47	S16	1414.8	-495	72	S41_C30	310.5	683.1				
23	PA0	-751.5	-683.1	48	S17	1414.8	-405	73	S42_C29	218.7	683.1				
24	VSS	-600.9	-675.65	49	S18	1414.8	-315	74	S43_C28	126.9	683.1				
25	PB2	-490.9	-675.65	50	S19	1414.8	-225	75	S44_C27	35.1	683.1				

*The IC substrate should be connected to Vss in the PCB layout artwork.

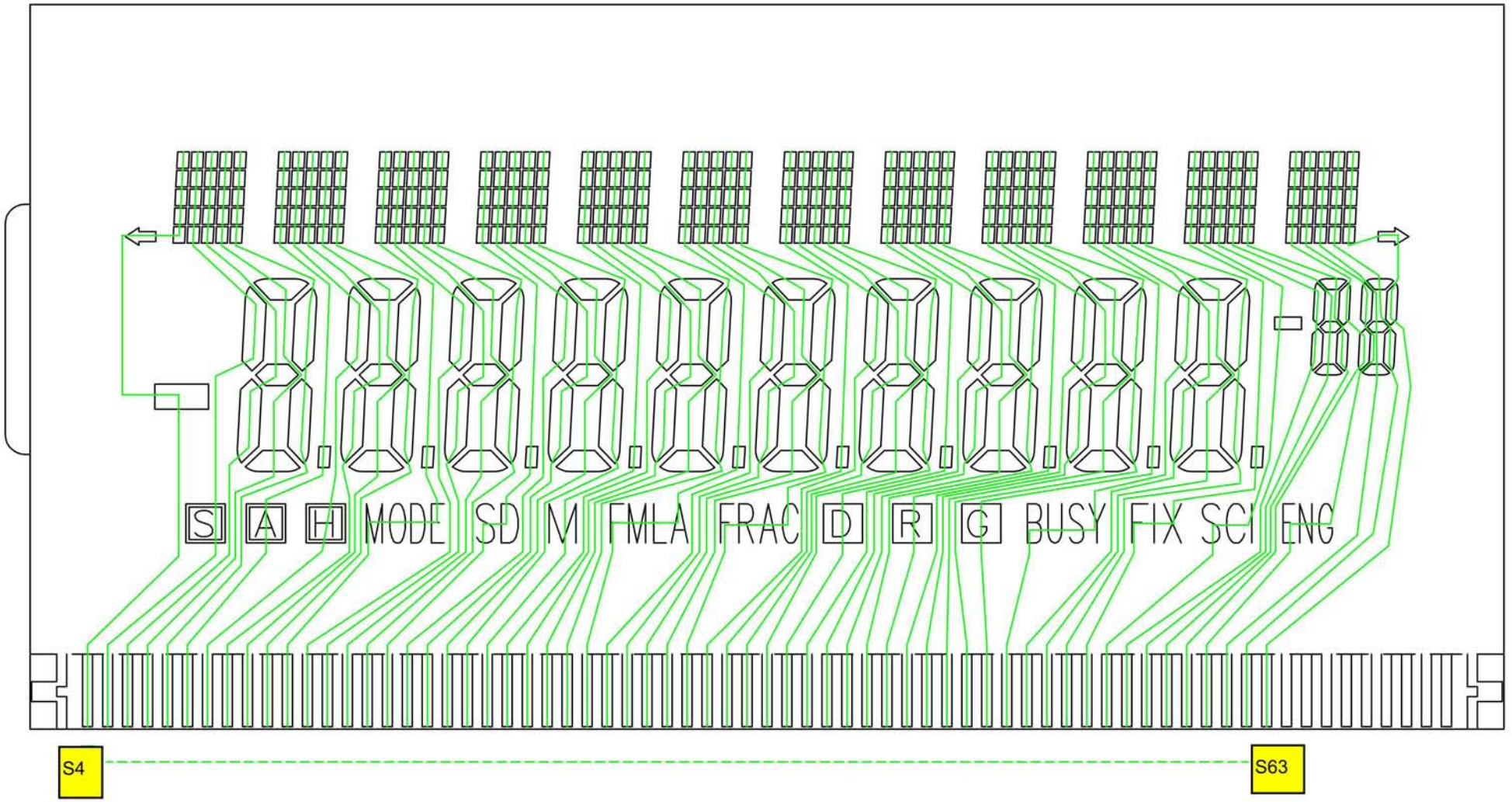


Customer's Approval	
Customer	
Date	



REVISED RECORD		SCALE	4:1	TOLERANCE	±0.2				
1	變更DOTS爲 5X7.	UNIT	mm	ORG DATE	99.02.12				
2	變更工作電壓 & Change Layout.	MATERIAL		DRAWN BY					
3				CHECKED BY					
4		FINISH		CONCURRED BY		DWG NO		DCN	A14	VERSION
5				APPROVED BY		P/N		P OF 3		C

Customer's Approval	
Customer	
Date	



SEGMENT

	REVISED RECORD	SCALE	4:1	TOLERANCE	±0.2			
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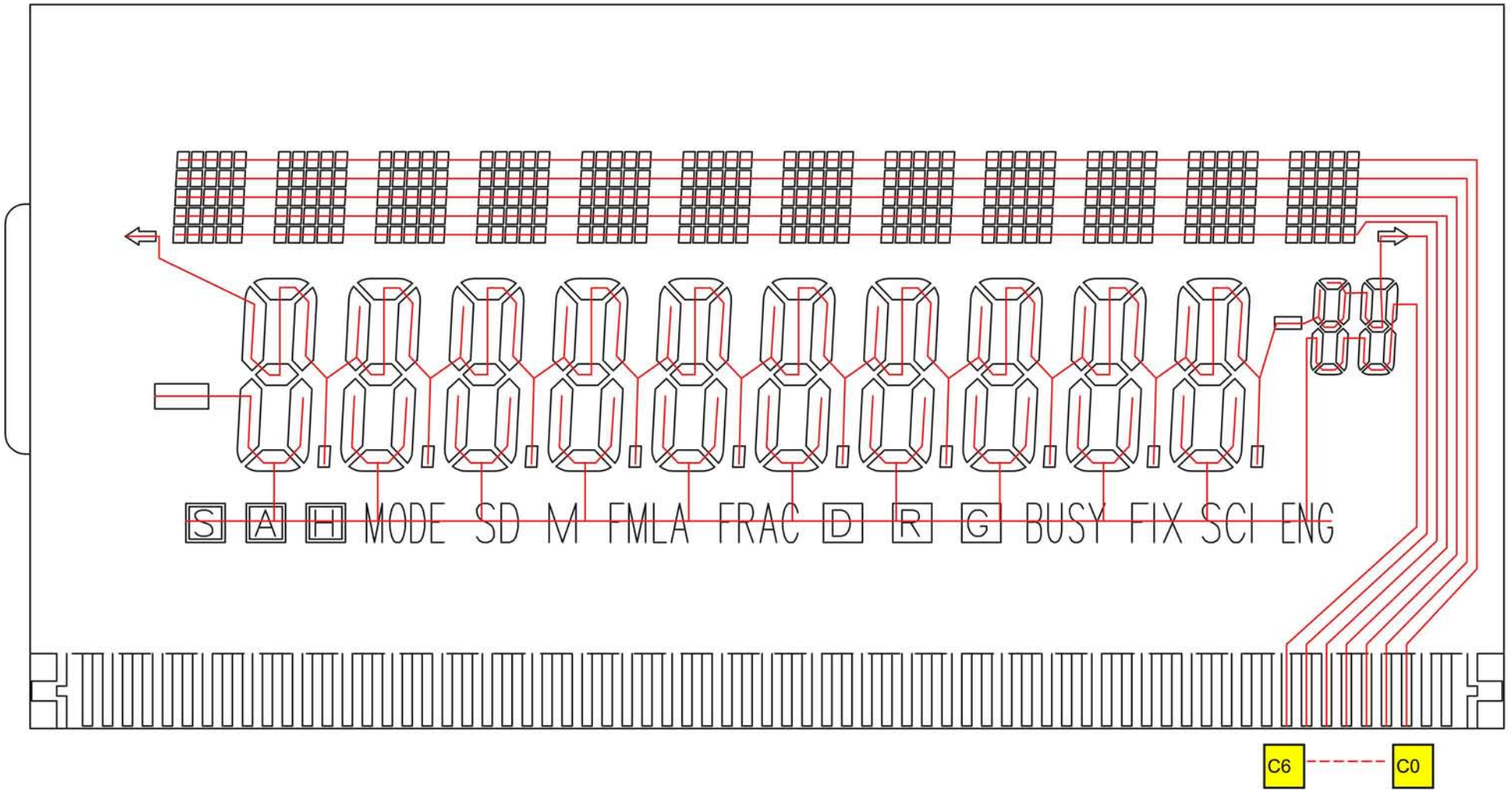
2	變更工作電壓 & Change Layout.	MATERIAL		DRAWN BY	MARRY			
3				CHECKED BY				
4		FINISH		CONCURRED BY		DWG NO	DCN A14	VERSION
5				APPROVED BY		P/N	P 2 OF 3	C

Customer's Approval	
Customer	
Date	



COMMON

	REVISED RECORD	SCALE	4:1	TOLERANCE	±0.2				
1	變更DOTS爲 5X7.	UNIT	mm	ORG DATE	99.02.12				
2	變更工作電壓 & Change Layout.	MATERIAL		DRAWN BY	MARRY				
3				CHECKED BY					
4		FINISH		CONCURRED BY		DWG NO		DCN	A14	VERSION
5				APPROVED BY		P/N		P 3 OF 3		C