Series

Single-Message

Single-Chip

6.6- to 40-Second

Voice Record & Playback Devices

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1. GENERAL DESCRIPTION

The Nuvoton® DL7801 ChipCorder® Series is a high quality, fully integrated, single-chip single-message voice record and playback device ideally suited to a variety of electronic systems. The message duration is user selectable in ranges from 6.6 seconds to 40 seconds, depending on the specific device. The sampling frequency of each device can also be adjusted from 4 kHz to 12 kHz with an external resistor, giving the user greater flexibility in duration versus recording quality for each application. Operating voltage spans a range from 2.4 V to 5.5 V to ensure that the DL7801 devices are optimized for a wide range of battery or line-powered applications.

The devices include an on-chip oscillator (with external resistor control), microphone preamplifier with Automatic Gain Control (AGC), anti-aliasing filter, Multi-Level Storage (MLS) array, smoothing filter, Pulse Width Modulation (PWM) Class D speaker driver, and current output. Voice signals can be fed into the chip through a differential microphone input for recording. The PWM output can directly drive a standard 8 Ω speaker or a typical buzzer, while the separate single-ended current output can drive an external amplifier.

Recordings are stored into the on-chip Flash memory cells, providing zero-power message storage. This unique single-chip solution is made possible through Nuvoton's patented Multi-Level Storage (MLS) technology. Audio data are stored directly in solid-state memory without digital compression, providing superior quality voice and music reproduction.

2. FEATURES

- User-friendly single-chip, single-message voice record & playback devices
- Wide operating voltage: 2.4V to 5.5V
- Push-button interface
  - Record is level-triggered
  - Playback is either edge- or level-triggered
- Selectable sampling frequency controlled by an external oscillator resistor

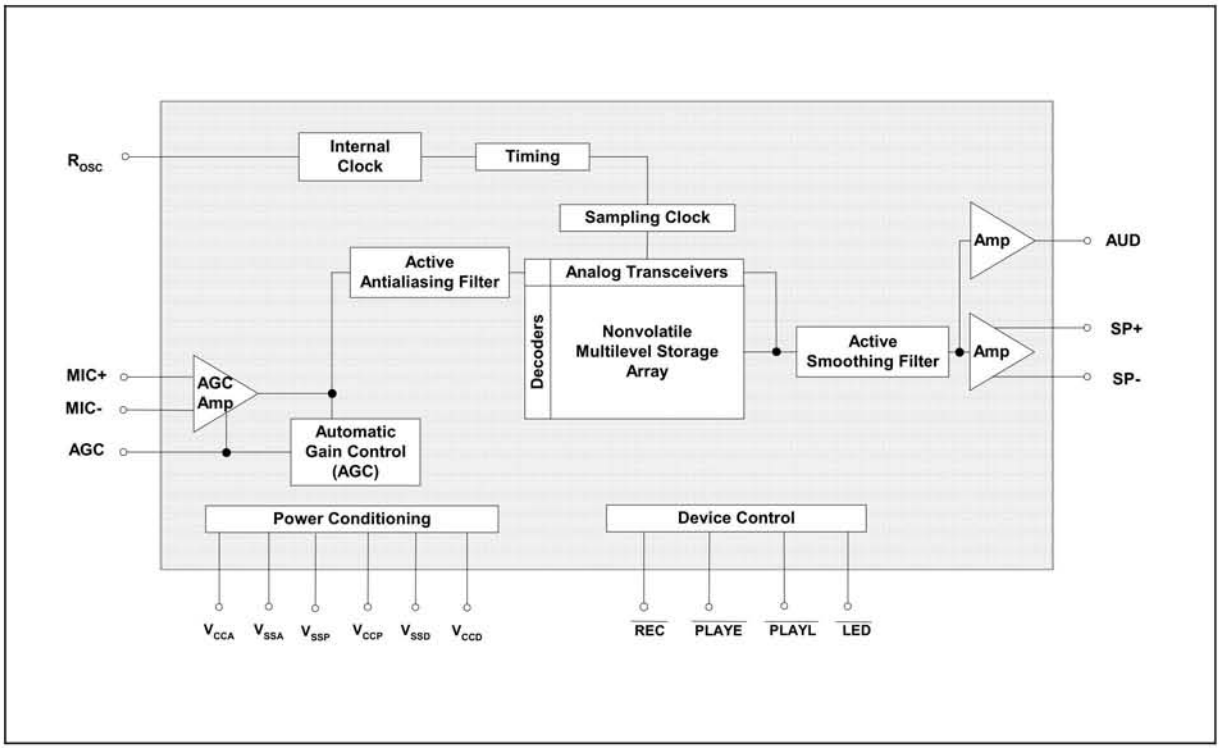
Sampling Frequency	12 kHz	8 kHz	6.4 kHz	5.3 kHz	4 kHz
Rosc	53 kΩ	80 kΩ	100 kΩ	120 kΩ	160 kΩ

- Variable duration selected by external oscillator resistor

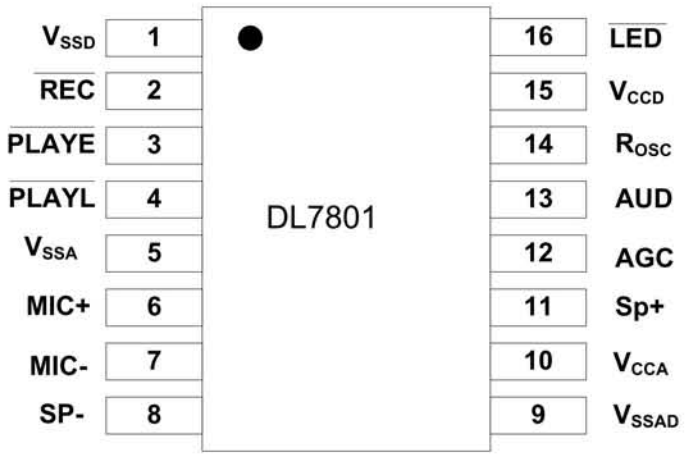
Sample Frequency	12 KHz	8 KHz	6.4 KHz	5.3 KHz	4 HKz
DL7801	6.6 secs	10 secs	12.5 secs	15 secs	20 secs
DL7802	8 secs	12 secs	15 secs	18 secs	24 secs
DL7803	10.6 secs	16 secs	20 secs	24 secs	32 secs
DL7804	13.3 secs	20 secs	25 secs	30 secs	40 secs

- Message and operation indicators
  - LED: stay on during recording, blink during playback operation
- Automatic power-down mode
  - Enters standby mode immediately after a record or playback cycle
  - Standby current: 1μA typical and 10μA maximum
- Dual output channels
  - PWM Class D speaker amplifier to directly drive an 8 Ω speaker or a typical buzzer
  - AUD single-ended current output to drive external power amplifier
- ChipCorder standard features
  - High-quality, natural voice and audio reproduction
  - Zero-power message storage: Eliminates battery backup circuits
  - 100-year message retention (typical)
  - 100,000 record cycles (typical)
- Package options: Leaded and Lead-free packaged units
- Available in die and 16L 150mil SOIC
- Temperature options:
  - Commercial: 0°C to +50°C (Die); 0°C to +70°C (Packaged)
  - Industrial: -40°C to +85°C (Packaged)

3. BLOCK DIAGRAM



4. PIN CONFIGURATION



SOIC

5. PIN DESCRIPTION

PIN NAME	SOIC / PDIP PIN NO.	FUNCTIONS
V_{SSD}	1	**Digital Ground**: V_{SSD} is the ground for digital circuits. It is important to have a separate path for each ground back to the system ground terminal to minimize noise.
$\overline{REC}$	2	**Record**: The device starts recording whenever $\overline{REC}$ transits from High to Low and stays at Low. Recording stops when the signal returns to High. This pin has an internal pull-up resistor [1] and an internal debounce on falling edge.
$\overline{PLAYE}$	3	**Edge-trigger Playback**: A playback operation starts when this input detects a low going signal exceeding the specified debounced time. This pin has an internal pull-up resistor [1] and an internal debounce on both falling & rising edge.
$\overline{PLAYL}$	4	**Level-trigger Playback**: A playback operation begins when this input detects a low going signal and remains at Low. Playback stops when the signal returns to High. This pin has an internal pull-up resistor [1] and an internal debounce on falling edge.
V_{SSA}	5	**Analog Ground**: V_{SSA} is the ground for analog circuits. It is important to have a separate path for each ground back to the system ground terminal to minimize noise.
MIC+	6	**Microphone Positive Input**: The input transfers the signal to the preamplifier. The internal Automatic Gain Control (AGC) circuit controls the gain of the preamplifier. An external microphone should be AC coupled to this pin via a series capacitor. The capacitor value, together with an internal 10 KΩ resistance on this pin, determines the low-frequency cutoff for the ISD1600B passband.
MIC-	7	**Microphone Negative Input**: This is the inverting input to the microphone preamplifier. It provides input noise-cancellation, or common-mode rejection, when the microphone is connected differentially to the device.
SP-	8	**Speaker Negative** : The SP-, Class D PWM output, provides a differential output with SP+ pin to drive 8Ω speaker or buzzer. During power down or recording, this pin is tri-stated.
V_{SSP}	9	**PWM Ground**: V_{SSP} is the ground for PWM speaker driver. It is important to have a separate path for each ground back to the system ground terminal to minimize noise.

PIN NAME	SOIC / PDIP PIN NO.	FUNCTIONS
V_{CCA}	10	**Analog power supply**: It is important to have a separate path for each power back to the power terminal to minimize the noises. Decoupling capacitors to V_{SSA} should be as close to the device as possible.
V_{CCP}	10	**V_{CCP}**: Power supply for PWM speaker drivers. It is important to have a separate path for each power back to the power terminal to minimize noise. Decoupling capacitors to V_{SSP} should be as close to the device as possible.
SP+	11	**Speaker Positive** : The SP+, Class D PWM output, provide a differential output with SP- pin to drive an 8Ω speaker or buzzer directly. During power down or recording, this pin is tri-stated.
AGC	12	**Automatic Gain Control**: The AGC dynamically adjusts the gain of the preamplifier to compensate the wide range of microphone input levels. The AGC allows the full range of signal to be recorded with minimal distortion. Nominal values of 4.7 μF give satisfactory results in most cases. Connecting this pin to ground provides maximum gain to the preamplifier circuitry. Conversely, connecting this pin to power supply provides minimum gain to the preamplifier circuitry.
AUD	13	**AUD**: The AUD provides a single-ended current output to drive an external amplifier. During standby or recording, this pin is tri-stated.
R_{OSC}	14	**Oscillator Resistor**: This enables the user to vary the record and/or playback duration of the device. A resistor connected between the R_{OSC} pin and V_{SSA} determines the sample frequency for the DL7801 device. Please refer to the Duration Section in Section 6.1.
V_{CCD}	15	**Digital power supply**: It is important to have a separate path for each power back to the power terminal to minimize noise. Decoupling capacitors should be as close to the device as possible.
$\overline{LED}$	16	**LED output**: This pin is Low during a record cycle and blinks during playback cycle. It can be used to drive an LED to indicate either a record or playback cycle is in progress.

Note: [1] 600kΩ (typical).

6. FUNCTIONAL DESCRIPTION

6.1. DETAILED DESCRIPTION

6.1.1 Audio Quality

Nuvoton's patented ChipCorder® MLS technology provides natural high quality record and playback solution on a single chip. The input audio signals are stored directly into the non-volatile memory and are reproduced in its natural form without any compression artifacts caused by the digital speech solutions. A complete sample is stored in a single cell, minimizing the memory needed to store a single message.

6.1.2 Duration

The DL7801 series offer single-chip solution with record & playback duration from 6.6 seconds to 40 seconds. Sampling frequency and duration are determined by an external resistor connected to the Rosc pin.

Sampling Frequency	Rosc	DL7801	DL7802	DL7803	DL7804
12 KHz	53 kΩ	6.6 secs	8 secs	10.6 secs	13.3 secs
8 KHz	80 kΩ	10 secs	12 secs	16 secs	20 secs
6.4 KHz	100 kΩ	12.5 secs	15 secs	20 secs	25 secs
5.3 KHz	120 kΩ	15 secs	18 secs	24 secs	30 secs
4 KHz	160 kΩ	20 secs	24 secs	32 secs	40 secs

6.1.3 Flash Storage

The DL7801 product utilizes the on-chip Flash memory providing zero-power message storage. The message is retained for up to 100 years without power. In addition, the device can be re-recorded typically over 100,000 times.

6.1.4 Basic Operation

The DL7801 ChipCorder® device is controlled by either the $\overline{\text{REC}}$, or one of the two playback modes, $\overline{\text{PLAYE}}$ and $\overline{\text{PLAYL}}$. The DL7801 parts are configured for simple design in single-message application. Detailed operations are explained in Section 6.2.

6.1.5 Automatic Power-Down Mode

At the end of a playback or record cycle, the DL7801 device automatically enters into a low-power mode, consuming typically 1μA, provided that $\overline{\text{PLAYE}}$, $\overline{\text{PLAYL}}$ and $\overline{\text{REC}}$ are High (see DC parameters Section). During a playback cycle, the device powers down automatically at the end of the message. During a record cycle, the device powers down immediately after $\overline{\text{REC}}$ is released to High.

6.2. FUNCTIONAL DESCRIPTION EXAMPLE

The following example operating sequences demonstrate the functionality of the DL7801 series.

6.2.1. Record a Message

The device starts recording from the beginning of the memory when $\overline{REC}$ transits from High to Low and stays at Low. A record cycle is completed when $\overline{REC}$ is pulled to High or entire memory is filled up. Then an End-of-Message (EOM) marker is written at the end of message, enabling a subsequent playback cycle to terminate appropriately. Hence, the device automatically enters into standby mode.

Record takes precedence over playback operation. If $\overline{REC}$ is pulled Low during a playback cycle, the playback immediately halts and recording starts from the beginning of the memory.

Holding $\overline{REC}$ Low after recording will increase standby current consumption.

6.2.2. Edge-trigger Playback

A playback operation starts from the beginning of the memory when $\overline{PLAYE}$ detects a low going signal exceeding the specified debounced time. Playback continues until an EOM marker is encountered. Upon completion of a playback cycle, the device automatically enters into standby mode.

During playback, a subsequent low going signal will terminate the current playback operation.

Holding this pin Low after playback operation will increase standby current consumption.

6.2.3. Level- trigger Playback

When $\overline{PLAYL}$ switches from High to Low and stays at Low, a playback starts from the beginning of the memory until either an EOM marker is reached, then it automatically powers down.

If $\overline{PLAYL}$ is pulled High at any time during playback, the playback operation stops immediately and the device enters into the power-down mode.

6.2.4. LED Operation

The $\overline{LED}$ is Low during recording, which turns on an LED as a recording indicator. However, during playback, the LED blinks a few times per second to indicate a playback operation. It returns to a High when operation stops.

6.2.5. R_{OSC} Operation

The duration can be varied by changing the value of R_{OSC}. This means the designer has the flexibility to choose different sampling frequency, up to 12 KHz, depending upon the needs.

This feature allows frequency shifting where a recorded audio can be played back faster or slower than normal for special sound effects.

Another feature is a “Pause” function that can be activated by taking the R_{OSC} resistor to V_{CC} to stop playback momentarily, and to resume when the resistor is switched back to ground.

7. TIMING DIAGRAMS

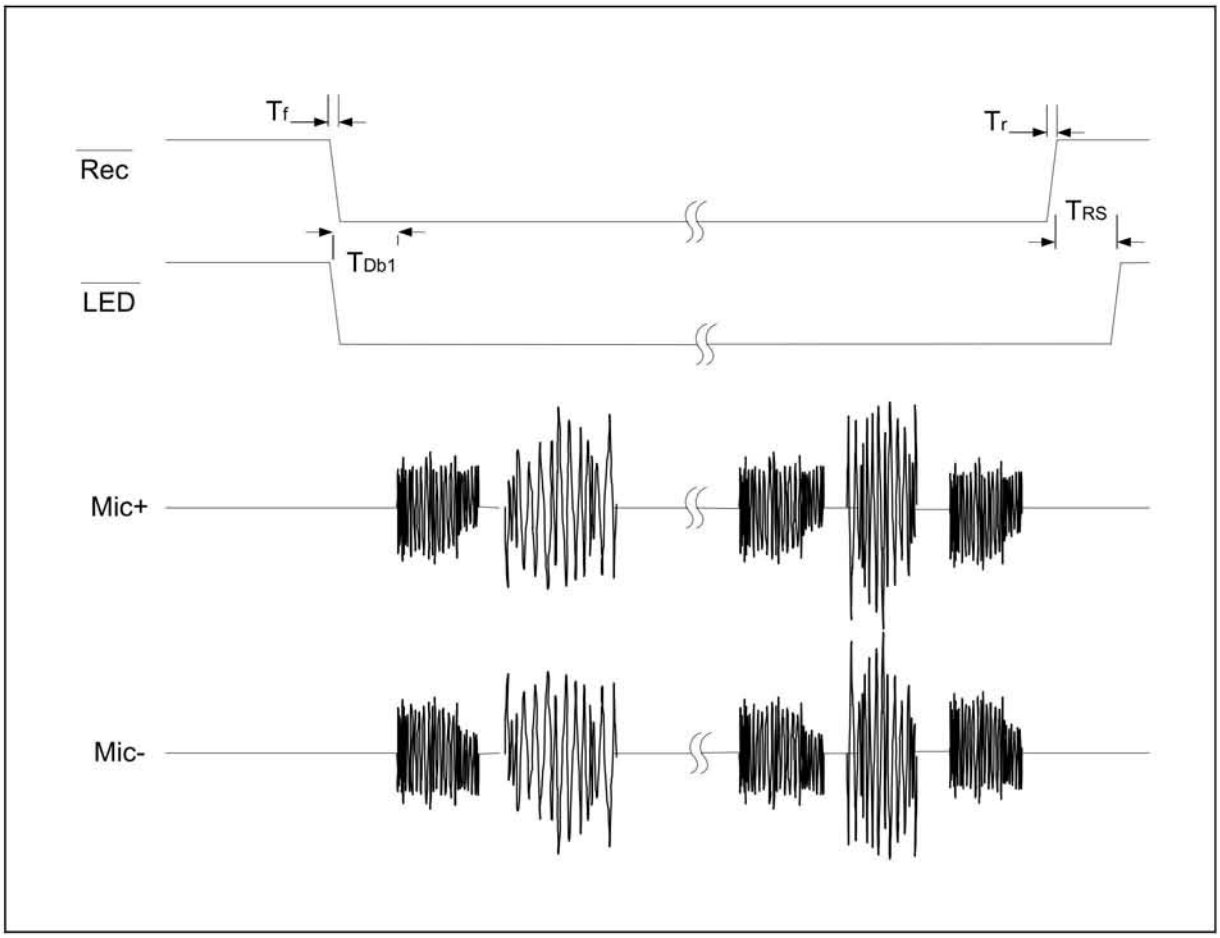


FIGURE 1: RECORD OPERATION

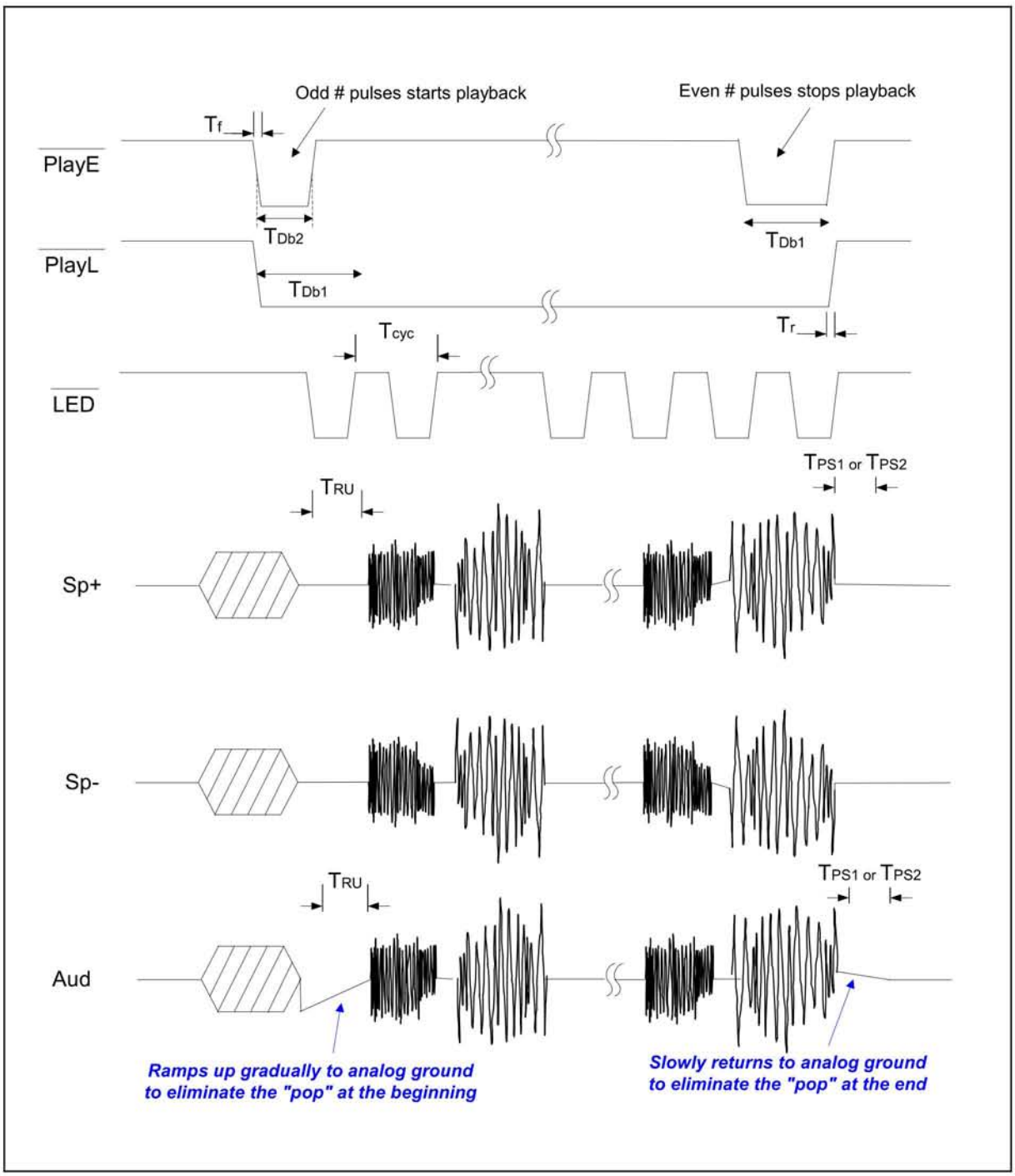


FIGURE 2: PLAYBACK OPERATION

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8. ABSOLUTE MAXIMUM RATINGS

ABSOLUTE MAXIMUM RATINGS (DIE)

CONDITIONS [1]	VALUES
Junction temperature	150°C
Storage temperature range	-65°C to +150°C
Voltage applied to all pins	(V_{SS} –0.3V) to (V_{DD} +0.3V)
Power supply voltage to ground potential	-0.3V to +7.0V

ABSOLUTE MAXIMUM RATINGS (PACKAGED PARTS)

CONDITIONS [1]	VALUES
Junction temperature	150°C
Storage temperature range	-65°C to +150°C
Voltage applied to all pins	(V_{SS} –0.3V) to (V_{DD} +0.3V)
Lead temperature (Soldering – 10 sec)	300°C
Power supply voltage to ground potential	-0.3V to +7.0V

[1] Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability and performance. Functional operation is not implied at these conditions.

8.1 OPERATING CONDITIONS

OPERATING CONDITIONS (DIE)

CONDITIONS	VALUES
Operating temperature range	0°C to +50°C
Supply voltage (V_{DD}) [1]	+2.4V to +5.5V
Ground voltage (V_{SS}) [2]	0V
Input voltage (V_{DD}) [1]	0V to 5.5V
Voltage applied to any pins	(V_{SS} –0.3V) to (V_{DD} +0.3V)

OPERATING CONDITIONS (PACKAGED PARTS)

CONDITIONS	VALUES
Operating temperature range (Case temperature)	-40°C to +85°C
Supply voltage (V_{DD}) [1]	+2.4V to +5.5V
Ground voltage (V_{SS}) [2]	0V
Input voltage (V_{DD}) [1]	0V to 5.5V
Voltage applied to any pins	(V_{SS} –0.3V) to (V_{DD} +0.3V)

[1] $V_{DD} = V_{CCA} = V_{CCD} = V_{CCP}$

[2] $V_{SS} = V_{SSA} = V_{SSD} = V_{SSP}$

9. ELECTRICAL CHARACTERISTICS

9.1. DC PARAMETERS

PARAMETER	SYMBOL	MIN	TYP [1]	MAX	UNITS	CONDITIONS
Supply Voltage	V_{DD}	2.4		5.5	V	
Input Low Voltage	V_{IL}	V_{SS}-0.3		0.3xV_{DD}	V	
Input High Voltage	V_{IH}	0.7xV_{DD}		V_{DD}	V	
Output Low Voltage	V_{OL}	V_{SS}-0.3		0.3xV_{DD}	V	I_{OL} = 4.0 mA[2]
Output High Voltage	V_{OH}	0.7xV_{DD}		V_{DD}	V	I_{OH} = -1.6 mA[2]
Record Current	I_{DD_Record}			20	mA	V_{DD} = 5.5V, No load, Sampling freq = 12 kHz
Playback Current	$I_{DD\_Playback}$			20	mA	
Standby Current	I_{SB}		1	10	μA	[3] [4]
Input Leakage Current	I_{ILPD1}			±1	μA	Force V_{DD} [5]
Input Current HIGH	I_{ILPD2}	-3		-10	μA	Force V_{SS} [5]
Preamp Input Resistance	R_{MIC+},R_{MIC-}		20		KΩ	Across both pins
MIC Input Voltage	V_{IN}		15	300	mV	Peak-to-Peak[6]
Gain from MIC to SP+/-	A_{MSP}	6		40	dB	V_{IN} = 15 to 300mV, AGC = 4.7μF, V_{DD} = 2.4V to 5.5V
Output Load Impedance	R_{EXT}	8			Ω	Speaker Load
Speaker Output Power	Pout		670		mW	V_{DD} = 5.5V; 15mVp-p 1kHz freq sinewave, R_{EXT} = 8Ω;
			313		mW	V_{DD} = 4.4V
			117		mW	V_{DD}= 3V
			49		mW	V_{DD}= 2.4V
Speaker Output Voltage	Vout		V_{DD}		V	R_{EXT} = 8Ω (Speaker), typical buzzer
AUD	I_{AUD}		-3.0		mA	V_{DD} =4.5V, R_{EXT}= 390Ω
Total Harmonic Distortion	THD		1		%	15mV p-p 1KHz sinewave, Cmessage weighted

Notes:
[1] Conditions: V_{CC} = 4.5V, 8kHz sampling frequency and T_A = 25°C, unless otherwise stated.
[2] LED output during Record operation.
[3] V_{CCA}, V_{CCD} and V_{CCP} are connected together. V_{SSA}, V_{SSP} and V_{SSD} are connected together.
[4] $\overline{REC}$, $\overline{PLAYE}$ and $\overline{PLAYL}$ must be at V_{CCD}.
[5] $\overline{REC}$, $\overline{PLAYE}$ and $\overline{PLAYL}$ are forced to specified condition.
[6] Balanced input signal applied between MIC and MIC REF as shown in the applications example. Single-ended MIC or MIC REF recommended to be less than 100 mV peak to peak.

9.2. AC PARAMETERS

CHARACTERISTIC	SYMBOL	MIN	TYP [1]				MAX	UNITS	CONDITIONS	
Sampling Frequency [2]	F_S	4					12	KHz	Vcc=2.4V~5.5V	
Duration [3]	Dur		DL7801	DL7802	DL7803	DL7804				
			6.6	8	10.6	13.3		Sec	SF=12kHz	Vcc=2.4 V~5.5V
			10	12	16	20		Sec	SF=8kHz	
			12.5	15	20	25		Sec	SF=6.4kHz	
			15	18	24	30		Sec	SF=5.3kHz	
			20	24	32	40		Sec	SF=4kHz	
Rising time	T_r	0					100	nsec		
Falling Time	T_f	0					100	nsec		
Debounce Time (Record & PlayL)	T_{Db1}		26.6	26.6	26.6	26.6		msec	SF=12kHz	Vcc=2.4 V~5.5V
			40	40	40	40		msec	SF=8kHz	
			50	50	50	50		msec	SF=6.4kHz	
			60.4	60.4	60.4	60.4		msec	SF=5.3kHz	
			80	80	80	80		msec	SF=4kHz	
Debounce Time (PlayE)	T_{Db2}		13.3	13.3	13.3	13.3		msec	SF=12kHz	Vcc=2.4 V~5.5V
			20	20	20	20		msec	SF=8kHz	
			25	25	25	25		msec	SF=6.4kHz	
			30.2	30.2	30.2	30.2		msec	SF=5.3kHz	
			40	40	40	40		msec	SF=4kHz	
Signal Ramp Up Time	T_{RU}	100						msec	Vcc=2.4V~5.5V	
Record Stop Time	T_{RS}		2 Sample Clock						Vcc=2.4V~5.5V	
PlayL Stop Time	T_{PS1}		T_{Db1}					msec	Vcc=2.4V~5.5V	
PlayE Stop Time	T_{PS2}		2 X T_{Db1}					msec	Vcc=2.4V~5.5V	
LED Cycle frequency	T_{Cyc}	1					6	Hz	Playback at any SF	

Notes:

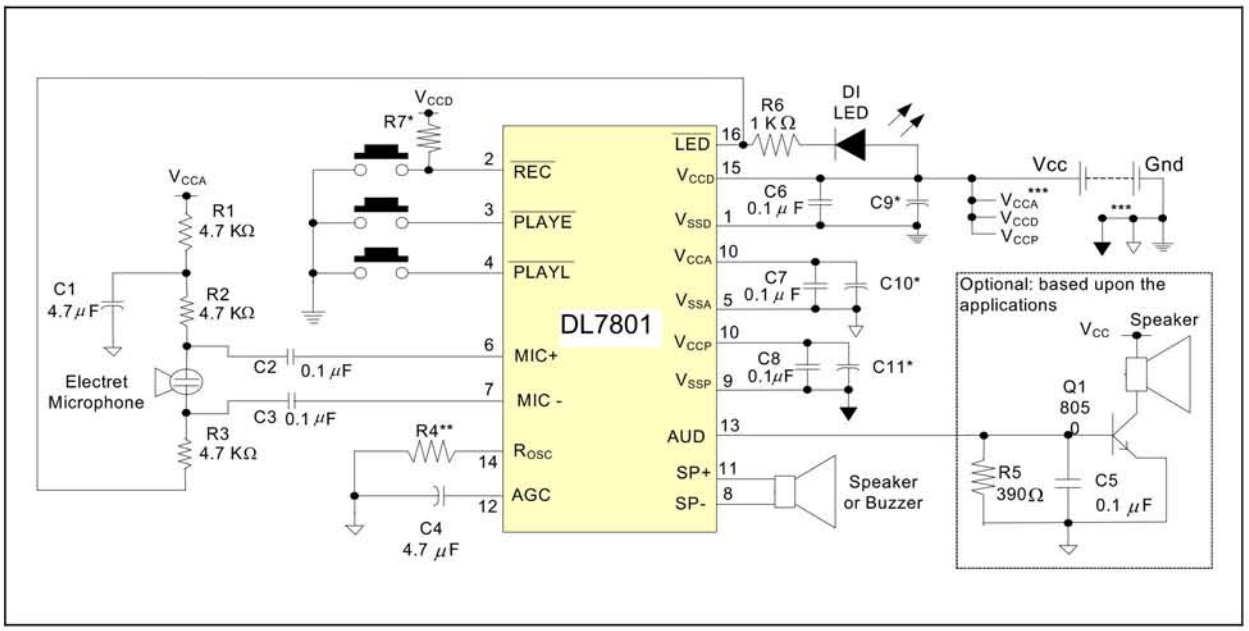
[1] Typical values : V_{CC} = 4.5V, sampling frequency (SF) = 8 kHz and @ T_A = 25°C, unless otherwise stated.

[2] Sampling Frequency can vary as much as ±2.25 percent over the commercial temperature and voltage ranges, and –6/+4 percent over the industrial temperature and voltage ranges.

[6] Duration can vary as much as ±2.25 percent over the commercial temperature and voltage ranges, and –6/+4 percent over the industrial temperature and voltage ranges.

10. TYPICAL APPLICATION CIRCUIT

The below example illustrates a typical applications of ISD1600B device.



Schematic shows both speaker and AUD outputs

Notes:

* These components may be needed in order to optimize for the best voice quality and system performance, which is also dependent upon the layout of the PCB. Pending upon system requirement, Cx can be 10 μF, 4.7 μF or other values. For R7, 1kΩ gives satisfactory result fro most cases.

** For Sampling Freq at 8 kHz, R4 = 80 KΩ

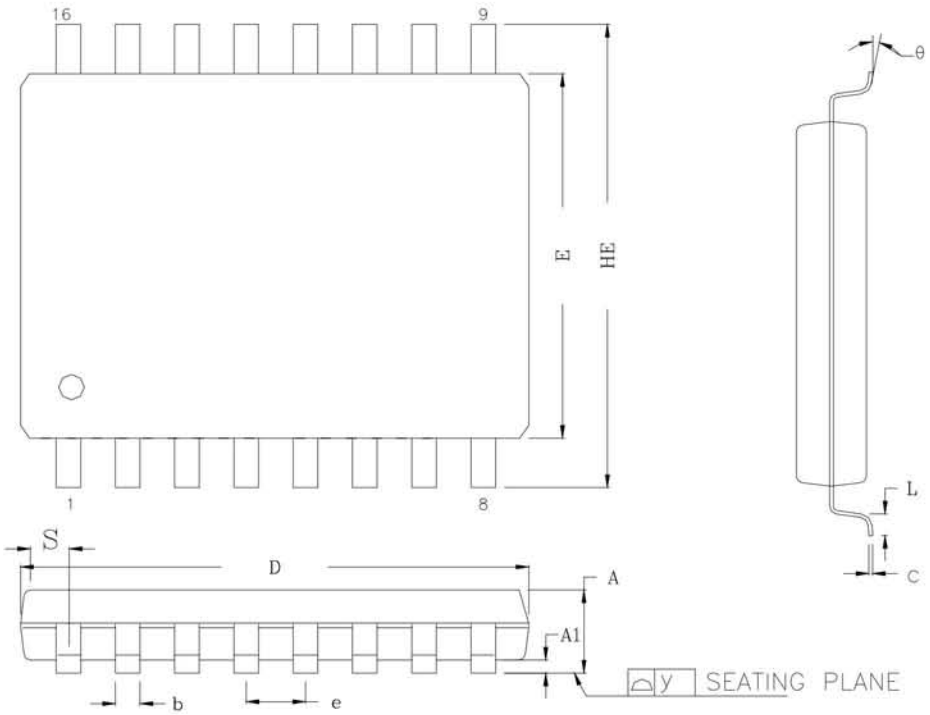
*** It is important to have a separate path for each ground and power back to related terminal to minimize the noise. Also, the power supplies should be decoupled as close to the device as possible.

Good Audio Design Practices

ChipCorder are very high-quality single-chip voice recording and playback devices. To ensure the highest quality voice reproduction, it is important that good audio design practices on layout and power supply decoupling are followed. See Application Information links below for details.

11. PACKAGE DRAWING AND DIMENSIONS

11.1. 16-Lead 150mil Small Outline Integrated Circuit (SOIC) Package

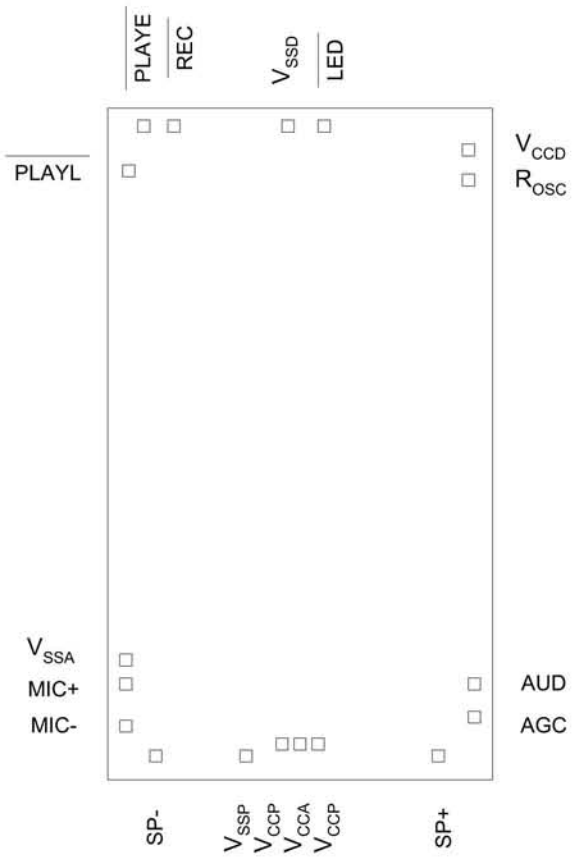


COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.35	——	1.75	0.053	——	0.069
A1	0.10	–	0.25	0.004	–	0.010
b	0.33	–	0.51	0.013	–	0.020
c	0.19	–	0.25	0.008	–	0.010
D	9.8	–	10.00	0.386		0.394
E	3.8	–	4.0	0.150		0.157
e	1.27 BASIC			0.050 BASIC		
HE	5.8	–	6.20	0.228	–	0.244
θ	0°	–	8°	0°	–	8°
L	0.40	–	1.27	0.016	–	0.050
S	0.394	–	0.648	0.0155	–	0.0255
y	–	–	0.10	–	–	0.004

11.2. Die Physical Layout

DL7801/7802/7803/7804

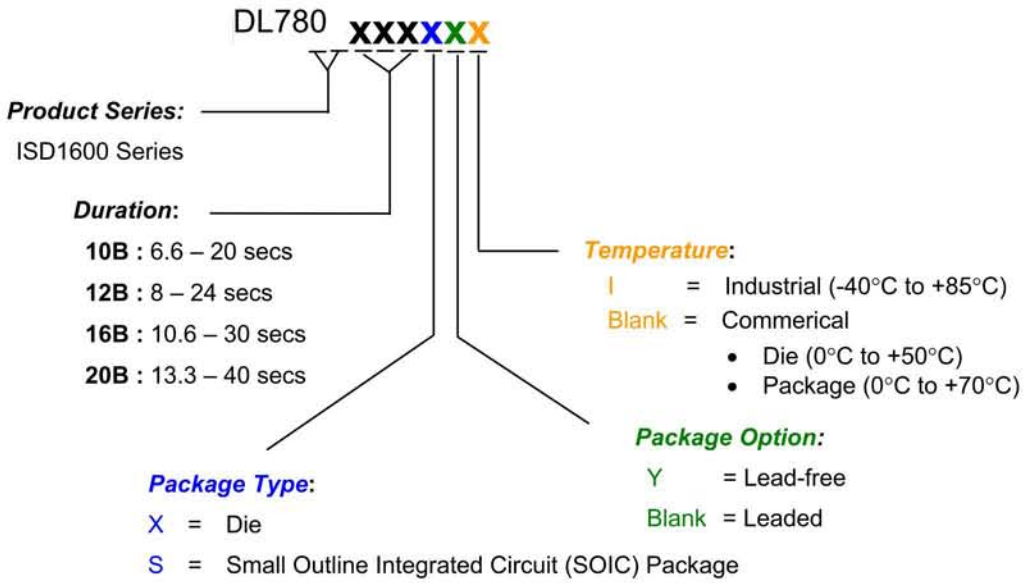


Notes:

1. The backside of die is internally connected to V_{SSA}. It **MUST NOT** be connected to any other potential or damage may occur.
2. For package, V_{CCA} and V_{CCP} pads are bonded together to one pin.

12. ORDERING INFORMATION

Product Number Descriptor Key



When ordering, please refer to the following valid part numbers that are supported in volume for this product series. Contact the local Nuvoton Sales Representative or Distributor for availability information.

13. VERSION HISTORY

VERSION	DATE	DESCRIPTION
A1	Apr 2005	Initial version
1	Jan 2006	Change to Preliminary Update Ordering info with Pb-free option
1.1	Apr 2006	Update application diagram
1.2	Jan 2007	Update Rosc resistor value Revise automatic power down mode Update standby current parameter Revise die physical layout section
1.21	Nov 2008	Update Application Circuit in Section 10 Remove PDIP package information Change to Nuvoton Logo
1.22	Dec 2008	Remove vAlert feature