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PSØ8

Single-chip Solution for Weight Scales

Final Version

Preliminary Datasheet

July 2008

Version 0.4

acam-messelectronic gmbh
solutions in time

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1 System Overview

1.1 Introduction

PS08 is a System-on-Chip for ultra low-power and high resolution applications. It was designed especially for weight scales but fits also to any kind of force or torque measurements based on metal strain gages. It takes full advantage of the digital measuring principle of PICOSTRAIN. Thus it combines the performance of a 28-Bit signal converter with a 24-Bit microprocessor. Additional elements like an LCD driver, 3k ROM with many complex pre-defined functions, 1k EEPROM program memory and an integrated 10 kHz oscillator round off the device. A minimum amount of external components is necessary to build a complete weighing electronic.

With PSØ8 it is possible for the first time to build solar cell driven weight scales based on metal strain gages. A sophisticated power management and the special features of the PICOSTRAIN measuring principle can reduce the total current of the system down to 15 µA – including the sensor current. This way the PSØ8 is perfectly suited for battery driven or solar cell driven weight scales.

On the other hand the PSØ8 offers a high resolution comparable to high-end ADC's. With maximum 1 million internal divisions (150,000 stable display divisions) it shows top performance. But it beats ADC with respect to current consumption. With PSØ8 it is possible to build legal for trade scales that run with 2 AA batteries for more than 1500 operating hours.

Throwing a glance at further specialties like software adjustment of the offset and gain compensation reveals that the PSØ8 opens the door to new and innovative product solutions.

1.2 Features

- PICOSTRAIN Front-End with up to 1 Mio. eff. scale divisions (@2mV/V) = 150.000 Peak-Peak Div.
- 24-Bit Microprocessor
- 1 k x 8-Bit EEPROM program memory, read protected
- 3 k ROM powerful program code like 48 Bit multiplication and division or binary to 7-segment conversion
- 8-layer hardware stack
- Embedded very low current 10 kHz oscillator
- Driver for external 4 MHz ceramic oscillator
- Standby current <1µA
- 5 programmable I/O-ports
- 4 x 14, 3 x 15, 2 x 16 LCD driver
- Embedded charge pump for driving the LCD
- Embedded bandgap voltage reference for low battery detection
- Ports for temperature measurement with low-cost carbon/metal film resistors
- Watchdog timer
- Serial SPI interface
- Supply voltage 2.2 to 3.6 V at 130 dB PSRR
- System operational current down to 15 µA
- As dice (115 µm pitch) or packaged (QFN56, 7x7 mm²)

1.3 Applications

Industrial
- Legal for trade scales
- Counting scales
- Torque indicators
- Pressure indicators

Consumer
- Solar scales
- Body scales
- Kitchen scales
- Postal scales
- Package scales

Important Note:
This datasheet is a preliminary version based on first engineering samples. It is not intended to be complete or correct in any detail. There might be major changes for the final version.

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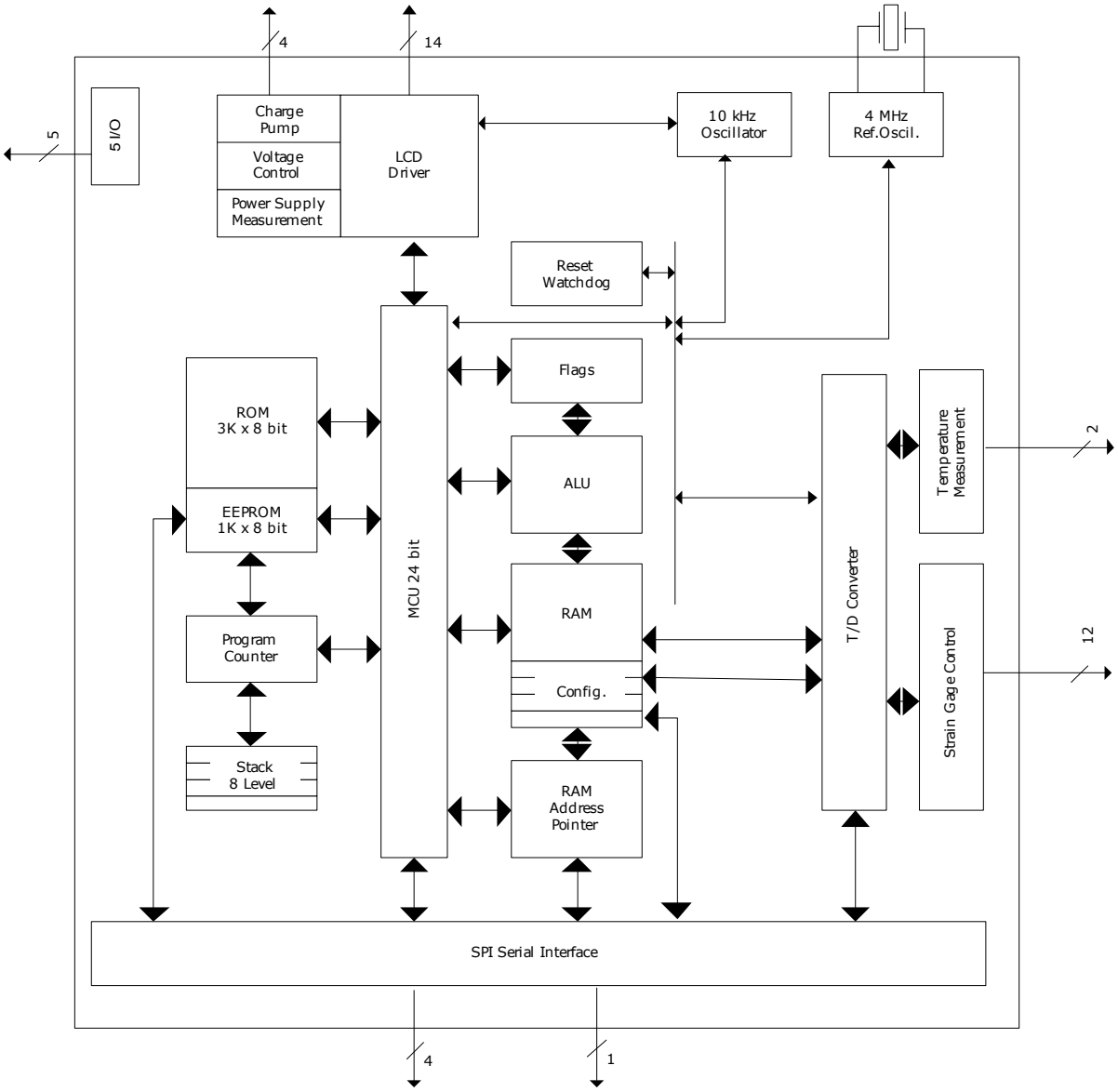
1.4 Architecture

Figure 1



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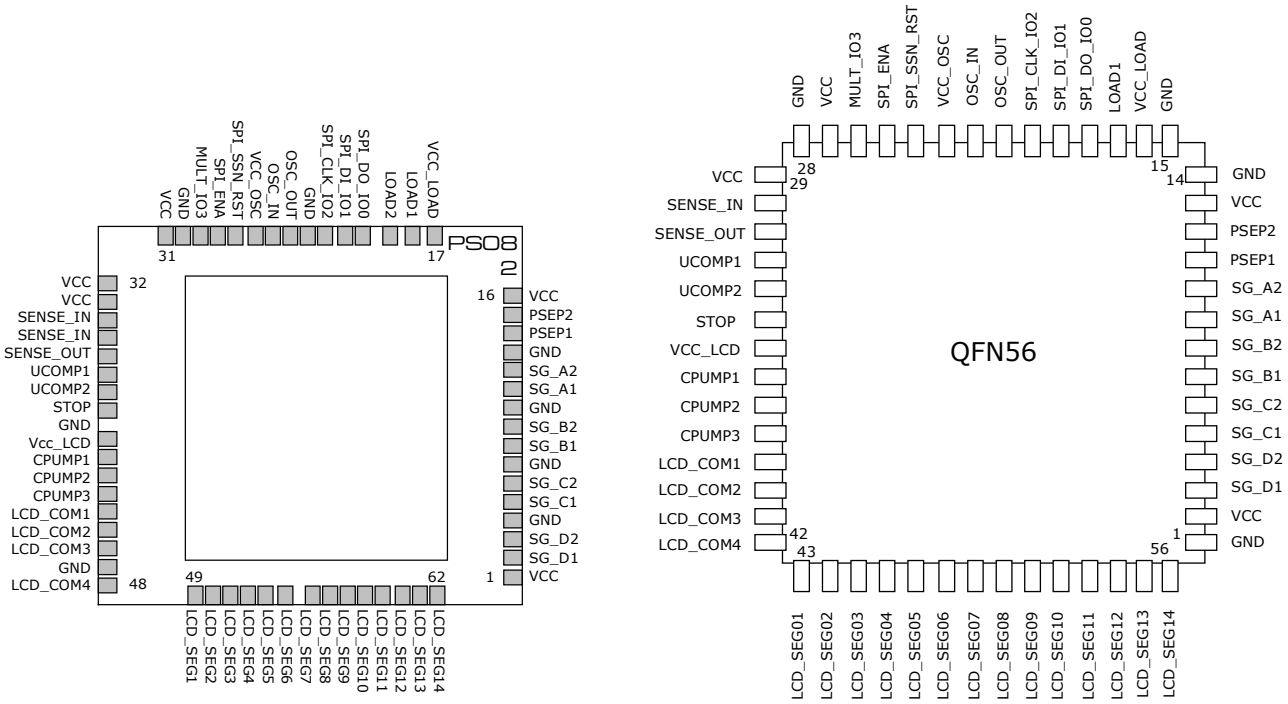
2 Characteristics and Specifications

2.1 Pin Assignment

Figure 2



Pin Assignment

2.2 Pin Description

Pure dice:

#Die	Name	Description	Type	If not used
1	VCC	Supply voltage digital part , I/O, 4MHz-osc.		
2	SG_D1	Port 1 halfbridge D	N Open Drain	
3	SG_D2	Port 2 halfbridge D	N Open Drain	
4	GND			
5	SG_C1	Port 1 halfbridge C	N Open Drain	
6	SG_C2	Port 2 halfbridge C	N Open Drain	
7	GND			
8	SG_B1	Port 1 halfbridge B	N Open Drain	
9	SG_B2	Port 2 halfbridge B	N Open Drain	
10	GND			
11	SG_A1	Port 1 halfbridge A	N Open Drain	
12	SG_A2	Port 2 halfbridge A	N Open Drain	
13	GND			
14	PSEP1	Port 1 temperature measurement	N Open Drain	
15	PSEP2	Port 2 temperature measurement	N Open Drain	
16	VCC	Supply voltage digital part , I/O, 4MHz-osc.		
17	VCC_LOAD	Power supply load output pins 1 and 2		
18	LOAD1	Load output to measuring capacitor	P Open Drain	
19	LOAD2		P Open Drain	
20	SPI_SO_IO0	Output serial SPI interface or IO0	Mult-IO	
21	SPI_SI_IO1	Input serial SPI interface or IO1	Mult-IO	
22	SPI_SCK_IO2	Clock serial SPI interface or IO2	Mult-IO	
23	GND			
24	OSC_OUT	Output to 4MHz ceramic resonator		
25	OSC_IN	Input to 4MHz ceramic resonator		

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26	Vcc_OSC	4MHz Oscillator supply voltage	Mult-IO	
27	SPI_CSN_RST	Slave select or RST input (High active)	Mult-IO with pull-down	
28	SPI_ENA	Serial SPI interface enable	Mult-IO	
29	MULT_IO3	Select for Wheatstone comparator Mux or IO3 or interrupt		
30	GND			
31	Vcc			
32	Vcc			
33	Vcc	Supply voltage digital part , I/O, 4MHz-osc.	Analog In	
34	SENSE_IN	Input internal CMOS comparator	Analog Out	
35	SENSE_OUT	Output internal CMOS comparator	Analog Out	
36	UCOMP1	External comparator circuit connection	Analog Out	
37	UCOMP2	External comparator circuit connection	Analog In	
38	STOP	Stop input measuring signal		
39	GND	GND		
40	VCC_LCD	Supply voltage LCD, 10kHz osc., bandgap		
41	CPUMP1	LCD voltage doubling and stabilization	Analog Out	
42	CPUMP2	LCD voltage doubling and stabilization	Analog Out	
43	CPUMP3	LCD voltage doubling and stabilization	Analog Out	
44	LCD_com1	LCD line driver for 1/2, 1/3, 1/4 duty	LCD Buffer	
45	LCD_com2	LCD line driver for 1/2, 1/3, 1/4 duty	LCD Buffer	
46	LCD_com3	LCD line driver for 1/3, 1/4 duty, row driver for 1/2 duty	LCD Buffer	
47	GND			
48	LCD_com4	LCD line driver for 1/4 duty, row driver for 1/2 , 1 /3 duty	LCD Buffer	
49	LCD_seg1	LCD row driver	LCD Buffer	
50	LCD_seg2	LCD row driver	LCD Buffer	
51	LCD_seg3	LCD row driver	LCD Buffer	
52	LCD_seg4	LCD row driver	LCD Buffer	
53	LCD_seg5	LCD row driver	LCD Buffer	
54	LCD_seg6	LCD row driver	LCD Buffer	
55	LCD_seg7	LCD row driver	LCD Buffer	
56	LCD_seg8	LCD row driver	LCD Buffer	
57	LCD_seg9	LCD row driver	LCD Buffer	
58	LCD_seg10	LCD row driver	LCD Buffer	
59	LCD_seg11	LCD row driver	LCD Buffer	
60	LCD_seg12	LCD row driver	LCD Buffer	
61	LCD_seg13	LCD row driver	LCD Buffer	
62	LCD_seg14	LCD row driver	LCD Buffer	

Packed, QFN56:

#QFN	Name	Description	Type	If not used
1	GND	Ground		
2	Vcc	Supply voltage digital part , I/O, 4MHz-osc.		
3	SG_D1	Port 1 halfbridge D	N Open Drain	
4	SG_D2	Port 2 halfbridge D	N Open Drain	
5	SG_C1	Port 1 halfbridge C	N Open Drain	
6	SG_C2	Port 2 halfbridge C	N Open Drain	
7	SG_B1	Port 1 halfbridge B	N Open Drain	
8	SG_B2	Port 2 halfbridge B	N Open Drain	
9	SG_A1	Port 1 halfbridge A	N Open Drain	
10	SG_A2	Port 2 halfbridge A	N Open Drain	
11	PSEP1	Port 1 temperature measurement	N Open Drain	
12	PSEP2	Port 2 temperature measurement	N Open Drain	
13	Vcc	Supply voltage digital part , I/O, 4MHz-osc.		
14	GND	Ground		

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15	GND	Ground		
16	Vcc_load	Power supply load output pins 1 and 2		
17	Load1	Load output to measuring capacitor	P Open Drain	
18	SPI_SO_IO0	Output serial SPI interface or IO0	Mult-IO	
19	SPI_SI_IO1	Input serial SPI interface or IO1	Mult-IO	
20	SPI_SCK_IO2	Clock serial SPI interface or IO2	Mult-IO	
21	OSC_OUT	Output to 4MHz ceramic resonator		
22	OSC_IN	Input to 4MHz ceramic resonator		
23	Vcc_OSC	4MHz Oscillator supply voltage	Mult-IO	
24	SPI_CSN_RST	Slave select or RST input (High active)	Mult-IO with pull-down	
25	SPI_ENA	Serial SPI interface enable	Mult-IO	
26	MULT_IO3	Select for Wheatstone comparator Mux or IO3 or interrupt		
27	Vcc			
28	GND	GND		
29	Vcc	Supply voltage digital part , I/O, 4MHz-osc.	Analog In	
30	SENSE_IN	Input internal CMOS comparator	Analog Out	
31	SENSE_OUT	Output internal CMOS comparator	Analog Out	
32	UCOMP1	External comparator circuit connection	Analog Out	
33	UCOMP2	External comparator circuit connection	Analog In	
34	STOP	Stop input measuring signal		
	GND	GND		
35	VCC_LCD	Supply voltage LCD, 10kHz osc., bandgap		
36	CPUMP1	LCD voltage doubling and stabilization	Analog Out	
37	CPUMP2	LCD voltage doubling and stabilization	Analog Out	
38	CPUMP3	LCD voltage doubling and stabilization	Analog Out	
39	LCD_com1	LCD line driver for 1/2, 1/3, 1/4 duty	LCD Buffer	
40	LCD_com2	LCD line driver for 1/2, 1/3, 1/4 duty	LCD Buffer	
41	LCD_com3	LCD line driver for 1/3, 1/4 duty, row driver for 1/2 duty	LCD Buffer	
42	LCD_com4	LCD line driver for 1/4 duty, row driver for 1/2 , 1 /3 duty	LCD Buffer	
43	LCD_seg1	LCD row driver	LCD Buffer	
44	LCD_seg2	LCD row driver	LCD Buffer	
45	LCD_seg3	LCD row driver	LCD Buffer	
46	LCD_seg4	LCD row driver	LCD Buffer	
47	LCD_seg5	LCD row driver	LCD Buffer	
48	LCD_seg6	LCD row driver	LCD Buffer	
49	LCD_seg7	LCD row driver	LCD Buffer	
50	LCD_seg8	LCD row driver	LCD Buffer	
51	LCD_seg9	LCD row driver	LCD Buffer	
52	LCD_seg10	LCD row driver	LCD Buffer	
53	LCD_seg11	LCD row driver	LCD Buffer	
54	LCD_seg12	LCD row driver	LCD Buffer	
55	LCD_seg13	LCD row driver	LCD Buffer	
56	LCD_seg14	LCD row driver	LCD Buffer	

2.3 Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
Vcc Vcc_load Vcc_osc Vcc_LCD	Supply voltage	Vcc vs. GND	-0.5	5.0	V
Vin	DC input voltage		-0.5	Vcc + 0.5	V
Tstg	Storage Temperature	Plastic package	-55	150	°C

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2.4 Normal Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
Vcc Vcc_load Vcc_osc Vcc_LCD	Supply voltage	Vcc vs. GND (* without EEPROM programming and voltage measurement)	2.2 (1.5*)	3.6	V
Vin	DC input voltage		0.0	Vcc	V
Vout	Output voltage		0.0	Vdd	V
Top	Operating temperature		-40	125	°C
Tstg	Storage temperature	Plastic package	-55	150	°C

2.4.1 Electrical Characterization

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
Vil	Input low voltage	CMOS			0.3Vcc	V
Vih	Input high voltage	CMOS	0.7Vcc			
Vhyst	Input hysteresys	Vcc = 3.6 V Vcc = 3.0 V Vcc = 2.7 V Vcc = 2.2 V Vcc = 1.8 V		400 280 225 150 80		mV
Voh	Output high voltage		0.8			V
Vol	Output low voltage				0.2Vcc	V
Vlbat	Low battery voltage detect		2.2		2.9	V
LCD_com LCD_seg	LCD driver Voltage stabilized	lcd_vlt = 0 lcd_vlt = 1 lcd_vlt = 2		2.0 2.5 3.0		V

2.5 Converter Precision

The following tables show the measurement capability for the PS∅8.

Table 1 Performance at Vcc = 3.6 V with external comparator

	ENOB ***dR/R strain resistance***				Resolution @ 2 mV/V max. out, ***Fast settle***			
Frequency (Hz)	No filter	SINC3	SINC5		ENOB	Divisions effective	Noise nV rms	Noise nV peak-peak
500	23.8	24.8	25.2		14.8	28,000	231	1,386
250	24.4	25.2	25.7		15.4	44,000	148	891
100	25.2	25.8	26.1		16.2	74,000	89	535
50	25.5	26.2	26.5		16.5	95,000	69	416
20	26.0	26.8	27.0		17.0	133,000	49	297
10	26.6	27.4	27.7		17.6	200,000	33	198
5	27.2	27.9	28.3		18.2	294,000	22	135

	Resolution @ 2 mV/V max. out, ***SINC3 Filter***				Resolution @ 2 mV/V max. out, ***SINC5 Filter***			
Frequency (Hz)	ENOB	Divisions effective	Noise nV rms	Noise nV peak-peak	ENOB	Divisions effective	Noise nV rms	Noise nV peak-peak
500	15.8	55,000	118	713	16.2	74,000	89	535
250	16.2	74,000	89	535	16.7	105,000	62	376
100	16.8	114,000	57	347	17.1	142,000	46	277
50	17.2	153,000	42	257	17.5	181,000	36	218
20	17.8	222,000	29	178	18.0	266,000	24	149
10	18.4	344,000	19	115	18.7	416,000	15	95
5	18.9	476,000	13	83	19.3	625,000	10	63

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Table 2 Performance at Vcc = 3.6 V with internal comparator

	ENOB ***dR/R strain resistance***				Resolution @ 2 mV/V max. out, ***Fast settle***			
Frequency (Hz)	No filter	SINC3	SINC5		ENOB	Divisions effective	Noise nV rms	Noise nV peak-peak
500	*23.0*	*24.0*	*24.4*		*14.0*			
250	*23.6*	*24.4*	*25.1*		*14.6*			
100	*24.4*	*25.0*	*25.3*		*15.4*			
50	*24.7*	*25.4*	*25.7*		*15.7*			
20	*25.2*	*26.0*	*26.2*		*16.2*			
10	*25.8*	*26.6*	*26.9*		*16.8*			
5	*26.4*	*27.1*	*27.5*		*17.4*			

Table 3 General

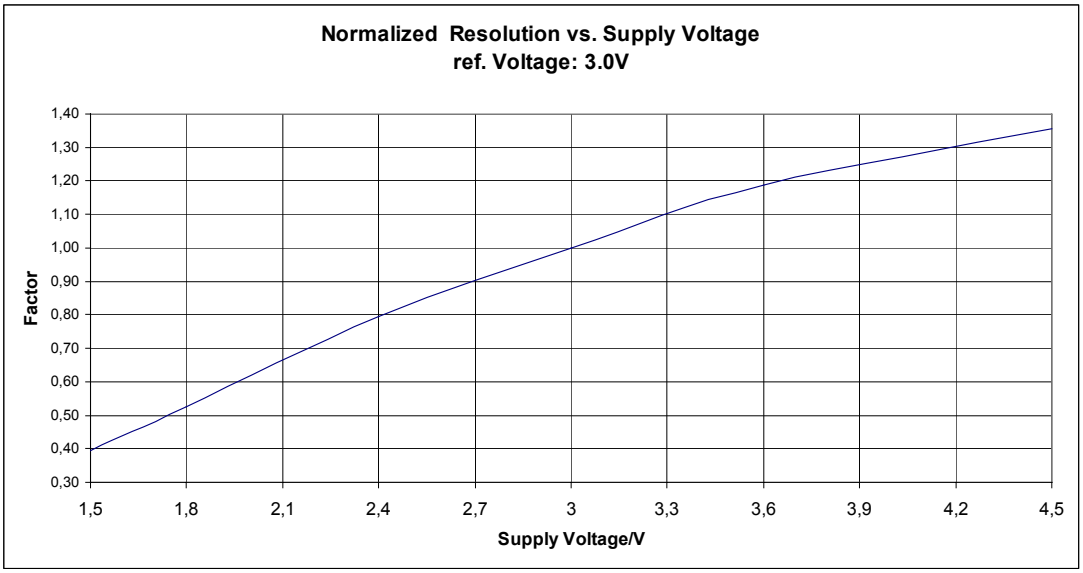
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
INL	Integral Non-linearity				0.0015	% of FS
	Offset drift	Total system, 1 kΩ DMS, 3V				
		Full-bridge		15		nV/K
		Half-bridge*		15		nV/K
	Gain drift over 0°C … 70°C	Total System. 1 KΩ DMS, 5V		< 1		ppm/K
PSSR	Power Supply Rejection Ratio Vcc	1.8V or 3.3 V +-0.3 V	106 @1.8V	130 @3.3V		dB

* if using recommended circuit

2.5.1 Resolution vs. Supply Voltage

PSØ8 can be driven over a very large supply voltage range. The resolution depends on the supply voltage. The higher the supply voltage the higher the achievable resolution. The diagram below shows the resolution vs. supply voltage which can be achieved with PSØ8. The values refer to 3.0 V.

Figure 3



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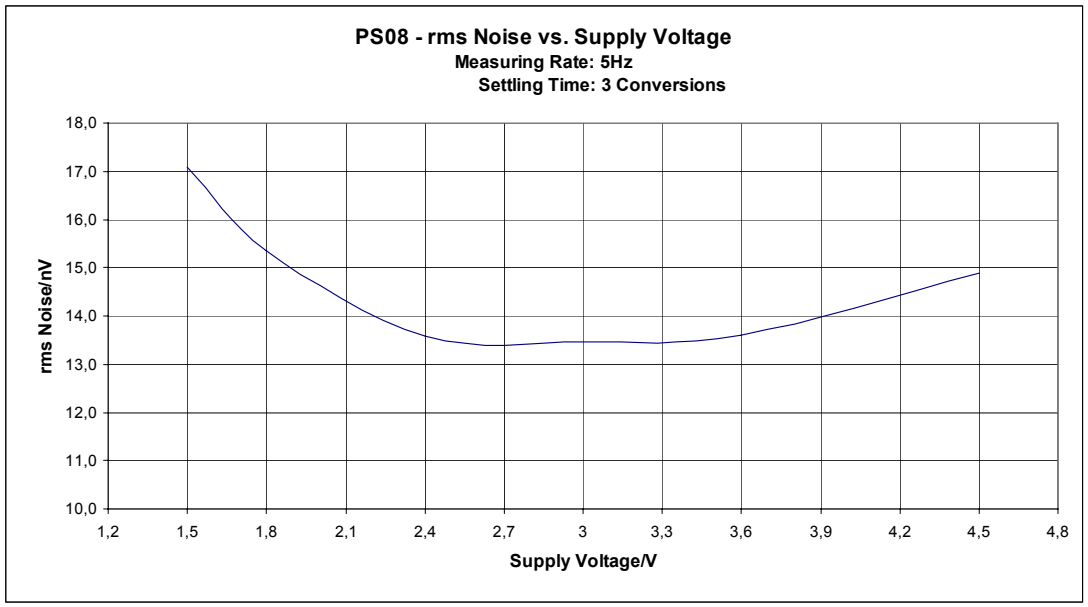
Following diagram shows how the input equivalent noise depends on the supply voltage. The lowest input noise is archived between 2.4 V and 3.6 V. The maximum differential input voltage (e.g. 6.6 mV @ 2mV/V and 3.3 V supply voltage) divided by the input noise gives the effective resolution.

Figure 4



2.5.2 Converter Precision with High Quality Load Cell

The following diagrams show measurement data of PSØ8 in combination with a C3 legal-for-trade load cell. With a SINC8 filter up to 1.000.000 internal scale divisions can be achieved. This is sufficient to realize more than 150.000 stable scale divisions. Please note that these values are captured with a high quality load cell.

	Fast settle	SINC3	SINC5	SINC8
effective Divisions	357.000	624.000	811.000	1.012.000
RMS-Noise/nV	20,1	11,5	8,9	7,1
effective Bits	18,4	19,3	19,6	19,9

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Figure 5

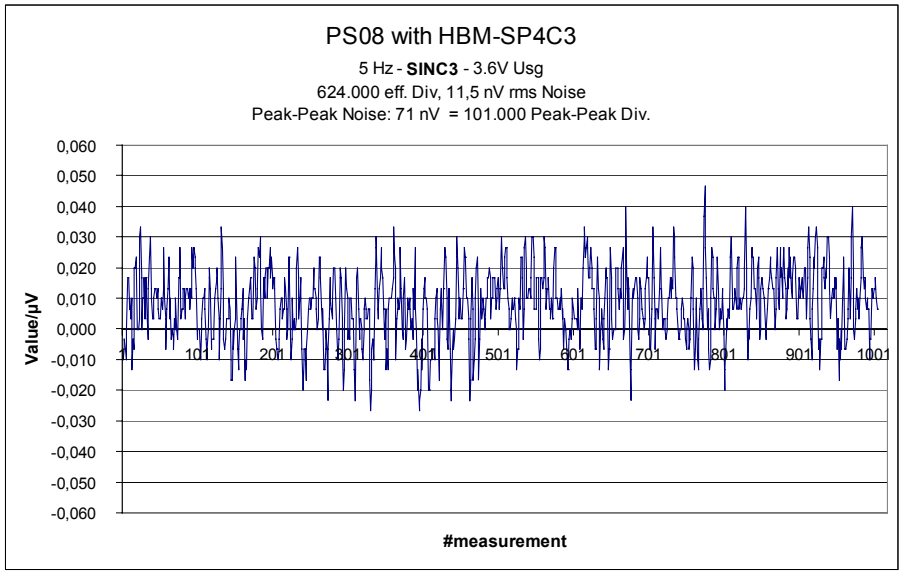
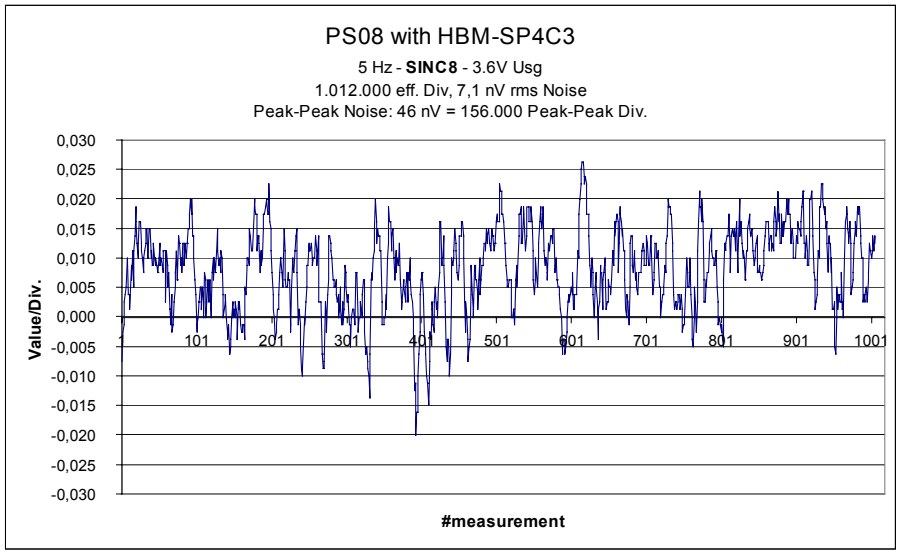


Figure 6



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2.6 Current Consumption

The following table shows the total current consumption of the scale including all currents.

Divisions * *	Update Rate	Double Tara*	Operating Current @ 3V		Scale type	Operating hours
2,000	3 Hz	yes	1 kOhm	15 µA	Solar	
2,000	5 Hz	yes	1 kOhm 350 Ohm	60 µA 90 µA	Postal, Body, Kitchen , Pocket	3,000 hours (1xCR2032)
5,000	5 Hz	yes	1 kOhm 350 Ohm	120 µA 220 µA	High-end postal, Kitchen, Pocket	1,500 hours (1xCR2032)
10,000	5 Hz	yes	1 kOhm 350 Ohm	300 µA 700 µA	High-end pocket, Counting	2,000 hours (1xCR2430)
80,000	5 Hz	no	1 kOhm 350 Ohm	1.9 mA 4.5 mA	Counting	1,500hours 2 x AA

* With double Tara there is no overload of the load cell if tara is set at max. load and additional max. load is put on the scale. In other words the sensor output is 1mV/V only at maximum load (no = 2 mV/V @ max load).
* * Divisions are peak-peak values with 5 Sigma (e. g. 80.000 divisions are 400.000 bits of effective resolution)

2.7 Timings

At Vcc = 3,3, V ± 0,3V, Ta –40°C to +85°C unless otherwise specified

2.7.1 Oscillators

Table 3 Oscillator timing

Symbol	Parameter	Min	Typ	Max	Units
Clk10kHz	10 kHz reference oscillator		10		kHz
to10st	Oscillator start-up				µs
ClkHS	High-speed reference oscillator		4		MHz
toHSst	Oscillator start-up time with ceramic resonator		50	150	µs

2.7.2 SPI-Interface

Table 4 Serial interface timing

Symbol	Parameter	Min	Typ	Max	Units
f_{clk}	Serial clock frequency			1	MHz
t_{pwh}	Serial clock, pulse width high	500			ns
t_{pwl}	Serial clock, pulse width low	500			ns
t_{sussn}	SSN enable to valid latch clock	500			ns
t_{pwssn}	SSN pulse width between write cycles	500			ns
t_{hssn}	SSN hold time after SCLK falling				
t_{sud}	Data set-up time prior to SCLK falling	30			ns
t_{hd}	Data hold time before SCLK falling	30			ns
t_{vd}	Data valid after SCLK rising				ns

Serial Interface (SPI compatible, Clock Phase Bit =1, Clock Polarity Bit =0):

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Figure 7 Write

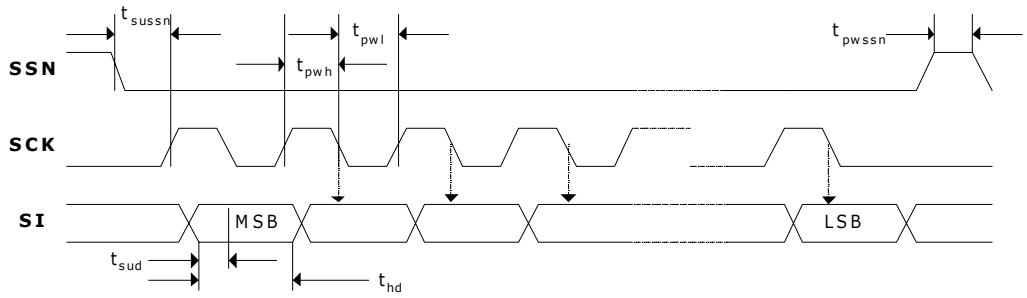
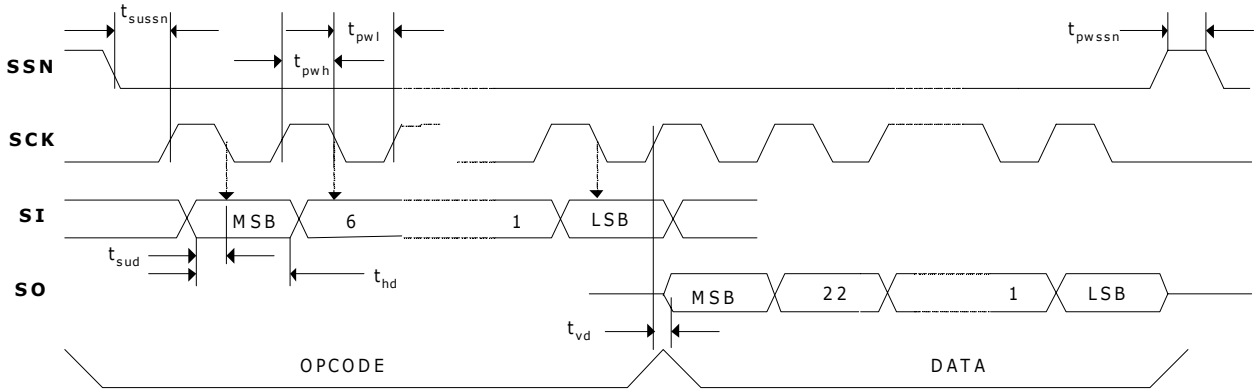


Figure 8 Read



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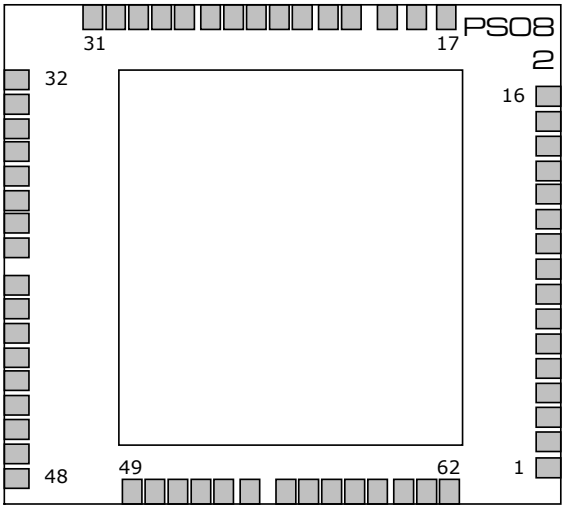
2.8 Package Information

2.8.1 PAD Assignment

Figure 9



2.8.2 Bonding PAD Location (only for Beta Version)

Table 6 Pad location

Pad #	Name	X [µm]	Y [µm]	Position	Pad#	Name	X	Y	Position
1	VCC	2583.8	193.8	right	32	VCC	83	2003.3	left
2	SG_D1	2583.8	316	right	33	VCC	83	1891.3	left
3	SG_D2	2583.8	431	right	34	SENSE_IN	83	1779.3	left
4	GND	2583.8	546	right	35	SENSE_OUT	83	1667.3	left
5	SG_C1	2583.8	661	right	36	UCOMP1	83	1555.3	left
6	SG_C2	2583.8	776	right	37	UCOMP2	83	1443.3	left
7	GND	2583.8	891	right	38	STOP	83	1331.3	left
8	SG_B1	2583.8	1006	right	39	GND	83	1219.3	left
9	SG_B2	2583.8	1121	right	40	VCC_LCD	83	1045	left
10	GND	2583.8	1236	right	41	CPUMP1	83	933	left
11	SG_A1	2583.8	1351	right	42	CPUMP2	83	821	left
12	SG_A2	2583.8	1466	right	43	CPUMP3	83	709	left
13	GND	2583.8	1581	right	44	LCD_com1	83	597	left
14	PSEP1	2583.8	1696	right	45	LCD_com2	83	485	left
15	PSEP2	2583.8	1811	right	46	LCD_com3	83	373	left
16	VCC	2583.8	1926	right	47	GND	83	261	left
17	VCC_LOAD	2115	2286	up	48	LCD_com4	83	149	down
18	LOAD1	1976.6	2286	up	49	LCD_SEG1	612.6	83	down
19	LOAD2	1835	2286	up	50	LCD_SEG2	724.6	83	down
20	SPI_SO_IO0	1656.2	2286	up	51	LCD_SEG3	836.6	83	down
21	SPI_SI_IO1	1544.2	2286	up	52	LCD_SEG4	948.6	83	down
22	SPI_SCK_IO2	1432.2	2286	up	53	LCD_SEG5	1060.6	83	down
23	GND	1320.2	2286	up	54	LCD_SEG6	1172.6	83	down
24	OSC_OUT	1208.2	2286	up	55	LCD_SEG7	1347	83	down
25	OSC_IN	1096.2	2286	up	56	LCD_SEG8	1459	83	down
26	VCC_OSC	984.2	2286	up	57	LCD_SEG9	1571	83	down
27	SPI_CSN_RST	872.2	2286	up	58	LCD_SEG10	1683	83	down
28	SPI_ENA	760.2	2286	up	59	LCD_SEG11	1795	83	down
29	MULT_IO3	648.2	2286	up	60	LCD_SEG12	1907	83	down
30	GND	536.2	2286	up	61	LCD_SEG13	2019	83	down
31	VCC	424.2	2286	up	62	LCD_SEG14	2131	83	down

PAD#: 56; Pad opening: 90µm width, 116µm height; Die size: 2770 x 2520 μm^2

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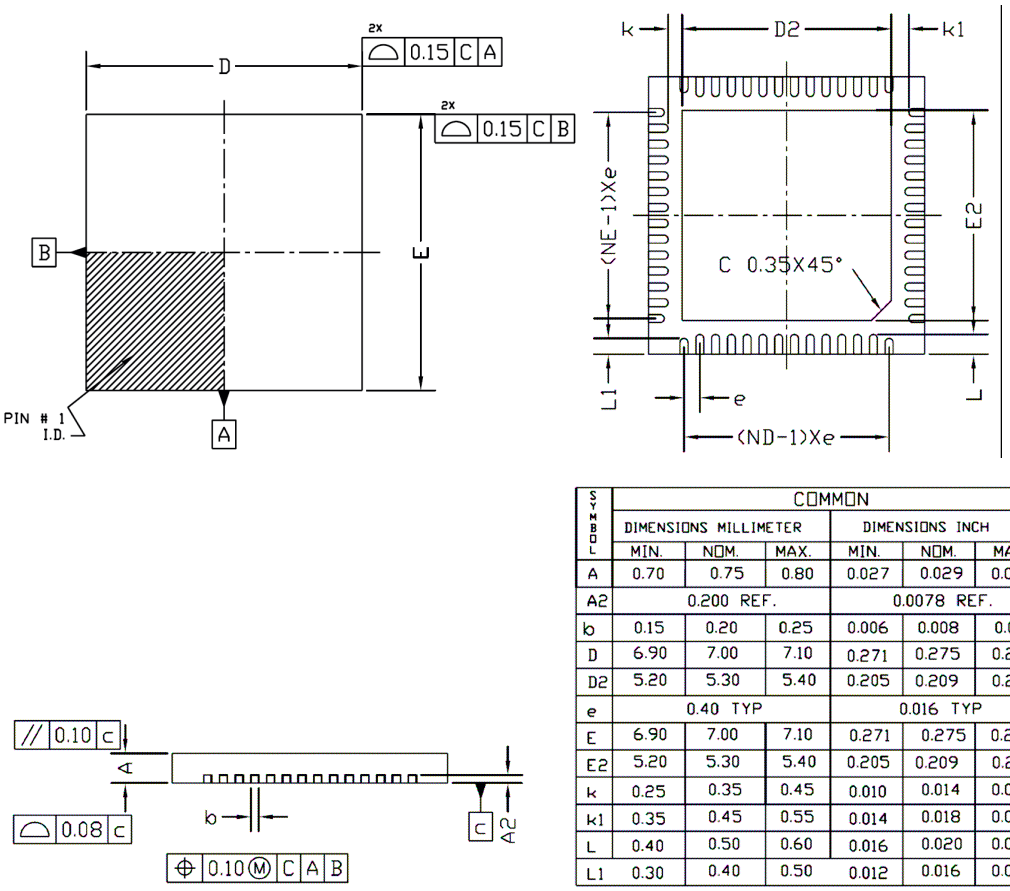
2.8.3 QFN56 Package Outline

QFN56, 7x7 mm², 0.4mm Pitch

Figure 10



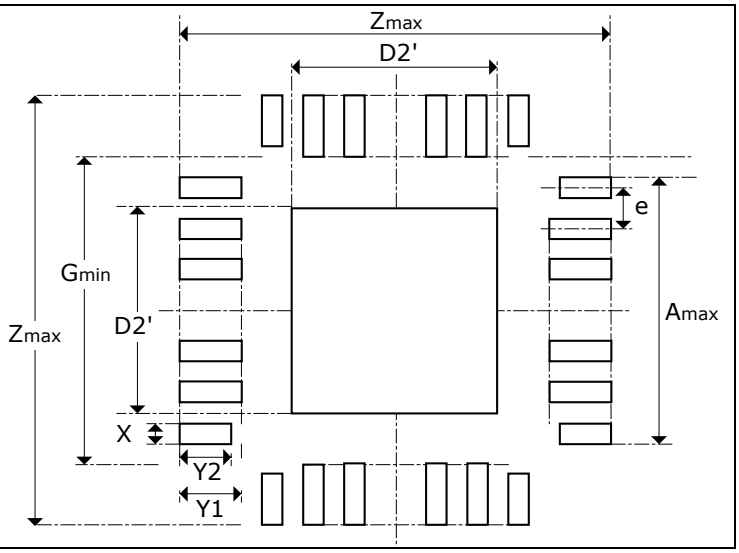
SYMBOL	COMMON					
	DIMENSIONS MILLIMETER			DIMENSIONS INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.027	0.029	0.031
A2	0.200 REF.			0.0078 REF.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	6.90	7.00	7.10	0.271	0.275	0.279
D2	5.20	5.30	5.40	0.205	0.209	0.213
e	0.40 TYP			0.016 TYP		
E	6.90	7.00	7.10	0.271	0.275	0.279
E2	5.20	5.30	5.40	0.205	0.209	0.213
k	0.25	0.35	0.45	0.010	0.014	0.018
k1	0.35	0.45	0.55	0.014	0.018	0.022
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.30	0.40	0.50	0.012	0.016	0.020

2.8.4 QFN56 Recommended Pad Layout

QFN56

		mm	inch
e	=	0.4	0.016
Gmin	=	6.3	
Zmax	=	8.0	
D2'	=	5.4	
Amax	=	5.45	
X	=	0.25	
Y1	=	0.85	
Y2	=	0.75	

Note: Size of ground plane may not be reduced. It should not contain any vias.



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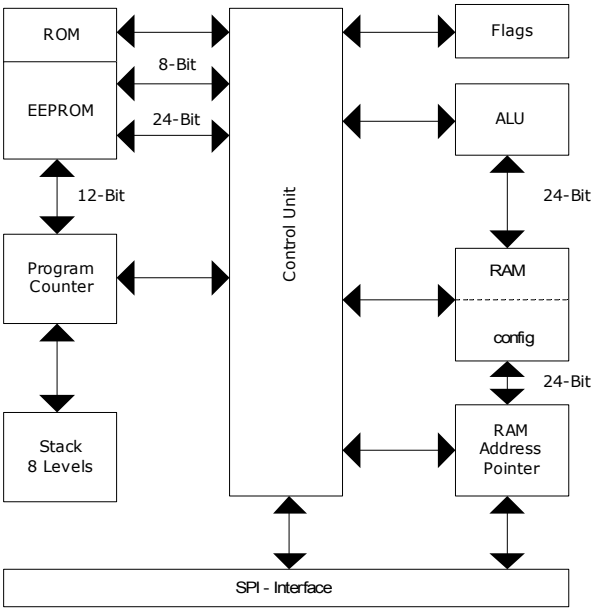
3 Central Processing Unit (CPU)

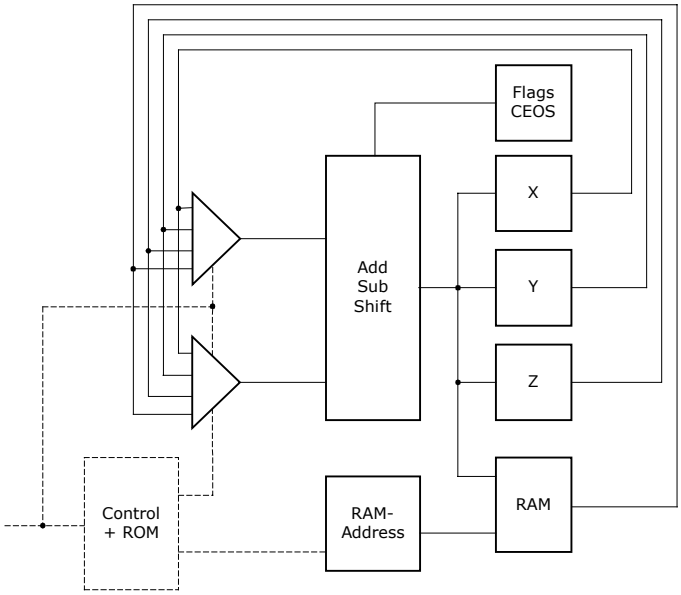
3.1 Block Diagram

Figure 11



3.2 Arithmetic Logic Unit (ALU)

Figure 12



3.2.1 Accumulators

The ALU has three 24-Bit accumulators, X, Y and Z. The RAM is addressed by the RAM address pointer and the addressed RAM cell is used as forth accumulator. A single RAM address is mapped into the ALU by the ram address pointer. So in total there are 4 accumulators. All transfer operations (move, swap) and arithmetic-operations (shift, add, mult24...) can be applied to all accumulators.

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3.2.2 Flags

The processor controls 4 flags with each operation. Not-Equal and Sign flags are set with each write access to one of the accumulators (incl. RAM). Additionally, the Carry and Overflow flags are set in case of a calculation (Add/Sub/shiftR). It is possible to query each flag by a jump instruction.

- Carry
  Shows the carry over in an addition or substraction. With shift operations (shiftL, rotR etc.) it shows the postponed bit.
- Not-equal zero
  This flag is set to zero in case a new result unequal zero is written into an accumulator (add,sub,move,swap etc.).
- Sign
  The Sign is set when a new result is written into an accumulator (add,sub,move,swap etc.) and the highest bit (MSB) is 1.
- Overflow
  Indicates an overflow during an addition or substraction of two numbers in the meaning of two's complement.

3.3 Memory Organization

3.3.1 ROM and EEPROM Organization

Table 1

4095 ... 1024	Program Memory ROM
1023 ... 48	Program Memory EEPROM bank 1 EEPROM bank 2 Program entry
47...45 44...42 41...39	Config Reg 15 (mirrored) Config Reg 14 (mirrored) Config Reg 16 (mirrored)
38...35 5...3 2...0	Config Reg 12 (mirrored) Config Reg 1 (mirrored) Config Reg 0 (mirrored)

The ROM area is starting at address 1024. All computation routines needed for the PICOSTRAIN measuring method reside here. There are also further helpful routines that are frequently needed in weight scale applications, e.g. decimal to 7-segment code conversion. These routines can be called by a program in the EEPROM. The program can also jump back from the ROM to the EEPROM when configured.
The EEPROM is 1024 bytes big, split in two blocks of 512 bytes. The program memory occupies 976 bytes starting from address 48. Each jump from the ROM into the EEPROM starts at address 48. The program in the EEPROM may find out the reason for the jump by means of the status information in register 22.

The lower 48 bytes in the EEPROM are reserved for an automatic configuration of the PSØ8 during a power-on reset. 3 successive bytes are added to a 24 bit word. So there are 16 words of 24 bit that can be read by the program code.

The lower bytes from 0 to 38 make 13 words of 24 bit and are used for configuration. During a power- on reset they are copied into RAM address 48 to 60.

EEPROM cells 39 to 47 are not necessary for the standard configuration. The processor can write to and read from those cells during operation (putepr and getepr). They can be used for saving calibration data.

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3.3.2 RAM Organization

Table 2

64 48	Config Reg 16 ... Config Reg 0
47 ... 32	User RAM 47 ... User RAM 32
31 ... 26 25 24 23 22 21 20 19 18 17 16	System RAM ... System RAM UBATT CAL HB1+ Flags (p1-p2)/p2 HB0 = (A-B)+(...) / (A+B)+(...) HB4 = (G-H)/(G+H) HB3 = (E-F)/(E+F) HB2 = (C-D)/(C+D) HB1 = (A-B)/(A+B)
15 ... 0	User RAM 15 ... User RAM 0

A..F = Discharging times at the different ports, see *3.4.2 Result Registers* for more details

3.3.3 RAM Address Pointer

The RAM has its own address bus with 64 addresses. The with of 24 Bit corresponds to the register width of the ALU. By means of the ram address pointer a single ram address is mapped into the ALU. It then acts as a fourth accumulator register. Changing the ram address pointer does not effect the content of the addressed ram. The RAM address pointer is modified by separate opcodes (ramadr, incramadr,...)

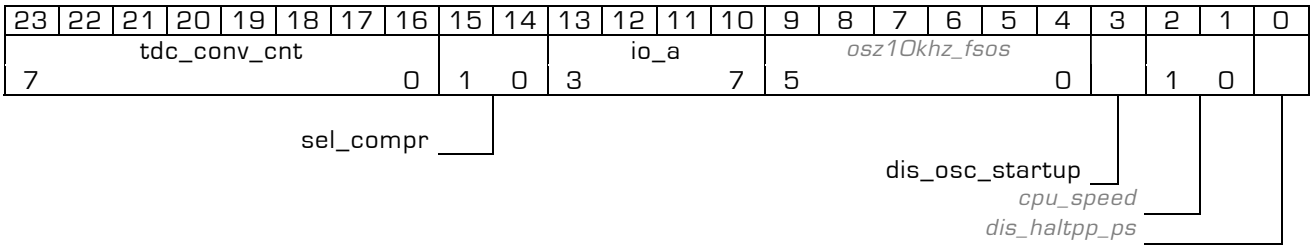
3.4 Register Set

3.4.1 Configuration Registers

PSØ8 has 16 configuration registers of 24 Bit width, to be addressed in the RAM from address 48 to 64. The configuration registers control the whole chip including the strain measurement and the LCD controller.

It is possible to write into the configuration registers
- By the microprocessor during operation
- Through the SPI interface from an external processor
- During the Power-on reset transferring a basic configuration from the EEPROM

Configreg_00: RAM address 48 EEPROM bytes 0 - 2



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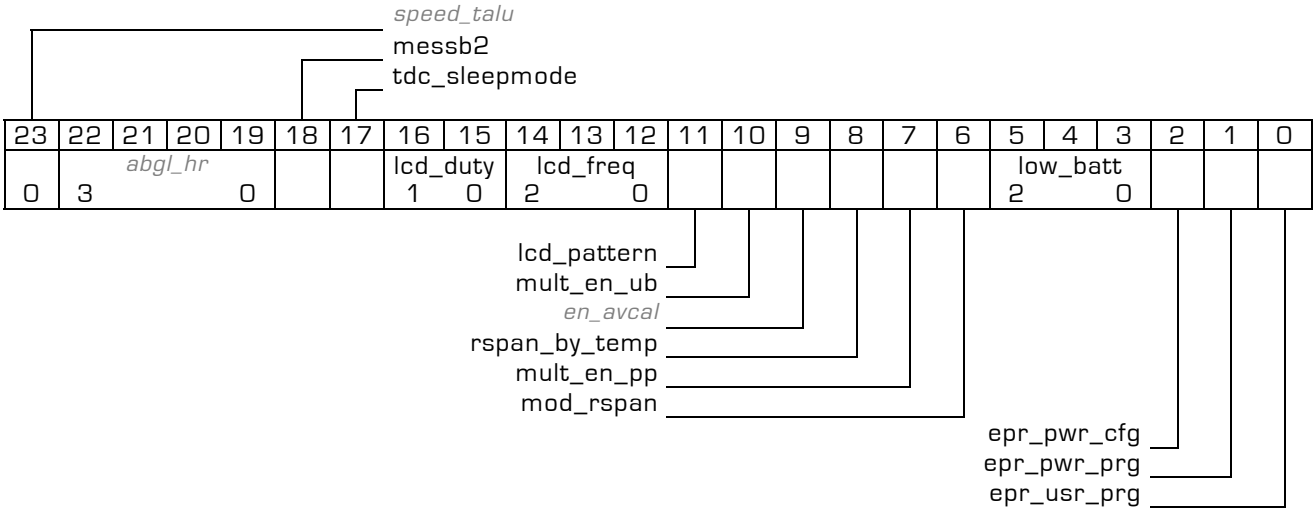
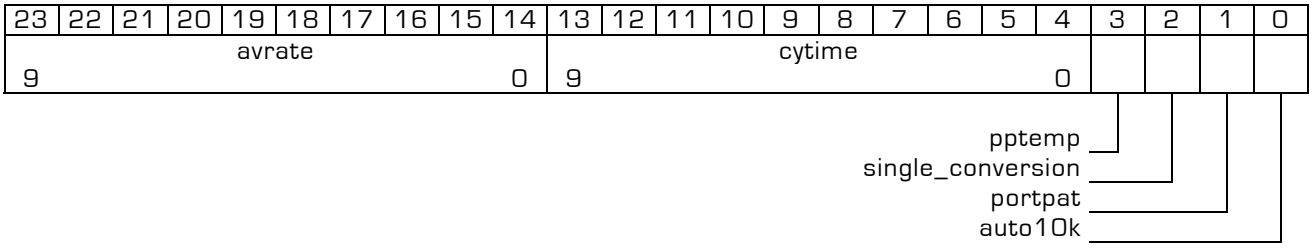
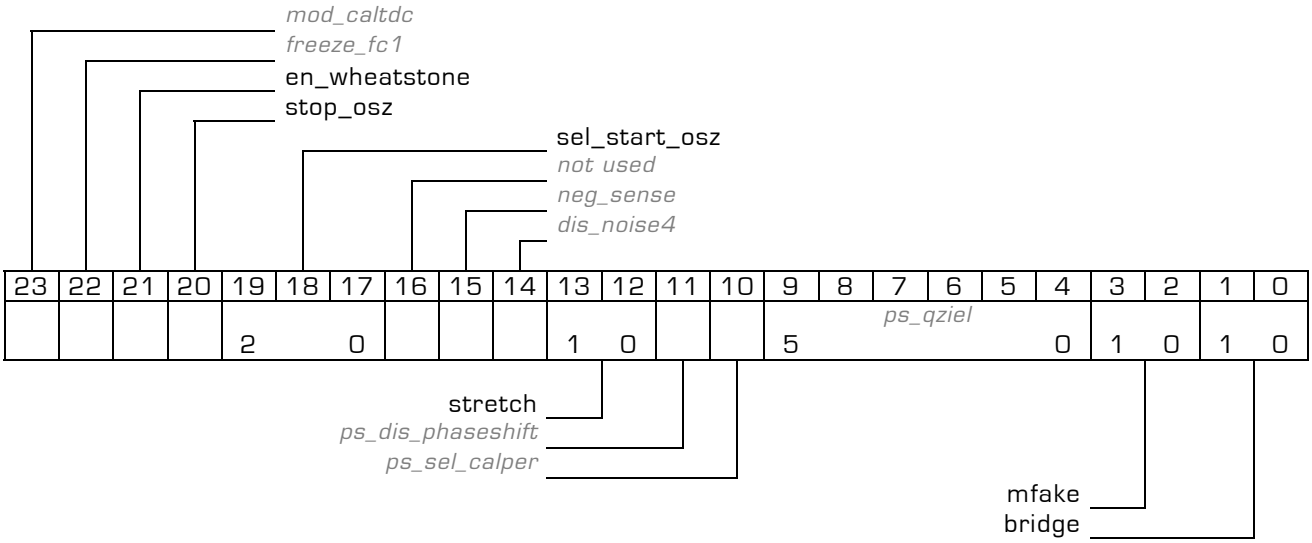
Configreg_01: RAM address 49 EEPROM bytes 3 - 5



Configreg_02: RAM address 50 EEPROM bytes 6 - 8



Configreg_03: RAM address 51 EEPROM bytes 9 - 11



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Configreg_04: RAM address 52 EEPROM bytes 12 - 14

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mult_Hb1																							
23																							0

Configreg_05: RAM address 53 EEPROM bytes 15 - 17

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mult_Hb2																							
23																							0

Configreg_06: RAM address 54 EEPROM bytes 18 - 20

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mult_Hb3																							
23																							0

Configreg_07: RAM address 55 EEPROM bytes 21 - 23

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mult_Hb4																							
23																							0

Configreg_08: RAM address 56 EEPROM bytes 24 - 26

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mult_TkG																							
23																							0

Configreg_09: RAM address 57 EEPROM bytes 27 - 29

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mult_TkO																							
23																							0

Configreg_10: RAM address 58 EEPROM bytes 30 - 32

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
calcor								Mult_Ub								Mult_PP							
7							0	7							0	7							0

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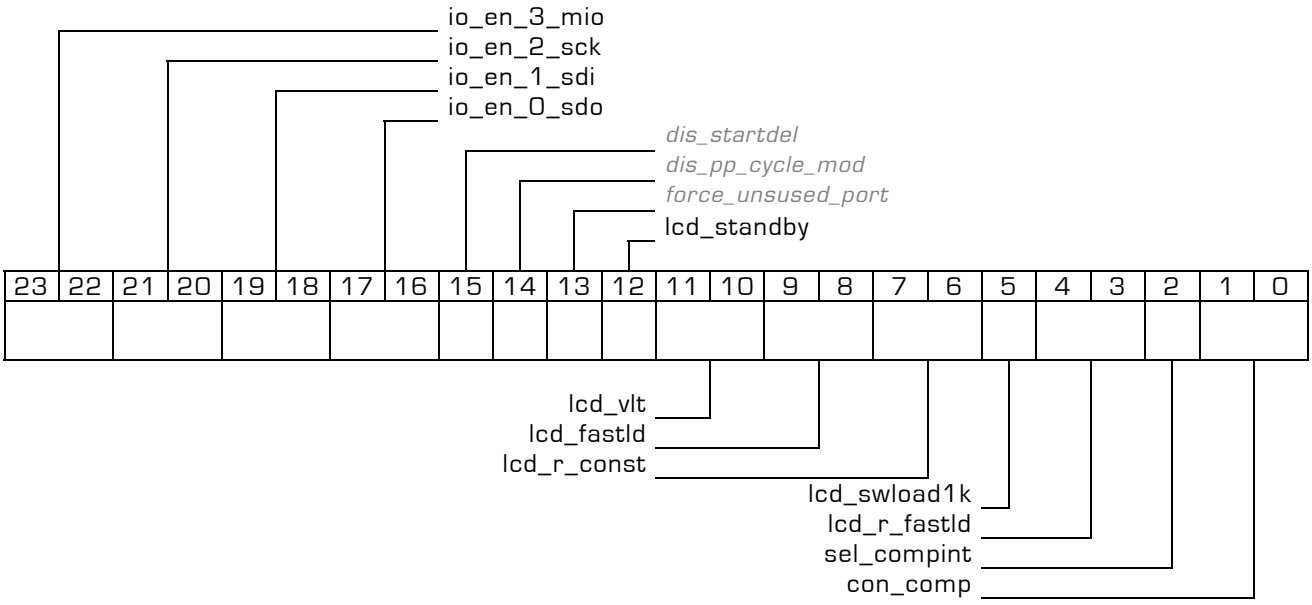
Configreg_11: RAM address 59 EEPROM bytes 33 - 35



Configreg_12: RAM address 60 EEPROM bytes 36 - 38

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
lcd_pos																							
23																							0

Configreg_13: RAM address 61 Not mirrored in the EEPROM !

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
lcd_segment																							
23																							0

Configreg_14: RAM address 62 EEPROM bytes 42 - 44

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
lcd_segment																							
47																							24

Configreg_15: RAM address 63 EEPROM bytes 45 - 47

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1'bx																lcd_segment							
15															0	55							48

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Configreg_16: RAM address 64 EEPROM bytes 39 - 41

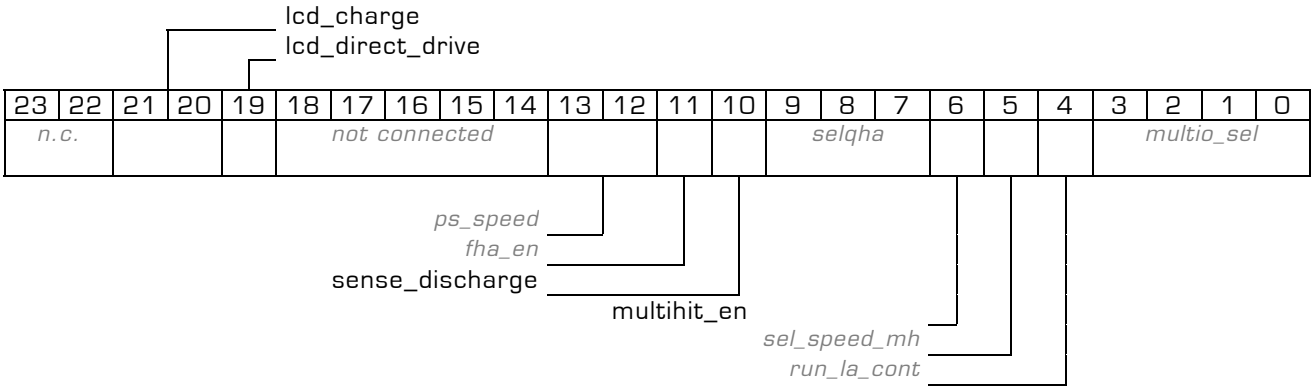

Table 3

Configuration Value	Register	Recomm. Default	Hardware Default	Description
abgl_hr[3:0]	*1*	*5*	*5*	*High resolution trim*
auto10k	2	1	1	Automatic calibration of the 10k oscillator every 0.6s by means of the 4 MHz quartz oscillator. May not be used in stretched-single mode
avrate[9:0]	2	25	1	Internal averaging rate
bridge[1:0]	3	0	0	0 = not reasonable (one Halfbridge) 1 = 2 half bridges 2 = not supported 3 = 4 half bridges
calcor[7:0]	*10*	*0*	*0*	*Correction factor for TDC calibration value* *cal := cal + calcor/8 = cal + [-127 to +128]/8* *= cal + [-15.875 to +16.000]*
con_comp[1:0]	11	3	3	Comparator switch-off mode 00 = off 01 = off between single measurements 10 = off during loading and between single measurements 11 = always on
cpu_speed[1:0]	*0*	*3*	*3*	*CPU ring oscillator speed* *00 = fast* *01 = default* *10 = slow* *11 = very slow*
cytime[7:0]	2	100	100	Cycle time in multiples 2 µs (8 * 4 MHz period, stretch = 0) or of 100 µs (10 kHz period, stretch = 1)
Special interal Bits	*0*	*0*	*0*	*Use default*
dis_noise4	*3*	*0*	*0*	*Disable main noise unit*
dis_osc_startup	0	1	0	Reduce current when starting the oscillator
dis_pp_cycle_mod	*11*	*0*	*0*	*Disable gain measurement with double cycle*

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Configuration Value	Register	Recomm. Default	Hardware Default	Description
dis_startdel	*11*	*1*	*1*	*Disable start delay*
en_avcal	*1*	*0*	*0*	*Enable TDC calibration value averaging by factor 16*
en_wheatstone	3	0	0	Enable Wheatstone mode
epr_pwr_cfg	1	0	0	as frontend := 0 stand-alone := 1 Configuration in the EEprom is used after a power-on reset
epr_pwr_prg	1	0	0	as frontend := 0 stand-alone := 1 Start user code at EEPROM address 48 after a power-on reset
epr_usr_prg	1	0	0	as frontend := 0 stand-alone := 1 Start user code at EEPROM address 48 after a measurement
Special internal Bits	*16*	*0*	*0*	*Use default*
force_unused_port	*11*	*0*	*0*	*force unused measurement ports to GND*
Special internal Bits	*3*	*0*	*0*	*Use default*
io_a[3:0]	0	0	0	I/O's Output: output value, can be read back Input: read input value
io_en_0_sdo[1:0]	11	3	2	Port definition 00 = output 01 = input with pull-up 10 = input with pull-down 11 = input
io_en_1_sdi[1:0]	11	3	2	Port definition 00 = output 01 = input with pull-up 10 = input with pull-down 11 = input
io_en_2_sck[1:0]	11	3	2	Port definition 00 = output 01 = input with pull-up 10 = input with pull-down 11 = input
io_en_3_mio[1:0]	11	3	2	Port definition 00 = output 01 = input with pull-up 10 = input with pull-down 11 = input
lcd_duty[1:0]	1	0	0	LCD duty cycle definition 0 = off 1 = 1/2duty 2 = 1/3duty 3 = 1/4duty
lcd_charge[1:0]	16	0	0	Selects number of LCD cycles before recharging 0 = recharging each cycle 1 = recharging each 2nd cycle 2 = recharging each 3rd cycle 3 = recharging each 4th cycle

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Configuration Value	Register	Recomm. Default	Hardware Default	Description
lcd_directdrive	16	0	0	Drive LCD directly from supply voltage
lcd_fastld[1:0]	11	2	2	Configures the number of fastload periods (10ms) with low-resistance voltage divider
lcd_freq[2:0]	1	4	0	Select LCD frequency (switch-on time of pixels)

Pixel	Time	Multiplex mode			
		1/4	1/3	1/2	Hz
0	8.0ms	15	20	31	Hz
1	4.8ms	26	34	52	Hz
2	4.0ms	31	42	62	Hz
3	3.2ms	30	52	78	Hz
4	2.4ms	52	69	104	Hz
5	2.0ms	62	83	125	Hz
6	1.6ms	78	104	176	Hz
7	1.2ms	104	138	208	Hz

lcd_pos[23:00]	12	o76543210	o76543210	Position of LCD segments
lcd_r_const[1:0]	11	1	0	Defines the cross resistance of the LCD voltage divider 0 = 15 k 1 = 200 k 2 = 800 k 3 = 1600 k
lcd_r_fastld[1:0]	11	0	0	Selects the resistor for fast charging the LCD pixels 0 = 15 k 1 = 200 k 2 = 800 k 3 = 1600 k
lcd_segment[23:0]	13	h000000	h000000	Display segments digits 2 to 0
lcd_segment[47:24]	14	h000000	h000000	Display segments digits 5 to 3
lcd_segment[55:48]	15	h000000	h000000	Display segments special characters (1/3 and 1/4 duty)
lcd_standby	11	0	0	0 = LCD active 1 = LCD voltage supply in stand-by
lcd_swload1k	11	1	1	LCD driver's voltage doubler uses 1 kOhm instead of 200 Ohm to charge capacitor
lcd_vlt[1:0]	11	1	1	LCD voltage 0 = 2 V 1 = 2.5 V 2 = 3 V 3 = 2 V without pump
low_batt[2:0]	1	0	0	Sets the voltage level for low battery detection and EEpromwrite 2.2 V, 2.3 V, 2.4 V to 2.9 V (2.2 V + 0.1 V * low_batt)
messb2	1	0	0	1 = Set TDC Measurement range 2
mfake[1:0]	3	0	0	Sets the number of fake measurements
Special internal bits	*3*	*0*	*1*	*Use recommended value*
mod_rspan	1	0	0	1 = Enable internal multiplication of gain compensation resistor Rspan

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Configuration Value	Register	Recomm. Default	Hardware Default	Description
mult_en_pp	1	0	0	1 = Enable multiplications in gain correction
mult_en_ub	1	0	0	1 = Enable multiplications for supply voltage correction
Mult_Hb1[23:0]	4	h100000	h100000	Multiplication factor for HB1 result h1 := h1 * [-2^23 to 2^23-1]/ 2^20
Mult_Hb2[23:0]	5	h100000	h100000	Multiplication factor for HB2 result h1 := h1 * [-2^23 to 2^23-1]/ 2^20
Mult_Hb3[23:0]	6	h100000	h100000	Multiplication factor for HB3 result h1 := h1 * [-2^23 to 2^23-1]/ 2^20
Mult_Hb4[23:0]	7	h100000	h100000	Multiplication factor for HB4 result h1 := h1 * [-2^23 to 2^23-1]/ 2^20
multio_sel[3:0]	*16*	*12*	*0*	*Use multio03 pin for diagnoses* *0 = multio* *1 = clk10khz* *2 = clkalu* *3 = load* *4 = epr_acc* *5 = portin_or* *6 = eprom read access* *7 = testo_tdc* *8 = phaseschifter out* *9 = start_stop* *10 = sense_ac1_comp2* *11 = sense_schmitt_trigger* *12 = interrupt*
High Resolution	*16*	*1*	*1*	*Switch high resolution, cannot be used with 1.5V Power Supply*
Mult_PP[7:0]	10	h80	h80	Multiplication factor for gain correction g := g * [0 to 255]/2^7
Mult_TkG[23:0]	8	h100000	h100000	Amplification for Rspan correction Rs := Rs * [-2^23 to 2^23-1]/ 2^20
Mult_TkO[23:0]	9	h000000	h000000	Offset value for Rspan, directly substracted
Mult_Ub[7:0]	10	h00	h80	Multiplication factor for gain compensation by means of voltage measurement hb = hb/(1 + ub*[-128 to 127]/2^21)
Special internal bit	*3*	*0*	*0*	*Use default*
osz10khz_fsos[5:0]	*0*	*h20*	*h20*	*Frequency trim of 10 kHz oscillator*
portpat	*2*	*1*	*0*	*Switch port patterns. 'On' stronly recommended*
pptemp	*2*	*0*	*0*	*Enable gain error and temperature measurement*
Special internal bit	*3*	*0*	*0*	*Use default*
ps_qziel[5:0]	*3*	*33*	*17*	*Use recommended value*
Special internal bit	*3*	*0*	*0*	*Use default*
Special internal bit	*16*	*0*	*0*	*Use default*
rspan_by_temp	1	0	0	Use temperature measurement instead of Rspan for temperature compensation
Special internal bit	*16*	*0*	*0*	*Use default*
sel_compint	11	0	0	1 = Select internal comparator

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Configuration Value	Register	Recomm. Default	Hardware Default	Description
sel_compr	0	0	0	Selects comparator working resistor 00 = 10k 01 = 10k 10 = 7k 11 = 4.1k
Special internal bit	*16*	*2*	*2*	*Use default*
Special internal bit	*16*	*0*	*0*	*Use default*
sel_start_osz[2:0]	3	0	0	Sets delay from start of 4 MHz oscillator to start of measurement 0 = off 1 = continuously on 2 = 100 µs 3 = 200 µs 4 = 300 µs 5 = 400 µs 6 & 7 are not connected
sense_discharge	16	1	0	Set fast discharge of comparator's low-pass capacitor
single_conversion	2	0	0	0 = Continuous mode 1 = Single conversion mode
speed_talu	*1*	*0*	*0*	*Use default*
stop_osz	3	0	0	Stop the oszillator by command (e.g. if there is no interrupt after AutoOn)
stretch	3	0	0	Select stretched mode 0 = off 1 = single R measurement 2 = 2xR (halfbridge), 200 µs delay 3 = 2xR (halfbridge), 300 µs delay
tdc_conv_cnt[7:0]	0	0	0	Single conversion timer based on 10 kHz/64 = 156.25 Hz
tdc_sleepmode	1	25	25	Mode without TDC or strain gage measurement, to be used for scanning buttons in case the scale is off, same as avrate=0

3.4.2 Result Registers

Content of the RAM result registers at the end of a measurement:

ram=16	: HB1=(A-B) / (A+B)	HB1 un-compensated
ram=17	: HB2=(C-D) / (C+D)	HB2 un-compensated
ram=18	: HB3=(E-F) / (E+F)	HB3 un-compensated
ram=19	: HB4=(G-H) / (G+H)	HB4 un-compensated
ram=20	: HB0=(A-B)+(..)/(A+B)+(..)	HB0 compensated sum
ram=21	: TMP=(p1-p2) / p2	Temperature
ram=22	: Status	
ram=23	: HB1+	Time measurement TDC at SG_A1, Pin11
ram=24	: CAL	Resolution TDC
ram=25	: UBATT	Measured supply voltage
ram=26-31	: NC	Free, can be used temporarily, will be overwritten during measurement
x-Akku	: HB0	Value of ram=20
y-Akku	: Temp	Value of ram=21
z-Akku	: Flags	Value of ram=63
ramadr	: 0	Value of RAM address pointer

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Descriptions:

A : Discharge time measurement at SG_A1
B : Discharge time measurement at SG_A2
C : Discharge time measurement at SG_B1
D : Discharge time measurement at SG_B2
E : Discharge time measurement at SG_C1
F : Discharge time measurement at SG_C2
G : Discharge time measurement at SG_D1
H : Discharge time measurement at SG_D2
P1: Discharge time measurement at TMP_1
P2: Discharge time measurement at TMP_2

Formats:

HB1: Result in 100 ppm, HB1/100 = result in ppm
HB2: Result in 100 ppm, HB2/100 = result in ppm
HB3: Result in 100 ppm, HB3/100 = result in ppm
HB4: Result in 100 ppm, HB4/100 = result in ppm
HB0: Result in 100 ppm, HB0/100 = result in ppm
TMP: Result(Tmp) = TMP/(1<<24)
Status: See below
HB1+: Result (HB1+)/ns = 250 * HB1+ /(1<<14) [4MHz clock]
CAL: Result (Cal)/ps = 250000 / CAL [4MHz clock]
UBATT: Result (UBATT)/V = 2.0+1.6*UBATT/64

HB1,HB2,HB3,HB4,HB0,TMP are given as two's complement. MSB = 1 indicates a negative value. To get the possitive value calculate h1000000000000-X.

3.4.3 Status Register

Table 4

Bit	Description
Status[23]= flg_io3_mio	Pin29
Status[22]= flg_io2_sck	Pin22
Status[21]= flg_io1_sdi	Pin21
Status[20]= flg_io0_sdo	Pin20
Status[19]= flg_rstpwr	1 = Power-on reset caused jump into EEPROM
Status[18]= flg_rstssn	1 = Pushed button caused jump into EEPROM
Status[17]= flg_wdtalt	1 = Watchdog interrupt caused jump into EEPROM
Status[16]= flg_endavg	1 = End of measurement caused jump into EEPROM
Status[15]= flg_intav0	1 = Jump into EEPROM in sleep mode
Status[14]= flg_ub_low	1 = Low voltage
Status[13]= flg_errtdc	1 = TDC error
Status[12]= flg_pslock[1]	1 = Phase shifter locked
Status[11]= flg_pslock[0]	1 = Phase shifter locked
Status[10]= flg_errprt	1 = Error at strain gauge ports
Status[09]= flg_timout	1 = Timeout TDC
Status[08]= 1'bx	1 = not used
Status[07]= flg_io3_mio_r	1 = Rising edge at Pin29, 0 = no edge
Status[06]= flg_io2_sck_r	1 = Rising edge at Pin22, 0 = no edge
Status[05]= flg_io1_sdi_r	1 = Rising edge at Pin21, 0 = no edge
Status[04]= flg_io0_sdo_r	1 = Rising edge at Pin20, 0 = no edge
Status[03]= flg_io3_mio_f	1 = Falling edge at Pin29, 0 = no edge
Status[02]= flg_io2_sck_f	1 = Falling edge at Pin22, 0 = no edge
Status[01]= flg_io1_sdi_f	1 = Falling edge at Pin21, 0 = no edge
Status[00]= flg_io0_sdo_f	1 = Falling edge at Pin20, 0 = no edge

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3.5 Instruction Set

The complete instruction set of the PSØ8 consists of 94 core instructions that have unique op-code decoded by the CPU. Further there are emulated instructions like no2lcd that are replaced automatically by the assembler and call a subroutines in the ROM code.

The variety of the instruction set allows to write comprehensive programs that cope with the 1 K size of the EEPROM.

Branch instructions:
There are 3 principles of jumping within the code:
- Jump. Absolute addressing with 12 Bit within the whole address space.
- Branch. Relative to the actual address with 8 Bit in the range of –128 to +127 bit addresses.
- Skip. jump ahead up to 3 op-codes (3 to 15 bytes).

The assembler puts together jump and branch into new code goto.
It is possible to jump into subroutines only by means of absolute jumps and without any condition.

Arithmetic operations:
The RAM is organized in 24 Bit words. All instructions are based on two's complement operations. A arithmetic command combines two accumulators and writes back the result into the first mentioned accumulator. The ram address pointer shows the RAM address that is handled in the same way as an accumulator. Each operation on the accumulator Affects the four flags. The flags refer to the last operation.

Table 5

Simple Arithmetic	Complex Arithmetic	Shift & Rotate	RAM access
abs	div24	clrC	clear
add	divmod	rotl	decramadr
compare	mult24	rotR	incramadr
compl	mult48	setC	move
decr		shiftL	ramadr
getflag		shiftR	swap
incr			
sign			
sub			

Logic	Bitwise	LCD display	EEPROM access
and	bitclr	dez2lcd	equal
eor	bitinv	newlcd	getepr
nor	bitset	no2lcd	putepr
invert		setLCD	
nand		clrLCD	
nor			
or			

Unconditional jump		Miscellaneous
goto	skip	clk10kHz
gotoBitC	skipBitC	clrwdt
gotoBitS	skipBitS	initTDC
gotoCarC	skipCarC	newcyc
gotoCarS	skipCarS	nop
gotoEQ	skipEQ	stop
gotoNE	skipNE	initAvg
gotoNeg	skipNeg	rollAvg
gotoOvrC	skipOvrC	
gotoOvrS	skipOvrS	
gotoPos	skipPos	
jsub		
jsubret		

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abs	**Absolute value of register**
Syntax:	abs p1
Parameters:	p1 = ACCU [x,y,z,r]
Calculus:	p1 := | p1 |
Flags affected:	C O S Z
Bytes:	2
Cycles:	2
Description:	Absolute value of register
Category:	Simple arithmetics

add	**Addition**
Syntax:	add p1,p2
Parameters:	p1 = ACCU [x,y,z,r] p2 = ACCU [x,y,z,r] or 24-Bit number
Calculus:	p1 := p1 + p2
Flags affected:	C O S Z
Bytes:	2 (p2 = ACCU) 4 (p2 = number)
Cycles:	2 (p2 = ACCU) 4 (p2 = number)
Description:	Addition of two registers or addition of a constant to a register
Category:	Simple arithmetic

and	**Logic AND**
Syntax:	and p1,p2
Parameters:	p1 = ACCU [x,y,z,r] p2 = ACCU [x,y,z,r] or 24-Bit number
Calculus:	p1 := p1 AND p2
Flags affected:	S Z
Bytes:	2 (p2 = ACCU) 5 (p2 = number)
Cycles:	3 (p2 = ACCU) 6 (p2 = number)
Description:	Logic AND of 2 registers or Logic AND of register and constant
Category:	Logic

bitclr	**Clear single bit**
Syntax:	bitclr p1,p2
Parameters:	p1 = ACCU [x,y,z,r] p2 = number 0 to 23
Calculus:	p1:=p1 and not (1<<p2)
Flags affected:	S Z
Bytes:	2
Cycles:	2
Description:	Clear a single bit in the destination register
Category:	Bitwise

bitinv	**Invert single bit**
Syntax:	bitinv p1,p2
Parameters:	p1 = ACCU [x,y,z,r] p2 = number 0 to 23
Calculus:	p1:=p1 eor (1<<p2)
Flags affected:	S Z
Bytes:	2
Cycles:	2
Description:	Invert a single bit in the destination register
Category:	Bitwise

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bitset	**Set single bit**
Syntax:	bitset p1,p2
Parameters:	p1 = ACCU [x,y,z,r] p2 = number 0 to 23
Calculus:	p1:=p1 or (1<<p2)
Flags affected:	S Z
Bytes:	2
Cycles:	2
Description:	Set a single bit in the destination register
Category:	Bitwise

clear	**Clear register**
Syntax:	clear p1
Parameters:	p1 = ACCU [x,y,z,r]
Calculus:	p1 := 0
Flags affected:	S Z
Bytes:	1
Cycles:	1
Description:	Clear addressed register to 0
Category:	RAM access

clk10khz	**Clock source 10 kHz**
Syntax:	clk10khz p1
Parameters:	p1 = number 0 or 1
Calculus:	-
Flags affected:	-
Bytes:	2
Cycles:	3
Description:	Change clock source of processor to 10 kHz. The clock of the processor is switched to the slower 10 kHz clock instead of the 40 MHz. The 10 kHz clock is still stable to variations in temperature and supply voltage. If p1 is set to 1 the 10 kHz clock is on, if p1 == 0 the 10 kHz clock is off.
Category:	Miscellaneous

clrC	**Clear flags**
Syntax:	clrC
Parameters:	-
Calculus:	-
Flags affected:	C O
Bytes:	1
Cycles:	1
Description:	Clear Carry and Overflow flags
Category:	Shift and Rotate

clrLCD	**Clear LCD**
Syntax:	clrLCD
Parameters:	-
Calculus:	-
Flags affected:	-
Bytes:	1
Cycles:	Subroutine call
Description:	Clear LCD registers 61 & 62. Use this opcode in combination with 'newlcd' to switch off all LCD segments. In real a subroutine in the ROM code is called. The assembler converts this command to the corresponding jump command.
Category:	LCD Display

clrwdt	**Clear watchdog**
Syntax:	clrwdt
Parameters:	-
Calculus:	-
Flags affected:	-
Bytes:	2
Cycles:	

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Description:	Clear watchdog. This opcode is used to clear the watchdog at the end of a program run. Apply this opcode right before 'stop'.
Category:	Miscellaneous

Compare	**Compare two values**
Syntax:	compare p1,p2
Parameters:	p1 = ACCU [x,y,z,r] p2 = ACCU [x,y,z,r] or 24-Bit number
Calculus:	---:=p2-p1 only the flags are changed but not the registers
Flags affected:	C O S Z
Bytes:	1 (p1=ACCU, p2=ACCU) 4 (p1=ACCU, p2=NUMBER)
Cycles:	1 (p1=ACCU, p2=ACCU) 4 (p1=ACCU, p2=NUMBER)
Description:	Compare of 2 registers by subtraction Compare of a constant with a register by subtraction The flags are changed according to the subtraction result, but not the registers contents themselves
Category:	Simple arithmetic

compl	**Complement**
Syntax:	compl p1
Parameters:	p1 = ACCU [x,y,z,r]
Calculus:	p1 := - p1 = not p1 + 1
Flags affected:	S Z
Bytes:	2
Cycles:	2
Description:	two's complement of register
Category:	Simple arithmetic

decr	**Decrement**
Syntax:	decr p1
Parameters:	p1 = ACCU [x,y,z,r]
Calculus:	p1 := p1 – 1
Flags affected:	C O S Z
Bytes:	1
Cycles:	1
Description:	Decrement register
Category:	Simple arithmetic

decramadr	**Decrement RAM address pointer**
Syntax:	decramadr
Parameters:	-
Calculus:	-
Flags affected:	-
Bytes:	1
Cycles:	1
Description:	Decrement RAM address pointer by one
Category:	Ram Access

dez2lcd	**Decimal to segment code**
Syntax:	dez2lcd p1
Parameters:	p1 = ACCU [x,y,z,r]
Calculus:	-
Flags affected:	-
Bytes:	2
Cycles:	3
Description:	Converts decimal code in register p1 to 7 segment code. A decimal number from 0 to 9 of the addressed register p1 is converted to standard 7 segment code (digits a-h). This opcode may be used for advanced LCD conversions routines, where opcode no2lcd is not sufficient dec hgfe dcba 0 --> 0b00111111=0x3F 1 --> 0b00000110=0x06

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	2 --> 0b00111011=0x3B 3 --> 0b01001111=0x4F 4 --> 0b01100110=0x66 5 --> 0b01101101=0x6D 6 --> 0b01111101=0x7D 7 --> 0b00000111=0x07 8 --> 0b01111111=0x7F 9 --> 0b01101111=0x6F
Category:	LCD Display

div24	**Signed division 24 Bit**
Syntax:	div24 p1,p2
Parameters:	p1 = ACCU [x,y,z,r] p2 = ACCU [x,y,z,r]
Calculus:	p1 := (p1 << 24) / p2 (if |p1| < |p2/2|)
Flags affected:	S & Z of p1
Bytes:	2
Cycles:	20
Description:	Signed division of 2 registers 24 bits of the division of 2 registers, result is assigned to p1
Category:	Complex arithmetic

divmod	**Signed modulo division**
Syntax:	divmod p1,p2
Parameters:	p1 = ACCU [x,y,z,r] p2 = ACCU [x,y,z,r]
Calculus:	p1 := p1 / p2 and p2 := p1 % p2
Flags affected:	S Z
Bytes:	2
Cycles:	
Description:	Signed modulo division of 2 registers 24 higher bits of the division of 2 registers, result is assigned to p1 the rest is placed to p2
Category:	Complex arithmetic

eor	**Exclusive OR**
Syntax:	eor p1,p2
Parameters:	p1 = ACCU [x,y,z,r] p2 = ACCU [x,y,z,r] or 24-Bit number
Calculus:	p1 := p1 xor p2 bit combination 0 / 0 and 1 / 1 returns 0 bit combination 0 / 1and 1 / 0 returns 1
Flags affected:	S Z
Bytes:	2 (p1=ACCU, p2=ACCU) 5 (p1=ACCU, p2=NUMBER)
Cycles:	3 (p1=ACCU, p2=ACCU) 6 (p1=ACCU, p2=NUMBER)
Description:	Logic XOR (exclusive OR, antivalence) of the 2 given registers Logic XOR (exclusive OR, antivalence) of register with constant
Category:	Logic

eorn	**Exclusive NOR**
Syntax:	eorn p1,p2
Parameters:	p1 = ACCU [x,y,z,r] p2 = ACCU [x,y,z,r] or 24-Bit number
Calculus:	p1 := p1 xnor p2 bit combination 0 / 0 and 1 / 1 return 1 bit combination 0 / 1 and 1 / 0 return 0
Flags affected:	S Z
Bytes:	2 (p1=ACCU, p2=ACCU) 5 (p1=ACCU, p2=NUMBER)
Cycles:	3 (p1=ACCU, p2=ACCU) 6 (p1=ACCU, p2=NUMBER)
Description:	Logic XNOR (exclusive NOR, equivalence) of the 2 given registers Logic XNOR (exclusive NOR, equivalence) of register with constant

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Category:	Logic

equal	**Write 3 Bytes to EEPROM**
Syntax:	equal p1
Parameters:	p1 = 24-Bit number
Calculus:	-
Flags affected:	-
Bytes:	3
Cycles:	
Description:	Write 3 bytes (p1) to configuration register of EEPROM. The equal opcode is used to write 3 bytes of configuration data directly to an EEPROM register. Therefore the opcode is simply used 16 times in the beginning of the assembler listing, fed with the configuration data given through p1. Like 'putepr' the configuration of the EEPROM is done in the lower area from byte 0..47, combined in 16x 24bit registers. From byte 48 upwards, the user code is written to the EEPROM. Use this opcode to provide your own configuration instead of the standard configuration.
Category:	EEPROM access

getepr	**Get EEPROM content**
Syntax:	getepr p1
Parameters:	p1 = ACCU [x,y,z,r]
Calculus:	p1 := EEPROM register content (addressed by RAM address pointer)
Flags affected:	S Z
Bytes:	1
Cycles:	6
Description:	Get EEPROM into register. The addressed register p1 gets the EEPROM register content which is addressed by the RAM address pointer. This opcode needs temporarily a place in the program counter stack (explanation see below).
Category:	EEPROM Access

getflag	**Set S and Z flags**
Syntax:	getflag p1
Parameters:	p1 = ACCU [x,y,z,r]
Calculus:	signum := set if p1 < 0 notequalzero := set if p1 <> 0
Flags affected:	S Z
Bytes:	1
Cycles:	1
Description:	Set the signum and notequalzero flag according to the addressed register, content of the register is not affected
Category:	Simple arithmetic

goto	**Jump without condition**
Syntax:	goto p1
Parameters:	p1 = JUMPLABEL
Calculus:	PC:= p1
Flags affected:	-
Bytes:	2 (relative jump) 3 (absolute jump)
Cycles:	3 (relative jump) 4 (absolute jump)
Description:	Jump without condition. Program counter is set to target address. The target address is given by using a jump label. See examples section for how to introduce a jump label.
Category:	Unconditional jump

gotoBitC	**Jump on bit clear**
Syntax:	gotoBitC p1, p2, p3
Parameters:	p1 = ACCU [x,y,z,r] p2 = NUMBER [0..23] p3 = JUMPLABEL
Calculus:	if (bit p2 of register p1 == 0) PC := p3
Flags affected:	-

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Bytes:	3
Cycles:	4
Description:	Jump on bit clear. Program counter will be set to target address if selected bit in register p1 is clear. The target address is given by using a jump label. See examples section for how to introduce a jump label.
Category:	Bitwise

gotoBitS	**Jump on bit set**
Syntax:	gotoBitS p1, p2, p3
Parameters:	p1 = ACCU [x,y,z,r] p2 = NUMBER [0..23] p3 = JUMPLABEL
Calculus:	if (bit p2 of register p1 == 1) PC := p3
Flags affected:	-
Bytes:	3
Cycles:	4
Description:	Jump on bit set. Program counter will be set to target address if selected bit in register p1 is set. The target address is given by using a jump label. See examples section for how to introduce a jump label.
Category:	Bitwise

gotoCarC	**Jump on carry clear**
Syntax:	gotoCarC p1
Parameters:	p1 = JUMPLABEL
Calculus:	if (carry == 0) PC := p1
Flags affected:	-
Bytes:	2 (relative jump) 3 (absolute jump)
Cycles:	3 (relative jump) 4 (absolute jump)
Description:	Jump on carry clear. Program counter will be set to target address if carry is clear. The target address is given by using a jump label. See examples section for how to introduce a jump label.
Category:	Goto on flag

gotoCarS	**Jump on carry set**
Syntax:	gotoCarS p1
Parameters:	p1 = JUMPLABEL
Calculus:	if (carry == 1) PC := p1
Flags affected:	-
Bytes:	2 (relative jump) 3 (absolute jump)
Cycles:	3 (relative jump) 4 (absolute jump)
Description:	Jump on carry set. Program counter will be set to target address if carry is set. The target address is given by using a jump label. See examples section for how to introduce a jump label.
Category:	Goto on flag

gotoEQ	**Jump on equal zero**
Syntax:	gotoEQ p1
Parameters:	p1 = JUMPLABEL
Calculus:	if (Z == 0) PC := p1
Flags affected:	-
Bytes:	2 (relative jump) 3 (absolute jump)
Cycles:	3 (relative jump) 4 (absolute jump)
Description:	Jump on equal zero. Program counter will be set to target address if the foregoing result is equal to zero. The target address is given by using a jump label. See examples section for how to introduce a jump label.
Category:	Goto on flag

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gotoNE	**Jump on not equal zero**
Syntax:	gotoNE p1
Parameters:	p1 = JUMPLABEL
Calculus:	if (Z == 1) PC := p1
Flags affected:	-
Bytes:	2 (relative jump) 3 (absolute jump)
Cycles:	3 (relative jump) 4 (absolute jump)
Description:	Jump on not equal zero. Program counter will be set to target address if the foregoing result is not equal to zero. The target address is given by using a jump label. See examples section for how to introduce a jump label.
Category:	Goto on flag

gotoNeg	**Jump on negative**
Syntax:	gotoNeg p1
Parameters:	p1 = JUMPLABEL
Calculus:	if (S == 1) PC := p1
Flags affected:	-
Bytes:	2 (relative jump) 3 (absolute jump)
Cycles:	3 (relative jump) 4 (absolute jump)
Description:	Jump on negative. Program counter will be set to target address if the foregoing result is negative. The target address is given by using a jump label. See examples section for how to introduce a jump label.
Category:	Goto on flag

gotoOvrC	**Jump on overflow clear**
Syntax:	gotoOvrC p1
Parameters:	p1 = JUMPLABEL
Calculus:	if (O == 0) PC := p1
Flags affected:	-
Bytes:	2 (relative jump) 3 (absolute jump)
Cycles:	3 (relative jump) 4 (absolute jump)
Description:	Jump on overflow clear. Program counter will be set to target address if the overflow flag of the foregoing operation is clear. The target address is given by using a jump label. See examples section for how to introduce a jump label.
Category:	Goto on flag

gotoOvrS	**Jump on overflow set**
Syntax:	gotoOvrS p1
Parameters:	p1 = JUMPLABEL
Calculus:	if (O == 1) PC := p1
Flags affected:	-
Bytes:	2 (relative jump) 3 (absolute jump)
Cycles:	3 (relative jump) 4 (absolute jump)
Description:	Jump on overflow set. Program counter will be set to target address if the overflow flag of the foregoing operation is set. The target address is given by using a jump label. See examples section for how to introduce a jump label.
Category:	Goto on flag

gotoPos	**Jump on positive**
Syntax:	gotoPos p1
Parameters:	p1 = JUMPLABEL
Calculus:	if (S == 0) PC := p1
Flags affected:	-
Bytes:	2 (relative jump)

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	3 (absolute jump)
Cycles:	3 (relative jump) 4 (absolute jump)
Description:	Jump on positive. Program counter will be set to target address if the foregoing result is positive. The target address is given by using a jump label. See examples section for how to introduce a jump label.
Category:	Goto on flag

incr	**Increment**
Syntax:	incr p1
Parameters:	p1 = ACCU [x,y,z,r]
Calculus:	p1 := p1 + 1
Flags affected:	C O S Z
Bytes:	1
Cycles:	1
Description:	Increment register
Category:	Simple arithmetic

incramadr	**Increment RAM address**
Syntax:	incramadr
Parameters:	-
Calculus:	-
Flags affected:	-
Bytes:	1
Cycles:	1
Description:	Increment RAM address pointer by 1
Category:	RAM access

initAvg	**Initialize rolling average**
Syntax:	initAvg p1,p2
Parameters:	p1 = ACCU[x] p2 = number from 3 to 17
Calculus:	-
Flags affected:	-
Bytes:	2
Cycles:	Subroutine call
Description:	Initialization of the rolling average subroutine. p1 sets the default value for the calculus. p2 defines the number of data points for the rolling average. In real a subroutine in the ROM code is called. The assembler converts this command to the corresponding jump command.
Category:	Miscellaneous

initTDC	**Initialize TDC**
Syntax:	initTDC
Parameters:	-
Calculus:	-
Flags affected:	-
Bytes:	2
Cycles:	3
Description:	Initialization reset of the TDC (time-to-digital converter). Should be sent after configuration of registers. The initTDC preserves all configurations .
Category:	Miscellaneous

invert	**Bitwise inversion**
Syntax:	invert p1
Parameters:	p1 = ACCU [x,y,z,r]
Calculus:	p1 := not p1
Flags affected:	S Z
Bytes:	2
Cycles:	2
Description:	Bitwise inversion of register
Category:	Logic

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jsub	**Unconditional jump**
Syntax:	jsub p1
Parameters:	p1 = JUMPLABEL
Calculus:	PC := p1
Flags affected:	C O S Z
Bytes:	3
Cycles:	4
Description:	Jump to subroutine without condition. The program counter is loaded by the address given through the jump label. The subroutine is processed until the keyword 'jsubret' occurs. Then a jump back is performed and the next command after the jsub-call is executed. This opcode needs temporarily a place in the program counter stack (explanation see below).
Category:	Unconditional Jump

jsubret	**Return from subroutine**
Syntax:	jsubret
Parameters:	-
Calculus:	PC := PC from jsub-call
Flags affected:	-
Bytes:	1
Cycles:	3
Description:	Return from subroutine. A subroutine can be called via 'jsub' and exited by using jsubret. The program is continued at the next command following the jsub-call. You have to close a subroutine with jsubret - otherwise there will be no jump back.
Category:	Unconditional Jump

move	**Move**
Syntax:	move p1,p2
Parameters:	p1 = ACCU [x,y,z,r] p2 = ACCU [x,y,z,r] or 24-bit number
Calculus:	p1 := p2
Flags affected:	S Z
Bytes:	1 (p1=ACCU, p2=ACCU) 4 (p1=ACCU, p2=NUMBER)
Cycles:	1 (p1=ACCU, p2=ACCU) 4 (p1=ACCU, p2=NUMBER)
Description:	Move content of p2 to p1 (p1=ACCU, p2=ACCU) Move constant to p1 (p1=ACCU, p2=NUMBER)
Category:	RAM access

mult24	**Signed 24-Bit multiplication**
Syntax:	mult24 p1,p2
Parameters:	p1 = ACCU [x,y,z,r] p2 = ACCU [x,y,z,r]
Calculus:	p1 := (p1 * p2) >> 24
Flags affected:	S & Z of p1
Bytes:	2
Cycles:	30
Description:	Signed multiplication of 2 registers like mult48, but only the 24 higher bits of the multiplication of 2 registers, result is stored in p1
Category:	Complex arithmetic

mult48	**Signed 48-Bit multiplication**
Syntax:	mult48 p1,p2
Parameters:	p1 = ACCU [x,y,z,r] p2 = ACCU [x,y,z,r]
Calculus:	p1,p2 := p1 * p2
Flags affected:	S & Z of p1
Bytes:	2
Cycles:	30
Description:	Signed multiplication of 2 registers

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	Higher 24 bits of the multiplication is placed to p1 Lower 24 bits of the multiplication is placed to p2
Category:	Complex arithmetic

nand	**Logic NAND**
Syntax:	nand p1,p2
Parameters:	p1 = ACCU [x,y,z,r] p1 = ACCU [x,y,z,r] or 24-Bit number
Calculus:	p1 := p1 nand p2 returns only 0 in case of bit combination 1 / 1
Flags affected:	S Z
Bytes:	2 (p1=ACCU, p2=ACCU) 5 (p1=ACCU, p2=NUMBER)
Cycles:	3 (p1=ACCU, p2=ACCU) 6 (p1=ACCU, p2=NUMBER)
Description:	Logic NAND (negated AND) of the 2 given registers Logic NAND (negated AND) of register with constant
Category:	Logic

newcyc	**Start TDC**
Syntax:	newcyc
Parameters:	-
Calculus:	-
Flags affected:	-
Bytes:	2
Cycles:	3
Description:	Start of TDC. This opcode can be used after configuration and initialization of the PSØ8 to start a new measurement cycle. Normally this is done by the PSØ8 ROM routines itself, but in case of custom-designed reset procedures this opcode can play a role.
Category:	Miscellaneous

newlcd	**Load new LCD data**
Syntax:	newlcd
Parameters:	-
Calculus:	-
Flags affected:	-
Bytes:	2
Cycles:	3
Description:	Load new LCD data. New segment data from register 61-63 is written to the LCD driver. Refreshes the display.
Category:	LCD display

no2lcd	**Covert 6 digits to LCD code**
Syntax:	no2lcd p1,p2
Parameters:	p1 = ACCU[x] p2 = number 1 to 6
Calculus:	-
Flags affected:	-
Bytes:	3
Cycles:	subroutine call
Description:	Converts the 6 digits of the decimal number in register x into 7-segment code. The position of the decimal point is determined with p2. Leading zeros before the decimal point are cleared. The conversion result is directly written to the LCD register 61-62 Use this opcode in combination with 'newlcd'. In real a subroutine in the ROM code is called. The assembler converts this command to the corresponding jump command.
Category:	LCD display

nop	**No operation**
Syntax:	-
Parameters:	-
Calculus:	-

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Flags affected:	-
Bytes:	1
Cycles:	1
Description:	Placeholder code or timing adjust (no function)
Category:	Miscellaneous

nor	**Logic NOR**
Syntax:	nor p1,p2
Parameters:	p1 = ACCU [x,y,z,r] p2 = ACCU [x,y,z,r] or 24-Bit number
Calculus:	p1 := p1 nor p2 returns only 1 in case of bit combination 0 / 0
Flags affected:	S Z
Bytes:	2 (p1=ACCU, p2=ACCU) 5 (p1=ACCU, p2=NUMBER)
Cycles:	3 (p1=ACCU, p2=ACCU) 6 (p1=ACCU, p2=NUMBER)
Description:	Logic NOR (negated OR) of the 2 given registers Logic NOR (negated OR) of register with constant
Category:	Logic

or	**Logic OR**
Syntax:	or p1,p2
Parameters:	p1 = ACCU [x,y,z,r] p2 = ACCU [x,y,z,r] or 24-Bit number
Calculus:	p1 := p1 or p2 returns only 0 in case of bit combination 0 / 0
Flags affected:	S Z
Bytes:	2 (p1=ACCU, p2=ACCU) 5 (p1=ACCU, p2=NUMBER)
Cycles:	3 (p1=ACCU, p2=ACCU) 6 (p1=ACCU, p2=NUMBER)
Description:	Logic OR of the 2 given registers Logic OR of register with constant
Category:	Logic

putepr	**Put register to EEPROM**
Syntax:	putepr p1
Parameters:	p1 = ACCU [x,y,z,r]
Calculus:	EEPROM register (addressed by RAM address pointer) := p1
Flags affected:	-
Bytes:	4
Cycles:	65536 = ~50ms
Description:	Put register into EEPROM. The content of the addressed register p1 is moved to the EEPROM (the EEPROM register address is set by the RAM address pointer). Only EEPROM register 14 and 15 are accessible via 'putepr'. This opcode needs temporarily a place in the program counter stack (explanation see below). 'putepr' should not be combined with the skip-opcodes due to the long execution time of this opcode (approx.: 50ms)
Category:	EEPROM access

ramadr	**Set RAM address pointer**
Syntax:	ramadr p1
Parameters:	p1 = 5-Bit number
Calculus:	-
Flags affected:	-
Bytes:	1
Cycles:	1
Description:	Set pointer to RAM address (range: 0..65)
Category:	RAM access

rollAvg	**Calculate rolling average**
Syntax:	rollAvg p1,p2
Parameters:	p1 = ACCU[x]

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	p2 = number from 3 to 17
Calculus:	ACCU[y] = ACCU[x] old p1 = rolling average result
Flags affected:	-
Bytes:	2
Cycles:	Subroutine call
Description:	Feeds p1 as new value into the rolling average subroutine. p2 defines the number of data points for the rolling average. The value falling out of the rolling average is stored on RAM address 13. The result is stored in the x ACCU. The previous result is stored in the y ACCU. In real a subroutine in the ROM code is called. The assembler converts this command to the corresponding jump command.
Category:	Miscellaneous

rotL	**Rotate left**
Syntax:	rotL p1[,p2]
Parameters:	p1 = ACCU [x,y,z,r] p2 = 4-Bit number or none
Calculus:	p1 := p1<< 1+ carry; carry:=MSB(x) (in case rotL p1, without p2) p1 := repeat (p2) rotL p1 (in case rotL p1,p2)
Flags affected:	C O S Z (of the last step)
Bytes:	1 (p1=ACCU, p2=none) 2 (p1=ACCU, p2=NUMBER)
Cycles:	1 (p1=ACCU, p2=none) 1+p2 (p1=ACCU, p2=NUMBER)
Description:	Rotate p1 left --> shift p1 register to the left, fill LSB with carry, MSB is placed in carry register Rotate p1 left p2 times with carry --> shift p1 register p2 times to the left, in each step fill LSB with the carry and place the MSB in the carry
Category:	Shift and rotate

rotR	**Rotate right**
Syntax:	rotR p1[,p2]
Parameters:	p1 = ACCU [x,y,z,r] p2 = 4-Bit number or none
Calculus:	p1 := p1>> 1+ carry; carry: =MSB(x) (in case rotR p1, without p2) p1 := repeat (p2) rotR p1 (in case rotR p1,p2)
Flags affected:	C O S Z (of the last step)
Bytes:	1 (p1=ACCU, p2=none) 2 (p1=ACCU, p2=NUMBER)
Cycles:	1 (p1=ACCU, p2=none) 1+p2 (p1=ACCU, p2=NUMBER)
Description:	Rotate p1 right --> shift p1 register to the right, fill MSB with carry, LSB is placed in carry register Rotate p1 right p2 times with carry --> shift p1 register p2 times to the right, in each step fill MSB with the carry and place the LSB in the carry
Category:	Shift and rotate

setC	**Set carry flag**
Syntax:	setC
Parameters:	-
Calculus:	-
Flags affected:	C O
Bytes:	1
Cycles:	1
Description:	Set carry flag and clear overflow flag
Category:	Shift and Rotate

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shiftL	**Shift Left**
Syntax:	shiftL p1,(p2)
Parameters:	p1 = ACCU [x,y,z,r] p2 = 4-Bit number or none
Calculus:	p1 := p1<< 1; carry :=MSB(x) (in case rotL p1, without p2) p1 := repeat (p2) shiftL p1 (in case rotL p1,p2)
Flags affected:	C O S Z
Bytes:	1 (p1=ACCU, p2=none) 2 (p1=ACCU, p2=NUMBER)
Cycles:	1 (p1=ACCU, p2=none) 1 + p2 (p1=ACCU, p2=NUMBER)
Description:	Shift p1 left --> shift p1 register to the left, fill LSB with 0, MSB is placed in carry register Shift p1 left p2 times --> shift p1 register p2 times to the left, in each step fill LSB with the 0 and place the MSB in the carry
Category:	Shift and rotate

setLCD	**Set LCD**
Syntax:	setLCD
Parameters:	-
Calculus:	-
Flags affected:	-
Bytes:	1
Cycles:	Subroutine call
Description:	Sets all LCD register 61 & 62 bits to 1. Use this opcode in combination with 'newlcd' for showing all LCD segments. In real a subroutine in the ROM code is called. The assembler converts this command to the corresponding jump command.
Category:	LCD Display

shiftR	**Shift right**
Syntax:	shiftR p1,(p2)
Parameters:	p1 = ACCU [x,y,z,r] p2 = 4-Bit number or none
Calculus:	p1 := p1>> 1; carry:=MSB(x) (in case rotL p1, without p2) p1 := repeat (p2) shiftL p1 (in case rotL p1,p2)
Flags affected:	C O S Z
Bytes:	1 (p1=ACCU, p2=none) 2 (p1=ACCU, p2=NUMBER)
Cycles:	1 (p1=ACCU, p2=none) 1 + p2 (p1=ACCU, p2=NUMBER)
Description:	Signed shift right of p1 --> shift p1 right, MSB is duplicated according to whether the number is positive or negative Signed shift p1 right p2 times --> shift p1 register p2 times to the right, MSB is duplicated according to whether the number is positive or negative
Category:	Shift and rotate

sign	**Sign**
Syntax:	sign p1
Parameters:	p1 = ACCU [x,y,z,r]
Calculus:	p1 := p1 / | p1 | p1 := 1 = 0x000001 if p1 >= 0 p1 := -1 = 0xFFFFFF if p1 < 0
Flags affected:	S Z
Bytes:	2
Cycles:	2
Description:	Sign of addressed register in complement of two notation. A positive value returns 1, a negative value returns -1 Zero is assumed to be positive
Category:	Simple arithmetic

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skip	**Skip**
Syntax:	skip p1
Parameters:	p1 = NUMBER [1,2,3]
Calculus:	PC := PC + bytes of next p1 lines
Flags affected:	
Bytes:	1
Cycles:	1 + skipped commands
Description:	Skip p1 without conditions
Category:	Unconditional jump

skipBitC	**Conditional skip**
Syntax:	skipBitC p1,p2,p3
Parameters:	p1 = ACCU [x,y,z,r] p2 = NUMBER[0..23] p2 = NUMBER[1,2,3]
Calculus:	if (bit p2 of register p1 == 0) PC := PC + bytes of next p3 lines
Flags affected:	-
Bytes:	1
Cycles:	1 + skipped commands
Description:	Skip p3 commands if bit p2 of register p1 is clear
Category:	Bitwise

skipBitS	**Conditional skip**
Syntax:	skipBitS p1,p2,p3
Parameters:	p1 = ACCU [x,y,z,r] p2 = NUMBER[0..23] p2 = NUMBER[1,2,3]
Calculus:	if (bit p2 of register p1 == 1) PC := PC + bytes of next p3 lines
Flags affected:	-
Bytes:	1
Cycles:	1 + skipped commands
Description:	Skip p3 commands if bit p2 of register p1 is set
Category:	Bitwise

skipCarC	**Skip carry clear**
Syntax:	skipCarC p1
Parameters:	p1 = NUMBER [1,2,3]
Calculus:	if (carry == 0) PC := PC + bytes of next p1 lines
Flags affected:	-
Bytes:	1
Cycles:	1 + skipped commands
Description:	Skip p1 commands if carry clear
Category:	Skip on flag

skipCarS	**Skip carry set**
Syntax:	skipCarS p1
Parameters:	p1 = NUMBER [1,2,3]
Calculus:	if (carry == 1) PC := PC + bytes of next p1 lines
Flags affected:	-
Bytes:	1
Cycles:	1 + skipped commands
Description:	Skip p1 commands if carry set
Category:	Skip on flag

skipEQ	**Skip on zero**
Syntax:	skipEQ p1
Parameters:	p1 = NUMBER[1,2,3]
Calculus:	if (notequalzero == 0) PC := PC + bytes of next p1 lines
Flags affected:	-

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Bytes:	1
Cycles:	1 + skipped commands
Description:	Skip p1 commands if result of previous operation is equal to zero
Category:	Skip on flag

skipNE	**Skip on non-zero**
Syntax:	skipNE p1
Parameters:	p1 = NUMBER[1,2,3]
Calculus:	if (notequalzero == 1) PC := PC + bytes of next p1 lines
Flags affected:	-
Bytes:	1
Cycles:	1 + skipped commands
Description:	Skip p1 commands if result of previous operation is not equal to zero
Category:	Skip on flag

skipNeg	**Skip on negative**
Syntax:	skipNeg p1
Parameters:	p1 = NUMBER[1,2,3]
Calculus:	if (signum == 1) PC := PC + bytes of next p1 lines
Flags affected:	-
Bytes:	1
Cycles:	1 + skipped commands
Description:	Skip p1 commands if result of previous operation was smaller than 0
Category:	Skip on flag

skipOvrC	**Skip on overflow**
Syntax:	skipOvrC p1
Parameters:	p1 = NUMBER[1,2,3]
Calculus:	if (overflow == 0) PC := PC + bytes of next p1 lines
Flags affected:	-
Bytes:	1
Cycles:	1 + skipped commands
Description:	Skip p1 commands if overflow is clear
Category:	Skip on flag

skipOvrS	**Skip on overflow**
Syntax:	skipOvrS p1
Parameters:	p1 = NUMBER[1,2,3]
Calculus:	if (overflow == 1) PC := PC + bytes of next p1 lines
Flags affected:	-
Bytes:	1
Cycles:	1 + skipped commands
Description:	Skip p1 commands if overflow is set
Category:	Skip on flag

skipPos	**Skip on positive**
Syntax:	skipPos p1
Parameters:	p1 = NUMBER[1,2,3]
Calculus:	if (signum == 0) PC := PC + bytes of next p1 lines
Flags affected:	-
Bytes:	1
Cycles:	1 + skipped commands
Description:	Skip p1 commands if result of previous operation was greater or equal to 0
Category:	Skip on flag

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stop	**Stop**
Syntax:	stop
Parameters:	-
Calculus:	-
Flags affected:	-
Bytes:	1
Cycles:	1
Description:	The DSP and clock generator are stopped, the converter and the EEPROM go to standby. A restart of the converter can be achieved by an external event like 'watchdog timer', 'external switch' or 'new strain measurement results'. Usually this opcode is the last command in the assembler listing.
Category:	Miscellaneous

sub	**Substraction**
Syntax:	sub p1,p2
Parameters:	p1 = NUMBER[1,2,3] p2 = NUMBER[1,2,3] or 24-Bit number
Calculus:	p1:= p2 – p1
Flags affected:	C O S Z
Bytes:	1 (p1=ACCU, p2=ACCU) 4 (p1=ACCU, p2=NUMBER)
Cycles:	1 (p1=ACCU, p2=ACCU) 4 (p1=ACCU, p2=NUMBER)
Description:	Subtraction of 2 registers Subtraction of register from constant
Category:	Simple arithmetic

swap	**Swap**
Syntax:	swap p1,p2
Parameters:	p1 = ACCU [x,y,r] p2 = ACCU [x,y,r]
Calculus:	p1 := p2 and p2 := p1
Flags affected:	-
Bytes:	1
Cycles:	3
Description:	Swap of 2 registers The value of two registers is exchanged between each other. Not possible with ACCU[z]
Category:	RAM Access

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4 System Reset, Sleep Mode and Auto-configuration

ALU activity is requested by a reset (power-on, watchdog), the end of measurement or in sleep mode the end of the conversion counter. A reset has priority over the last two items. First the ALU jumps into the ROM code starting with address 1024. There a first check is done whether the ALU was activated after a reset or not.

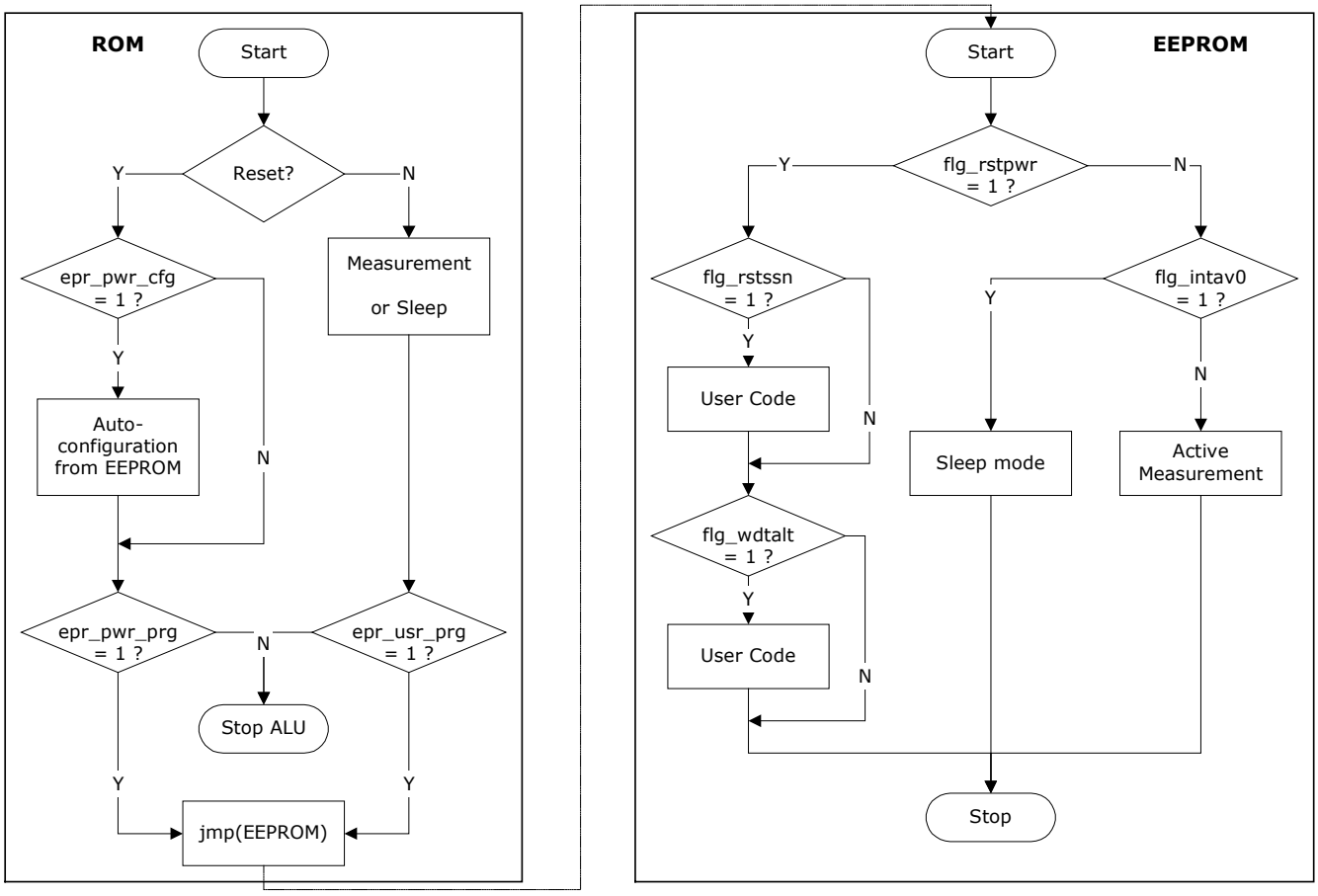
In case of a reset the flag epr_pwr_cfg is checked to decide whether the auto-configuration data from the EEPROM have to be copied into the RAM or not.

In the following flag epr_pwr_prg is checked to decide whether EEPROM code (starting at address 48) shall be executed. In stand alone operation this is reasonable and epr_pwr_cfg bit should be 1. In frontend operation this unlikely and with epr_pwr_cfg = 0 the µP is stopped.

In case the ALU is started not by a reset the TDC unit starts a measurement or, in sleep mode, the conversion counter is started without a measurement. Afterwards the flag epr_usr_prg is checked to decide about a jump into the EEPROM (address 48). Again, in stand-alone operation epr_usr_prg =1 is reasonable, in front-end operation epr_usr_prg = 0 will be more likely.

In the EEPROM code first the flag flg_rstpwr should be checked to see whether the reason for the jump was a reset. If yes, a detailed check is recommended to see whether the reset comes from a power-on reset, a pushed button, the watchdog interrupt.
Otherwise a check of flag flg_intav0 will indicate if the chip is still in sleep mode or if an active strain measurement is running.

Figure 13



At the end the ALU is stopped. This implements a complete reset of the ALU including the start flags. Also the program stack is reset. Only the RAM data remain unchanged.

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4.1 Power On Reset
When applying the supply voltage to the chip a power-on reset is generated. The whole chip is reset, only the RAM remains unchanged.

In case epr_pwr_prg = 1 the user code at EEPROM address 48 is started.

4.2 Watchdog Reset
A power-on reset can also be triggered by the watchdog timer. This happens in case the microprocessor is started four times without being reset by the opcode "clrwdt". Status bit flg_wdtalt in register 22, bit 17, indicates a timeout of the watchdog timer.

In case epr_pwr_prg = 1 the user code at EEPROM address 48 is started.

4.3 External Reset on Pin 27
In stand-alone mode (SPI_ENA = 0) it is possible to apply an external power-on at pin 27 (SPI_CSN_RST). This can be used for a reset button. The status of the button can be requested from status bit flg_rstssn in register 22, bit 18.

In case epr_pwr_prg = 1 the user code at EEPROM address 48 is started.

4.4 Sleep Mode
In sleep mode only the 10 kHz oscillator is running. At regular intervals the microprocessor is waked up but without doing a measurement. In this phase it can check the I/O's. A start-up of the microprocessor from sleep mode is indicated by status bit flg_intav0 in register 22, bit 22.

Configuration:	tdc_sleepmode	Register 1, Bit 17
	tdc_conv_cnt[11:0]	Reg0, Bits 23 to 14

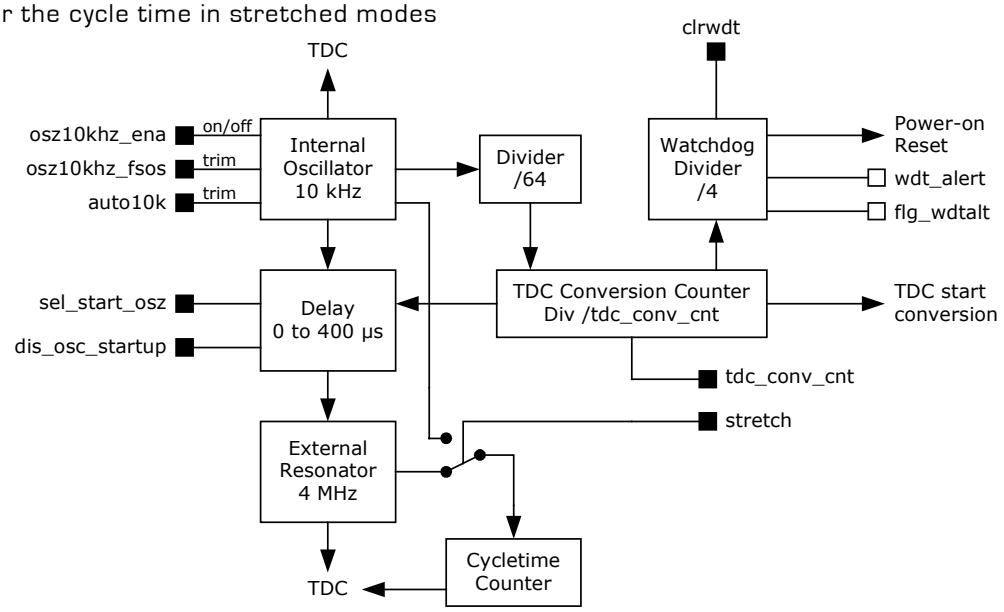
Sleep mode is activated by setting tdc_sleepmode = 1. This is equivalent to set avrate = 0.
In sleep mode the conversion counter tdc_cnv_cnt () is running to the end and then immediately starting the user program beginning at address 48 in the EEPROM.

After running in sleep mode the TDC has to be reinitialized for measurements.

5 CPU Clock generation
The basic clock for the system is the internal, low-current 10 kHz oscillator. It is used

- to trigger measurements in single conversion mode
- for the TDC unit in measurement range 2 as pre-counter
- as basis for the cycle time in stretched modes

Figure 14



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5.1 Watchdog counter and Single conversion counter

The TDC conversion counter starts a measurement in single conversion mode. It is running continuously. The single conversion rate is given by 10kHz / 64 / tdc_conv_cnt.

With the beginning of a measurement the watchdog counter is increased. The watchdog counts the conversions. At the end of a measurement the microprocessor starts to run the user code. In normal operation the watchdog by CLRWDT has to be reset before the user code ends. The watchdog causes a power-on reset in case the TDC doesn't finish its measurement because of an error or the EEPROM code does not run to end.

It is possible to switch off the watchdog when controlling the PSØ8 by the SPI interface (SPI_ENA = 1) sending SPI opcode watch_dog_off. Further the watchdog is reset by each signal edge at the SPI_CSN_RST pin.

6 IO-pins

PSØ8 has 5 I/O pins: SPI_DO_IO0, SPI_DI_IO1, SPI_CLK_IO2, MULT_IO3 and SPI_CSN_RST.

Pins SPI_DO_IO0, SPI_DI_IO1, SPI_CLK_IO2, SEL_WHEAT_IO3 and SPI_CSN_RST can be programmed as inputs or outputs with pull-up or pull-down resistors in case the chip is in stand-alone mode (SPI interface not used, SPI_ENA=1). PIN MULT_IO3 can be used as input only when Wheatstone mode is not used.

Pin 27, SPI_CSN_RST can be used as reset input in case the SPI interface is not used (SPI_ENA = 0). The reset is high active.

6.1 Configuration

Pin29	MULT _IO3	Configreg_11, bit 22,23	io_en_3_mio
Pin22	SPI_CLK_IO2	Configreg_11, bit 20,21	io_en_3_sck
Pin21	SPI_SDI_IO1	Configreg_11, bit 18,19	io_en_3_sdi
Pin20	SPI_SDO_IO0	Configreg_11, bit 16,17	io_en_3_sdo

Port definition 00 = output
01 = input with pull-down
10 = input with pull-up
11 = input

6.2 Output – write

The outputs are set in configuration register 1.

Pin29	MULT _IO3	Configreg_01, bit 13	io_a[3]
Pin22	SPI_CLK_IO2	Configreg_01, bit 12	io_a[2]
Pin21	SPI_SDI_IO1	Configreg_01, bit 11	io_a[1]
Pin20	SPI_SDO_IO0	Configreg_01, bit 10	io_a[0]

6.3 Input – read

Status[23]= flg_io3_mio	Pin29
Status[22]= flg_io2_sck	Pin22
Status[21]= flg_io1_sdi	Pin21
Status[20]= flg_io0_sdo	Pin20
Status[07]= flg_io3_mio_r	Rising edge at Pin29
Status[06]= flg_io2_sck_r	Rising edge at Pin22
Status[05]= flg_io1_sdi_r	Rising edge at Pin21
Status[04]= flg_io0_sdo_r	Rising edge at Pin20
Status[03]= flg_io3_mio_f	Falling edge at Pin29
Status[02]= flg_io2_sck_f	Falling edge at Pin22
Status[01]= flg_io1_sdi_f	Falling edge at Pin21
Status[00]= flg_io0_sdo_f	Falling edge at Pin20

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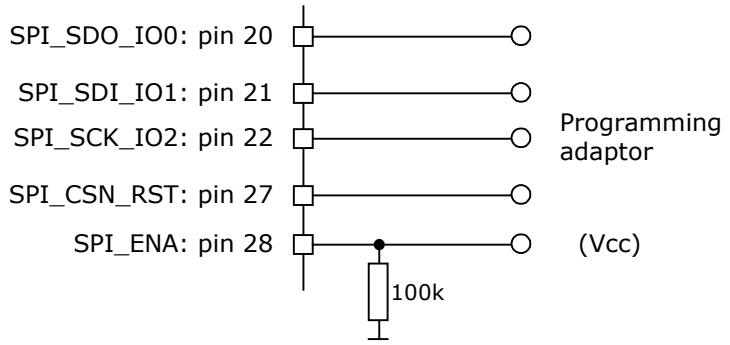
7 SPI-Interface

7.1 Interfacing

The SPI interface is used to write the program, configuration and calibration data into the EEPROM.
It can further be used to operate the PSØ8 as a pure converter chip by means of an external microcontroller. In this case the pull-down resistors are no longer necessary.
Pulling SPI_ENA high switches the SPI interface on, the pins are used for the SPI interface and no longer as I/O ports. It is necessary to send a positive pulse on the CSN line before each opcode.

Figure 15



7.2 SPI Timing

Here we describe only the SPI timing for operation as a pure converter that communicates with an external microcontroller. PSØ8 supports only 1 mode out of 4 possible ones:
Clock Phase Bit = 1, Clock Polarity Bit = 0
Data transfer with the falling edge of the clock.
The clock starts from low.

Figure 16

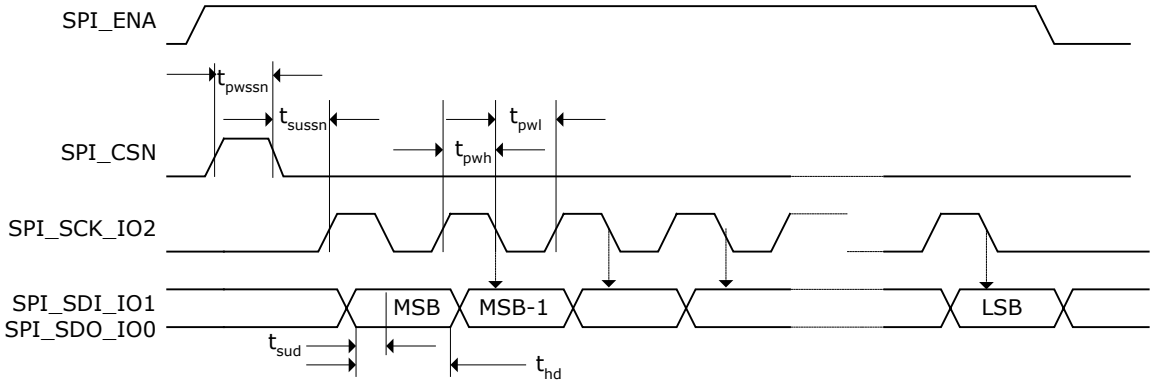


Table 6 SPI Timings

Time:	Description:	t_{min} [ns]
tpwssn	Pulse width SSN	500
tsussn	Setup time SSN / SCK	500
tpwh	Pulse width SCK high	500
tpwl	Pulse width SCK low	500
tsud	Setup time data	30
thd	Hold time data	30

tpwh and tpwl together define the clock frequency of the SPI interface. Consequently, 1µs corresponds to a clock rate of 1 MHz to run the SPI transmission.

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7.3 SPI-Instructions

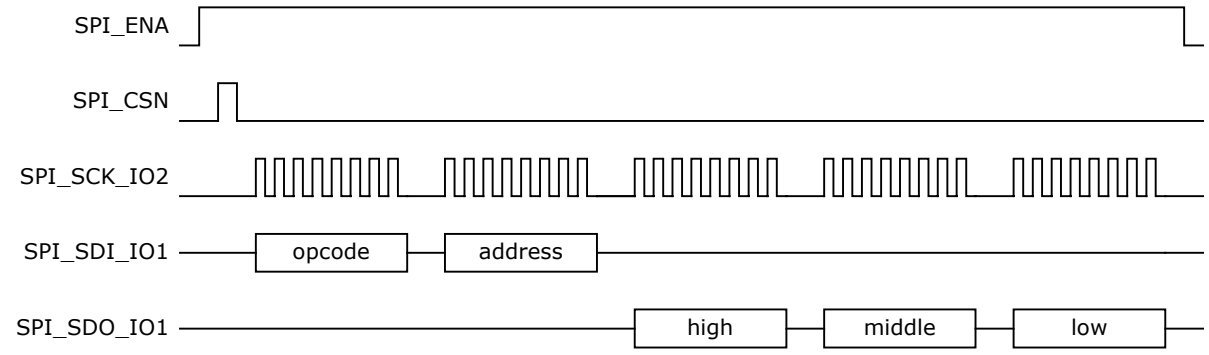
RAM Write	= b00000000	= h00	
RAM Read	= b01000000	= h40	
New_LCD	= b01000110	= h46	
Power reset	= b11110000	= hF0	
Init reset	= b11000000	= hC0	
Start_new_cycle	= b11001100	= hCC	(continuous)
Start_TDC_cycle	= b11001110	= hCE	(single conversion)
watch_dog_off	= b10011110	= h9E	
watch_dog_on	= b10011111	= h9F	
EEPROM Access:			
EEprom_bgap_off	= b10000110	= h86	
EEprom_bgap_on	= b10000111	= h87	
EEprom_enable_off	= b10010000	= h90	
EEprom_enable_on	= b10010001	= h91	
EEprom_read	= b10100000	= hA0	(protected read)
EEprom_write	= b10100001	= hA1	
EEprom_erase	= b10100010	= hA2	
EEprom_bwrite	= b10100011	= hA3	
EEprom_berase	= b10100100	= hA4	

It is necessary to switch on the bandgap and to enable the access before writing to or reading from the EEPROM.

send EEprom_bgap_on, EEprom_enable_on

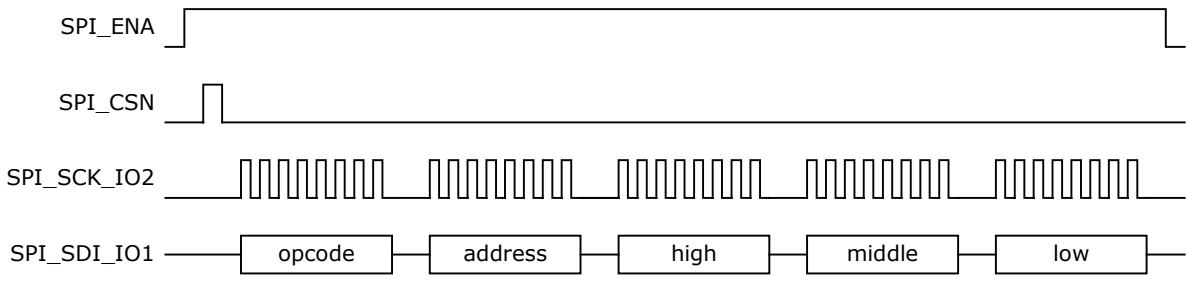
7.2.1 RAM Read Access

Figure 17



7.2.2 RAM Write Access

Figure 18



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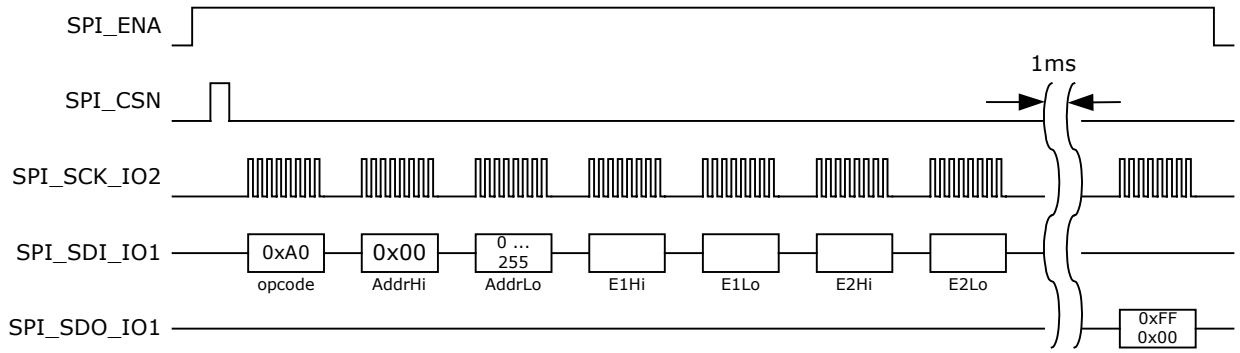
7.2.3 EEPROM Read Access / Read Protection

The PSØ8 EEPROM is protected against unauthorized reading. It is only possible to compare known data with the EEPROM content. Reading from addresses 0 to 255 checks the 16 bit words of both EEPROM's. Therefore the command EEProm_read is followed by EEPROM1 high word, EEPROM1 low word, EEPROM2 high word, EEPROM2 low word, The chip compares the transmitted data with the EEPROM content. The result is available after 1 ms on the SDO port. =xFF stands for correct data, 0x00 for wrong data.

Figure 19

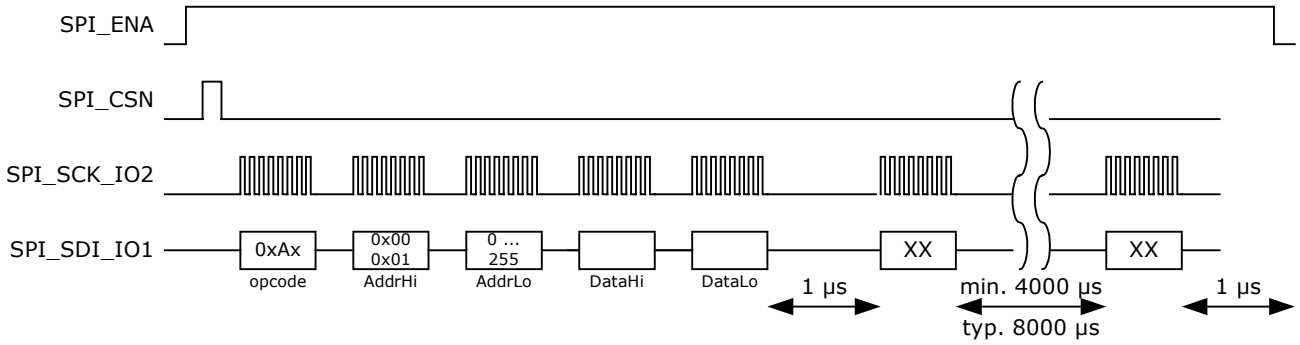


An unauthorized person has to test all possible combinations. This will last for $2^{31}*256*1ms$ = 17 years.

7.2.4 EEPROM Write Access

The EEPROM is split into two blocks of 512 bytes or 256 words. The blocks are addressed by the lowest bit of the first sent address byte. All write commands are followed by 16 bit data words with the higher 8 bits to be sent first. Programming is started by a sixth data word and stopped 4 ms later by a seventh data byte.

Figure 20 EEProm_write



EEProm_erase: Erases a 16 bit word at address AddrLo in block AddrHi. Looks the same as EEProm_write but the data bytes are ignored.

EEProm_erase: Erase the complete block addressed in AddrHi. Looks the same as EEProm_write but the AddrLo and data bytes are ignored. For erasing the complete EEPROM this command has to be sent twice (AddrHi = 0 & 1).

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8 LCD-Driver

The LCD driver has the following features:

- 18 pins for
  - 1/4 duty with maximum 6 digits including comma and 8 special characters
  - 1/3 duty with maximum 5 digits including comma and 5 special characters
  - 1/2 duty with maximum 4 digits including comma
- Stabilization of the display voltage to 3 V, 2.5V and 2V
- Integrated voltage doubler for 3 V and 2.5 V displays
- Energy efficient 2 V operation without voltage doubling
- Operation at un-stabilized supply voltage like lithium batteries or solar cells
- Currentless stand-by
- Driver strength adjustable to segment size and current consumption
- Outputs free configurable so that already wired displays can be connected
- Implemented conversion tables for 7 segment digits
- Implemented ROM code for 24 Bit number conversions

8.1 Basic Configuration

With lcd_duty the LCD is switched and set to a specific multiplex mode

lcd_duty	= 0	off
	= 1	2x multiplex
	= 2	3x multiplex
	= 3	4x multiplex mode

lcd_freq controls the switch-on time of the pixels. The longer a pixel is on the less current is needed because of the lower number of reloads. For a flicker-free display an update rate > 30 Hz is recommended. Therefore the switch-on time depends on the selected multiplex mode.

lcd_freq[2:0] =	Pixel on-time	Multiplex mode 1/4	1/3	1/2
0	8.0 ms	15	20	31 Hz
1	4.8 ms	26	34	52 Hz
2	4.0 ms	31	42	62 Hz
3	3.2 ms	30	52	78 Hz
4	2.4 ms	52	69	104 Hz
5	2.0 ms	62	82	125 Hz
6	1.6 ms	78	104	176 Hz
7	1.2 ms	104	138	208 Hz

The display has a stand-by mode. I this mode the display is switched off, but the voltage generation is switched high resistive. So it is possible to switch on the display very fast. This might be helpful in auto-on mode.

lcd_standby	= 0	LDC on
	= 1	Standby

8.2 LCD-Power supply

The PSØ8 has an integrated charge pump to double and stabilize the voltage for driving 3 V and 2.5 V LCD displays. 2 V displays need no voltage doubling. The choice for the external capacitors depends on the size or capacitance of the display.

Configuration: Register 11, Bits 10,10: lcd_vlt
Register 16, Bit 19: lcd_direct_drive

lcd_vlt[1:0]	= 0	2.0 V
	= 1	2.5 V
	= 2	3.0 V
	= 3	2.0 V without voltage doubling

lcd_directdrive = 1 LCD is driven directly from Vcc without regulation and charge pump. This reduces the LCD current and should be used in solar applications.

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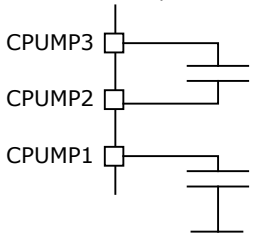
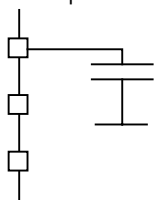
- 3 V and 2.5 V operation with voltage doubling



In a first step both capacitors are charged to half the display voltage, 1.5 V or 1.25 V. This voltage can be seen at pins CPUMP1 and CPUMP3. In a second step both capacitors are switched into series. Pin CPUMP3 then shows the full lcd voltage while pins CPUMP1 and CPUMP2 show half th lcd voltage.

- 2 V operation without voltage doubling



In this mode the lcd voltage is stabilized from an un-stabilzed supply voltage charging the capacitor to the lcd voltage. The supply voltage may not drop below 2 V in this mode.

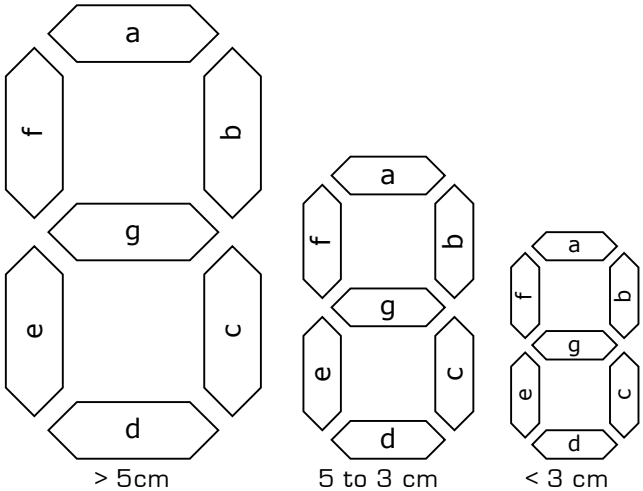
- Direct drive
  A third option is to drive the LCD directly from the power supply without regulation. Therefore no external capacitors are necessary and the output drivers are set low resistive.
  lcd_r_const = 0 (10 kOhm).
  lcd_vlt[1:0] = 0 2.0 V

8.3 LCD Output Driver configuration

The internal resistance of the output drivers can be adopted to the size of the display. By this means the current consumption can be optimized. The size of the display influences

The inner resistance of the drivers
The minimum charge time of the charge pump
The reload time of the display

Figure 21



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Configuration

Config.bit	big	medium	small	Function
lcd_fastld[1:0]	3	2	1	Configures the number of fastload periods (10ms) with low-ohmic voltage divider
lcd_swload1k	1	1	1	0 = charge capacitors by 200 Ohm resistors 1 = charge capacitors by 1 kOhm resistors not relevant in direct drive mode
lcd_r_const[1:0]	1	2	3	Defines the cross resistance of the LCD voltage divider 0 = 15 k 1 = 200 k 2 = 800 k 3 = 1600 k
lcd_charge[1:0]	0	2	3	Selects how many LCD clock cycles it is waited before recharging 0 = each cycle 1 = second cycle 2 = fourth cycle not relevant in direct drive mode
lcd_r_fastld	3	2	1	Configures the number of fast-load periods(10ms) with low-resistance voltage divider

LCD driving methods
In each mode the outputs drive 4 voltage levels, 0, 1/3, 2/3 and full LCD voltage.

Figure 22

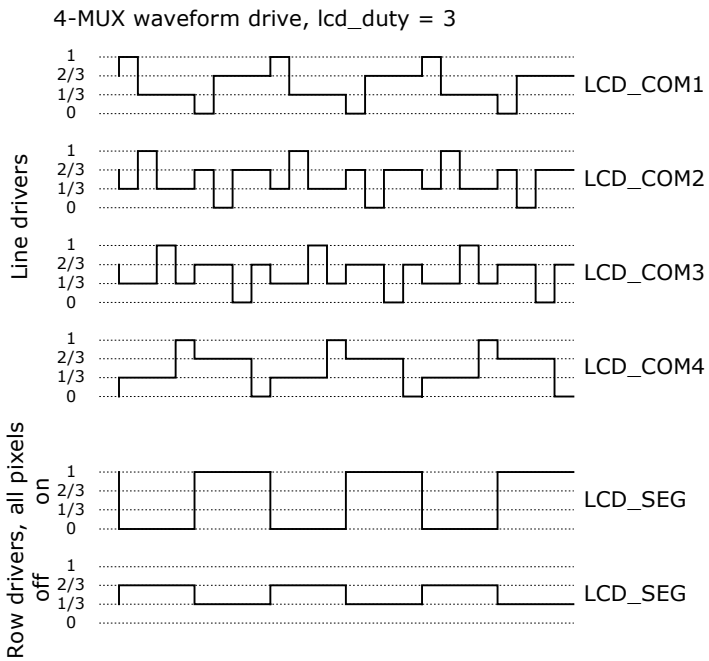

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Figure 23

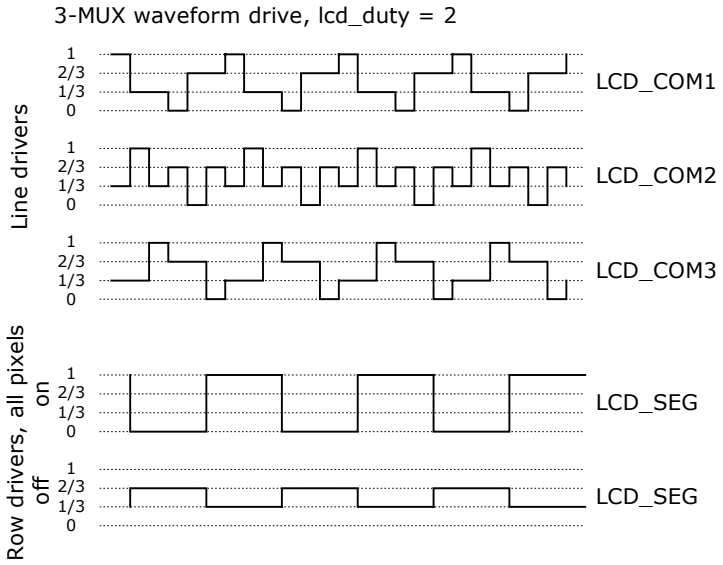
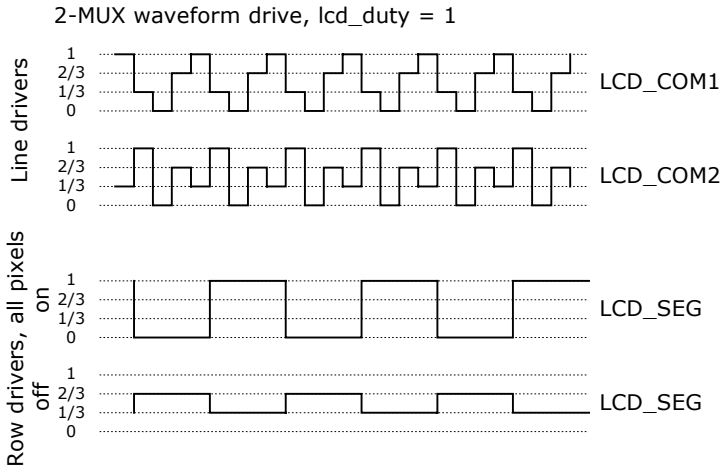
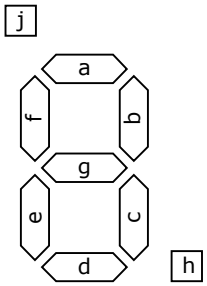


Figure 24



8.4 LCD Control

8 segments are form a digit. Each segment is named by a character from a to g. The dot is named h.



The single segments are switched on or off by setting the bits in the configuration registers 13, 14 and 15 to "1" or "0". The assignment does not depend from the multiplex mode. It looks like the following:

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Table 7

Digit	Segment		Hex Value
	hgfe	dcba	
"0"	0011	1111	3F
"1"	0000	0110	06
"2"	0101	1011	5B
"3"	0100	1111	4F
"4"	0110	0110	66
"5"	0110	1101	6D
"6"	0111	1101	7D
"7"	0000	0111	07
"8"	0111	1111	7F
"9"	0110	1111	6F

Position in the Configuration Memory:

In 2x multiplex the lower 32 bit of lcd_segment are used.

In 3x multiplex each digit is represented by a 3x3 matrix, including one additional special character. The lower 40 bits of lcd_segment are used for the 5 digits. The special signs are controlled by bits 40 to 44.

Table 8

Digit	lcd_segment	configreg	Used with
6	[55:48]	15	1/4
5	[47:40]	14	1/4, 1/3
4	[39:32]	14	1/4, 1/3
3	[31:24]	14	1/4, 1/3,1/2
2	[23:16]	13	1/4, 1/3,1/2
1	[15:8]	13	1/4, 1/3,1/2
0	[7:0]	13	1/4, 1/3,1/2

With dez2lcd (D) there is a special code for the processor to convert decimal data to characters 0 to 9. It converts the lowest four bit of the addressed accumulator (representing 0 to 9) into standard 7 segment code.

For further comfort, in the ROM code there is a subroutine for a complete conversion of a 24 bit number. In the assembler the subroutine is represented by opcode no2lcd. The value of the X-accumulator is converted and written into the lower 48 bit of the LCD memory (lcd_segment[39:0]. The signed original is written back to the X-accumulator and can be used to set the sign on the display. The position of the comma is shown in the Y-accumulator. Leading zero's are suppressed. The LCD driver ignores the upper 2 digits in 2x multiplex and the upper digit in 3x multiplex. The special characters in 3x and 4x multiplex will not be changed (lcd_segment[55:48]). In 2xmultiplex the comma of the display might be used for special characters. In this case they must be restored after the conversion.

Note:
It is necessary to inform the LCD driver separately about new data in the LCD register 13 to 15. This is done by opcode newlcd.

Code snippet:

```
        ramadr 20       ; HBO result
        move   x , r    ; Load x-accumulator with the result
        move   y , 2    ; Load y-accumulator with the comma position
        no2lcd          ; Convert into 7-Segment display format
        newlcd          ; Update LCD
        clrwdt          ; Set back the watchdog
        stop            ; Stop the uC
```


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8.5 Connecting Schemes

Figure 25 4-MUX (¼ duty)

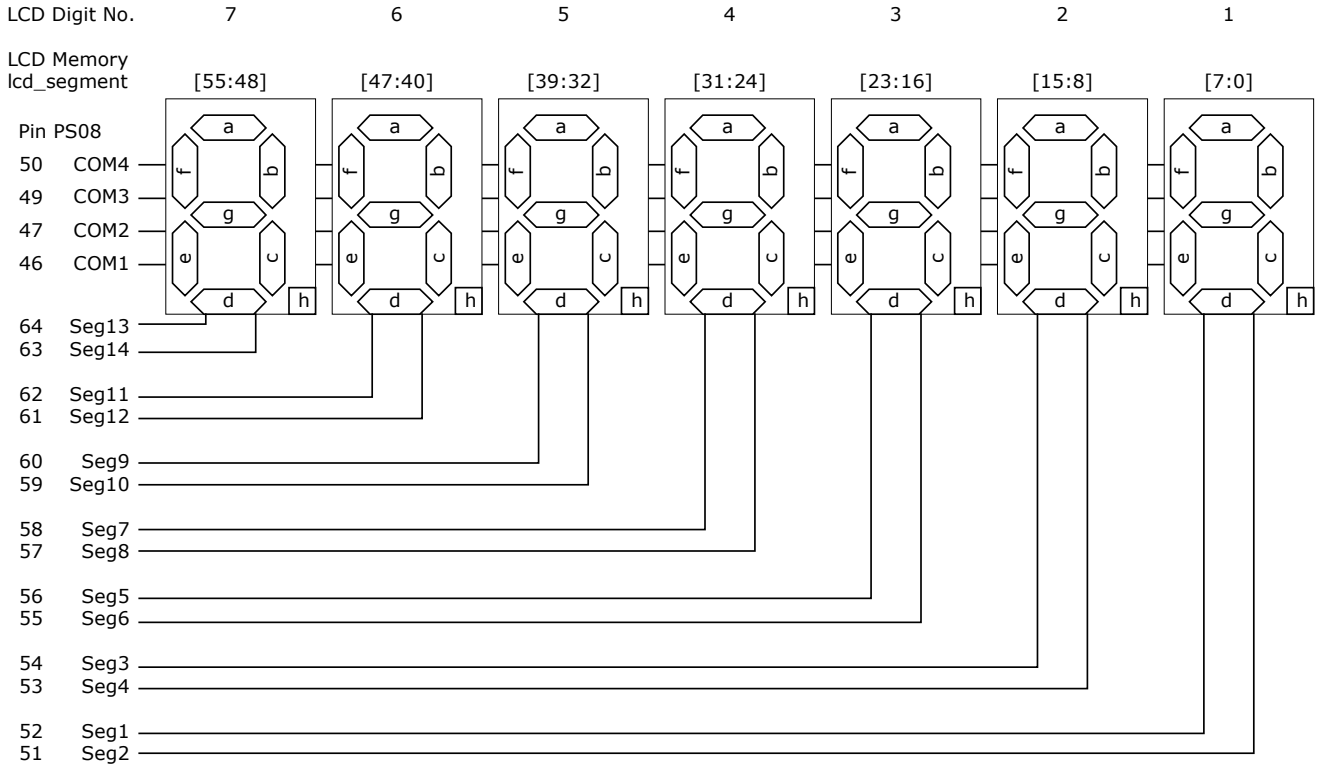

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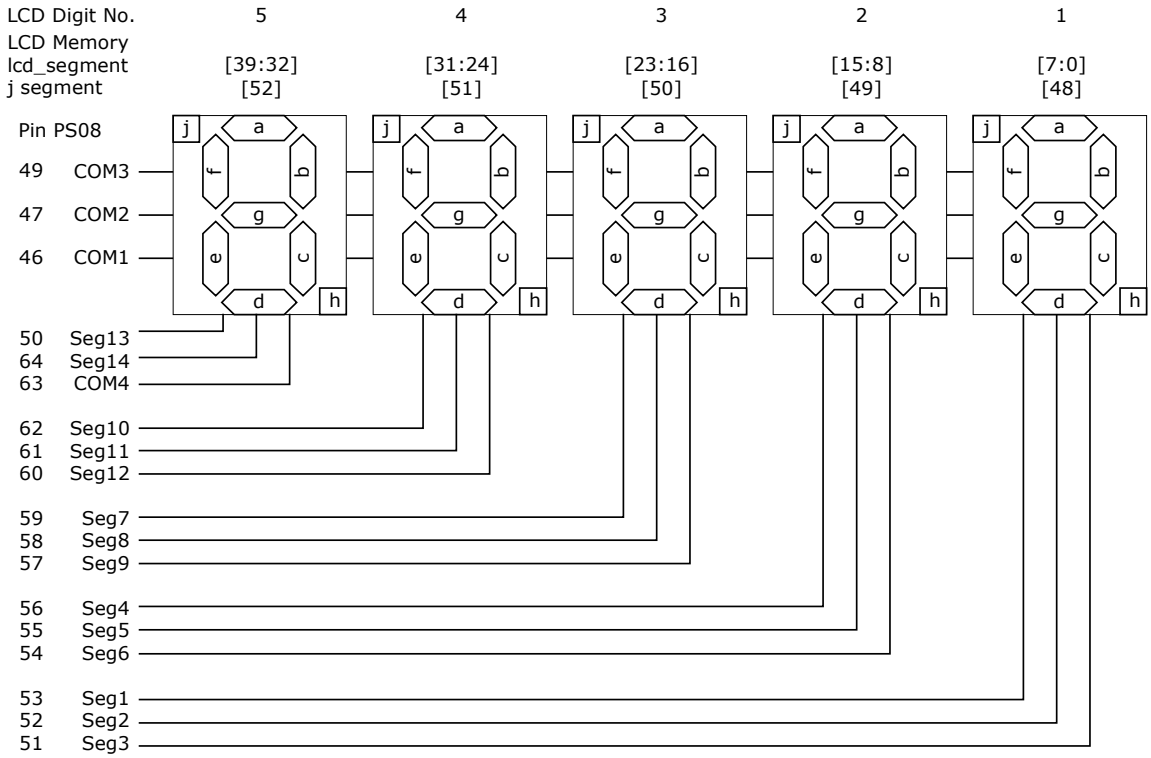
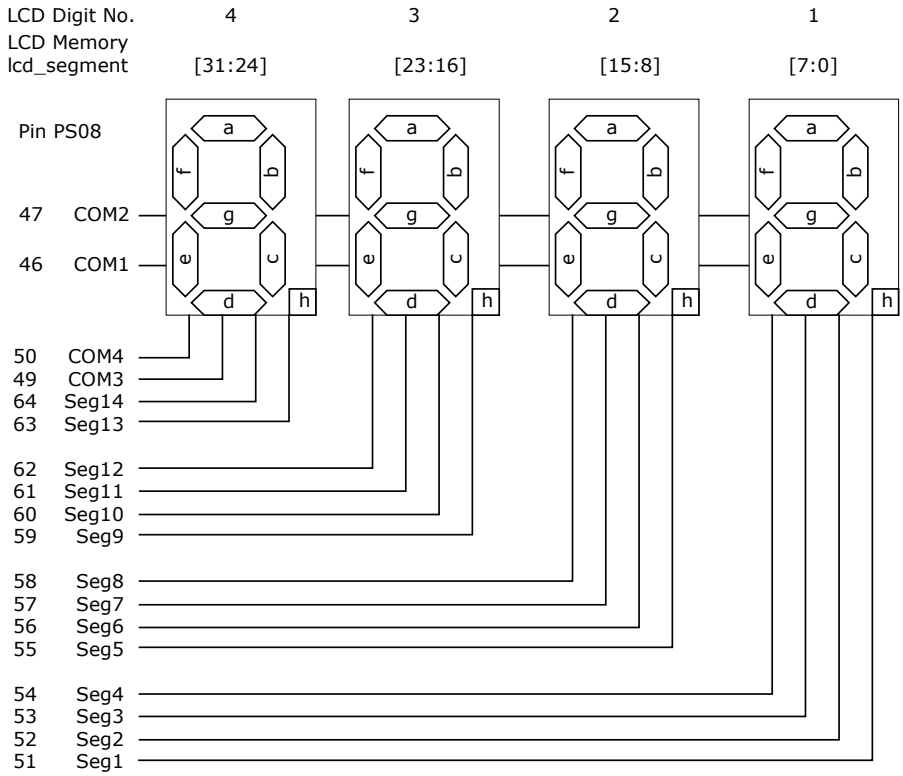
Figure 26 3-MUX (1/3 duty)



2-MUX (½ duty)

Figure 27 2-MUX (½ duty)



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8.6 Setting the Segment Position

Each segment of the configuration bits lcd_segment can be linked to an arbitrary crossing of the line and common drivers. This offers a high flexibility and allows to connect existing LCD's.

Limitations:
The segment lines and eventually common lines3,4 have to be connected to the right digit of the display. The order within one digit is free. Otherwise the command no2lcd will mix up the digits.

In register lcd_segment the program sets the segments to be displayed. In lcd_pos defines which bit in lcd_segment refers to the one out of the 8 target segments.

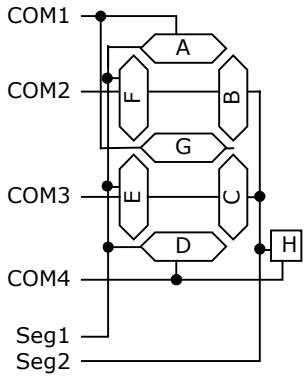
Table 9 lcd_pos

lcd_segment[] bits	Show segment	lcd_pos[] (select Seg&Com cross point)
7, 15, 23, 31, 39, 47, 55	h	23 to 21
6, 14, 22, 30, 38, 46, 54	g	20 to 18
5, 13, 21, 29, 37, 45, 53	f	17 to 15
4, 12, 20, 28, 36, 44, 52	e	14 to 12
3, 11, 19, 27, 35, 43, 51	d	11 to 9
2, 10, 18, 26, 34, 42, 50	c	8 to 6
1, 9, 17, 25, 33, 41, 49	b	5 to 3
0, 8, 16, 24, 32, 40, 48	a	2 to 0

Example:

LCD wiring

PS08 Pins:



LCD connection table

Pin	1	2	3	4	5	6	7	8	...
COM1	1A	1G	2A	2G	3A	3G	4A	4G	...
COM2	1F	1B	2F	2B	3F	3B	4F	4B	...
COM3	1E	1E	2E	2E	3E	3E	4E	4E	...
COM4	1D	1D	2D	2D	3D	3D	4D	4D	...

lcd_segment		
1. Digit	7	h
	6	g
	5	f
	4	e
	3	d
	2	c
	1	b
	0	a

lcd_pos	
bits	value
23 ... 21	7
20 ... 18	2
17 ... 15	1
14 ... 12	6
11 ... 9	3
8 ... 6	4
5 ... 3	5
0 ... 2	0

LCD display example wiring		
COM4 SEG2	H	1. Digit
COM3 SEG2	C	
COM2 SEG2	B	
COM1 SEG2	G	
COM4 SEG1	D	
COM3 SEG1	E	
COM2 SEG1	F	
COM1 SEG1	A	

The PSØ8 is adjusted to an LCD easiest by trial and error.

Method:
1. Switch on the LCD
2. Set lcd_segment[] bit 0 = '1' to display segment 'a' in digit 1 (config_reg address 61)
3. Set all lcd_pos bits to 1

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3. Move a 0 from lcd_pos[2:0] to lcd_pos[5:3] to lcd_pos[8:6] ... until the correct segment is on.
4. Set lcd_segment[] bit 1 = '1' to display segment 'b' in digit 1 (config_reg address 61)
5. Move a 1 from lcd_pos[2:0] to lcd_pos[5:3] to lcd_pos[8:6] ... until the correct segment is on. Keep the lcd_pos bits you got before for segment a.
... repeat until segment h is checked

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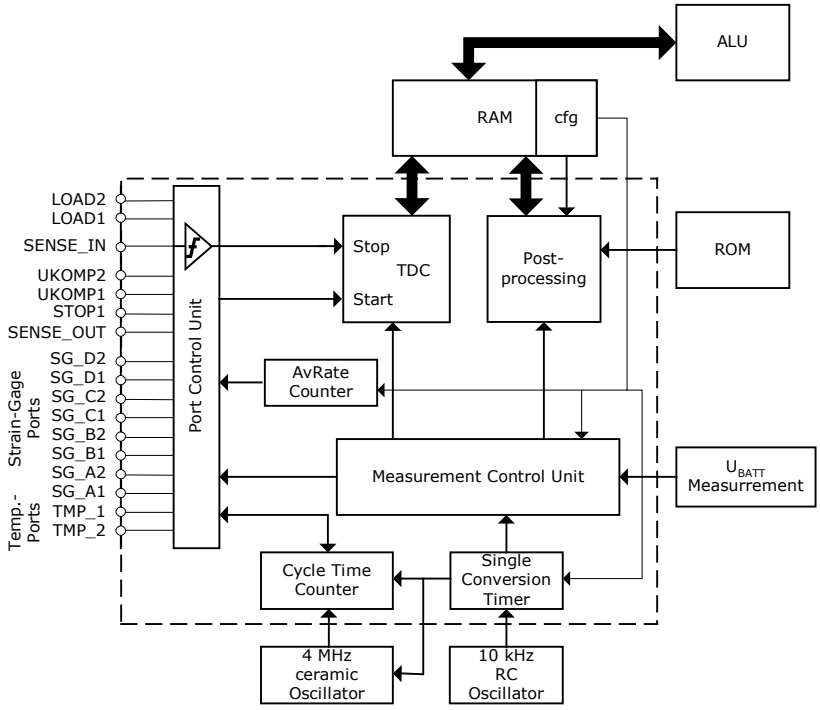
9. Converter Front-End

Figure 28



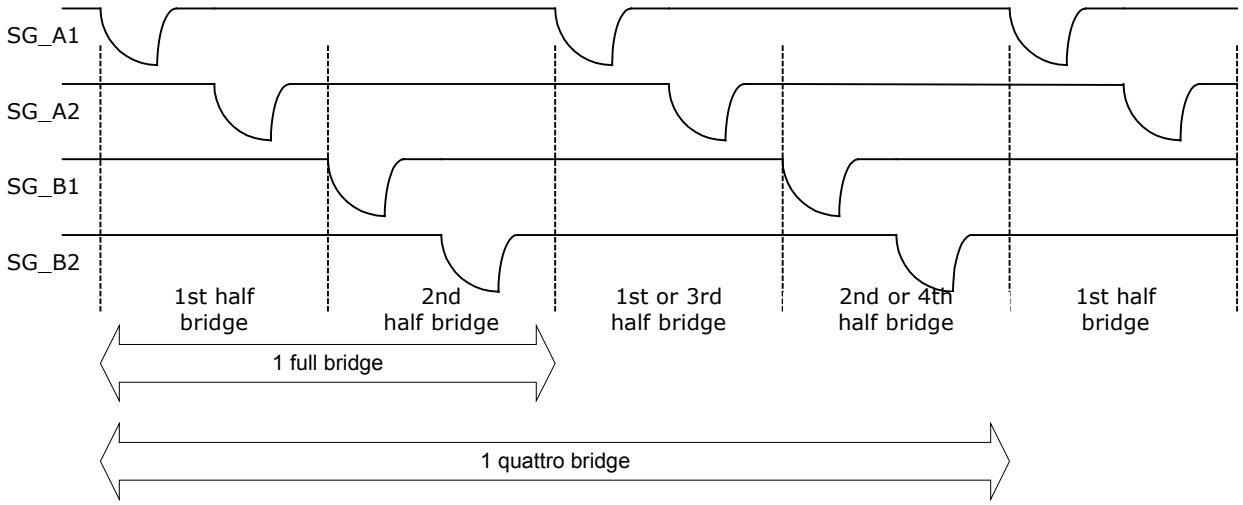
9.1 Operating Principle

The PICOSTRAIN based converter has ports to measure 4 independent half bridges, two half bridges that form a full bridge, a classical Wheatstone bridge or a single half bridge.

As add-on feature there are ports for measuring temperature by means of a KTY or a carbon film resistor. In case of an uncompensated loadcell the loadcell itself can be compensated by the temperature measurement and the RSPAN_BY_TEMP option.

The strain itself is measured by means of discharge time measurements. The discharge time is defined by the strain gauge resistance and the capacitor Cload.

Figure 29



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The recommended values for Cload are:

Rsg = 350 Ohm:	Cload ≈ 300 to 400 nF
Rsg = 1000 Ohm:	Cload ≈ 100 to 150 nF (33 nF for very-low current applications)

Recommended capacitor types are:

X7R	for consumer applications
COG or CFCAP	for higher end applications e.g. legal for trade scales

There is no need for narrow tolerances. The capacitance may vary for more than 20% without problems. For further information please refer to chapter 9.5.

The measuring unit controls the on-time of the 4 MHz oscillator and can measure the operating voltage.

Finally it does the data processing and transfers the final result into the RAM.

9.2 Modes and Timings

There are four operating modes that vary in the timing between the single discharge time measurements.

- Continuous mode — standard mode, all applications > 500 µA
- Stretched Continuous Mode 1 & 2
- Single Conversion Mode — Lowest current consumption, low sampling rate
- Stretched Single Conversion Mode 1&2 — Very low current consumption, oversampling

Figure 30

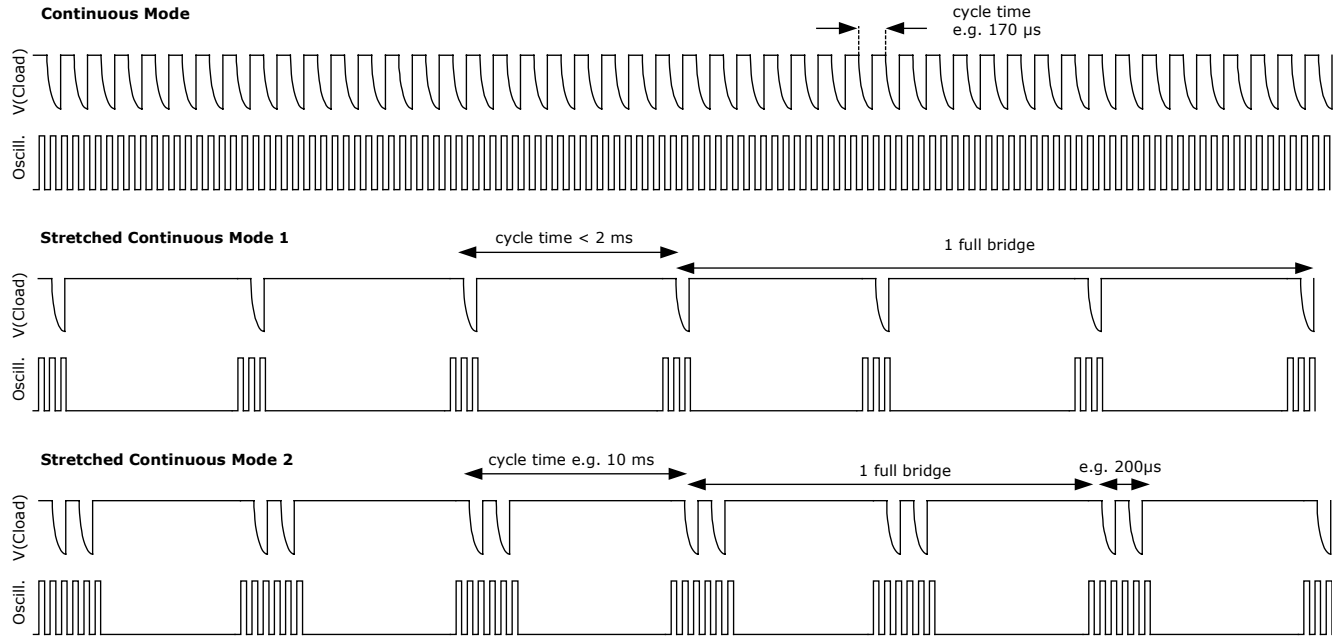

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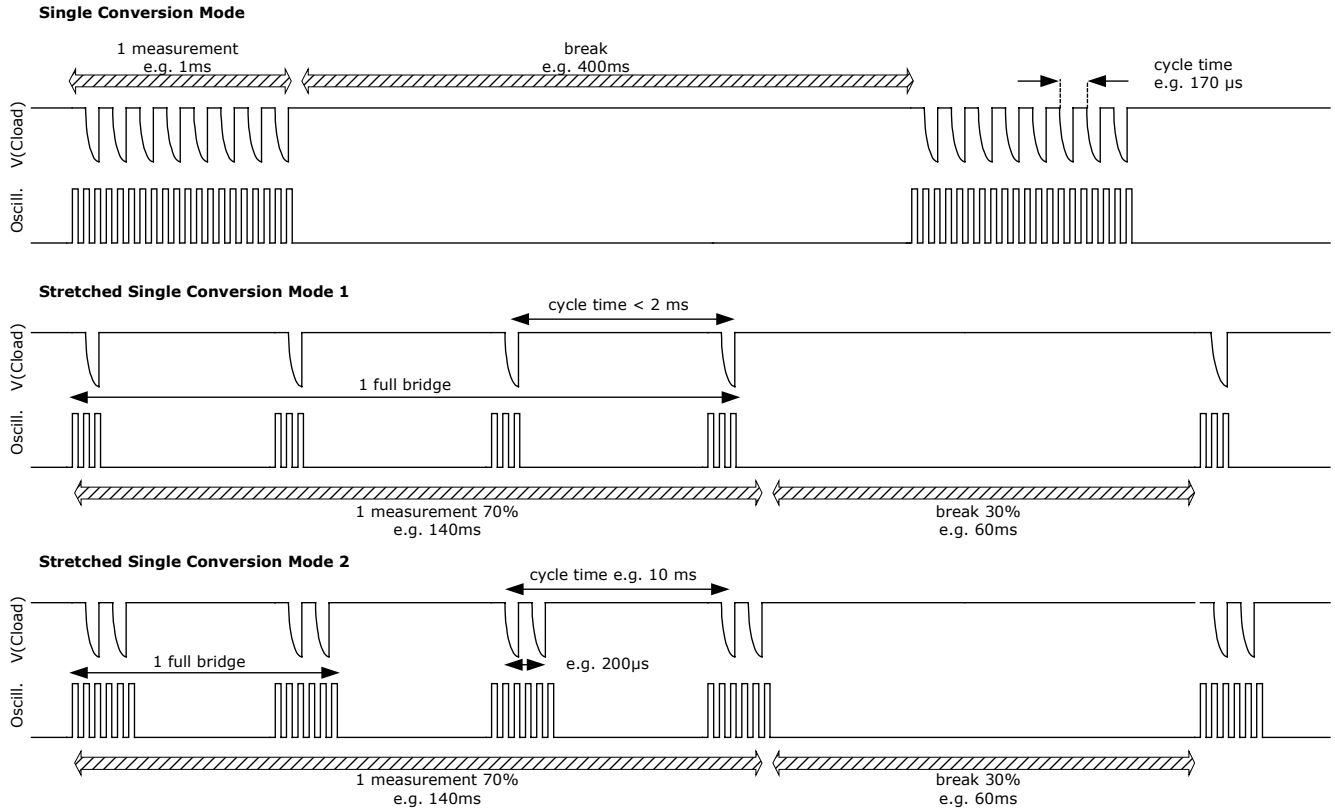
Figure 31



Four major parameters define the operation mode:

- single_conversion — Selects between continuous operation and single separated measurements.
- stretch — Selects between 4 MHz oscillator continuously running while measuring and running the oscillator only for the duration of 1 or 2 discharge cycles.
- cycletime — Defines the time interval between single or pairs of discharge cycles. It is based on the 4 MHz clock or in stretched mode on the 10 kHz clock.
- avrate — Defines the number of complete ratio measurements that build a complete single measurement (internal averaging).

9.2.1 single_conversion

Configuration: Register 2, Bit 2: single_conversion

single_conversion = 0 — Selects continuous mode. In this mode the PSØ8 is continuously measuring. The 4 MHz oscillator is on continuously. This takes about 130 µA @ 3.0 V.

single_conversion = 1 — Selects single conversion mode. In this mode the PSØ8 makes one complete measurement and then switches off the 4 MHz oscillator for the duration of the single conversion counter.

9.2.2 stretch

Configuration: Register 3, Bits 12, 13: stretch

stretch = 0 — off

stretch = 1 — The 4 MHz oscillator is on only for the duration of a single discharge time measurement. The cycle time (time between subsequent discharge time measurements) is calculated on the basis of the 10 kHz oscillator

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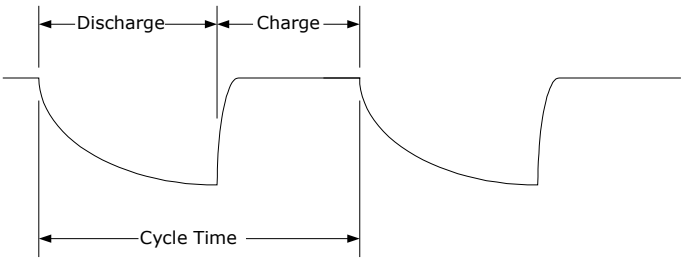
stretch = 2 or 3 — The 4 MHz oscillator is on only for the duration of a single half bridge measurement (two discharge time measurements). The cycle time (time between subsequent half bridge time measurements) is calculated on the basis of the 10 kHz oscillator. The time interval between the two discharge time measurement for a halfbridge is 200 µs in case stretch = 2 or 300 µs in case stretch = 3

9.2.3 cytime (Cycle Time)

The cycle time is the time interval between subsequent discharge time measurements. It covers the discharge time and the time to charge again C_{load}. Following figure illustrates this relation.

Figure 32 Voltage at Cload



The discharge time is given by the value of the strain gage resistor and the selected capacitor C_{load}. If the recommended values are used (e.g. 400 nF with 350 Ohm SG) the discharge time is in the range of 80 to 120 µs (@3.3V). The charge time has to be large enough to provide a full recharge of C_{load}. The minimum should be 30% of the total time (discharge + charge). Measurements are not possible if the cycle time is shorter or in the range of the discharge time and an overflow will occur. The upper limit of the cycle time is only given by the max. value of the cycle time register.

Configuration: Register 2, Bits 4 to 13: cytime

The cycle time is generated by the high speed clock divided by 8 or, in case stretch mode is selected, by the 10 kHz oscillator.

Examples:
Continuous mode: CYTIME = 80 → 80 *8 *250 ns = 160 µs @ 4 MHz high speed clock.
CYTIME = Cycle time [µs] / 2µs
Stretched continuous mode: CYTIME = 10 → 10 * 100 µs = 1 ms

With the recommended C_{load} values the cycle time should not fall below 150 µs.

9.2.4 avrate (Averaging Rate)

By setting the internal average rate the resolution of the PSØ8 can be improved.

Configuration: Register 2, Bits 14 to 23: avrate

The averaging rate sets the number of complete ratio measurements within one complete measurement cycle. The number of cycle times for one AVRate depends on the number of selected halfbridges. For every halfbridge 2 cycle times are needed.

Fullbridge → 4 Cycles per AVRate
Quattro Bridge → 8 Cycles per AVRate

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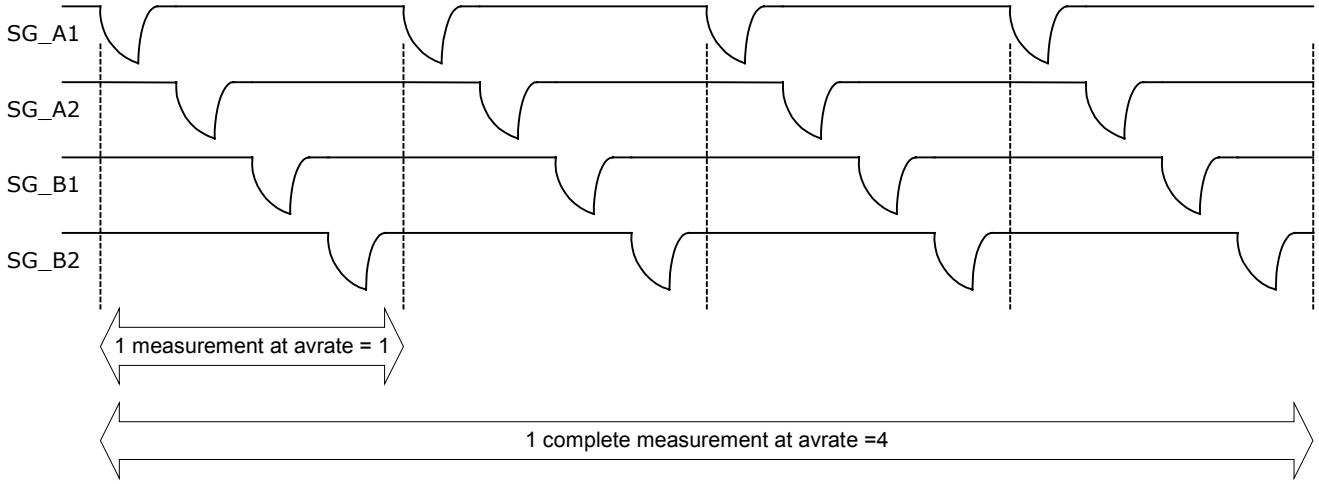
Figure 33 Example: Full bridge



9.2.5 Mode Selection Criteria

Applications	Mode		Parameters	Description
Highest resolution with no current limitation Standard mode for all applications with > 500 µA current capability	Continuous	Continuous mode	single_conversion = 0 stretch = 0 cycle time = cytime*8*250 ns	Continuously measuring, 4 MHz oscillator on all the time
High resolution but lower current		Stretched continuous mode 1	single_conversion = 0 stretch = 1 cycle time = cytime*100 µs	Continuously measuring. 4 MHz oscillator on only during the discharge time measurement. The cycle time should be less than 2 ms for sufficient oversampling.
High resolution but lower current		Stretched continuous mode 2	single_conversion = 0 stretch = 2 or 3 cycle time = cytime*100µs	Continuously measuring. 4 MHz oscillator on only during the discharge time measurement. At sample rates > 100 Hz it takes more current than mode 1.
Lowest current consumption Mechanically stable applications like pressure sensors	Single conversion	Single conversion mode	single_conversion = 1 stretch = 0 cycle time = cytime*8*250ns	option with lowest current consumption, undersampling -> no suppression of mechanical vibrations
High resolution but low current, e.g. battery driven legal-for-trade scales with 3000 divisions		Stretched single conversion mode 1	single_conversion = 1 stretch = 1 cycle time = cytime*100µs	option with very low current consumption and oversampling for suppression of mechanical vibrations. The cycle time should be less than 2 ms for sufficient oversampling. Good performance with measuring time 70%, 30% break
High resolution but low current, e.g. solar scales		Stretched single conversion mode 2	single_conversion = 1 stretch = 2 or 3 cycle time = cytime*100µs	option with very low current consumption and oversampling for suppression of mechanical vibrations. At basic sample rates > 100 Hz it takes more current than mode 1.

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9.3 Performance settings

9.3.1 Resolution and AVRate

The averaging rate for one measurement defines the possible resolution. The higher avrate[] the higher is the resolution. The resolution increases by the square root of the total number of cycle times.

Calculating the resolution:

The base resolution for a half bridge at avrate =1 and recommended discharge time (80 to 120 µs) in fast settling mode and 2mV/V excitation is:

With internal comparator: 13.3 Bit eff.
With external bipolar comparator: 13.8 Bit eff.

At higher values of avrate[] the resolution is calculated as:

$$\text{Resolution} = \text{Resolution}[AVRate = 1] + \frac{\ln\left(\sqrt{AVRate * Bridge - factor}\right)}{\ln(2)}$$

The Bridge-factor is: 2 for full bridges
4 for quattro bridges

Example 1:

AVRate = 12, Quattro bridge, internal comparator

Resolution = 13.3 + LN(√(12*4))/ln(2) = 13.3 + 2.8 = 16.1 Bit eff. = 70,000 effective divisions = 10,000 peak-peak divisions in fast settle mode (without SINC-filter)

Example 2:

AVRate = 450, Full bridge, external comparator

Resolution = 13.9 + LN(√(450*2))/ln(2) = 13.8 + 4.9 = 18.7 Bit eff. = 425,000 effective divisions = 70,000 peak-peak divisions in fast settle mode.

9.3.2 Conversion Time/Measuring Rate (Continuous Mode)

The time for one complete measurement can be calculated by means of following formula:

Tconversion = CycleTime*(2*AVRATE * Bridge-factor + 6 +MFake*2 + 1)

Mfake = #Fake measurements, Temperature measurement on

Mfake-Register	#Fake Measurements
0	0
1	2
2	4
3	16

Example1:
Cycle time = 110µs
AVRate=12
Quattro bridge
Mfake=1
Tconversion = 110µs*(2*12*4+6+2+1) =11.55 ms → The maximum measuring rate is 86.6 Hz

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Example2:
Cycle time = 110µs
AVRate=450
Full bridge
Mfake=2

Tconversion = 110µs*(2*450*2+6+4+1) =199.21 ms → The maximum measuring rate is 5.02 Hz

9.3.3 Conversion Time / Measuring Rate (Single Conversion Mode)

If PSØ8 is configured to run in Single Conversion Mode (Bit 4 in configreg_02), the measuring rate is defined by the value in tdc_conv_cnt[23:16] in configreg_00. This value corresponds directly to the conversion time (multiplied by 6.4ms).

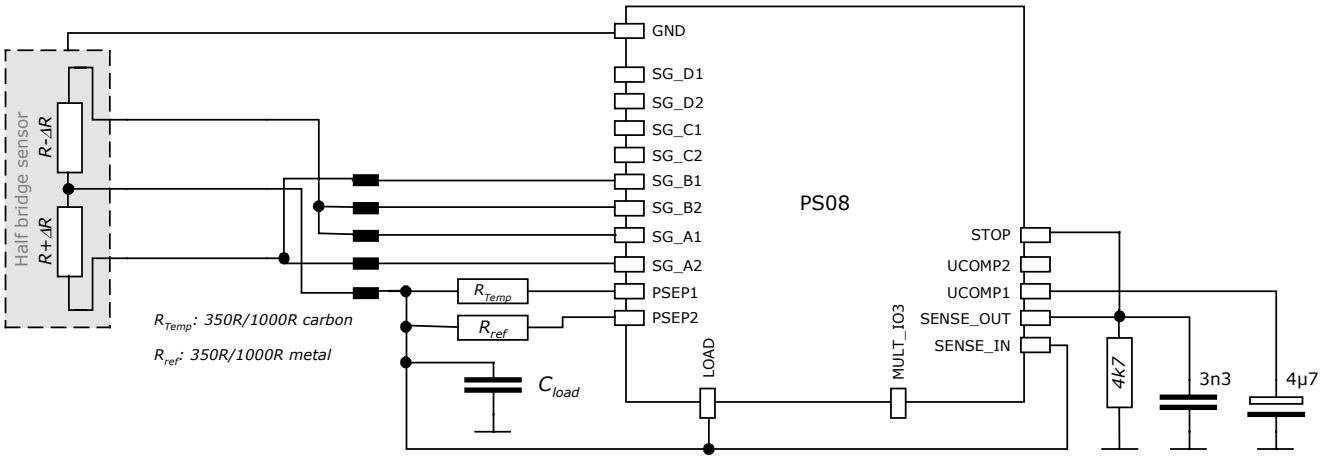
Example:
configreg_00: 0x158200 → tdc_conv_cnt[23:16] = 0x15 = 21 decimal
→ 21 x 6.4ms = 0.1344 ms
→ measuring rate = 1 / 0.1344ms = 7.44 Hz

Note:
In case you use single conversion the time needed for one complete measurement should fit into the time slot given through the conversion counter (tdc_conv_cnt).

9.4 Connecting the Strain Gage

9.4.1 Half Bridge Mode (connected as Full Bridge)

Figure 34



Note:
To get better temperature drift behavior it is recommended to connect the half bridge also to port B. This connection corresponds to a full bridge and needs to be configured accordingly with bridge[1:0]=1 (2 half bridges) in register 03.
The multiplication factors should have opposite sign, e.g. Mult_Hb1 = +1, Mult_Hb2 = -1.

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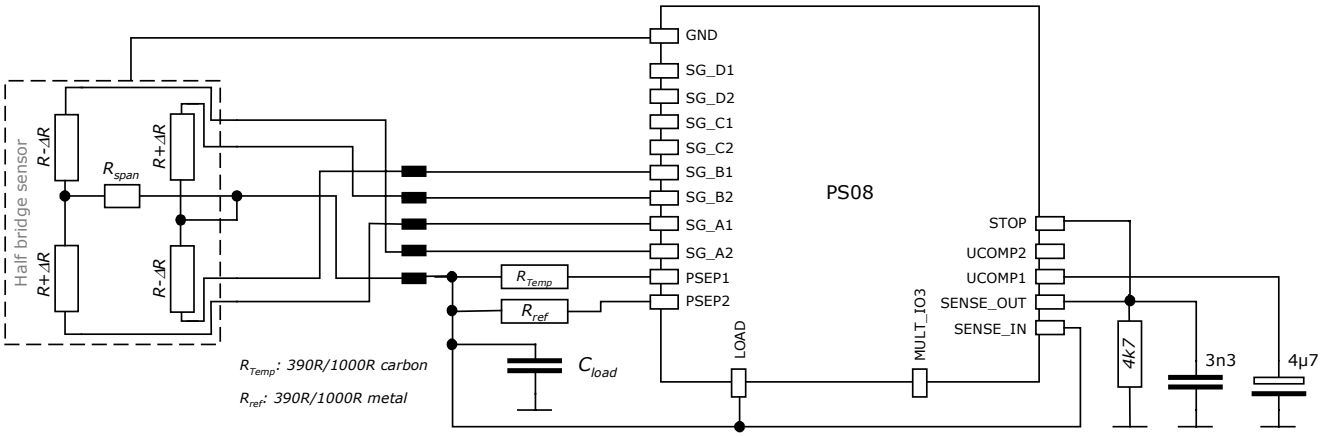
9.4.2 Full Bridge Mode

Figure 35

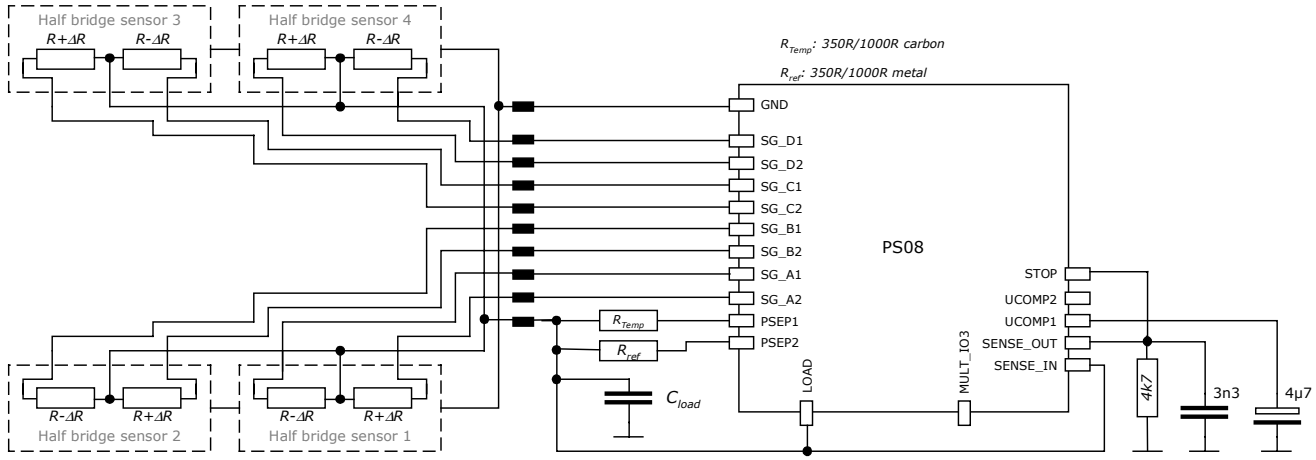


Note:
Note:
To get it is recommended to connect the half bridge also to port B. This connection corresponds to a full bridge with good temperature drift behavior and needs to be configured accordingly with bridge[1:0]=1 (2 half bridges) in register 03.
The multiplication factors should have opposite sign, e.g. Mult_Hb1 = +1, Mult_Hb2 = -1.

9.4.3 Quattro Bridge Mode

(Four load cells)

Figure 36



Note:
In this mode the multiplication factors have all the same sign.

Configuration by setting bridge[1:0] = 3 in register 2.

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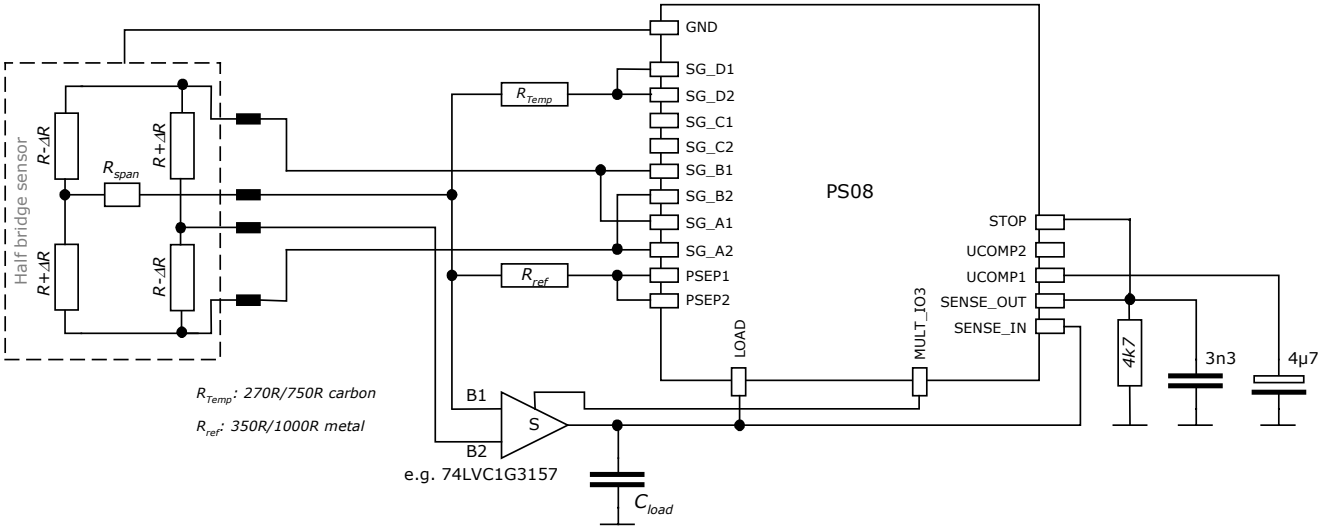
9.4.4 Wheatstone Mode

An external analog switch like 74LVC1G3157 is need when measuring Wheatstone bridges.

Figure 37

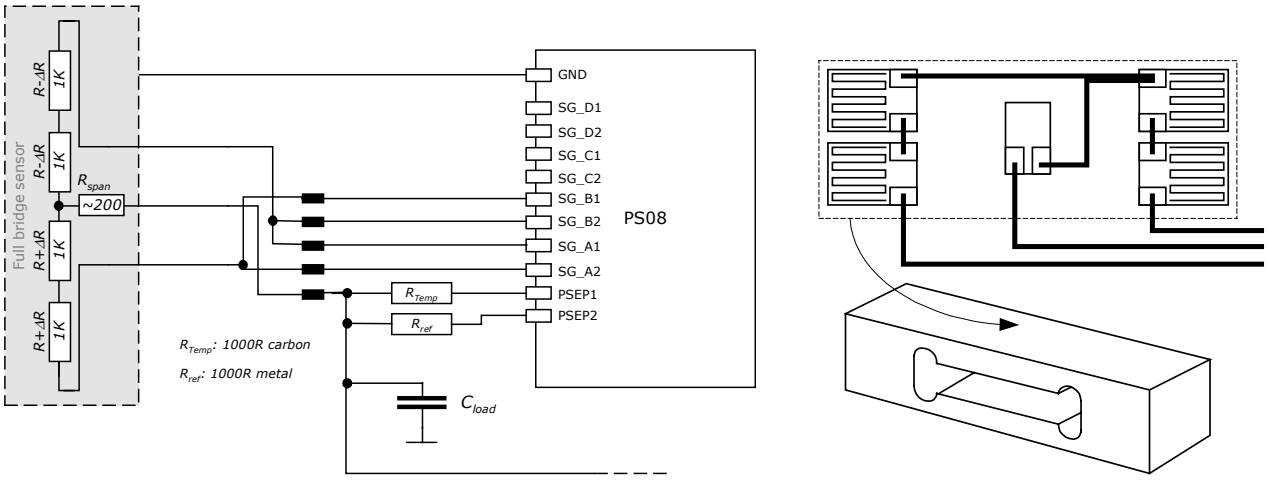


Note:

In Wheatstone mode the system looses 0.6 Bit of resolution. Therefore we recommend the Wheatstone mode only for first tests with existing Wheatstone load cells or for applications with long wires (> 1 m) between load cell and electronics.

Configuration by setting bridge[1:0] = 1 in register 2.

9.4.5 Full Bridge as Half Bridge for Lower Current



Note:
This wiring is very well suited for solar applications. The resistance of the half bridge is doubled to 2 kOhm. The current into the sensor is reduced by a factor 2.

To get better temperature drift behavior it is recommended to connect the half bridge also to port B. This connection corresponds to a full bridge and needs to be configured accordingly with bridge[1:0]=1 (2 half bridges) in register 03.
The multiplication factors should have opposite sign, e.g. Mult_Hb1 = +1, Mult_Hb2 = -1.

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9.5 Load-Capacitor (Cload)

The discharging capacitor is an important part of the circuit and has direct influence on the quality of the measurement and the temperature stability. Therefore, we recommend the following values and materials:

Rsg = 350 Ohm → Cload ≈ 300 nF to 400 nF
Rsg = 1000 Ohm → Cload ≈ 100 nF to 150 nF

Recommended materials:

- COG* (for highest accuracy)
- CFCAP® multilayer ceramic from Taiyo Yuden
- X7R (with some small losses in temperature stability)
- Polyester (with some small losses in temperature stability)

We do **not recommend** the use of Z0G capacitors !

*COG capacitor up to 100nF are available by Murata GRM31 series

Notes:

- COG capacitor are definitely the first choice for high end application (e.g. 6k divisions or higher legal-for-trade scales).
- CFCAP are also a good choice for high end scales and legal-for-trade scales
- For consumer scales X7R are the first choice because of their low cost. But they introduce additional gain drift at lower temperatures (< +10 °C).
- For consumer applications also a lot of other capacitors are well suited (e.g. Polyester).

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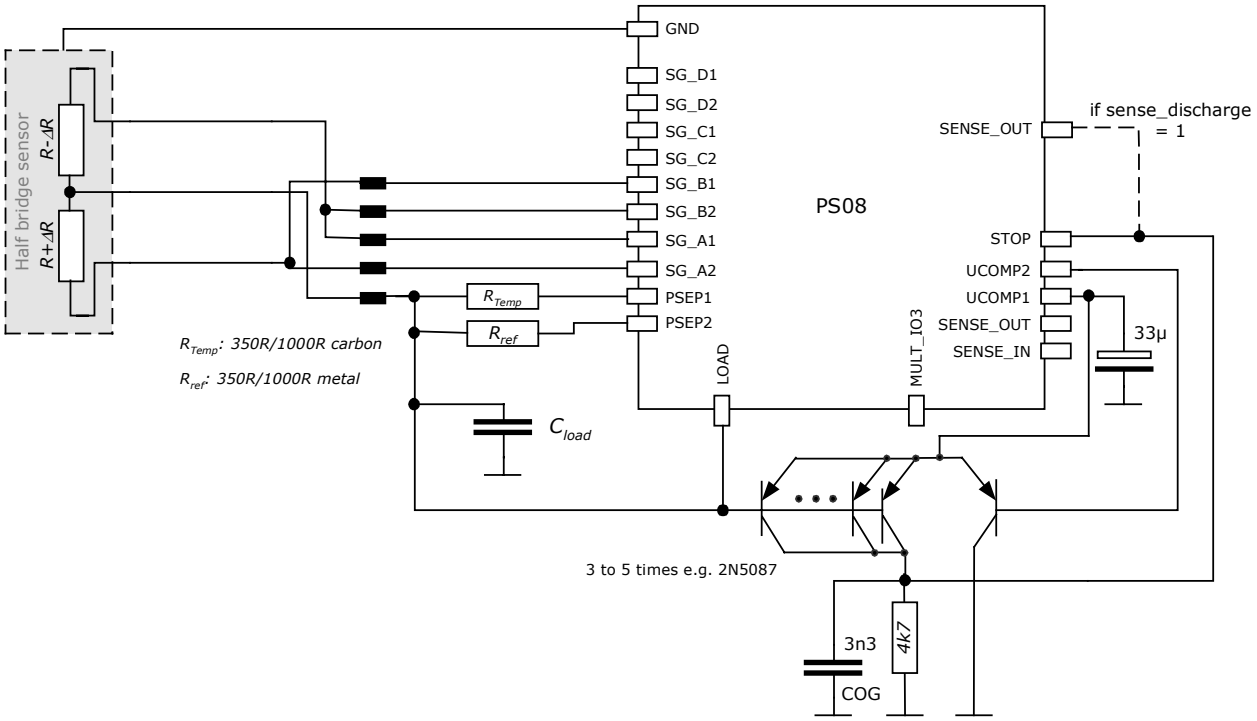
9.6 The Comparator

The end of the discharge cycle is triggered by a comparator. PSØ8 offers an internal comparator that is selected by setting reg11, sel_compint = 1. By means of the internal comparator it is possible to reach about 60,000 divisions peak-peak at 2 mV/V, 5 Hz update rate and SINC3 software filter.

The precision of the measurement can be improved by using an external bipolar comparator. With an external bipolar comparator up to 120k divisions @5Hz update rate can be reached.

Figure 38



Recommendations:
- Low-noise PNP transistors like 2N5087 / CMKT5087 or BC859 should be used
- 5 transistors in parallel should be used at the LOAD side
- It is not necessary to have matched transistors
- Use a COG-type capacitor for the low-pass filter capacitance

When should an external comparator be used?

There are three possible reasons:

a) Very high resolution

The user is looking for the best possible resolution in your application, e.g. in counting scales.

b) Lowest current

The user is looking for the lowest possible current consumption in your application, e.g. in solar scales. Because of the lower noise, the AVRate can be reduced at a given resolution and therefore the operating current is reduced. With the bipolar comparator the operating current can nearly be halved.

c) Ultra low voltage

In case the user wants to run his application down to < 2.1 V Vcc, e.g. with 1.55 V silver oxide batteries. Then the bipolar comparator shows significantly better results.

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9.6.1 Comparator Control

The comparator can be switched on for only the duration of the measurement for current saving reasons or continuously (con_comp[1:0]). Further, the working resistance of the internal comparator can be changed (sel_compr[1:0]).
We recommend the following settings:

CON_COMP = 'b10 → on during measurement
SEL_COMPR = 'b10 → 7k resistor selected

If CON_COMP is set to 'b11 (on) the comparator needs approx. 130 µA @ 3.0 V of constant current.

Capacitors at UCOMP1 and STOP

The capacitors at UCOMP1 and STOP are important for the low noise figure. For best performance we recommend 33 µF for C_{UCOMP1} and 2.2 to 2.7 nF for C_{STOP}. Please use COG-material for C_{STOP}. For Cucomp1 an ordinary electrolytic capacitor can be used.

In case the internal comparator is used C_{UCOMP1} and C_{STOP} have to be connected as well as the 4.7k Ohm resistor. Nevertheless, smaller values are possible, too.

Recommended values:

C_{UCOMP1}: not below 1 µF

C_{STOP}: lower than Cucomp2/3000

Example:

C_{UCOMP1} = 1 µF → Cstop < 1 µF/3000 → 330 pF selected.
The noise will slightly increase by about 0.2 – 0.3 Bit.

9.7 Rtemp / Rref

The two resistors Rtemp and Rref are needed for two reasons

- Correction of the delay time of the comparator
- Temperature measurement

The two resistors have to be connected in any case. In case of no temperature measurement both resistors can be of the same type (e.g. carbon resistors).

9.7.1 Correction of Comparator Delay

Because the focus of the comparator performance is on ultra low noise it has a delay time which cannot be neglected. This delay time depends on temperature and results in a gain error which is too high for precise weight scale applications. Rtemp and Rref are used to measure the delay time periodically during the operation. The PSØ8 corrects the measuring result with the measured delay time value.

The delay time of the comparator depends on the value of C_{UCOMP1} and C_{STOP}. Because these values can be changed by the user there is a possibility to adjust the correction routine by the register Mult_PP[7:0].

A good value for the recommended C_{UCOMP1} and C_{STOP} values (33 µF and 2.7 nF) is 0x1A0 (decimal 160). If the capacitor values are increased the correct Mult_PP value has to be higher or vice versa. If the selected Mult_PP value is too low the gain will decrease with higher temperature or lower voltage.

At the correct value of Mult_PP the gain of the electronic is absolutely stable over a very wide temperature and voltage range. The temperature drift of the gain is <1ppm/K. The power supply rejection ratio (PSRR) is >130 dB.

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9.7.2 Temperature Measurement

Temperature measurement is done by measuring the ratio of the discharge times of two resistors, a temperature dependent one and a temperature stable one. The sensitive resistor may be an KTY-type or even cheaper a carbon film resistor. The reference resistor can be a metal film resistor.

9.7.3 Values for Rtemp and Rref

The values for Rtemp and Rref has to be adjusted to the Strain Gage resistor and the kind of bridge.

Therefore the resistors should have following values:

Normal:	R = Rsg	(e.g. 1000 Ohm with 1000 Ohm bridges)
(Half-, Full-, Quattro Bridge):		
Wheatstone Bridge:	R = 0.75*Rsg	(e.g. 750 Ohm with 1000 Ohm Bridges)

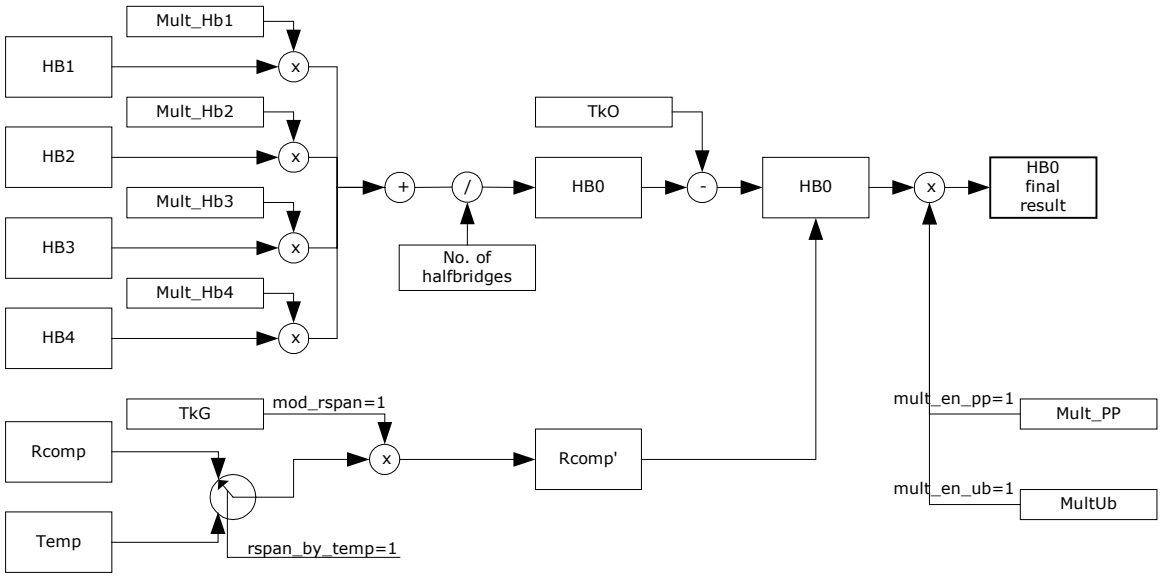
9.8 Post-processing

At the end of a measurement the converter does the post-processing of the measurement by means of ROM based routines. It stores the readily calibrated and scaled results in the result registers in the RAM. Afterwards, in case epr_usr_prg =1, the EEPROM program is started.

Specialties of the post-processing are:

- The results of the four half-bridges have independent multiplication factors. This offers the possibility to do a software correction for off-center weights in quattro applications.
- If the sensors are connected in half-bridge or full-bridge mode, the multiplication factors should have opposite signs. That means to choose e.g. Mult_HB1 = 1.234 and Mult_HB2 = -1.234.
- The strain sensors and the span compensation resistor are separated. The gain correction can therefore be adjusted by software. Even the temperature measurement can be used instead of the span compensation resistor. By this method it is possible to make high-quality load cells out of standard load cells just by software.
- The corrected result may further be multiplied by correction factors depending on the battery voltage. This supports power supply rejection and allows an operation directly from a battery without regulation.

Figure 39



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A simple example program to display the results could be:

```
ramadr    20      ; HB0 result
move      x , r   ; Load x-Accu with the result
move      y , 2   ; Load y-Accu with the comma position
no2lcd            ; Convert into 7-segment display
newlcd            ; Indicate new value to the LCD-driver
clrwdt            ; setback the watchdog
stop              ; Hold the µC
```

9.8.1 Temperature Compensation of Gain and Offset Drift of the Loadcell

If there is a compensation resistor (Rcomp or Rspan) on the load cell PS08 can measure this resistor and correct it by algorithm in the µP. By doing this the gain and offset behavior of the loadcell can be improved by PS08. This is a very comfortable method to improve the quality of the complete scale without modifying the loadcell or the electronic.

There are several possibilities how to use the compensation resistor:

a) If the compensation is already matched to the sensor, then no further adaptations are needed and the resistor can be used as usual.
b) If the compensation resistor is matched to the sensor, but the bridge has an offset drift, this offset drift can be eliminated by software.
c) If a run in the temperature drift chamber is done, the correction factors for TK-Gain and TK-Offset can be determined very appropriate. In this case the compensation of the whole system can be improved significantly. With such a method of post correction after fabrication of the scale, the complete scale can be offset and gain adjusted nearly perfect and much better than required for high end scale. (e.g. gain drift < 1 ppm/K and offset drift < 10 nV/K for the complete scalehave been achieved).
d) If the gain error of the load cell is known (e.g. stable over production lot but wrong) it can be corrected directly by PS08 without going into a climate chamber.

Furthermore it is worth to mention that by possibility c) a badly matched Rcomp can be corrected by software. So it is not necessary to trim Rcomp manually.

In case you want to use temperature correction of PSØ8 please contact us to give you further hints on how to make the compensation properly.

9.8.2 Off-center Correction for Quattro Scales

Several scales like body scales have four load cells, each with a half-bridge sensor on it. The indicated weight might vary with the position on the platform in case the load cells do not all have exactly the same sensitivity. PSØ8 allows to correct the gain of the half-bridges just by software without trimming or adding an additional trim circuit. Each half bridge result is assigned its own multiplication factor (Mult_HB1 to Mult_HB4). By simply four measurements it is possible to calculate the multiplication factors for the correction. Therefore a nominal load has to be put on each corner of the scale.

Please contact acam for the algorithm to calculate the factors Mult_HB1 to Mult_HB4.

9.8.3 Gain-Drift of PSØ8 itself

The PSØ8 has a very low gain drift of ≤ 1ppm/K in case the MULT_PP factor is set properly. The reason for this gain drift is different than in an A/D-Converter. Because of this, we give some background information in this section to understand the cause of the gain drift of PSØ8 and also some hints how to measure it properly.

Background: In a classical A/D converter application the temperature drift of the resistors of the operational amplifier have to match very exactly. A missmatch is seen as gain drift. In PSØ8 the physical reasons are totally different. PSØ8 has a TD-Converter with no preamplifier The gain drift in PSØ8 is mainly caused by the comparator circuit. To be more specific, from the delay time of the comparator which varies over temperature.

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In order to minimize the temperature drift of the comparator delay we recommend following hardware setting.

The capacitor of the comparator circuit should be in the range of 2.2 to 2.7 nF and of COG material (capacitor which is connected to STOP, pin 40).

The resistor of the comparator circuit should be 4.7 to 5.6 kOhm
(resistor which is connected to STOP, pin 40).

Select sel_compr[15:14] in register 0 to 4.1 k or 7 k
(in the evaluation software this can be found on the sheet PSØ8 → Comparator → Comparator resistor value)

Set con_comp[1:0] in register 11 to 'ON during Load'
(in the evaluation software this can be found on the sheet PSØ8 → Comparator → Comparator control)

MULT_PP Value

With above hardware recommendations the system has a remaining gain error of approximately –4 ppm/K. This is very stable over production and does not depend on matching. This remaining gain error can be reduced to < 1 ppm by choosing the right MULT_PP factor. Once established during development phase this value can be used for the whole series production. Good values of MULT_PP are in the range of 1.2 to 1.3 and slightly depend on the cycle time and load capacitor.

9.9 Highest Resolution with PSØ8

PSØ8 covers a lot of applications and gives a lot of possibilities in respect to configuration. So it is possible to configure the chip especially for a very low current consumption or for a very high update rate or for a very high resolution. Depending on the target application the configuration and the electrical set up has to be adapted. In this subchapter we focus on how to set up the chip for highest resolution.

Electrical setup:

Linear stabilized voltage supply in the range between 3.3 to 3.6 volts (no switched power supply)

Electrolytic block capacitor for VCC_LOAD >= 680 µF

Select C_{UCOMP1} as 33 µF with a 2.2 uF ceramic capacitor in parallel.

Increase Cload so that the discharge time is approximately 110 µs to 130 µs, e.g. with a 350 Ω sensor use a 400 nF COG capacitor.

Parameter settings:

Select multiplication factors of half-bridges > 1 (Mult_HB1..Mult_HB4)
(Evaluation-Software: sheet ALU → Multiplication Factor HB1 .. HB4)

Set parameter ps_qziel[5:0] in register 3 to 33 decimal.
(Evaluation-Software: sheet PSØ8 → PSØ8 Adjust 1)

Set parameter en_avcal in register 1 (bit 9) to 1
(Evaluation-Software: sheet ALU → Enable 16-time averaging of TDC cal value)

Set parameter mult_pp[7:0] in register 10 to tested value (e.g. 1.25)
(Evaluation-Software: sheet ALU → Multiplication Factor for Gain Correction)

Select avrate[23:14] in register 2 to reach needed update rate
(Evaluation-Software: sheet PSØ8 → averaging rate)

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General hints:

Connect the half-bridges in opposite direction and select therefore one multiplication factor positive, the other one negative, e.g. Mult_HB1 = 4, Mult_HB2 = -4.
The higher the averaging rate the better the resolution. On the other hand, the update rate decreases with higher averaging rate.
For high resolution we recommend the use of a multilayer PCB, at least double-layer. Multilayers will reduce the crosstalk between the PCB wires.

Of course the resolution can also be improved by using a rolling average / SINC filter. For this purpose specical subroutines are already coded in the ROM.

9.10 PSØ8 with external microprocessor

Although PSØ8 has an integrated, powerful 24-bit microprocessor, it is of course possible to run the chip as a converter and connect it to an external microprocessor. In this case the PSØ8 acts as a slave and the microcontroller as a master. The communication protocol is SPI.

There are several SPI instructions available as described in chapter 7. SPI-Interface. With the help of read and write instructions as well as PSØ8 specific instructions like 'Init reset' or 'Start_new_cycle' the chip can be operated as a SPI slave device. The basic structure of the sequence initiated by the microcontroller is as follows:

Powerreset → Configuration of Registers → Initreset → Start_new_cycle

Regarding the configuration of the registers there is one specialty we want to point out:
The addressing of the configuration registers is not continuously. In particular, configreg_00 to configreg_12 is consecutive from RAM address 48 to 60, but then configreg_spec follows at RAM address 64. The 3 missing registers configreg_13 to configreg_15 don't need to be configured because they contain the content for the LCD display which changes rapidly.
The default configuration for configreg_spec can be found in 3.4.1 Configuration Registers.

10 Oscillators

PSØ8 has an internal low-current 10kHz oscillator which is used for basic timer functions and for the definition of the cycle time in stretched modes and measuring range 1.
Further, PSØ8 has an oscillator driver for an external 4 MHz ceramic resonator. This one is used for the time measurement and for the definition of the cycle time in measuring range 2. It needs about 130 µA @ 3.0 V.

Configuration: Register 3, Bits 17 to 19: sel_start_osz
0 = Switch off oscillator
1 = oscillator continuously on
2 = Measurement started with 100 µs delay after switching on the oscillator
3 = Measurement started with 200 µs delay after switching on the oscillator
4 = Measurement started with 300 µs delay after switching on the oscillator
5 = Measurement started with 400 µs delay after switching on the oscillator
6 & 7 are not connected
Register 2, Bit 0: auto10k

This oscillator can be switched on continuously or only for the duration of the measurement, including some lead time to reach the full oscillation amplitude (sel_start_osz[2:0]). The startup time for the 4MHz oscillator is about 50µs to 100µs and slightly depends on the supply voltage.

Auto-calibration:

The internal 10 kHz oscillator may be automatically calibrated by means of the 4 MHz oscillator. The frequency varies with temperature and voltage. This would impact the update rate and sampling rate as the 10 kHz is the basis for the TDC conversion counter and in stretched mode also the cycle time. It is recommend to use the auto-calibration option setting auto10k = 1.

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Note:
Auto-calibration is not recommended in stretched single conversion modes

11 Voltage Measurement

An internal bandgap reference is used for measuring the voltage. This is done 40 times per second. The result is stored in the RAM at address 25, UBATT. It is calculated as Voltage = 2.0 V + 1.6 V* UBATT/64.

The result can be used for
- Low-battery detection: the level is set in configuration register low_batt[2:0]

low_batt	0	1	2	3	4	5	6	7
Level (V)	2.2	2.3	2.4	2.5	2.6	2.7	2.8	2.9

Flag flg_ub_low in the status register indicates if the voltage is below the set level .

- Power supply rejection: The measured voltage can be used to correct the dependency of the gain from the voltage. It is switched on by setting configuration bits mult_en_ub = 1 and mult_ub[7:0]. The result of the strain measurement will be corrected according to HB = HB/(1 + UB*[-128 ... 127]/2^21).

- EEPROM protection: when the voltage is below 2.4 V the automatic EEPROM write (putepr) is prohibited. This protcets the EEPROM against corrupt data.

Caution: If the supply voltage goes below 2.1V the voltage measurements becomes incorrect (the displayed value is to high) and the measured values cannot be used. In 1.5 V systems there is no possibility to measure the supply voltage with PSØ8.

12 Auto-on

PSØ8 can be used to run scales in a true auto-on mode. During the stand-by phase the PSØ8 measures with avrate = 1 (minimum resolution) and low update rate (e.g. 1 Hz). In such a configuration the whole system current can be reduced to 2 µA. In case a significant change in weight is detected, the averaging rate and update rate can be increased by reconfiguring avrate and tdc_conv_cnt by means of the software. As a big advantage the scale can display immediately a correct result without delay.

13 Measurement Range 1

In this mode the measurement range of the TDC is reduced to 15 µs. Therefore the discharge time has to be reduced to < 10 µs.

Recommended capacitor values are

Configuration: Register 1, Bit 18: messb2 = 0

In measuring range 1 the cycle time is generated by the internal 10 kHz clock.

Advantage: No need for the external 4 MHz oscillator

Disadvantages: Reduced resolution. This mode can be used up to 2000 scale divisions (10000 internal). The current consumption is higher than without measurement range 1 because the TDC high speed unit is running during the whole discharge time measurement.

The 10 kHz oscillator can not be calibrated (auto10k =! 0).

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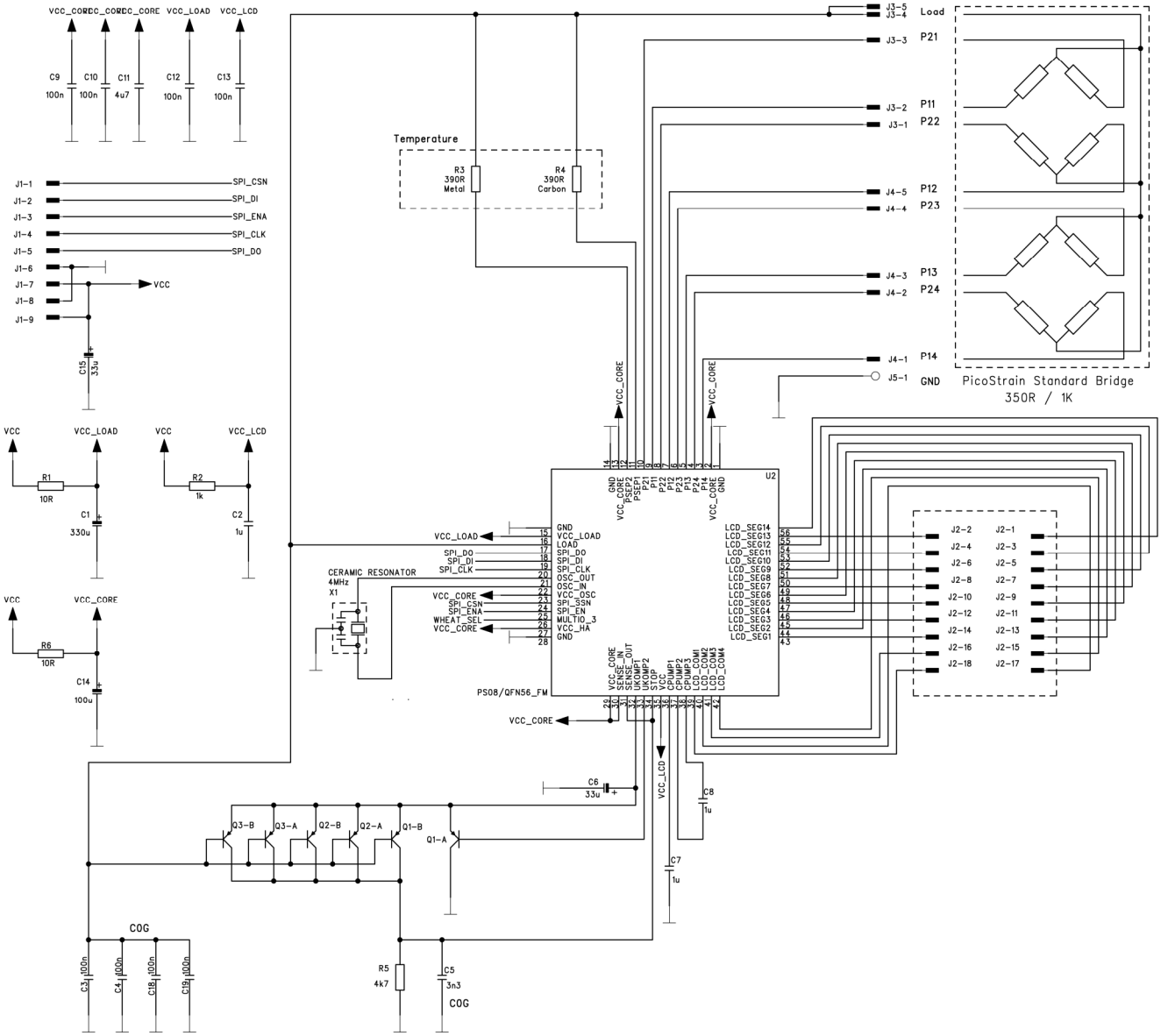
14 Sample Circuits

14.1. High-end application circuit



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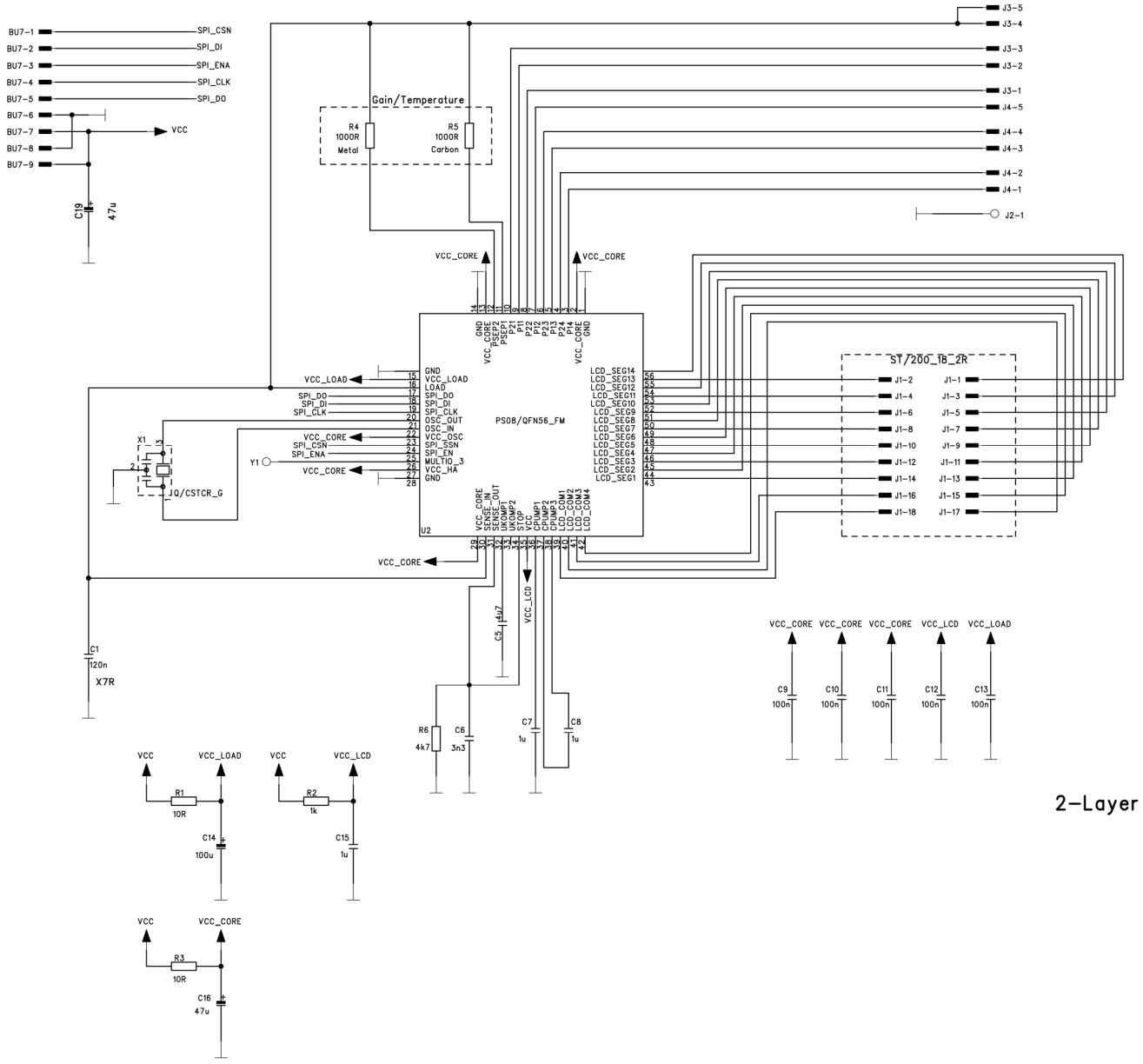
14.2 Low-end application circuit



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15 Known Bugs

1. I/O Pins — In case mod_rspan is set to 1 there might be situations where the status of the input pins regarding rising or falling edge is not correctly updated.
Workarround: There is a software workarround availabe from acam as an additional header file. Please contact acam.

Last Changes

16.04.2008 First Edition
14.05.2008 v0.2: p.22: cytime
21.05.2008 v0.3: p.49 new opcode New_LCD
11.07.2008 v0.4: GND connections added in wiring schemes, corrections LCD lanels

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